Use of an NSGA-II Genetic Algorithm and Active Gate Driving to Improve Simulated GaN Power Electronic Switching Waveforms

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Abstract

This paper investigates the use of Evolutionary Multi-objective Optimization (EMO) algorithms to automatically optimise active gate driver patterns for hard-switched GaN bridge-legs. In the paper, a simulation model of an active gate driver is developed for dynamic GaN transient shaping. Pattern discovery across a Pareto-optimal solution space is performed using a multi-objective Non-dominated Sorting Genetic Algorithm (NSGA-II). Three key measurable indicators are used to give each gate pattern performance metrics. These include: GaN device drain current overshoot, switching energy loss, and post-edge current ringing derived from spectral analysis of the current waveform. Active gate driving results are compared against the baseline of constant-resistance gate driving. We demonstrate the use of inequality constraints to refine the search space by circumscribing the optimisation region, resulting in a faster convergence. Simulated results show that an active gate driver under control of an NSGA-II-based pattern generator would be capable of finding unique optimal gate drive patterns that, simultaneously reduce current overshoot, ringing, and switching loss. Ringing is typically a result of parasitic loop inductance of the layout interacting with device parasitic capacitance. It is shown that beneficial patterns can be found for a range of values of parasitic loop inductances, and that active gate driving could therefore help to compensate for parasitic loop inductance that may be unavoidable due to, for example, voltage clearance and creepage distances.

Keywords — Active gate drive, Genetic Algorithm, Parasitic Loop Inductance, GaN, EMI, NSGA-II

1. Introduction

This paper investigates, via simulation, the reduction of ringing, switching loss, and current overshoot in GaN bridge legs, through use of an active gate driver, for a given parasitic loop inductance, see Fig. 1. In particular, the automated generation of the gate driver profiles, or patterns, is addressed.

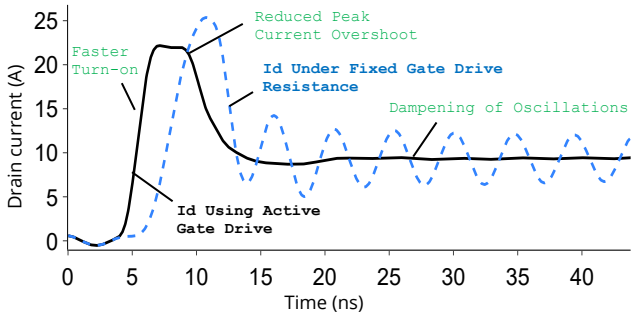

Fig. 1 - Simulated waveforms of the optimised (solid line) and non-optimised (dashed line) GaN drain current at turn-on, using the optimisation method developed in this paper.

In a hard-switched bridge leg configuration at turn-on, current rises before device voltage falls, leading to instantaneous switching loss. Increasing the di/dt and dv/dt can significantly reduce the total energy lost at turn-on $E_{turn-on}$ [1]. However, this tends to cause substantial unwanted ringing, where the circuit's parasitic inductance rings with the parasitic device capacitances [2]. Additional device stress, loss, and EMI are the result [2]. It is common practice, therefore, to optimise Printed Circuit Board (PCB) layout to minimise loop inductance, in part by refining component placement [3]. While such an approach does bring improved switching performance, it can only be optimised to a degree. There is a trade-off with cost, since certain measures to reduce parasitic inductance require more expensive PCB fabrication processes, or other costly measures to maintain voltage clearance and creepage distances. In addition, inductance may provide gains in certain situations, such as limiting short circuit currents or invoking partial soft switching of the power device(s). Moreover, some applications might not allow for significant loop inductance reduction [4], making it an inseparable part of the design. This, in turn, makes the full exploitation of GaN devices challenging.

The literature shows that active gate driving can beneficially shape switching waveforms in GaN-

based switching converters [5]. The fast nanosecond-scale switching transients of GaN devices require a gate driving variability that is over an order of magnitude faster than what is required for silicon devices. One means of modulating the gate signal at the required rate is via digitally controlled drivers [6][7], whose complex gate waveforms are defined by over 100 parameters, with varying degrees of granularity. A number of research papers propose means to efficiently find appropriate gate drive patterns that improve switching waveforms [8][9], however these address patterns with only a few parameters. For complex parameters, the computerised searching of the whole solution space is impractical, especially since these profiles may need to be optimised as a function of operating conditions, such as output current, ambient temperature, and DC voltage, as well as component characteristics which are subject to manufacturing tolerances.

The contributions of this paper are:

1. To provide an experimentally derived LTspice model for a GaN buck converter and custom integrated active gate driver in Section 2.
2. To provide control strategies for the active gate driver model to combat switching problems induced by high switching speed and loop inductance, Section 3.
3. To present a closed-loop simulation system with data extraction for subsequent use by an NSGA-II-based optimisation algorithm that finds the required gate control patterns, Section 4.
4. To demonstrate the use of two and three objective parameters to automatically find gate profiles that optimise current overshoot, ringing, and spectral content, and give examples of how the visualised solution space can be used for best performer selection, also in Section 4.

2. Simulation Model and Active Gate Controller

This section presents the models, algorithms, and user control used in this research.

2.1. Converter Circuit Simulation Model

The simulation model of the hard-switched synchronous buck converter is implemented in Analog Devices' LTSpice programme, see Fig. 2. An active gate driver model controls the upper control device, whereas the lower device is controlled using a conventional driver.

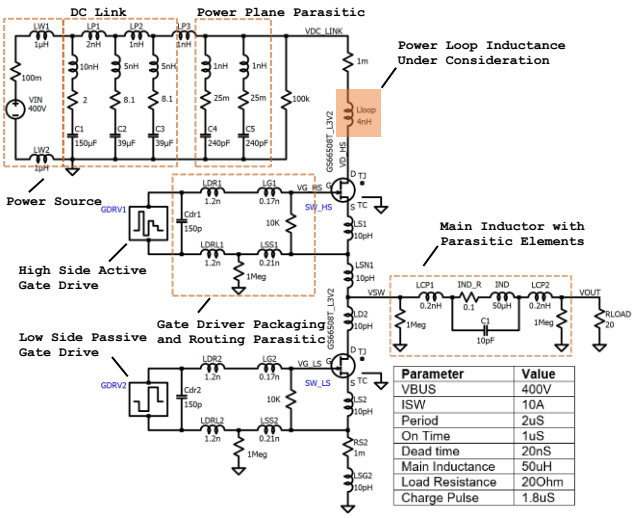

Fig. 2 - Converter simulation model, table of operating parameters, and highlighted inductance L_{loop}.

The choice of parasitic impedances used in the simulation model is largely based on experimental findings [7] on similar converter designs. Parasitic impedances of passives and power rails are taken into account. The power rail capacitance inferred from PCB manufacturer data and trace areas is 240 pF, whilst the equivalent series resistance (ESR) is 25 mΩ and the equivalent series inductance (ESL) is 1 nH.

Power loop parasitic inductance and device output capacitance are the main contributors to device voltage and current overshoots, and ringing [6][9]. The total loop inductance comprises fixed components such as packaging, and components that the designer can influence during the layout. The parasitic inductance L_{loop}, highlighted in Fig. 2, represents this variable component, and will be swept from 2 to 8 nH in Subsection 4.4, to represent optimised and sub-optimal layouts. L_{loop} combines all parasitic inductances in the loop through the DC-link capacitor, the upper control power device, the common source inductance L_s, to switching node, lower synchronous power device, and return path to the capacitor. Parasitic inductance due to PCB routing and solder connections are represented by LS1, LSN1, LD2, LS2, and LSG2, all approximated as 10 pH.

The DC-link capacitors are modelled as series LCR strings, where the ESR and ESL values have been measured at 1 MHz with 10 V dc bias on a Wayne-Kerr 65120P impedance analyser. The GaN switching devices used are GS66508T [10], and the simulation models are provided by GaN Systems [11].

The converter is set to switch at 2 MHz, with a duty ratio of 50%. The input DC Voltage VIN is 400 V and the output current is 10 A. The main inductor of 50 µH has been calculated to deliver a switching ripple current of 1 A.

2.2. Overview of the Active Gate Driver Simulation Model

The driver model used here is based on the integrated active gate driver circuit of [6]. This driver controls GaN power devices by activating a pre-programmed sequence of individual pull-up and pull-down actions, that actively steer the gate current, to speed up or slow down the switching of the GaN device. In the integrated circuit, this function is implemented with different numbers of pull-up and pull-down transistors.

The model used here, shown in Fig. 3, models these transistors with an ideal switch, series resistances, and output capacitance that was determined from post-layout simulation. The implemented model only pulls in one direction per switching edge. Gate loop parasitic elements include soldering interfaces, bond-wires, and driver transistor output capacitance, using values from [6], where bond-wire inductances L_{dr1} and L_{drl1} are derived using Q3D simulations.

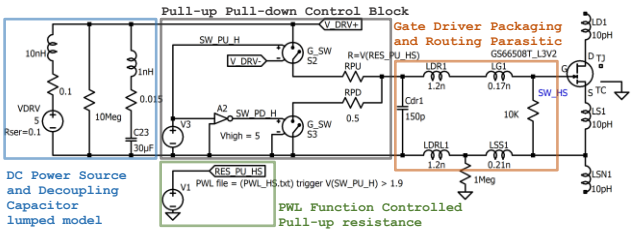

Fig. 3 – Active gate driver simulation model circuit diagram for the upper GaN device, comprising a power source, decoupling capacitor, resistance selection control block, and packaging and routing parasitics.

The gate-drive pattern is initiated by the rising edge of a pulse width modulated (PWM) signal. This edge triggers the Piecewise Linear (PWL) function that defines the net pull-up resistance value against time. The gate drive control strategies presented in the following sections provide this function, which is referred to as the gate pattern. In the model, the PWL function profile is read from a .txt file that is updated by the driver control software for each new pattern iteration.

2.3. Active Gate Driver Pattern Control and Parameter Choices

The Graphical User Interface (GUI) shown in Fig. 4 has been developed to manually test specific gate driving patterns. It is not used in the automated pattern generation shown in the following sections; However, it provides a useful overview of the degrees of freedom available when creating patterns and is therefore included here.

As a baseline, this control GUI can be used to drive GaN devices with a constant pull-up resistance by configuring the PWL function to be a single step function. Alternatively, an arbitrary PWL function can be set as illustrated in Fig. 4 (top). The settings for amplitudes and durations are shown in the settings field in Fig. 4 (bottom).

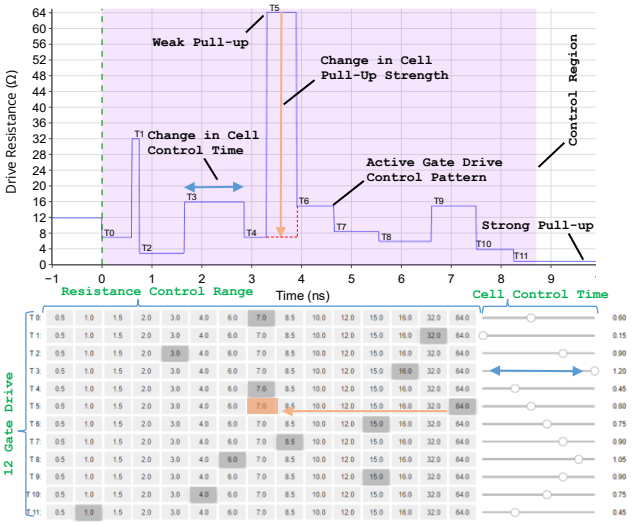

Fig. 4 – GUI showing the programmed resistance sequence (PWL function) (top) and the respective settings (bottom). The pattern shown here is a sequence of 12 pull-up resistance values, and time durations ranging from 0.15 to 1.2 ns.

The gate driver of [6] has effective pull-up and pull-down resistance ranges from 0.14 – 64 Ω. In order to reduce the search space in this work, the resolution is reduced, and only the following resistances are assumed to be available: 0.5, 1, 1.5, 2, 3, 4, 6, 7, 8.5, 10, 12, 15, 16, 32, 64 Ω. As possible activation times for each resistance value, a range of 0.15 ns to 1.2 ns in steps of 150 ps is chosen. These timings are informed by the capabilities of the driver IC of [6], although values from the higher resolution driver of [7] could equally have been used.

3. Turn-on Transient Parameters and Optimisation Strategies

This section provides details behind the simulation scaling, underlying optimisation parameters, and metrics that are used to analyse and improve the turn-on switching transient. This is followed by an introduction to the EMO NSGA-II algorithm used to accelerate optimal gate drive pattern discovery.

3.1. Turn-on Transient Optimisation Parameters

Optimisation of transient ringing and energy loss reduction relies on the evaluation of critical performance metrics. Simulation is integrated together with the control software in a closed loop system. The algorithm extracts simulation data and performs post-simulation analysis of the turn-on transient. Firstly, high-side peak drain-source

current overshoot $i_{D\_HS\_OS}$ is extracted from the current waveform i_{D_HS}.

Secondly, turn-on switching loss E_{turn_on} for each transient is calculated by integrating instantaneous power loss over the turn-on period. As part of the integration process, energy E_{Coss} stored inside the device output capacitance [12] is not considered, resulting in the expression:

$$E_{turn\_on} = \int \left(i_{D\_HS} \times v_{DS\_HS}\right) dt \qquad (1)$$

3.2. Drain Current Ringing and Spectral Analysis

As has been noted in [2], exacerbated oscillations of drain current are undesirable due to consequential EMI and arising stability concerns [13]. As it will be shown in Section 4.2, two proposed evaluation metrics ($i_{D\_HS\_OS}$, E_{turn_on}) provide insufficient data for the algorithm to optimise the gate pattern. Hence a third optimisation parameter indicating the amount of ringing associated with drain current (i_{D_HS}) transient is required.

Among the methods to identify the severity of the current oscillation is to perform a Fast Fourier Transform (FFT) of each turn-on transient. However, the raw spectrum contains too much information to be used on its own and is accommodated by components at lower and higher frequencies that do not directly correlate with the ringing observed in the time domain [14]. Besides, it is desirable to have a single value metric of the spectrum that would encode features of the graph that are considered important. Hence, the proposed strategy for ringing evaluation is to integrate the FFT spectrum over a specified frequency range, providing the algorithm with a single performance metric.

A suitable frequency range has been determined by performing a set of simulations with constant gate drive resistances selected at two extremes and one middle value of 0.5, 64, and 12 Ω respectively. For all three sets of results $L_{loop} = 4\,nH$. Time-domain data from 0 to 44 ns, windowed with a Blackman function [15], is used in the spectral analysis. The resulting time-domain current waveforms and calculated frequency-domain data are shown in Fig. 5. Driving with 64 Ω constant resistance results in a very slow rise time towards 10 A of nominal current, and leads to low spectral content. On the other hand, rapid turn-on with 0.5 Ω resulted in excessive peak current and accompanying high-frequency ringing. Selecting 12 Ω pull-up resistance lies in the middle of these two extremes and demonstrates lower peak overshoot and dampened ringing, evidenced by 20 dB lower spectral peak at 390 MHz. An increase or decrease of the loop inductance will shift the ringing frequency lower or higher accordingly.

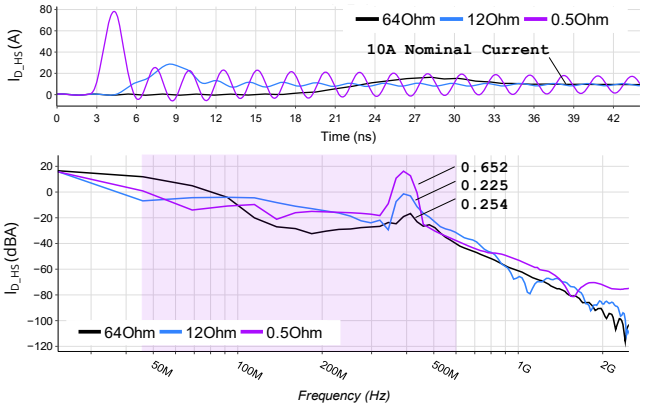

Fig. 5 – Time-domain turn-on transient waveforms of high-side drain current for a set of three constant gate resistances (top). Calculated spectral envelopes (bottom), together with evaluation of the integration over the highlighted window 45-600 MHz.

Based on the acquired spectrum, an integration range of 45-600 MHz was selected to accommodate a wide range of ringing frequencies. The integration results, as shown in the line labels in Fig. 5, bottom, provide a performance approximation for each spectral envelope. A low integration value indicates lower ringing; similarly, larger peeks in the spectrum will result in a much greater integration value and, therefore, lower performance metrics. With the proposed ringing evaluation strategy in place, a corresponding range of parameters is used as part of the optimisation strategy and best performing gate pattern selection:

1. High side drain current peak overshoot ($i_{D\_HS\_OS}$)
2. Hard switching transient Energy loss ($E_{turn\text{-}on}$)
3. Spectrum integration metric signifying the extent of drain current ringing ($FFT_{integration}$)

3.3. Simulation Specifics

Simulations performed in this work were made using LTSpice and split across eight threads of a i7-4720HQ quad-core processor [16], with simulation time taking ~9 seconds on average. Simulation across 16 threads on a newer i7-10700K [17] processor reduced average time down to ~4.5 seconds. Even if each simulation took one second to perform, brute force pattern selection would take for the first three driving cells 20 days, for four driving cells six years, and for all 12 driving cells 1.2×10^{17} years.

3.4. Multi-objective Optimisation Algorithm

Due to the high number of control parameters, identification of an advantageous gate drive pattern is a highly dynamic optimisation problem and heuristic change of control parameters does not lead towards intuitive results. To avoid combinatorial explosion, a biologically inspired metaheuristic algorithm has been used to find an optimal solution in a reasonable computation time. The evolutionary multi-objective optimisation algorithm NSGA-II [18] has previously demonstrated its ability and has been used for numerous applications relying on multi-objective optimisation. Its operation process resembles the genetic algorithm [19], with modifications on mating and survival selection. Its fast nondominated sorting procedure, use of elitist strategy, and efficient constraint-handling all facilitate rapid gate drive pattern iteration and discovery.

First, non-dominated sorting is used on the initial population. It is achieved by the selection of individuals that are on the frontier of optimal solutions. If a number of optimal solutions are larger than population size N, then the crowded-comparison approach is used to keep diversity among population members. Based on the rank and crowding distance, parents are selected from the combination of offspring and current generation and usage of the binary tournament selection. Crossover and mutation are applied to the parent population to generate offspring of size N. The new offspring and overall population are sorted again based on the non-domination resulting in best N individuals. The outlined process allows NSGA-II to have good global search and well-distributed nondominated solutions at the Pareto-front.

The upper and lower bounds of control parameters, as well as their number, is based on the active gate driver control dimensionality that has been previously specified in Section 2.3 (8 timing steps, 15 resistance ranges and 12 driving cells). That way, the vector specifying upper bounds of control parameters is provided by

$$Upper\ Bound = [t_0 \dots t_n, r_0 \dots r_n] \qquad (2)$$

where the total number of configurable banks is provided by n , the maximum number of configurable timing steps is given by t_n, and r_n is the number of resistance values that can be selected. A Python framework implementation of single and multi-objective optimisation algorithms has been developed by J. Blank [20]; this library allowed quick integration of the genetic algorithm together with the active gate drive and analysis system. From the formulated problem, NSGA-II configuration parameters were initially selected empirically by evaluating the total number of iterations and convergence rates towards the Pareto-front. The final choice of parameters is shown in Table 1. A detailed description of each parameter can be found in [20].

Parameter	Value	Parameter	Value
Population size	40	Crossover index	10
Offspring number	15	Mutation probability	10
Crossover probability	0.9	Mutation index	10

Table 1 Configuration parameters used by NSGA-II

4. Simulation Results

This section presents results in the following order: First, two-parameter optimisation strategies will be demonstrated together with the shortcoming of using only two metrics for pattern selection. Next three-parameter optimisation will be introduced with 3D visualisation sets facilitating cherry-picking of gate drive patterns based on the optimal results acquired. Finally, suppression of adverse oscillations is demonstrated for circuits with varying power loop inductance.

4.1. Constant Gate Drive Resistance Metrics

For the Evolutionary Multi-objective Optimisation performance analysis and underperforming pattern identification, a baseline data set for circuit operation under different constant gate drive pull-up resistance was first generated. The resistance range used is identical to the one utilised by the active gate driver: {0.5, 1.0, 1.5, 2.0, 3.0, 4.0, 6.0, 7.0, 8.5, 10.0, 12.0, 15.0, 16.0, 32.0, 64.0} Ω. Simulation results for constant drive resistance is provided in Fig. 6 with a solid line demonstrating constant resistance gate drive for varying resistance and three sets of parasitic power L_{loop} inductance. The results demonstrate how increases in inductance and pull-up strength (low resistance) reduce turn-on energy loss by reducing device drain-to-source voltage as a consequence of the high di/dt . Improvements in the loop inductance start to decline as the pull-up strength decreases, and in the region of 6 to 16 Ω, divergence in the energy loss for the same constant resistance is not as drastic. Nonetheless, it is expected to observe a certain level of improvement in the highlighted region for energy loss and current overshoot with the increase of L_{loop}. Both aspects are addressed in Section 4.4.

4.2. Two-Objective Optimisation with NSGA-II

To identify optimal operation regions, NSGA-II was used to perform two-objective turn-on transient optimisation with power loop parasitic inductance of $4\ nH$. Peak current overshoot and energy loss are the two optimisation parameters that the algorithm must reduce at each iteration until an optimal point is reached. After performing transient optimisation for over 8,000 simulations in an autonomous way, NSGA-II produced patterns converging towards the Pareto-optimal front across the majority of the solution space shown in Fig. 6.

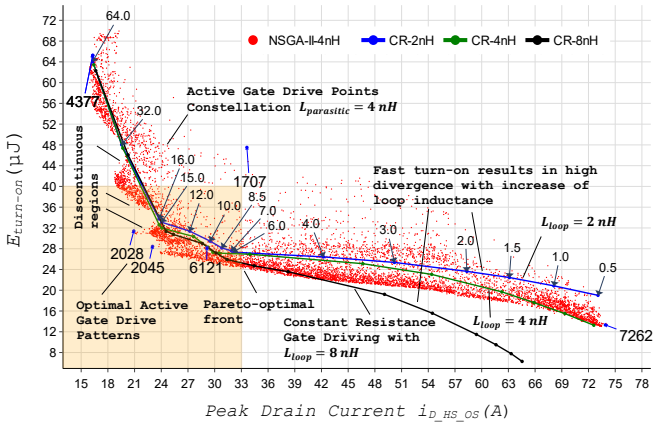

Fig. 6 – Scattered plot simulation results achieved with NSGA-II for loop inductance of 4 nH, together with data for constant resistance gate driving for three values of loop inductance: 2 nH, 4 nH, 8 nH.

Exploring acquired results at the Pareto-front, it is evident that the patterns discovered with NSGA-II can strike a better balance between $i_{D\_HS\_OS}$ overshoot and $E_{turn\text{-}on}$ switching transient loss, compared to fixed-resistance driving. On the other hand, the distribution of points in Fig. 6 indicates that discovered pattern selection can produce both optimal drive patterns - (2028, 2045), suboptimal (6121) and considerably worse results - (1707). Equivalently, not all gate-driving strategies are desirable. Points constellation at the far ends of the graph demonstrates that slow patterns (4377) (mostly high drive resistance) or too aggressive patterns (7262) (mostly low drive resistance) results in either high loss or excessive overshoot, respectively. Operating in these regions undermines GaN device ability of fast switching and poses operation stability concerns.

Simulation results constellations in Fig. 6 all the way to pattern 2045 show Pareto-optimal distribution of results. However, going further along the optimal frontier, the region with higher energy loss contains multiple discontinuous regions in the nonconvex Pareto-optimal front. Indicating that even with the vast number of simulations acquired, a high number of gate control parameters pose challenges for an algorithm to maintain a high spread of non-dominated solutions. A large subset of parameters does not produce enough selection pressure for the population to move towards Pareto-optimal region fast enough. With the explored solution space and known capabilities of the active gate driver, a more refined search can be performed by defining a desirable solution space. For this reason, the highlighted region is used to set inequality constraints in Subsections 4.3 and 4.4, resulting in greater selection pressure and a faster convergence rate of NSGA-II.

Nonetheless, even with data points located at the Pareto-optimal frontier, selection of the unsurpassed solution has some challenges associated with it. This point can be emphasised looking in the highlighted area of Fig. 6. Two gate patterns, 2028 and 2045, have been selected and the corresponding transient waveforms shown in Fig. 7. Even though both patterns are located close to the Pareto-frontier, pattern 2045 demonstrates the highest drain current ringing across all waveforms. In contrast, the use of pattern 2028 shows successful damping of the ringing, improved switching loss, and reduced current overshoot, compared to constant 12 Ω gate driving.

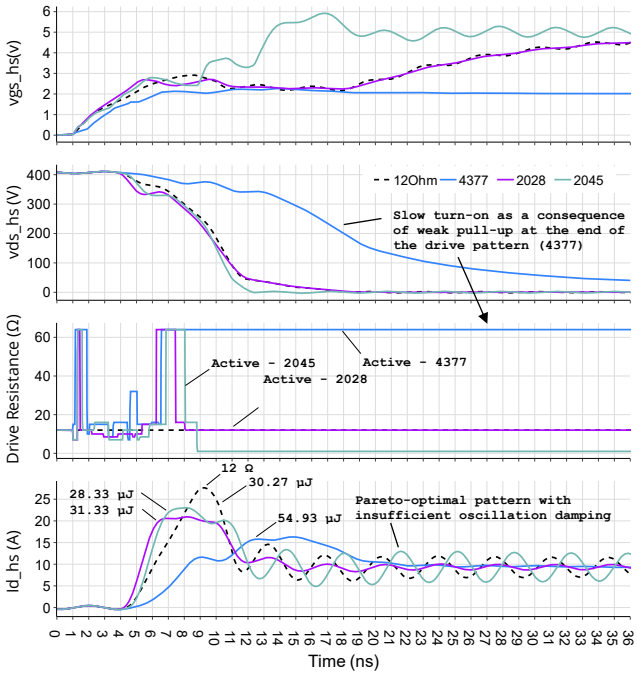

Fig. 7 – Transient waveforms of selected gate patterns from Fig. 6 showing gate-source voltage, drain-source voltage, gate pull up resistance pattern, and drain current with the line labelled switching loss for each transient.

This demonstrates that selecting the “best” pattern from a two-dimensional scatter plot is problematic without knowing the underlying ringing that is accompanying every discovered pattern. In fact,

selection of the unsurpassed pattern can be deceiving and result in ringing that is higher than constant gate driving, as is the case with pattern 2045.

4.3. Three Objective Constrained Optimisation with NSGA-II

With the identified limitation of the two-parameter optimisation strategy, a third parameter is added that describes how well each drive pattern is able to suppress ringing between 45 and 600 MHz. This parameter is obtained by integrating the spectrum of the high-side device current i_{D_HS} between these bounds. It is then used by NSGA-II as part of three-objective optimisations. FFT implementation specifics and justification of the integration interval are outlined in Subsections 3.1 and 3.2.

Discovery of patterns in the desirable solution space requires subjecting NSGA-II to inequality constraints for all three optimisation parameters. The following upper limits have been used: drain current overshoot of 30 A, energy loss of 40 µJ and spectrum integration threshold of 0.2. These limits allow elimination of the majority of irrelevant patterns by having a better non-domination rank than any infeasible solution and, most importantly, converge faster towards the desirable solutions region. Results achieved with active gate driving under control of NSGA-II for $L_{loop} = 4\,nH$ are shown in Fig. 8 with the additional 3rd z-axis revealing the spectrum integration metric.

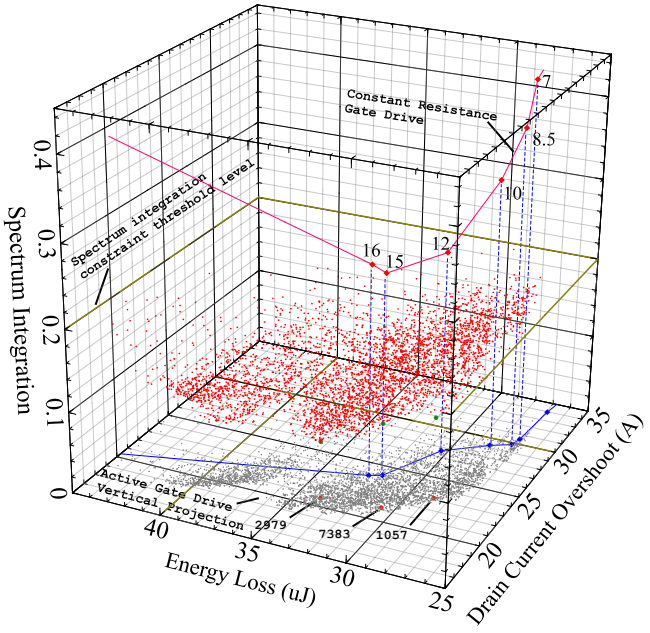

Fig. 8 – Three-dimensional simulation results with constrained optimisation strategy for 4 nH of loop inductance, accompanied with constant gate driving and spectrum metrics for each gate pull-up resistance; grey and blue plots are the projection onto the x-y plane.

The applied constraints confine the solution space, and the optimised patterns are now crowded in a much smaller region. As a result, the x-y plane of Fig. 8. corresponds to the area highlighted in Fig. 6.Patterns with low spectrum integration values in the z-axis correlate with the low ringing of the drain current in the time domain. Vertical projections of the data points onto the x-y plane given for both plots are intended to help with visualisation and depth of field perception. The constant-resistance projection works as a borderline, stipulating clear separation of worst-performing active gate drive patterns and providing the decision-maker with a frontier below which optimal results reside.

Applying inequality constraints for NSGA-II led to an increase in backpressure and gave rise to results previously unseen. Now, not only do a greater number of patterns outperform constant-resistance with lower $E_{turn\text{-}on}$ and $i_{D\_HS\_OS}$ overshoot, but they also demonstrate lower ringing compared to constant-resistance drive with the lowermost integration value of 0.25 for 12 Ω constant resistance.

Due to the nature of multi-objective optimisation, it is seen as unlikely to have a 'globally best' solution. With some results better in one particular optimisation parameter and other solutions better in another. With the obtained set of non-dominated solutions, nailing down the entire set to only a few or even a single solution becomes a Multi-Criteria Decision Making (MCDM) problem.

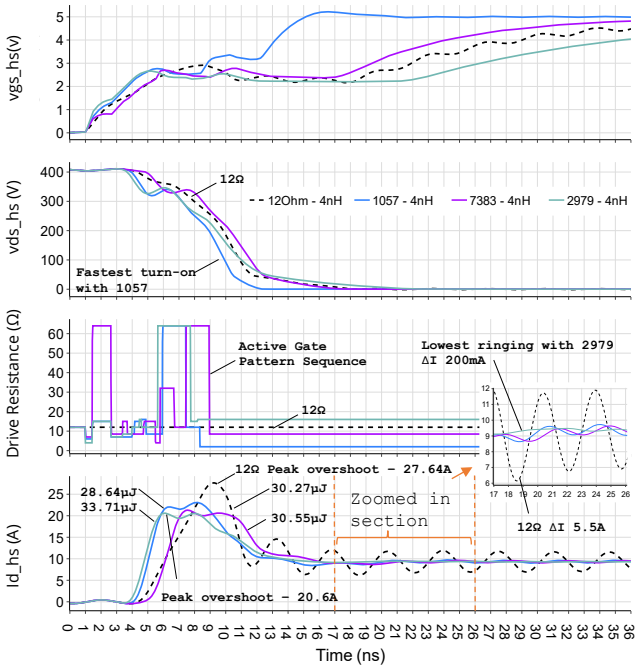

Fig. 9 – Turn-on transient waveforms for selection of three drive patterns (1057, 7383, 2979) and constant resistance of 12 Ω.

However, knowing the design constraints and desirable optimisation outcomes, the decision-maker will be able to cherry-pick the solution that

best suits their design requirements. From the performed simulation, a set of three drive patterns are selected, as highlighted in Fig. 8; each pattern lays at the 3D space of the Pareto-optimal frontier. The subsequent transient turn-on waveforms are shown in Fig. 9. Selected pattern 2979 demonstrates superior damping of oscillations, moderate energy loss of 33.71 µJ and peak current overshoot of 20.6 A. Pattern 1057 achieves the lowest energy loss of 28.64 µJ with a slight increase in ringing and 23 A of peak current overshoot. Finally, pattern 7383 lies in the mid-range of the two selected patterns, with a current overshoot of 21.3 A, energy loss of 30.55 µJ, and a minor increase in ringing. From the selection of patterns, prevalent dominance of the active gate driver against constant resistance is witnessed. Equally, the constellation of Pareto-optimal results and tight crowding of solutions demonstrates the advantageous use of constrained optimisation.

4.4. Power Loop Parasitic Inductance Adverse Effects Elimination

It is not always possible to achieve the optimal balance of PCB routing, components placement and subsequent loop inductance minimisation. Hence, optimising and shaping of the switching transient for high loop inductance becomes a feasible solution. For the next set of simulations, the parasitic loop inductance L_{loop} shown in Fig. 2 has been swept across the following values: {2 nH, 4 nH, 8 nH}. Simulations with constant gate driving have been performed first, followed by NSGA-II active gate driver transient optimisation. Apart from using similar inequality constraints introduced in Subsection 3.4, data points with spectrum integration value above 0.1 are omitted to clear up the solution space and eliminate all data points with higher than tolerable values of ringing; the final results are shown in Fig. 10.

Interpolation of outlined data is easier to perceive, starting from projections of the scatter data and constant resistance onto the x-y plane. Both signify a slight decrease in switching loss and current overshoot with the increase of parasitic inductance, namely emphasised by inductance frontier levels on the x-y plane. As has been shown previously in Fig. 6, energy loss reduces with an increase of pull-up strength or use of higher loop inductance with the same pull-up resistance. Similar results are observed in Fig. 10 where the divergence of both constant resistance and active gate patterns is evident from the x-y plane projections.

A speed-up in turn-on transient and high di/dt induces voltage across the parasitic L_{loop} that opposes the very same changing current, “delaying” current flow through the GaN device and decreases energy loss. Similarly, slow turn-on leads to a decrease in di/dt transition, less current opposition, extension of transient crossover and rise in energy loss. Driving a GaN device with a constant resistance and increased loop inductance comes at the expense of oscillation and ringing, which is evident from the z-axis spectrum integration values in Fig. 10.

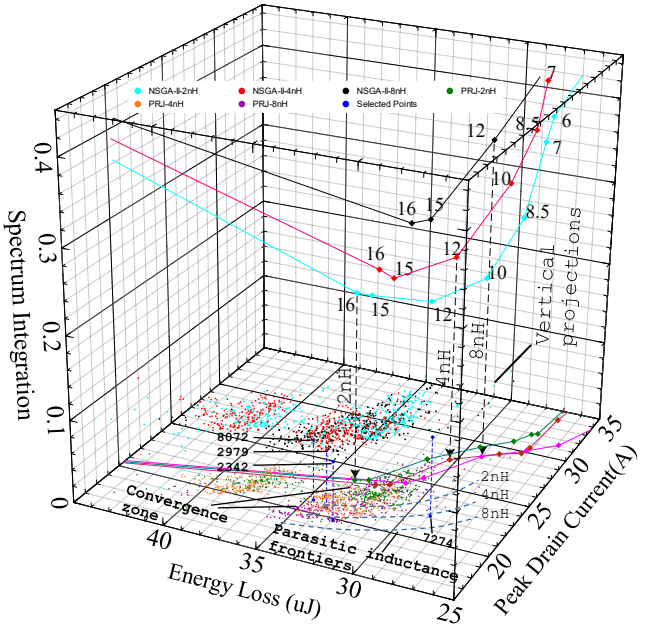

Fig. 10 – 3D scatter plot for three sets of loop inductances; results provided for constant resistance driving and constrained NSGA-II optimisation, with projection onto the x-y plane for both sets of results and traced frontier levels for increasing values of parasitic inductance.

Spectrum integration results demonstrate the ability of NSGA-II optimised drive pattern to reduce spectral frequency peaks and dampen adverse ringing effects for all three sets of parasitic inductances. However, the selection of optimal drive patterns from the constellation of results is an MCDM problem and is mainly design-driven. Nonetheless, the user is provided with a clear selection of drive patterns that can be chosen based on the application needs and desirable improvements. As part of this work, a set of three patterns has been selected based on the lowest level of spectrum integration results across the z-axis. Drain current transient waveforms in Fig. 11 demonstrate a successful reduction in peak current overshoot to 21.2 A for $L_{loop} = 2\,nH$ with pattern 8072, and 19.8 A for $L_{loop} = 8\,nH$ with pattern 2342.

Voltage peak oscillation dropdown at the DC-link has been reduced by 10 V in comparison to constant gate drive. Although an optimised gate drive pattern completes the switching transition fast enough not to incur excessive losses, a minor increase in energy loss across all three active drive

patterns is observed from line labelled results in Fig. 11.

The selected drive patterns are the best at damping drain current oscillations that unfavourably happens at the expense of energy loss. Hence, if a slight increase in current overshoot and ringing is tolerable, the user could select pattern 7274, outperforming constant driver resistance with energy loss of 28.86 µJ, peak current overshoot of 22.2 A, and a slight increase of ringing compared to pattern 2342, primarily due to the stronger pull-up at the end of the drive pattern.

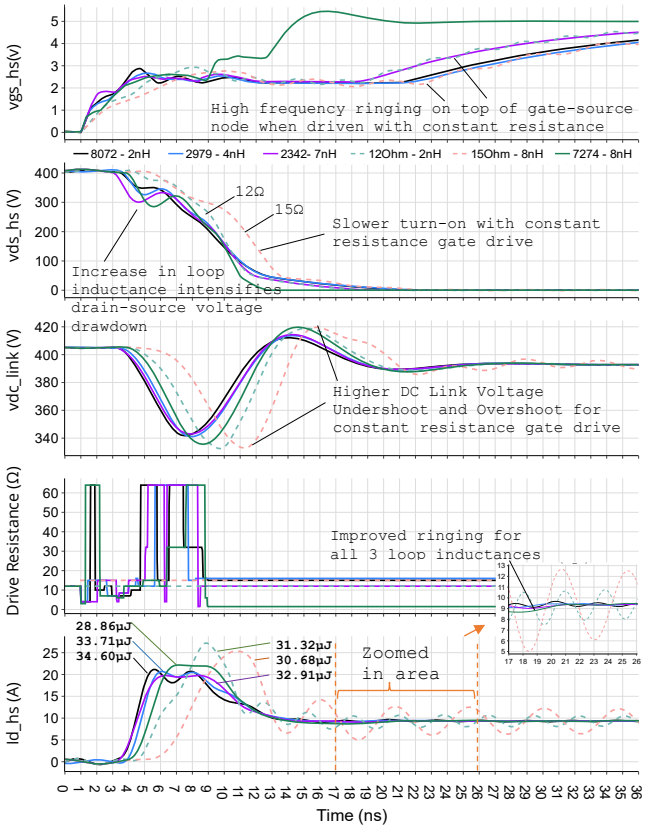

Fig. 11 – Simulation turn-on transient results for a set of 3 in loop inductance values {2nH, 4nH, 8nH} with active gate optimisation strategy for each one selected based on lowest ringing achieved, compared together with best constant resistance driving for L_{loop} of 2 nH and 8 nH with the line labelled switching loss and zoomed-in section of drain current waveform.

Improvements in oscillation are more evident with the FFT analysis shown in Fig. 12. Results in the frequency domain demonstrate a reduction in spectral content across the whole range of frequencies. That way, a circuit with $L_{loop} = 8\,nH$ driven by the 2342 active gate drive pattern reduces the 220 MHz frequency peak by 29.4 dB. relative to the level seen with 15 Ω constant gate resistance. Similarly, spectral peaks for other gate drive patterns have been attenuated in comparison to constant gate drive. Pattern 7274 demonstrates comparable improvement in spectral content reduction. However, due to more aggressive turn-on, it possesses higher ringing in higher frequency ranges starting from 500 MHz all the way to 2 GHz. In contrast, spectrum levels for other patterns in high-frequency ranges have been reduced by 10 dB on average, demonstrating the ability of the active gate drive to counteract higher than anticipated power loop parasitic inductance and ringing.

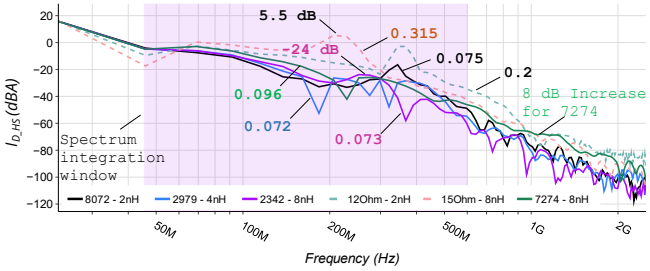

Fig. 12 - FFT spectral envelopes for five simulated switching time-domain transient waveforms from Fig. 11 and line labelled integration results in the region from 45 MHz to 600 MHz

5. Conclusions

This paper addresses the process of GaN active gate drive pattern discovery where nature-inspired natural selection, mutation, and survival of the fittest have been used by an NSGA-II algorithm to iterate and methodically frame gate-drive patterns without human intervention in an autonomous way. The provided optimisation strategy and analysis framework is topology-agnostic and can be implemented for any type of design where orchestration of pull-up and pull-down resistance can be beneficially used for switching transient waveform improvements.

The use of only energy loss and current overshoot metrics proved to be insufficient to provide the decision-maker with enough information on how well a particular pattern dampens oscillations. Performing FFT analysis for drain current transient and subsequent spectral envelope integration resulted in a single performance metric that was successfully used by NSGA-II to optimise the switching transient, dampen current oscillations and alleviate high-frequency spectral peaks and EMI. Visualising results in a 3D solution space allowed the identification of optimal operation frontiers and elimination of outliers that do not satisfy design requirements. Similarly, the rapid pattern iteration process has proven the ability to mitigate high values of parasitic loop inductance and exploit it to reduce current overshoot and energy loss, further facilitating and utilising high-speed switching capabilities of GaN devices for hard switching applications with a reduced risk of being damaged. In the end, the decision-maker is provided with a set of optimal patterns, any of

which could be cherry-picked based on the crucial design requirements.

5.1. Further Work

This work demonstrates an optimisation strategy for a single pull-up resistance. However, it is possible that higher control granularity and switching transient improvements can be achieved by driving pull-up and pull-down resistances in tandem.

Among the insights from the conveyed work was the fact that drain current overshoot has a direct correlation with spectral content in the frequency domain. Selection of the drive pattern can be problematic if no ability to interact with a 3D plot exists. Hence, it seems possible that providing only energy loss and spectrum integration data in a 2D scatter plot will be enough to determine an optimal drive pattern, making it possible to eliminate the $i_{D\_HS\_OS}$ parameter altogether, further simplifying optimal pattern selection.

6. References

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