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MEDIUM VOLTAGE DC SOLID STATE CIRCUIT BREAKER BENCH TEST

Brandt, Jonathan J.

Monterey, CA; Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL

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THESIS

MEDIUM VOLTAGE DC SOLID STATE CIRCUIT BREAKER BENCH TEST

by

Jonathan J. Brandt

September 2022

Thesis Advisor: Di Zhang
Co-Advisor: Yuntao Xu

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Next generation fleets will rely on medium-voltage direct-current (MVDC) electric power distribution systems utilizing high power density and high efficiency components. One key gap to make such MVDC systems feasible is a super-fast, high efficiency, and high-power density protection device. The U.S. Navy has previously developed a 1 kV, 1 kA solid state circuit breaker (SSCB). A new 2 kV, 1.2 kA SSCB has been designed by NPS with collaborating partners that has quadrupled power density. This innovative insulated gate bipolar transistor (IGBT)-based SSCB consists of anti-series IGBT modules, a parallel resistor-capacitor (RC) branch, and an electronically triggered metal-oxide varistor (MOV) branch. The novel electronically controlled MOV is comprised of a MOV in series with a silicon controlled rectifier (SCR) passively triggered during the IGBT turn-off process, improving the trade-off between the leakage current and clamping voltage. The use of a lower IGBT gate voltage allows the elimination of current limiting inductors, increasing the SSCB power density. This thesis focuses on the switching and thermal tests necessary to validate the implemented concepts, and the data will be used for down-selecting technical directions, improving the SSCB performance. The results show that the SSCB is sufficient to interrupt most faults while containing peak current and voltage within design parameters and the efficiency target can be met with comfortable thermal margins.

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MEDIUM VOLTAGE DC SOLID STATE CIRCUIT BREAKER BENCH TEST

Jonathan J. Brandt
Lieutenant, United States Navy
BS, Citadel, Military College of South Carolina, 2016

Submitted in partial fulfillment of the
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Approved by: Di Zhang
Advisor

Yuntao Xu
Co-Advisor

Douglas J. Fouts
Chair, Department of Electrical and Computer Engineering

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ABSTRACT

Next generation fleets will rely on medium-voltage direct-current (MVDC) electric power distribution systems utilizing high power density and high-efficiency components. One key gap to make such MVDC systems feasible is a super-fast, high-efficiency, and high power density protection device. The U.S. Navy has previously developed a 1 kV, 1 kA solid state circuit breaker (SSCB). A new 2 kV, 1.2 kA SSCB has been designed by NPS with collaborating partners that has quadrupled power density. This innovative insulated gate bipolar transistor (IGBT)-based SSCB consists of anti-series IGBT modules, a parallel resistor-capacitor (RC) branch, and an electronically triggered metal-oxide varistor (MOV) branch. The novel electronically controlled MOV is comprised of a MOV in series with a silicon-controlled rectifier (SCR) passively triggered during the IGBT turn-off process, improving the trade-off between the leakage current and clamping voltage. The use of a lower IGBT gate voltage allows the elimination of current limiting inductors, increasing the SSCB power density. This thesis focuses on the switching and thermal tests necessary to validate the implemented concepts, and the data will be used for down-selecting technical directions, improving the SSCB performance. The results show that the SSCB is sufficient to interrupt most faults while containing peak current and voltage within design parameters and the efficiency target can be met with comfortable thermal margins.

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Table of Contents

List of Figures

List of Tables

List of Acronyms and Abbreviations

AC	Alternating Current
BAA	Broad Agency Announcement
BOD	Breakover Diode
CB	Circuit Breaker
DC	Direct Current
DLO	Diesel Locomotive Cable
EMI	Electromagnetic Interference
FLASH	Fast Light-weight Altitude-Ready Solid State Circuit Breaker for Hybrid Electric Propulsion
GPM	Gallons per Minute
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
MVDC	Medium Voltage Direct Current
MW	megawatt
NASA	National Aeronautics and Space Administration
NEAT	NASA Electric Aircraft Testbed
NPS	Naval Postgraduate School
ONR	Office of Naval Research

RC Resistor-Capacitor

RTD Resistance Temperature Detector

SCR Silicon Controlled Rectifier

SSCB Solid State Circuit Breaker

STO Soft Turn Off

TVS Transient Voltage Suppressor

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CHAPTER 1:
Introduction

Medium Voltage Direct Current (MVDC) architectures for power distribution systems are becoming more attractive as industries are realizing the impacts of high-efficiency, high-power density, Direct Current (DC) distribution systems. MVDC distribution systems have been implemented or researched in maritime vessels [1]–[8], DC microgrids [9], [10], and electrified aircraft [11]–[13]. The U.S. Navy demand signal started as early as 2013 with Office of Naval Research (ONR) Broad Agency Announcement (BAA) calling for research into MVDC systems [14].

The rising importance of MVDC systems has led to research into the protection devices used between electric power sources, the distribution buses, and the loads [15]. In Alternating Current (AC) systems, a mechanical Circuit Breaker (CB) is typically used which can open contacts and interrupt fault current at zero crossings of the AC currents . DC power systems do not inherently have a zero current crossing, and must therefore, utilize a fault interruption system that can handle high voltage and high current simultaneously. Solid State Circuit Breaker (SSCB) technology can manage this fault interruption with no moving parts, no arc flash, and at rates far superior to their legacy counterparts [9], [15], [16].

1.1 Significance of Research

The SSCB tested in this study is a high-power density, high-efficiency, and high-reliability design with a power rating of 2.4 MW for hybrid-electric aircraft applications. Due to its benefits, such a SSCB can also be applied in U.S. naval vessels, DC microgrids, and other systems utilizing DC distribution systems. The compactness and low loss of the SSCB can provide designers with increased design freedom and flexibility.

An MVDC distribution system relies upon connecting AC generators to the DC bus through various power electronics elements, such as three phase rectifier and inverters [7], [8]. Through the use of power converters, the speed of the generators is decoupled from the load conditions, including the load level and required motor speed. In other words, the generators may operate at any speed to achieve the highest system efficiency regardless of the power

requirements of the loads [2], [3]. In addition, the generator does not need to work at the harmonics of 50 or 60 Hz. This will further enhance U.S. Navy capabilities by reducing the acoustic signature of the ship [17].

On critical systems, two electric sources are provided for reliability to ensure protection against loss of power. In an AC system, when two parallel sources of electric power are combined, in order to minimize the associated current surge when the CB is closed, the amplitudes, phase angle, and frequency of the voltages on the two sides of the CB must be matched. Critical DC power systems technology has previously utilized auctioneering diodes, providing power from one of at least two DC sources to the load, depending on the operating source with the highest voltage at the time less the voltage drop across the diode [18]. These auctioneering diodes and the critical loads themselves still need fault protection provided by an SSCB. However, without an AC source with its inherent large impedance, the total system impedance will be reduced, and the MVDC system and SSCB need to account for a potentially higher surge current developing as a result [19]. The DC distribution system can also benefit from reduced power cabling size as the AC distribution system is affected by the skin effect of transmission cables and loads have no reactive current component, limiting the total system current to only the real component transmitted through the entire power cable [17].

MVDC research interest was expressed by ONR in the 2013 BAA as well as in the Technology Development Roadmap [4], [14]. Further guidance and study has been conducted with efforts for interface standards for naval vessels [20]. These efforts have been necessary for describing the future of U.S. Navy MVDC distribution and giving guidance to future research. This direction has resulted in developments and improvements in electric propulsion, pulsed power loads, and large DC loads on a growing MVDC bus [7], [8], [21].

In addition to researches into naval applications, MVDC distribution has been explored for aviation applications [9], [12], [13]. Similar advantages that have been capitalized in maritime applications may also be utilized in aviation development. High power densities are necessary due to the weight limitations of an airframe for high system efficiency, as well as space constraints. However, added challenges exist due to operating through lower atmospheric pressures [13].

Advances in SSCB technologies have made the use of MVDC distribution possible. Improvements in the voltage blocking and current carrying capabilities have made Si Insulated Gate Bipolar Transistor (IGBT) selection feasible at useful power levels [22]. This has enabled MW capable devices for power distribution, bus coupling, and load protection [9].

1.2 Research Method

SSCB technology requires gating circuitry to control the on-state and off-state of the power electronics devices, a method to clamp the peak voltage and dissipate inductive energy within the system during the turn-off process, and the current carrying devices under normal operating conditions. The system developed and tested in this research can simulate a rigid DC bus supplying load currents through the SSCB. The SSCB is tested to verify the voltage blocking, current carrying, thermal management, and fault current interruption capabilities. Testing of the SSCB included controlling the current carrying devices, modifications and improvements to the voltage clamping circuitry, and methods to reduce overall inductance within the SSCB for peak voltage limitation. Two different tests are conducted: a switching performance test to quantify the fault protection capabilities of the SSCB and a thermal performance test to quantify thermal efficiency properties of the SSCB. The switching performance test is a high voltage, high current transient test performed in an iterative process that improves various components and functions throughout the SSCB as well as improving the dynamic performance of the SSCB. The thermal test is a low voltage, high current continuous test performed to evaluate the thermal performance of the IGBT, the free-wheeling diode, the cold plate of the SSCB and the cooling system. The physical hardware of the system was assembled and tested within an interlocked safety cage due to the high voltage and current present throughout the testing.

1.3 NASA FLASH Introduction

The National Aeronautics and Space Administration (NASA) Fast Light-weight Altitude-Ready Solid State Circuit Breaker for Hybrid Electric Propulsion (FLASH) SSCB development began in early 2020 [23]. This proposal offered a simple and elegant solution for achieving an SSCB with nominal specifications for a coupling device in a hybrid-electric, subsonic aircraft. The plan detailed a 3 year, 3 phase project to advance existing technologies

in a novel implementation to achieve a 2 kV, 1.2 kA SSCB rated for 35 000 feet altitude. This advanced SSCB would continue to promote U.S. Navy deployment of new technologies on aircraft and promote further applications in maritime vessels and DC grids requiring MVDC distribution and high power DC loads [4], [23]. This thesis focused on the second phase of this development: a 2 kV, 1.2 kA SSCB prototype, down-selecting the ideal components to meet or exceed design specifications and deliver a ready-to-test product for NASA Electric Aircraft Testbed (NEAT).

The Naval Postgraduate School (NPS) design proposed to NASA was for a Si semiconductor device that utilized "advanced insulation, control, and packaging technologies" to achieve a novel SSCB for hybrid-electric propulsion aircraft [23]. To make this device suitable for aircraft, it needs to have high power density and high efficiency due to aircraft weight and size limitations. The project would expand upon current U.S. Navy research efforts on MVDC SSCBs that were only in the 1 MW range and provide a 2.4 MW solution with higher power densities than previously achieved [4]. The design criteria included: 2 kV DC voltage, 1.2 kA DC current, 99.5% efficiency, 100 kW/kg specific power, altitude capability at 35 000 ft, and a response time in the tens of μs [23] and is shown in Figure 1.1.

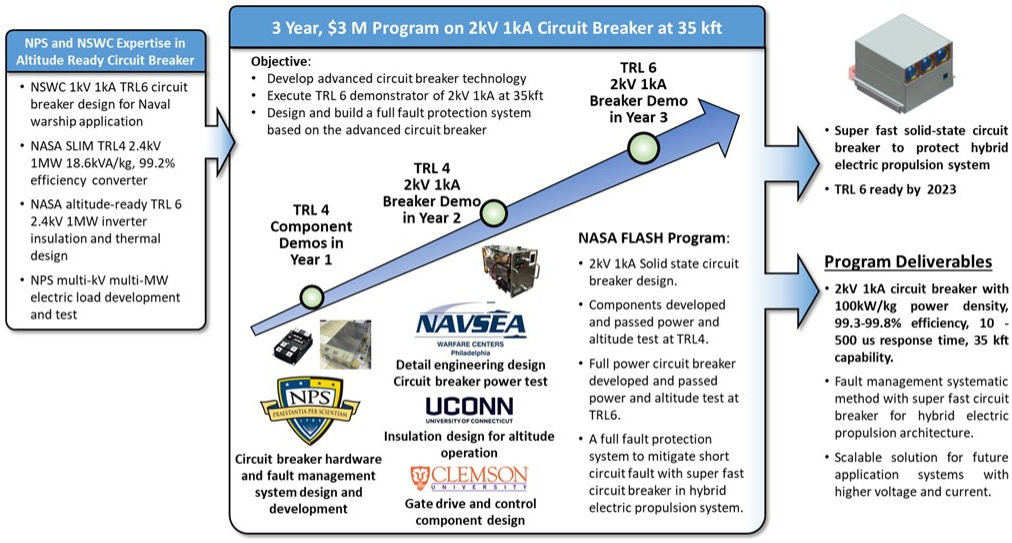

Figure 1.1. Three Year Timeline for SSCB Development and Testing. Source: [23].

This three year project, specifically the second phase, was the impetus for the hardware benchmark testing performed in Chapter 3 and Chapter 4.

1.4 Chapter Overview

Chapter 2 discusses the topology and operating principles of the SSCB as well as the NASA FLASH SSCB design improvement theory. Chapter 3 discusses the fault performance switching test used for the SSCB including the hardware, instrumentation, test setup and procedure as well as the results of the test and improvement iterations. Chapter 4 discusses the thermal efficiency performance test used for the SSCB including the hardware, instrumentation, test setup and procedure as well as the results of the test iterations. Finally, Chapter 5 summarizes the testing results and presents ideas for future MVDC SSCB research.

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CHAPTER 2:
Background

In this chapter, the SSCB is introduced. A detailed description of SSCB topology and operating principles are discussed. Understanding the individual components and their functions are essential for the operation as a whole of the SSCB. Finally, the improvements proposed for an SSCB for an MVDC distribution system on a hybrid-electric aircraft are discussed which are the basis for this research project.

2.1 Solid State Circuit Breaker Fundamentals

SSCBs are semiconductor-based power and load protection devices that have much faster fault interruption capability compared with their legacy, mechanical counterparts. These semiconductor devices can interrupt fault currents without arcing due to no moving parts, allowing for longer interruption lifetime and less required maintenance [9]. Their prevalence has grown from the laboratory to commercial and military applications through advances in MVDC technologies. The range of applications continues to grow as power distribution systems are branching from AC to DC distribution methods. The shift in distribution systems has been driven by increased demand for fuel efficiency, more rapid power demand shifts, and ease of maintenance [3], [5], [6], [10]. In military applications, the newest classes of ships utilize electric propulsion engine rooms, DC distribution systems, and pulsed power loads on the DC bus which all require SSCB technology to interface the components of the system [4], [7], [8], [17], [21]. The high-power density, high efficiency, and high reliability of these components have made MVDC distribution and the SSCB essential for the future naval force. In addition to naval vessels, SSCBs are being developed for use in aircraft. Along with reducing carbon emissions and achieving higher fuel efficiencies, the requirements from large DC loads are demanding improvements upon SSCBs [13].

The legacy mechanical circuit breaker used in AC systems relies upon mechanical contacts that are separated to interrupt the system currents from source to load. This mechanical interruption is possible with minimal arcing due to a natural zero crossing of the AC current. In higher power systems, a mechanical circuit breaker may also include an arc chute, which

allows for any arc generated during power interruption to be dissipated through the high resistance chute. Additionally, the mechanical circuit breaker relies upon an air gap to provide galvanic isolation, removing the voltage from one side of the contacts to the other. This system, due to the mechanical actuation of large contacts for interruption, as well as the need to wait for a natural zero crossing, can take as long as tens of milliseconds for fault protection to occur. The mechanical actuation causes wear and tear on moving parts, and the arcs generated can pit the contacts over time, requiring additional maintenance to repair and replace these components.

The legacy AC mechanical circuit breaker is insufficient for MVDC distribution systems as there are no inherent zero current crossings in DC systems. Any interruption of current by these devices will generate severe arcs, requiring larger arc chutes than seen on an equivalent AC system. An SSCB utilized in MVDC applications prevents arc generations through the use of solid-state power electronic devices. The current interruption by these devices has no moving parts, eliminating the process by which an arc is generated. To dissipate the inductive energy within the system, a voltage clamping device is used that rapidly converts the energy into heat.

The inductive energy mainly comes from system line inductance, the current limiting devices, and parasitic inductance within the solid-state devices [11]. The basic equation describing the inductance, voltage, and current relationship is described as

$$di/dt = \frac{V_{sys}}{L_{sys} + L_{CB}} \tag{2.1}$$

where L_{sys} is the system line inductance and L_{CB} is the current limiting inductance added to the SSCB and any parasitic inductance within the SSCB control circuitry. The peak fault current achieved during fault interruption is defined as

$$I_{pk} = I_{th} + \frac{V_{sys}}{L_{sys} + L_{CB}} * t_d \tag{2.2}$$

where I_{th} is the threshold current for fault detection, and t_d is the response time from fault detection to current interruption. Based on Equation 2.2, if L_{sys} is close to zero in the worst case, a current limiting inductor must be installed in the SSCB to limit di/dt, such that the peak current will not exceed a maximum threshold within t_d. Although a lower I_{th} and t_d

can help to limit the fault current, allowing the protection system to respond to a system fault earlier and faster, the impact is limited if the system current rising rate is very high. In addition, a lower I_{th} or t_d could make the SSCB sensitive to the system noise, especially in a harsh Electromagnetic Interference (EMI) environment, such as the converter based high power system.

If the fault current is interrupted by the semiconductor device directly, a transient over-voltage can damage the SSCB. The transient over-voltage can be estimated as

$$V_{SSCB} = V_{sys} + L_{total} * di/dt \tag{2.3}$$

where the system inductance, L_{total} is the algebraic sum of system inductance and SSCB parasitic and installed inductance. For example, if the total inductance is 10 μH and the di/dt is 1 kA/μs, such a transient over-voltage is 10 kV, which is likely in excess of design parameters. To overcome this issue, a voltage clamping circuit, such as a Metal Oxide Varistor (MOV), is connected in parallel with the SSCB to limit the maximum voltage experienced by the circuit.

2.2 SSCB Design Considerations

An SSCB consists of three main elements: the current carrying and interrupting device, the fault current limiting device, and the voltage clamping and energy dissipation circuit. Typically, the current carrying and interrupting device is an IGBT, Metal Oxide Semiconductor Field Effect Transistor (MOSFET), or Integrated Gate Commutated Thyristor (IGCT) [9]. These semiconductor devices have seen improvements over the years that have led to higher voltage and higher current carrying capabilities while reducing on-state power losses, making them the backbone of MVDC electrical distribution systems and supporting newer high power loads. While the details and intricacies vary within a given SSCB topology, these components are generally universal to any given system. Other components include passive or active sensing and controlling devices, remote operating and communications devices, or additional semiconductor devices to overcome previous inadequacies in voltage blocking, current carrying, or energy dissipation effects [9], [10].

Because the IGBT itself can only conduct current in one direction, an anti-parallel diode is

placed from the IGBT emitter to the IGBT collector. This allows for bidirectional current conduction. However, this configuration only allows voltage blockage in the forward direction when the IGBT is in the off-state. To ensure voltage blockage in both directions, two anti-series IGBTs are necessary. Without the second IGBT in an anti-series configuration, the IGBT would only be able to block voltage in the forward direction, as the anti-parallel diode becomes forward biased if a negative voltage was applied across the IGBT as seen from collector to emitter. The IGBTs are placed in a configuration where the conduction path in either direction goes from emitter to collector of one IGBT through the diode, then collector to emitter through the second IGBT in the on-state. This is referred to as an "ECCE" configuration. The second configuration is where the emitters of the IGBTs are connected, referred to as an "CEEC" configuration, and is shown in Figure 2.1. Both configurations are functionally the same with current conduction through one IGBT and one diode.

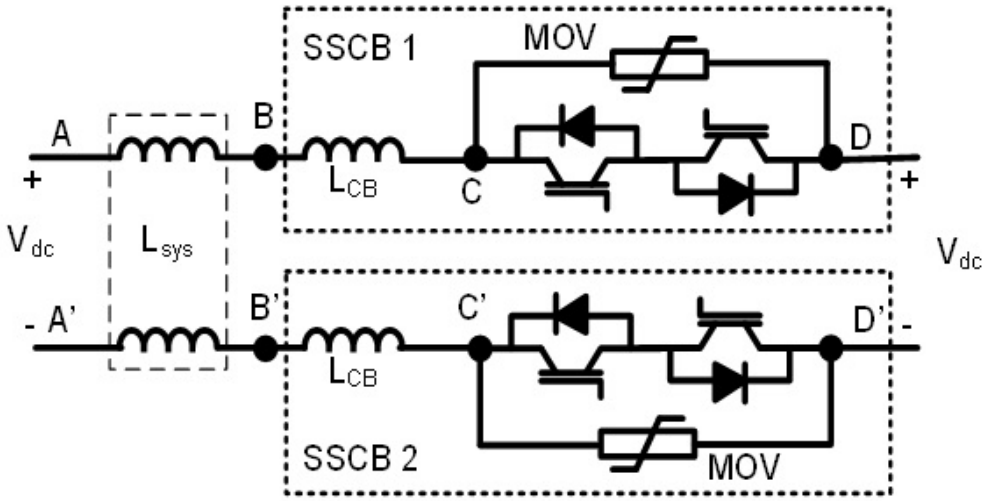

Figure 2.1. Generic "CEEC" SSCB Topology

The two anti-series IGBTs with anti-parallel diodes are connected with a parallel MOV branch. The MOV acts as the energy dissipation circuitry, providing a path for current commutation when the SSCB is turned off. Additionally, the MOV branch provides for voltage clamping, acting in a highly non-linear fashion when dissipating the inductive energy of the system. Also shown in Figure 2.1 is a series connected, current limiting inductor.

The inductor, when installed, aids the SSCB in limiting the current rate of change during a fault. This device yields additional time for the SSCB to detect and clear a fault current while minimizing the peak current experienced during the fault. However, the inductor adds additional weight to the system, dramatically lowering the SSCB power to weight ratio, or, the specific power. Additionally, because the inductor is in line with the SSCB, it will carry full system current when operational, adding further losses to the system, reducing the SSCB efficiency. L_{sys} is the system inductance of the MVDC system determined mainly by the length and type of cabling used. L_{CB} is the parasitic inductance of the SSCB as well as any additional current limiting inductor.

To ensure single-point fault protection, demonstrated in Figure 2.2, IGBTs are placed in the anti-parallel, anti-series configuration as shown in Figure 2.1. In Figure 2.1, an SSCB is placed on each pole. This layout does demand four IGBTs within a single conduction loop, increasing the amount of conduction losses throughout the system, affecting the total system efficiency. However, this configuration can allow the system to continuously operate at full power with single point ground fault.

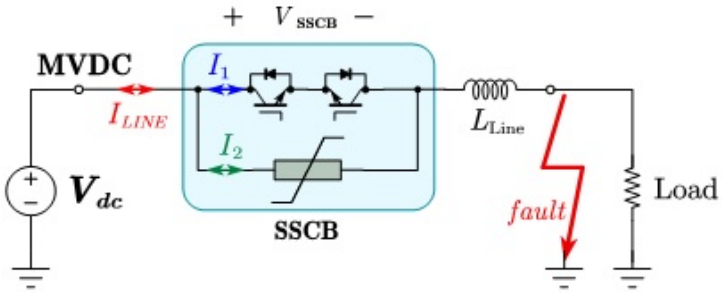

Figure 2.2. A Basic Fault on One Leg of the SSCB

In a critical system on board an aircraft, for example, the system must be capable of continual operation at full power with single point ground fault. For this reason, an SSCB is installed on each pole of the MVDC distribution legs. Should a single point fault occur, one SSCB would be sufficient to interrupt that fault as shown in Figure 2.2. In this case, both SSCBs would share the voltage blocking from the source to the fault. Should a second fault on the opposite pole occur, this second fault may bypass one of the two SSCBs in the system, requiring a single SSCB to interrupt the fault current and block all system voltage. Shown

in Figure 2.3, one fault occurs downstream of the positive pole SSCB and a second fault occurs on the upstream side of the negative pole SSCB. This fault bypasses the negative pole SSCB as viewed in Figure 2.3.

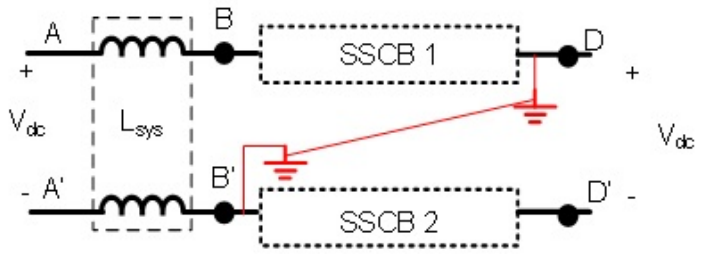

Figure 2.3. Design Case Fault Where One SSCB is Removed From the System

This is the fault each SSCB needs to be designed to handle. Thus, the IGBT and the auxiliary system components must be rated sufficiently to handle the total system voltage as well as any additional inductive voltage experienced during transient fault protection. To reduce cost and weight, the voltage rating of the device should be minimized to limit conduction losses from the SSCB.

2.2.1 Solid State Circuit Breaker Functionality

To enable the IGBT-based SSCB, a positive voltage, called gate voltage, is supplied to the gate terminal of the IGBT which allows the device to conduct in the forward direction. This is referred to as the IGBT on-state. When the IGBT is carrying current, I_C, the voltage across the IGBT, V_{CE}, will increase correspondingly. The voltage and current relationship is non-linear which is heavily affected by applied gate voltage, V_{GE}, as is shown in Figure 2.4, and is referenced to a 150 °C junction temperature. Due to the physics in developing a conduction channel, the higher the gate voltage applied, the lower the resistivity within the IGBT channel. In turn, this results in lower conduction loss.

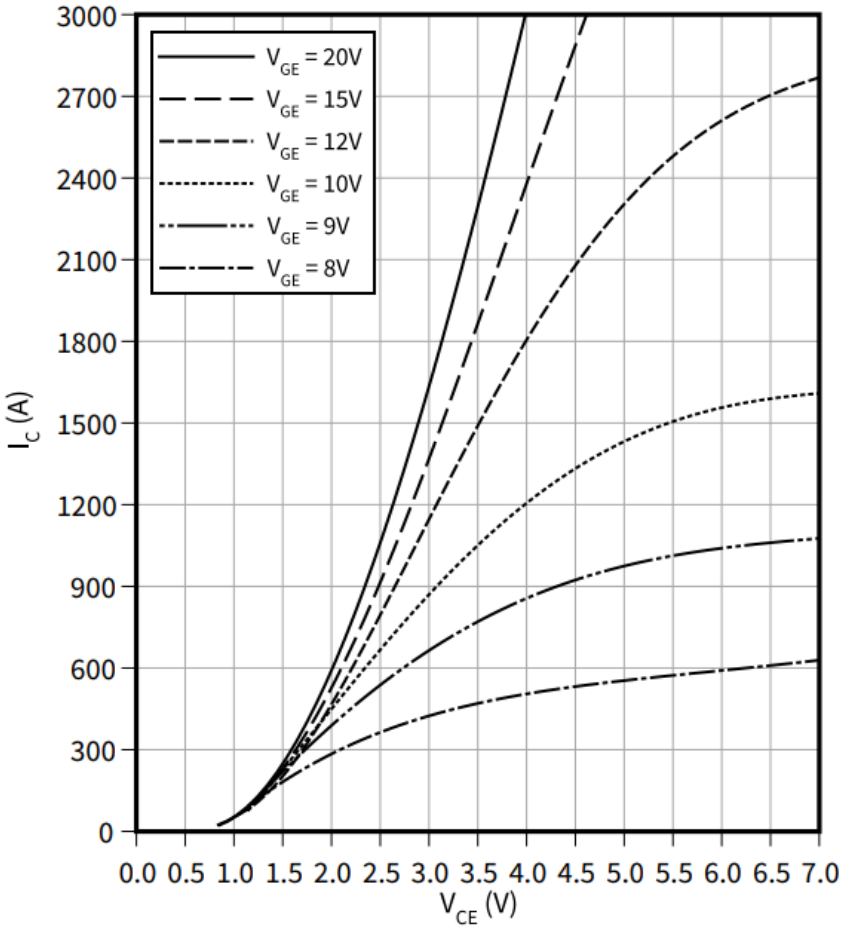

Figure 2.4. IGBT Operating Curves for Various Gate Voltages. Source: [24].

The IGBT in an SSCB normally operates in the saturation region when the load current is within its rated range, and the voltage drop across the device is only a few volts. However, once the current is sufficiently high, the IGBT will exit the saturation region and enter the active region. Consequently, the IGBT voltage will increase dramatically with the load current, until the IGBT reaches the saturation current level, which appears as a flattened curve in Figure 2.4. However, a small change in gate voltage in the active region can result in massive shifts in the saturation current level.

To turn off the IGBT, the gate voltage is removed, or forced to a negative value. As the voltage potential is removed from the gate, or a negative voltage is applied, the conduction channel

rapidly narrows until the current is reduced to zero. However, the inherent inductance within the system will continue to drive the current. As the IGBT is turned off, the current is commutated to the energy dissipation component, generally a MOV.

The MOV performs two functions: it clamps the voltage rise due to the inductance of the system as described in Equation 2.1 as well as dissipates the inductive energy into heat. A MOV can clamp the voltage similar to back-to-back zener diodes. When the voltage across the MOV is low, the resistance internal to the MOV is very high, mirroring an open circuit, allowing very little leakage current through the device. As the voltage across the MOV increases, the MOV resistance decreases. Thus, limited voltage will appear across the MOV when it is carrying high fault current. In other words, the MOV clamps the voltage across the IGBT, so the IGBT does not experience excessive voltages described in Equation 2.3, which may result in punch through of the solid-state device, causing failure.

Since the clamping voltage of the MOV is higher than the DC bus voltage, the voltage difference will drive the system fault current down eventually clearing the fault. During the fault clearing process, the current of the MOV can be expressed as

$$i_{MOV} = i_{peak} - \frac{V_{clamp} - V_{DC}}{L_{sys} + L_{CB}} * t_{clear} \tag{2.4}$$

where L_{sys} and L_{CB} are the system and SSCB inductances respectively, V_{clamp} is the clamping voltage of the MOV, i_{peak} is the peak fault current, and t_{clear} is the time to clear the fault.

Since the MOV is carrying high fault current and withstanding high clamping voltage at the same time, the MOV generates high power loss which can only be absorbed by the MOV itself. Such dissipated energy will heat the MOV internally, causing degradation or even failure of the metal-oxide material. A single event with sufficient energy or several events with sufficient accumulated energy in a short period may cause the same catastrophic effect.

If the clamping voltage is considered approximately constant, the total energy absorbed by the MOV can be calculated as

$$E_{MOV} = \frac{1}{2} * (L_{sys} + L_{CB}) * {I_{peak}}^2 * \frac{V_{clamp}}{V_{clamp} - V_{DC}} \tag{2.5}$$

where the inductance, voltage, and current are defined the same as in Equation 2.4. By

fixing the system operating voltage, and selecting an appropriate clamping voltage, the energy dissipated through the MOV is proportional to the sum of the inductances and the square of the peak current. Minimizing the energy dissipated in the MOV will result in less required maintenance to replace a MOV prior to failure, generating longer useful lifetime of a MOV and the SSCB.

Assisting the MOV in operation, a Resistor-Capacitor (RC) snubber may be included. The introduction of a capacitive element into the circuit limits the voltage rate of change during the turn-off transient expressed as

$$i_C = (C_{snubber} + C_{CB}) * dv/dt \tag{2.6}$$

where $C_{snubber}$ is the RC snubber capacitance and C_{CB} is the parasitic capacitance within the SSCB. An RC snubber cannot effectively limit the peak voltage alone, because of the low energy density of the capacitor. In addition, the RC snubber may cause an oscillation in the voltage across the IGBT due to the interaction with the system inductance. Thus, an RC snubber is generally used to limit the transient voltage rising rate only, and the peak SSCB voltage is clamped by the MOV.

During normal operation, the voltage across the SSCB is determined by the on-state IGBT and diode voltage drops. Each of these devices experiences a non-linear voltage rise with respect to the conducted current. Figure 2.5 shows the nominal I-V curves for the forward biased diode and the on-state IGBT at different operating temperatures. The IGBT has a positive temperature coefficient, resulting in a higher V_{CE} at higher temperatures for the same I_C, whereas the diode experiences a negative temperature coefficient in the rated load current range of the SSCB, resulting in lower V_F at higher temperatures for the same I_F [24].

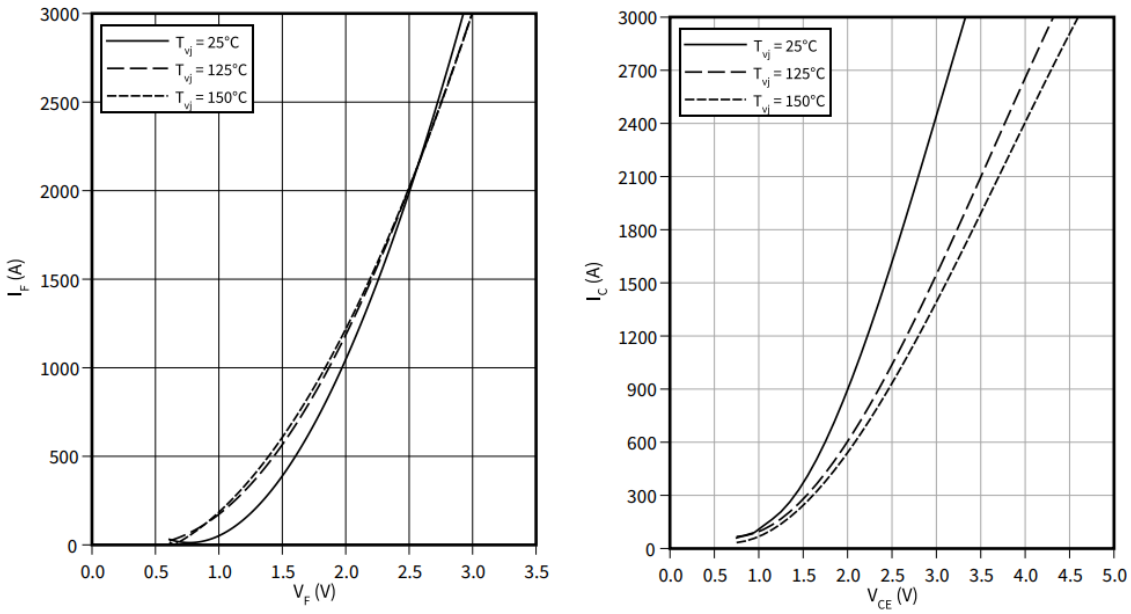

Figure 2.5. I-V Curves for Diode and IGBT. Source: [24].

For the 3.3 kV module in [24], when a 1200 A flows through the SSCB at 25 °C with V_{GE}=15 V, the voltage drop across the IGBT and the diode are 2.3 V and 2.2 V respectively. As the temperature goes up, the voltage drop across the IGBT goes up while the voltage drop across the diode slightly goes down. This keeps the on-state voltage in one SSCB relatively constant near 4.5 to 5 VDC.

Since the IGBT module is not switched continuously, the efficiency of the SSCB depends on the conduction losses of the IGBT and diode which are determined by the load current and applied gate voltages. The gate voltage also determines the point at which the IGBT transitions from the saturation region, where the voltage across the IGBT is relatively low, to the active region, where the voltage across the IGBT is significantly high. For example, at 150 °C, when 15 V applied to the gate, the IGBT will saturate at 6.4 kA. Due to the positive temperature coefficient explained above, at lower temperatures, this saturation current would be at even higher values. At 150 °C, with 12 V gate voltage, the IGBT will start to exit the saturation region at 2.7 kA. At lower temperatures, such transition will occur at a higher current. During a fault condition, the current through the IGBT will first rise rapidly, but will eventually be limited to the current saturation level of the IGBT. Therefore, the peak

fault current can be limited and remain constant even without a current limiting inductor until the control circuitry turns off the IGBT.

A lower gate voltage can reduce the peak fault current. However, by operating at a lower gate voltage, the IGBT experiences higher conduction losses. From Figure 2.4, for a target of 1200 A, a 15 V gate, which is typically recommended by the devices vendors, would lead to a 2.8 V_{CE} drop across the IGBT. At the same current, a gate of 12 V increases the V_{CE} to a 3.1 V. In other words, this reduced gate voltage would introduce an additional 360 W of power losses internally to the IGBT when operating at nominal system voltage and current values. For a nominal 2.4 MW MVDC system operating at 2 kV and 1.2 kA, the 360 W of power loss introduced in the IGBT would only represent a 0.03% increase in system losses through two operating SSCBs. This loss is negligible for a targeted efficiency of 99.5%. Especially, the additional loss can be partially compensated by the elimination of the current limiting inductor introduced in Section 2.3.

The typical switching waveforms of a traditional SSCB are shown in Figure 2.6. The top figure depicts the waveform of the voltage across SSCB, V_{SSCB}, and the bottom figure depicts the waveforms of the current flowing through the IGBT, I_1, and the current through the MOV, I_2. As shown in Figure 2.6, before t_0, the system is under normal operation, V_{SSCB} is close to zero, and the system current only flows through the IGBT. At t_0, a short circuit fault occurs, and the IGBT current will increase rapidly. The rising rate is determined by the DC bus voltage, V_{DC}, the value of system inductance, L_{sys}, and the inductance of the current limiting inductor, L_{CB}, as described in Equation 2.1. Once the fault current exceeds the predefined protection threshold, I_{th}, at t_1, the fault protection scheme is activated. As the protection is activated, the fault current will continue to increase until the IGBT is turned off at t_3 and the fault current is commutated from IGBT to MOV from t_3 to t_4. All the energy in the system is dissipated through the MOV from t_4 to t_5 where no further current flows and the SSCB blocks nominal bus voltage.

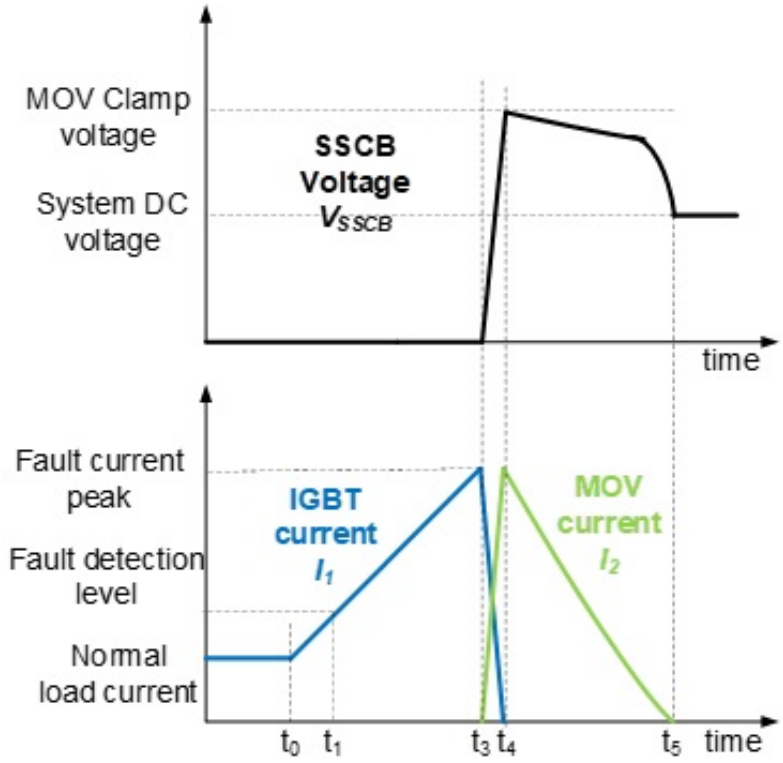

Figure 2.6. MOV Clamped SSCB Voltage During Nominal Operation

When the IGBT begins to turn off, the current is commutated through the RC and MOV parallel branches where it is converted into heat. The voltage across the SSCB is reduced from the peak until no further current flows, and the SSCB voltage equals the system voltage described in Equation 2.3. This interruption process is shown in Figure 2.6 from t_3 to t_5. This voltage limiting process is handled entirely by the MOV. Without sufficient design margin, the MOV may be subjected to excessive energy dissipation, described in Equation 2.5, causing catastrophic failure of the MOV. The peak current amplitude and clamping duration determine the selection of the appropriate MOV for the voltage clamping and energy dissipation portion of the SSCB.

Protection of the IGBT module is provided by the gating circuitry through a number of components. The most critical protection function is called desaturation protection. As mentioned above, the IGBT will exit the saturation region when high current saturates the

device, causing the voltage across the IGBT to increase. When the IGBT is turned on, the blanking capacitor, $C_{blanking}$, will begin to charge. The charging rate is determined by an RC time constant. The charging process stops when the IGBT enters the saturation region and V_{CE} drops below the voltage of the blanking capacitor. During a fault as I_C increases, the IGBT voltage increases as well, resuming the charging of the blanking capacitor when V_{CE} rises above the voltage across the blanking capacitor. Once the voltage of the blanking capacitor is higher than a preset value, for example 8 V, the gate drive will turn off the IGBT. Proper tuning of the blanking capacitor is necessary to guarantee a proper detection process to prevent inadvertent protections when turning on an IGBT or due to system noise. The Soft Turn Off (STO) resistor, R_{STO}, provides a soft turn-off effect for the IGBT module by using a resistance typically higher than that used for the normal turn-off process. A higher R_{STO} results in a longer time to discharge the IGBT gate capacitance, resulting in a slower IGBT turn-off process. This reduces the di/dt during the turn-off transient, lowering peak IGBT voltage. The other two components within the gating circuitry that control the transient behavior of the IGBT are the turn-on, R_{on}, and turn-off, R_{off}, resistors. R_{on} and R_{off} control the rate at which the internal capacitances of an IGBT module are charged and discharged, respectively, under normal operation conditions, thus affecting the switching time of the device. As is the case with the R_{STO}, a higher turn-on resistance will result in a higher RC time constant, which results in a longer time to turn on the module. This slows down the switching transient from the off to the on state. R_{off} performs the same function during the on to off transition.

Resetting the SSCB is as simple as ensuring the fault is cleared, and resupplying the positive gating voltage to the IGBT, turning the SSCB back on. Because there are no moving parts and no closing springs to recharge, the SSCB is rapidly ready to return to operation.

2.3 SSCB Hardware Design Improvements

The traditional MVDC SSCB utilizes a current limiting device in the path to reduce the fault current rising rate during fault conditions. An inductor, shown in Figure 2.1, acts to limit the rate of change of current rise through the device. This component adds weight, occupies more space, and reduces the power efficiency and specific power of the SSCB. By reducing the gate voltage and allowing the IGBT to enter the active region during fault

interruption, the SSCB can achieve the same fault interruption capabilities without the bulky inductor [11] and is shown in Figure 2.7.

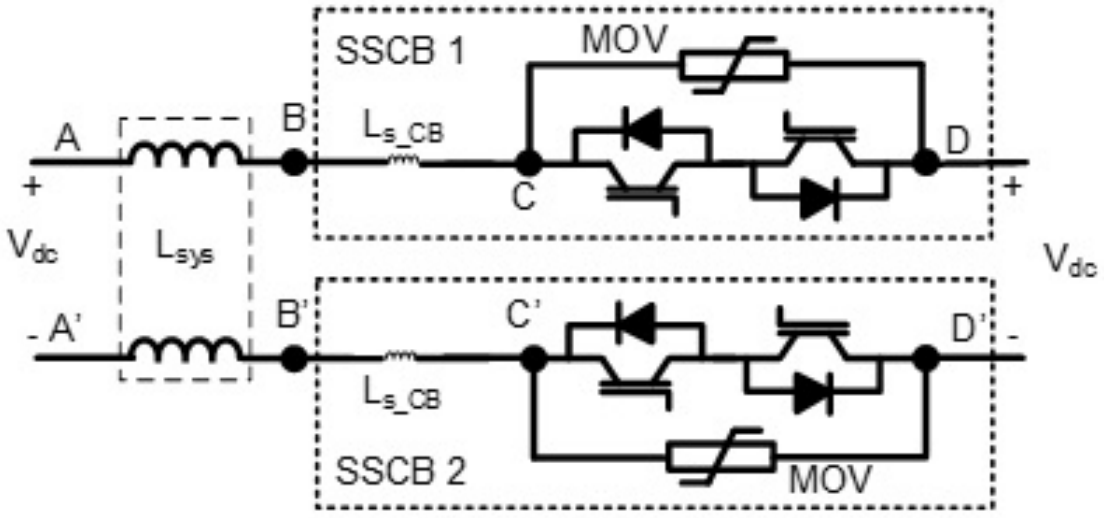

Figure 2.7. SSCB Design Without a Current Limiting Inductor

With reduced V_{GE}, the IGBT exits the saturation region and enters the active region at lower current levels, causing an extreme non-linear change in the I-V characteristics shown in Figure 2.4. The system response to this change in operating behavior is shown in Figure 2.8.

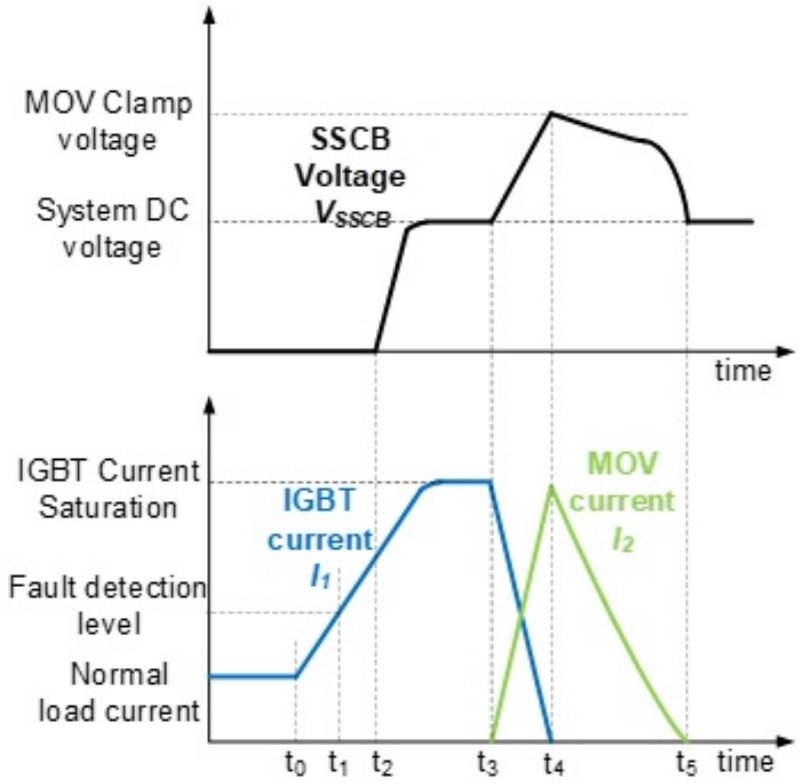

Figure 2.8. MOV Clamped SSCB Voltage with IGBT in Current Saturated Active Region Mode of Operation

As shown in Figure 2.4, a reduced gate voltage will lower the current level when the IGBT starts to enter the active region. When a fault condition occurs, the rise in current is similar to Figure 2.6 with a much higher slope. However, instead of the current continuing to rise until IGBT is turned off, I_C will saturate and be held nearly constant. This can be seen in the period between t_2 and t_3 in Figure 2.8. In this period, SSCB voltage rises until it reaches the system DC bus voltage. Once the IGBT is turned off, the MOV branch is able to clamp the rise in peak voltage, dissipate the current into heat, and return the SSCB to nominal system voltage.

The MOV is a highly nonlinear device that, in the standby region when the voltage across the MOV is low, appears as a large resistor with low leakage currents in the nA to μA range. In contrast to the high energy rating during transients, the continuous power rating of the device is very low, generally less than 1 W. Therefore, the maximum continuous DC

operating voltage must be higher than the steady state DC voltage. Ideally, the clamping voltage of the MOV should be as close to the nominal DC bus voltage as possible. However, the MOV can only clamp the peak voltage around two to three times the DC bus voltage. For example, a V172BB60 MOV can block up to 2150 VDC continuously, which is higher than 2 kV DC bus. However, the clamping voltage of the MOV when carrying 5 kA is 5 kV. Thus, a 6.5 kV IGBT module must be used to handle the transient voltage, resulting in a higher power loss and cost.

To reduce the peak voltage, a novel voltage clamping circuit is used, as shown in Figure 2.9, which combines mature and reliable Silicon Controlled Rectifier (SCR) technologies with the traditional MOV to reduce the peak clamping voltage. The electronically triggered MOV utilizes an SCR triggered by Breakover Diode (BOD) pairs where the BOD, with an advantage of a sharp breakover voltage, assists the MOV in the standby period improving the maximum blocking voltage of the electronically triggered MOV unit. The SCR, capable of supporting a high pulse current, provides rapid fault current commutation by inserting the MOV into the circuit for fault current dissipation. Additionally, the BOD provides a passive triggering mechanism for the SCR gate, eliminating the need to design separate gate drive circuitry [25].

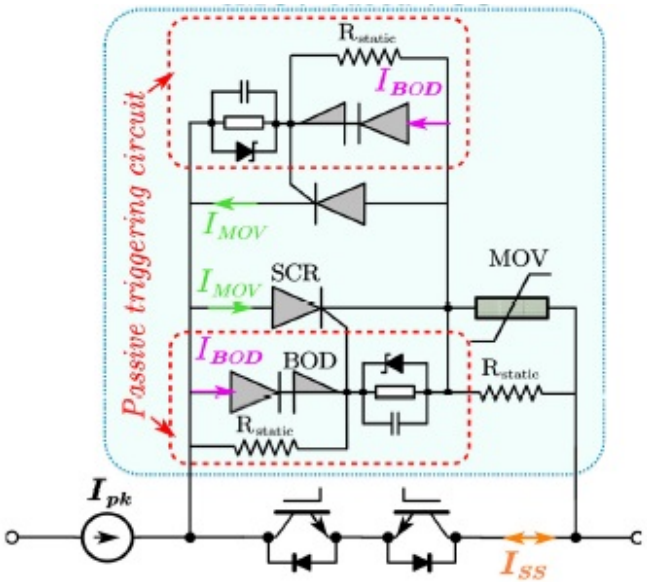

Figure 2.9. Electronic Triggered MOV Design. Source: [25].

Conduction through the MOV branch is initiated though an SCR that is gated on during current commutation. The gating process happens as the voltage rises as current is commutated to the RC snubber during the initial IGBT turn-off transient, raising the voltage in the SSCB explained in Equation 2.6 to a predetermined level, triggering a BOD, which in turn triggers the SCR. As the SCR is triggered, a path for commutation through the MOV is opened. After that, the MOV clamps the SSCB voltage, drives the fault current to zero, and brings the SSCB voltage to system voltage as described in Equation 2.1 and Equation 2.3.

With the novel voltage clamping design, the voltage rating of the IGBT can be reduced significantly, which can improve the system efficiency. In addition, because there is no need to connected multiple MOVs in parallel to limit the peak voltage, the specific power and power density of the SSCB is also improved compared with the traditional design.

These two major changes are the backbone of this thesis: the function of the current limiting inductor is realized with reduced gate voltage and the peak SSCB voltage is reduced to only 1.5 times higher than system DC voltage with a novel voltage clamping circuit. It is critical to verify the feasibility of the new technologies through a series of experiments.

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CHAPTER 3:
Switching Performance Test

3.1 Test Setup

The SSCB system design consists of four IGBT modules arranged in an anti-series, anti-parallel fashion that allows for two-way conduction and bipolar voltage blocking, as well as fault interruption from most line to line short circuit faults and double ground faults. These IGBTs are the current carrying components of the SSCB which also includes the gate control circuitry, fault detection and interruption circuity, and energy dissipation components. The typical MVDC system consists of a rigid DC bus provided by a battery, for example, system inductance from the power cabling or transmission lines, and the DC load, such as motor drives. A nominal test design was developed to simulate a rigid DC bus, transmission line inductance, an SSCB to include control, interruption, and energy dissipation circuitry, and the instrumentation necessary to monitor the circuit variables. The design can be seen in Figure 3.1. Each component of the test setup was selected to meet or exceed required parameters of the NASA FLASH SSCB design.

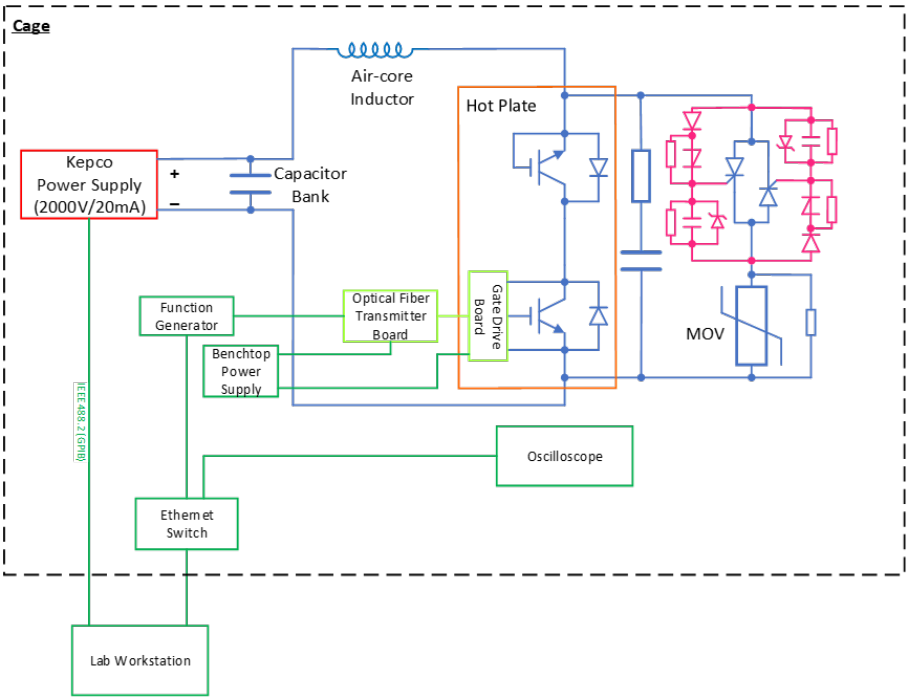

Figure 3.1. Nominal Switching Test Configuration Including Hardware, Instrumentation, and Controls

The test was designed to simulate the system involving the MVDC distribution bus, one pole of the SSCB, and the related system inductance. Additionally, the required instrumentation and control equipment is included.

3.1.1 Hardware Selection

To simulate a rigid DC bus, a 816 μF capacitor bank was selected utilizing 12 capacitors in parallel [26]. This capacitor bank was rated for 2.1 kVDC, exceeding the 2 kVDC bus requirement. The capacitor bank was connected to a DC power supply capable of charging the capacitor bank to the nominal DC bus voltage. A power supply was selected to provide 2 kVDC charging to the capacitor bank, resupplying the system following fault simulation. The power supply was unable to provide any appreciable amount of current during the fault to affect the system performance, limited to 20 mA of output current [27]. The system inductance was simulated utilizing an air-core inductor, with 2 kVDC Diesel Locomotive Cable (DLO) cable [28]. Taps were provided throughout the inductor to allow selection of inductance at 25 μH intervals. This allowed for testing from a minimum inductance of

a direct short at 0.65 μH by bypassing the inductor completely, to a maximum expected system inductance of 50 μH. The current carrying portion of the SSCB was selected as a 3.3 kVDC Infineon IGBT module rated at 1.5 kA [24]. This module was selected for sufficient margin to peak voltage during fault interruption, transient response characteristics, and sufficient margin to required current capabilities. For the SSCB control circuitry, a novel circuit board was developed to allow for selectable gate voltages from 10 V to 15 V and modified for different turn-on and turn-off resistances, as well as an adjustable desaturation protection circuit, designed by collaboration partners at Clemson University. Transient voltage suppression circuitry utilizing a novel arrangement of MOV, BODs, and an SCR was designed through partners at Virginia Polytechnic Institute and State University [25], [29]. The MOV and the SCR are connected in series, each with a high-resistance resistor in parallel to assure proper static voltage sharing. The transient voltage sharing between the MOV and the SCR is determined by their parasitic capacitance and any external capacitance if connected in parallel. Two 600 VDC BODs were placed in series between the SCR anode and gate to provide a 1200 VDC nominal triggering voltage for SCR activation. Once this voltage potential was reached, the BODs would conduct, turning on the SCR. The commutated fault current initiated from the SCR is directed through the MOV [30]. An RC snubber is incorporated for initial voltage containment during current commutation [31], [32].

For the "operational" temperature tests, a thermal hot plate was modified to allow mounting of the IGBT module to the heating surface. A Thermo-Scientific aluminum hot plate was chosen for mounting the IGBT as the hot plate surface could be removed and taps drilled for mounting the IGBTs under test [33]. Additionally, the surface temperature could be read by an infrared pyrometer to ensure surface temperatures of the hot plate and IGBT module were at the required temperatures.

3.1.2 Instrumentation Selection

The instrumentation necessary to monitor the systems performance included an 8-channel oscilloscope, active voltage probes, Rogowski coils, and a fiber optic voltage probe. To measure the gate voltage, V_{GE}, an isolated voltage measuring probe was used. This probe allowed for accurate differential measurements of the gate with very high bandwidth, slew rates, and complete galvanic isolation from the circuit due to power over fiber and opti-

cal sensing units [34]. Rogowski coils were selected to measure currents for their high accuracy and bandwidth, linear measurement at high di/dt, and low inductance allowing for a rapid current measurement without needing to be placed in line with the circuitry under test [35]. Tektronix active voltage probes were selected for their high bandwidth, large voltage differential, and floating measurement capabilities [36]. Due to the rapid fault interruption capabilities of the SSCB, these high-end, rapid measuring devices were necessary to accurately measure the voltages and currents throughout the system during the switching test. These measuring devices were inputs to the 8-channel oscilloscope selected for the remote monitoring and adjustment capabilities, high bandwidth and sample rate, and onboard memory capacity [37]. These measuring instruments were placed at key points throughout the circuit shown in Figure 3.2 to directly measure, or calculate if necessary, specific variables of interest during the switching test.

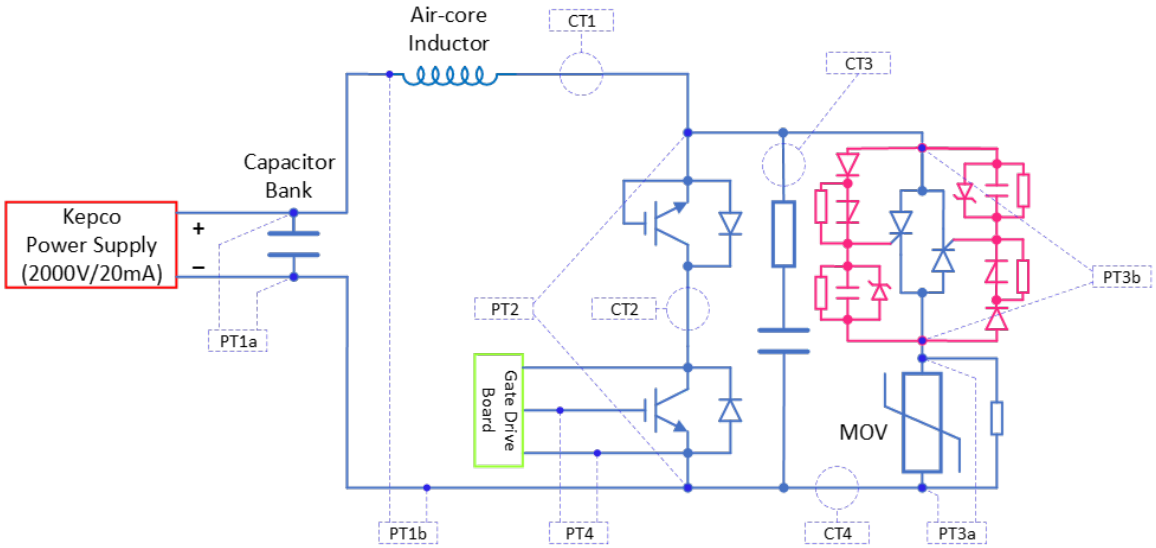

Figure 3.2. Nominal Switching Test Voltage and Current Measurement Locations

The locations of interest for measuring voltage and current through the SSCB and the testing system for SSCB performance evaluation were able to be reconfigured based on instrumentation availability, component location and orientation, as well as other measurements and information of interest such as V_{CE} which requires relocating voltage probes from the nominal measuring locations across the SSCB to across the IGBT module.

3.1.3 Switching Test Layout

Figure 3.1 shows the layout for the proposed switching test setup. In this test, which is conducted inside an interlocked safety cage due to high voltages, a fault is simulated by gating the IGBT on and short circuited back to a capacitor bank. This fault would discharge the capacitor bank through the SSCB. The in-line air-core inductor limits the current rate of change through the SSCB in the same manner which the system inductance would limit the current rate of change. The system inductance has a critical impact on the current profile experienced during the short circuit and the fault clearing transient response. When the fault condition is sensed, the gate is turned off and the IGBT switches to the off-state as explained in Chapter 2. The system inductance continues to drive current in to the RC snubber, rapidly raising voltage across the SSCB. The BOD and SCR control circuitry fires, commutating the remaining current through the MOV. The energy within the system is dissipated within tens to hundreds of microseconds depending on the total system inductance. After the completion of current interruption, the off-state IGBT, along with the anti-parallel diode in the anti-series IGBT module, blocks the DC bus voltage, and the SSCB is ready to be reset and returned to the on state.

In Figure 3.3, the completed layout of the hardware and instrumentation can be seen. The probe locations for voltage and current are adjustable, but nominally the capacitor bank voltage (MVDC bus voltage), inductor current (system current), IGBT voltage, IGBT gate voltage, SCR voltage, MOV voltage, MOV current, and RC snubber current were measured. From these values, additional mathematical calculations could be performed including power and energy calculations.

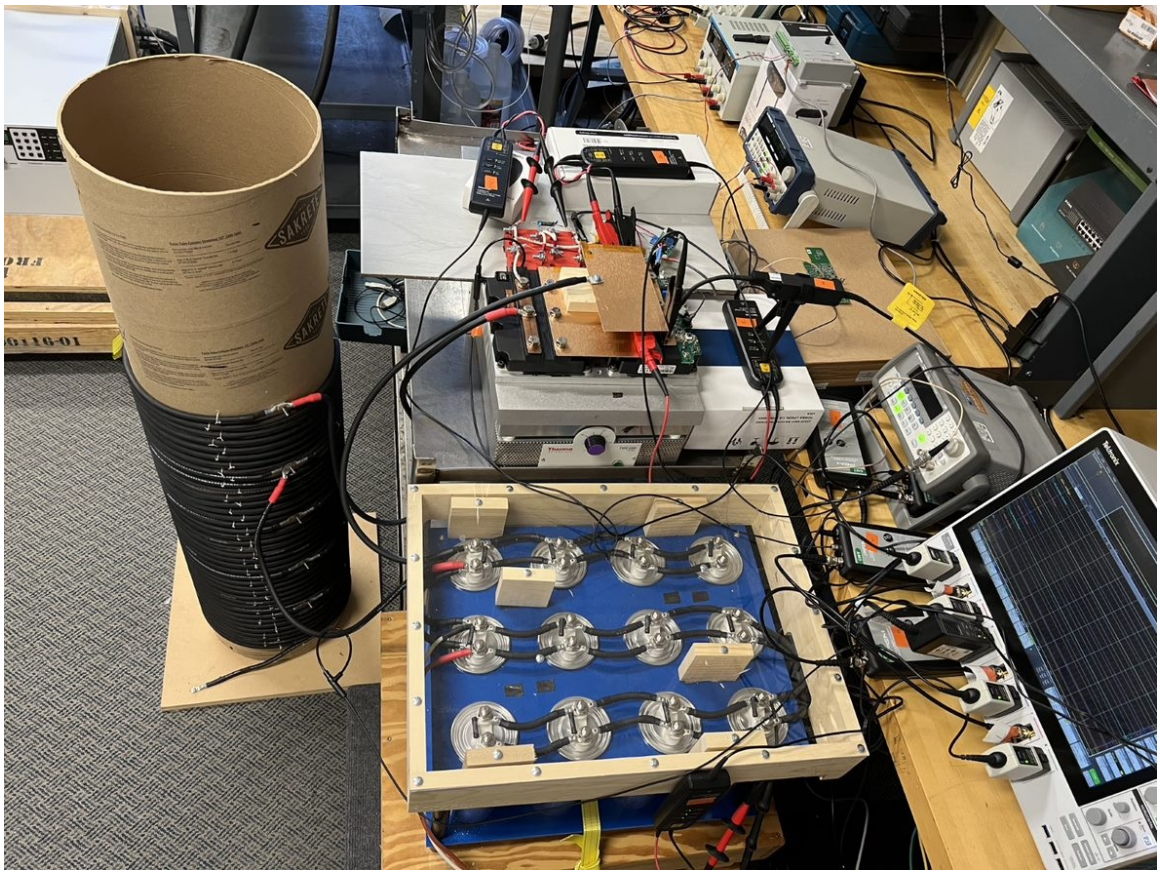

Figure 3.3. Hardware Assembled Testing Setup for Switching Performance Test

3.2 Switching Performance Test

The initial switching test was performed utilizing the nominal switch test setup, with only one SSCB pole under test. Two identical IGBT modules were connected in accordance with Figure 3.1 such that one module was conducting through the anti-parallel diode, while the other module was controlled in the on-state and off-state via the gate. Controlling parameters for the test included a gate voltage of -8 VDC for holding the SSCB in the off-state, and 10, 12, and 15 VDC for turning the SSCB on, initiating the fault test. External inductance was selected for the testing between 25 μH and 50 μH, as well as a direct connection from the capacitor bank to the SSCB with a calculated system inductance of 1 μH in the loose configuration and 0.65 μH in the tight configuration. These benchmark tests were to observe the saturation region and active region behavior of the IGBT at different gate

voltages, through different system inductances, and monitor the SSCB performance. All other parameters remained in their nominal values.

Before the first switching test of the 1500 A IGBT module was performed for this thesis, several other IGBT modules of various manufacturers and ratings were evaluated and eliminated for having a "harsh" turn-off characteristic, for example a di/dt that was too high resulting in peak voltages that were in excess of component design parameters. Minor modifications to the connections between the IGBT modules and electronic MOV, as well as the connections within the snubber and electronic MOV, were optimized during this phase of testing. These earlier IGBT modules and MOV configurations were not selected for the SSCB proposed in this thesis, and are therefore not included in the testing procedures or results. One thing of note was that a high voltage event occurred in previous tests that resulted in a faulted SCR that required replacement during benchmark testing of the selected Infineon 1500 A IGBT module.

3.2.1 Benchmark Switching Performance Test

For the first performance test, shown in Table 3.1, the DC bus voltage was stepped up incrementally from 200 V to 2000 V while observing the SSCB response with 15 V applied at the gate, through 25 μH system inductance. The gate was applied from 50 to 167 μs to control the maximum current and consequently the peak voltage during commutation.

Table 3.1. V_{GE}=15 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω L_{sys}=25 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
200	100	711	1217	2167
400	100	1425	1236	2480
500	100	1764	1253	2653
500	125	2065	1259	2736
500	150	2291	1268	2776
500	167	2426	1268	2804
600	167	2958	1271	2899
800	125	3362	1268	2945
1000	100	3577	1273	2949
1200	100	4275	1281	2996
1400	50	2861	1268	2906
1600	50	3262	1279	2930
1800	50	3655	1275	2964
2000	50	4045	1277	3016

The benchmark testing done on the SSCB at 15 V_{GE} was performed to evaluate the current interruption behavior of the SSCB under typical IGBT gate drive conditions, and observe operation of the electronically triggered MOV. The final 2000 V test waveforms are shown in Figure 3.4.

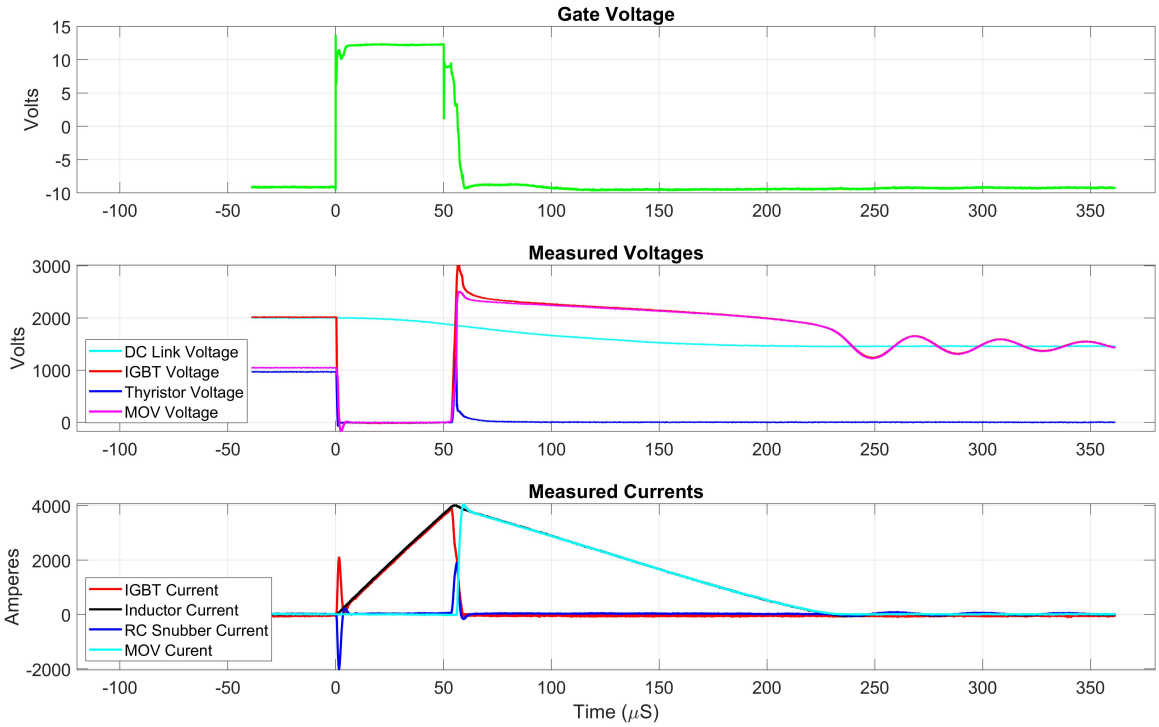

Figure 3.4. Benchmark Full Switch Test Transient Response, V_{sys}=2000 V, V_{GE}=15 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω L_{sys}=25 μH

This nominal transient waveform is similar to that shown in Figure 2.6. As the IGBT current rises linearly through the system inductance, the current rate of change is controlled. After reaching 50 μs, the positive gate voltage is removed, and the gate is driven down to -8 V. This turns off the IGBT module, and begins to commutate the current from the IGBT into the RC snubber. This causes the RC snubber voltage to rise, which is sensed across the electronic firing circuit to the MOV. The voltage continues to rise across the BOD until the trigger voltage is reached, and the voltage across the BOD collapses and rapidly drops towards zero. This process turns on the SCR which in turn allows conduction through the MOV. The RC snubber and IGBT currents begin commutation to the MOV parallel branch as the IGBT continues to turn off. The voltage rises across the IGBT until reaching a peak value, clamped by the MOV. After the IGBT turns off, the remaining system current is fully commutated through the MOV, removing energy from the system inductance, driving voltage across the SSCB back to nominal bus voltage at approximately 350 μs after the fault

initiation. The DC bus voltage decreases from the nominal 2000 V at the start of the test to approximately 1500 V due to the capacitor bank discharging and limited replenishing current from the DC power supply. Upon test initiation, the RC snubber is seen to discharge the stored energy through the IGBT, causing a spike in IGBT current not consistent with system current. No active region operation was observed, as seen by the IGBT voltage dropping toward 3 V during the on state portion of the test. By utilizing the nominal V_{GE} of 15 V, the IGBT and SSCB maintained operations in the saturation region. A zoomed in portion of the switch performance during SSCB turn-off transient is shown in Figure 3.5.

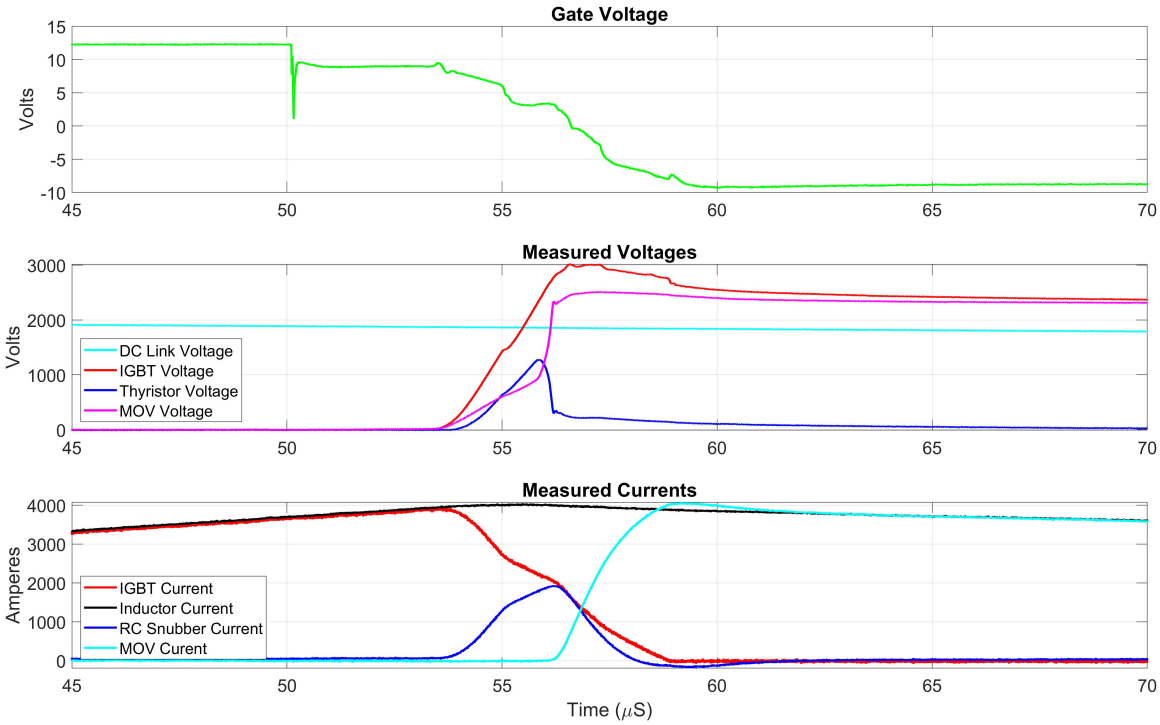

Figure 3.5. Benchmark Full Switch Test Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=15 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω L_{sys}=25 μH

The BOD performance can be seen from observing the “Thyristor Voltage” blue curve in the middle graph. The voltage rise across the SCR is due to the rise in voltage across the RC snubber and IGBT, connected in parallel with the electronic MOV branch consisting of the serial connection of the SCR and MOV, and determined by the voltage division between

the SCR and MOV. The voltage is seen to rise nearly linearly until reaching approximately 1200 V, where the BOD is triggered, and voltage, within 1 μs, drops and current conduction through the SCR and MOV is initiated. This whole process occurs in approximately 3 μs. As the MOV current begins to rise, there is a rapid rise in MOV voltage. This results in a very sharp increase in the MOV voltage until the clamping voltage is reached at approximately 6 μs after the IGBT is commanded to turn off. The clamped voltage of the MOV and the additional voltage due to the parasitic inductance in the current commutation loop determine the peak voltage across the IGBT during the turn-off transient, approximately 3000 V during this test. The current through the IGBT is reduced from approximately 3950 A to 0 A in 5 μs. This rapid interruption of fault current is one of the advantages of the SSCB. After the IGBT is completely off, all the remaining system inductive current is discharged through the MOV.

3.2.2 Reduced Gate Voltage Switching Performance Test

The next test conducted was performed at V_{GE} of 12 V, while maintaining the same L_{sys} of 25 μH. As performed in the benchmark test, DC bus values were incremented while adjusting the gating t_{on} length to maintain peak voltage values below the IGBT voltage rating. Two additional tests were run at a higher system inductance, 50 μH, and are shown as the last two entries in Table 3.2. Tests with an asterisk are ones in which the IGBT entered desaturation region due to high I_C, which is detected by the desaturation protection circuitry on the gate drive board, resulting in the soft turn-off of IGBT.

Table 3.2. V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=25 μH and 50 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
500	100	1801	1258	2693
1000	100	3538	1272	2981
1200	100	3979	1265	2925*
1400	100	4074	1265	2936*
1600	100	4140	1265	2938*
1800	100	4236	1263	2952*
2000	100	4299	1261	2949*
2000	100	3224	1275	3012
2000	167	3884	1268	2950*

In this test, the IGBT was seen to enter desaturation under certain conditions, which was not unexpected, due to the reduced gate voltage V_{GE}. The desaturation detection and soft turn-off components, $C_{blanking}$ and R_{STO}, were not yet tuned for optimal settings, and would require adjustments and further testing. Indications of the IGBT leaving the saturation region mode of operation and entering the active region of operation were not apparent, as V_{CE} remained fairly low, never exceeding 8V, during the on state portion of the test. The final 2000 V waveforms at 25 μH are shown in Figure 3.6. The desaturation pin voltage is shown in the top graph instead of V_{GE} to shown when desaturation occurs. The gating signal for this test was 100 μs but the actual on-time was around 54 μs, due to desaturation detection.

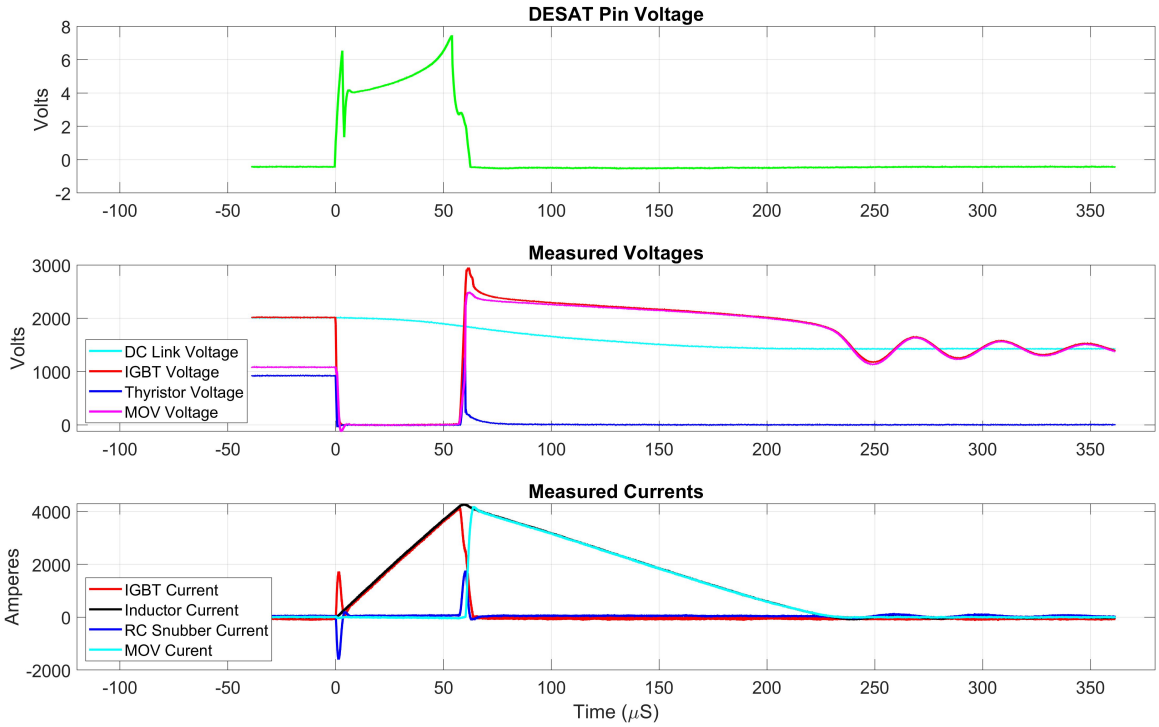

Figure 3.6. Full Switch Test Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=25 μH

The transient waveforms in this test are similar to those shown in Figure 3.4. As the IGBT current rises linearly through the system inductance, the rate of change is controlled. After approximately 54 μs, the gate control circuitry identifies a fault condition due to high I_C and turns off the IGBT. As the IGBT begins to turn off, the RC snubber voltage begins to rise as electric charge is directed into the capacitor. Once the SCR is gated on by the triggered BOD, the SCR voltage rapidly drops towards 0 V, and the MOV voltage rapidly rises to clamping voltage similar to the 15 V test. Current is directed through the MOV as the IGBT module finishes switching to the off-state and the IGBT voltage decays to MOV voltage. After approximately 250 μs, the turn-off transient is complete as all the remaining inductive energy is dissipated through the MOV. A zoomed in view of the turn-off transient is shown in Figure 3.7.

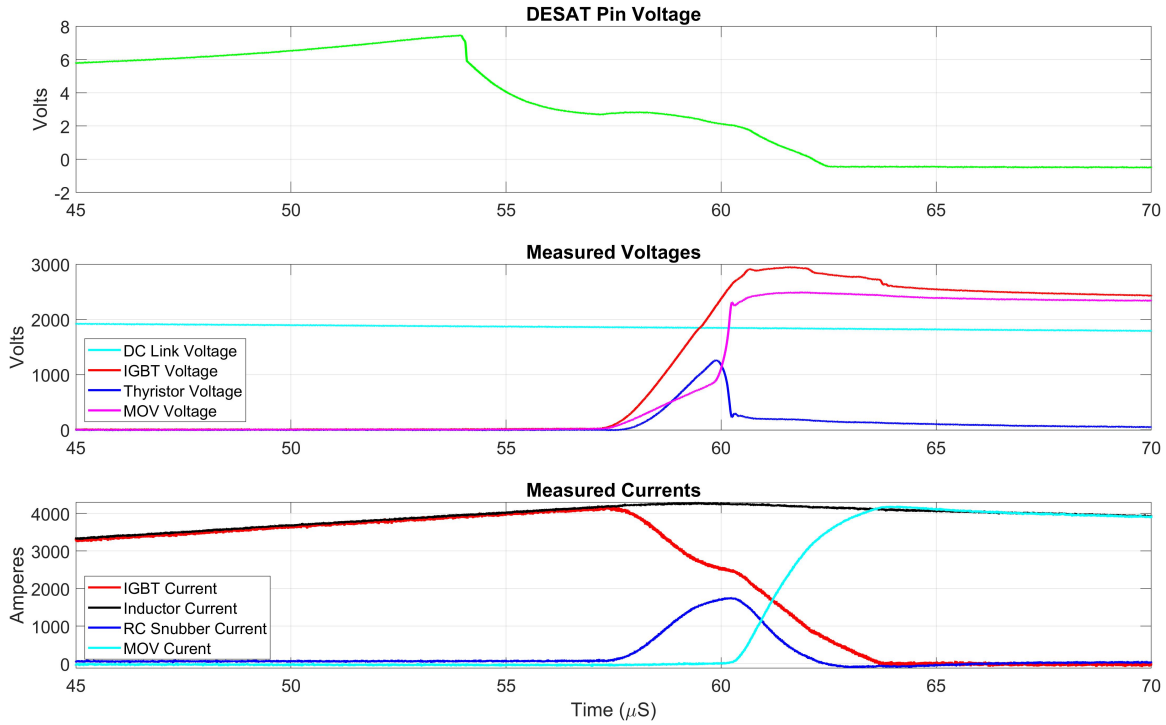

Figure 3.7. Full Switch Test Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=25 μH

The peak current observed during this fault test was 4299 A, whereas the 15 V_{GE} test showed a peak current of 4045 A for a commanded conduction period half as long. As was the case in the previous test, the BOD and SCR voltage rise and subsequent rapid drop can be seen. This behavior indicates the BOD is operating as expected, triggering around 1200 V and initiating current commutation through the MOV. It takes the IGBT about 6 μs to drop from around 4000 A to 0 A. The rapid rise in MOV voltage up to the clamping voltage can clearly be seen in the middle graph. The MOV voltage is clamped at slightly above 2500 V, and the SSCB voltage is contained within 3000 V. The SSCB voltage drops toward the MOV voltage as current conduction through the IGBT is cut off. The energy remaining in the system is dissipated through the MOV from around 64 μs until the end of the transient, about 190 μs later.

Figure 3.8 shows the system response for 50 μH full system inductance. The effects of

adding an additional current limiting inductor can be seen when comparing the results of this test to the previous, lower system inductance test.

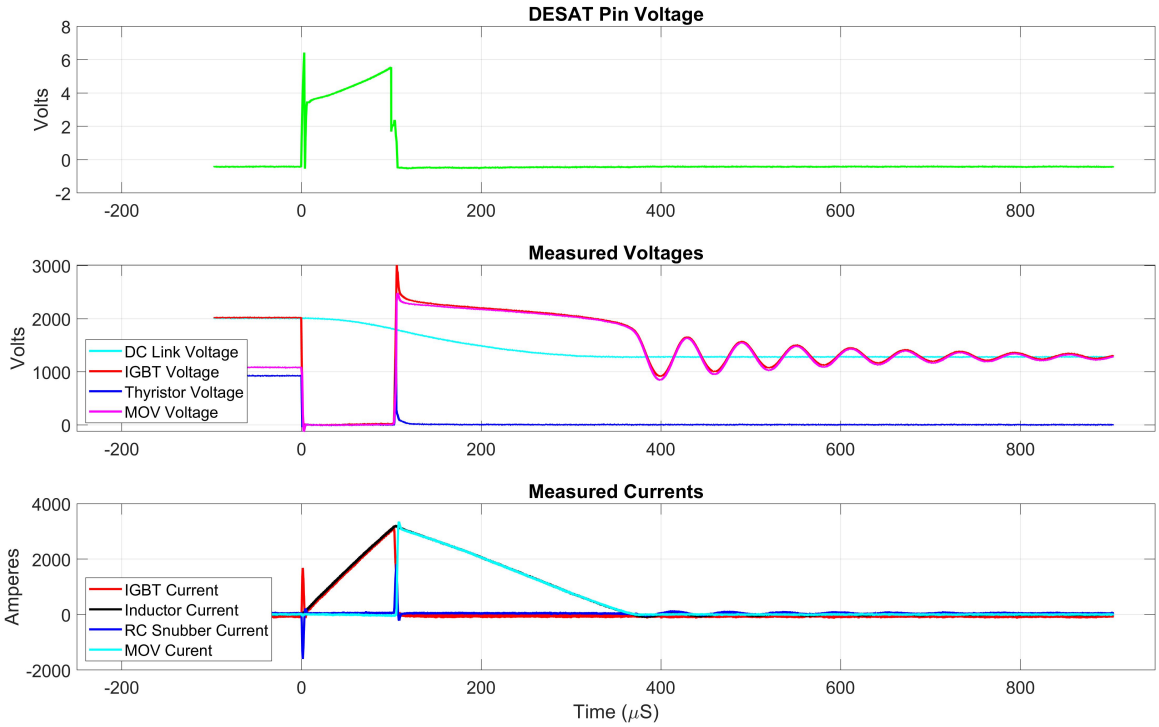

Figure 3.8. Full Switch Test Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=50 μH

The transient waveforms are similar to those shown in Figure 3.6. As the IGBT current rises linearly through the system inductance, the current rate of change is controlled, however at a lower rate compared to the previous test. After the full gate signal period of 100 μs, the gate is turned off. The desaturation pin voltage is shown instead of V_{GE} to compare the differences in desaturation pin voltage under different operating conditions. As the IGBT begins to turn off, the RC snubber voltage begins to rise as electric charge is directed into the capacitor. Once the SCR is gated on by the triggered BOD, the SCR voltage rapidly drops toward 0 V, and MOV voltage rapidly rises to the clamping voltage. Current is directed through the MOV as the IGBT module finishes switching off and IGBT voltage decays to MOV voltage. All the system energy is dissipated after approximately 800 μs. A longer period is required to dissipate the energy as the additional system inductance provides more

energy for the same current through the system. As is the case in the previous test, no sign of active region operation is apparent as the IGBT voltage rises from approximately 3 V during the initiation of the turn-off sequence. A zoomed in view of the turn-off transient is shown in Figure 3.9.

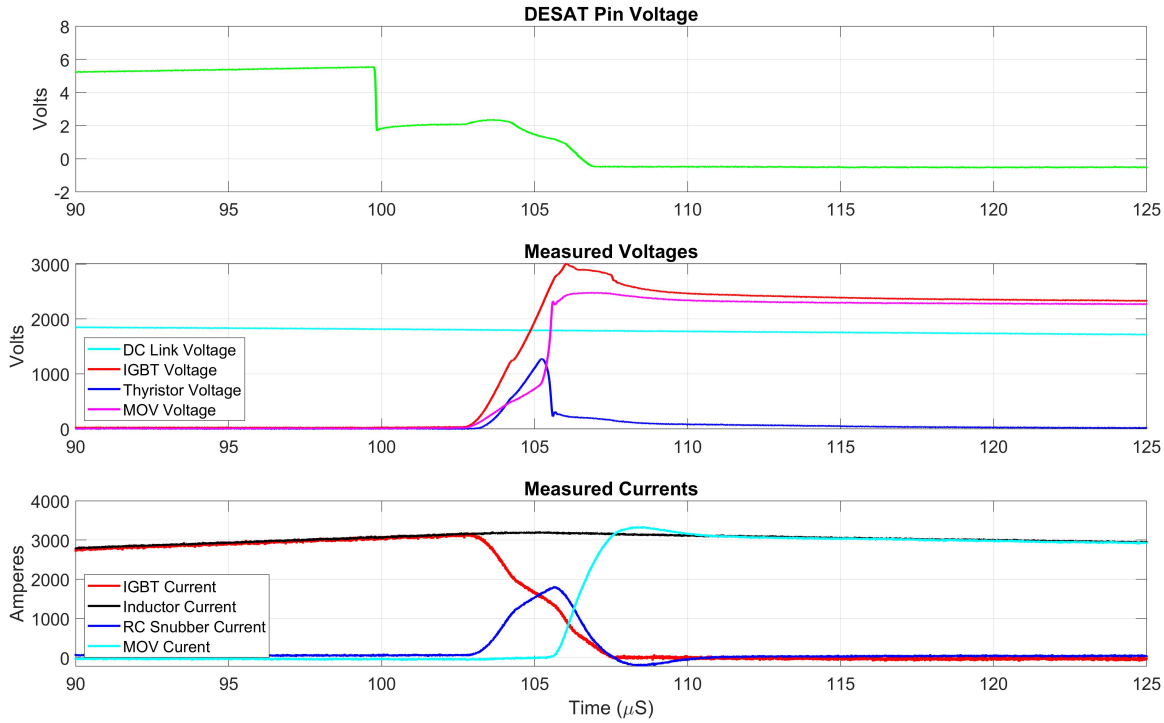

Figure 3.9. Full Switch Test Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=50 μH

Peak voltage across the IGBT and MOV are very similar to the 25 μH test case, however the peak currents through the IGBT of 3224 A is dramatically reduced due to the lower di/dt and the non-stiff capacitor bank voltage. As was the case in the previous test, the BOD voltage rise and subsequent rapid drop can be seen. The graph shows the BOD triggering around 1200 V which in turn initiates the current through the MOV. The current fall time for the IGBT is about 4 μs from 3000 A to 0 A. The rapid rise in MOV voltage to a clamping voltage of slightly below 2500 V can be seen as well. This is a lower clamping voltage than the previous test due to lower system current through the device. The current remaining in

the system is dissipated through the MOV from 106 μs until the end of the transient, almost 300 μs later.

The next test conducted involved removing nearly all the system inductance, L_{sys}. This was done by disconnecting the air-core inductor from the system, connecting the cables to the same lug on the air-core inductor. Estimated inductance from test performance was 2 μH. Tests in Table 3.3 with an asterisk are ones in which the IGBT is turned off due to desaturation protection, caused by the rapid rise in I_C during the short circuit condition.

Table 3.3. V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=2 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
500	10	2805	1255	2501
800	10	2888	1274	2852
1000	10	3599	1249	2728*
1200	10	4284	1258	2808*
1400	10	4917	1263	2849*
1600	10	5497	1270	2887*

During this test, a relatively short on-time of 10 μs is issued by the gate drive board to avoid excessively high fault current which could arise if the SSCB would not respond properly. The IGBT entered desaturation protection at system voltages at or above 1000 V, and the active region conduction properties were not apparent. Due to the high di/dt rates experienced during the tests with limited system inductance, the peak currents experienced were of concern, limiting further testing at higher voltages until active region operations could be observed. The final 1600 V test waveforms are shown in Figure 3.10.

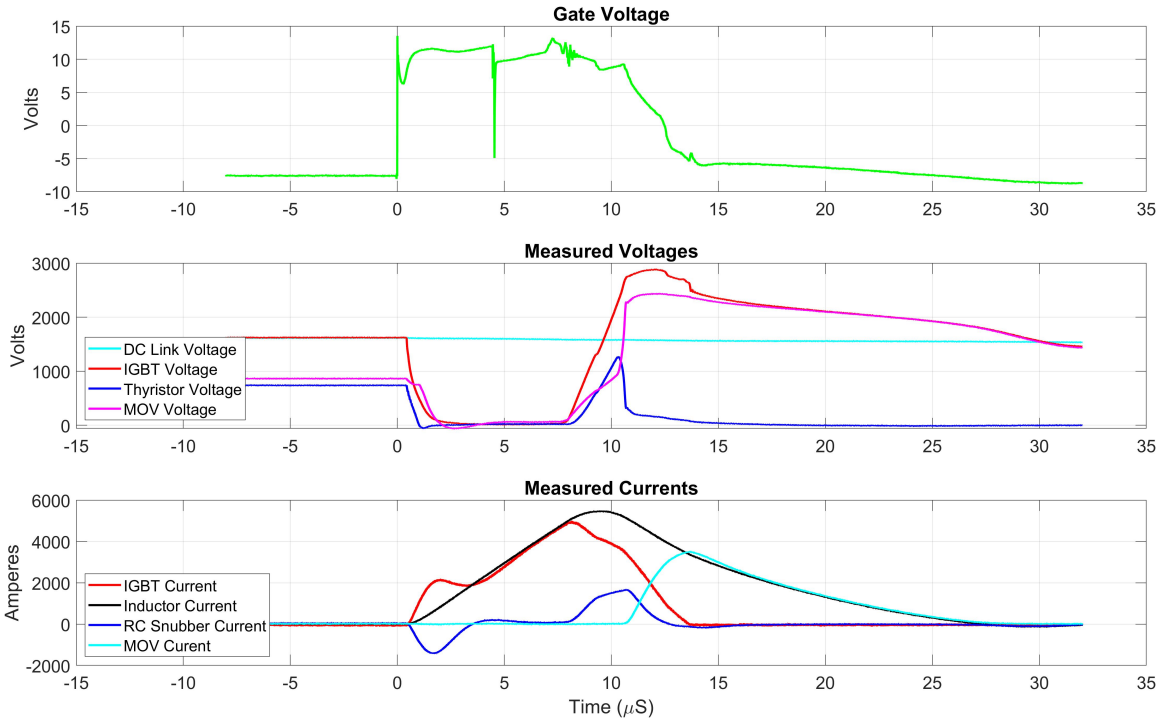

Figure 3.10. Full Switch Test Transient Response, V_{sys}=1600 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=2 μH

As is the case in earlier tests, the RC snubber is discharged through the IGBT upon test initiation. The IGBT current rises with system current until approximately 7 μs after test initiation where desaturation protection has activated and the IGBT soft turn-off of has occurred. As the IGBT turns off and the current flow is initiated into the RC snubber, the voltage across the BOD rises until triggered 10 μs into the test. This initiates current flow through the MOV and an immediate rise to a clamping voltage of approximately 2450 V is achieved. The total time for the IGBT to stop conducting current during the transient is about 5 μs. All behaviors of the SSCB operated as expected up to the highest test voltage in this test. Maximum current through the IGBT of 4996 A was a sufficient data point to suggest circuit tuning would be necessary to achieve active region operation and prevent further uncontrolled increases of fault current at higher operating voltages.

The same loose cable connection test was performed at a V_{GE} of 10 V to observe indications of active region operation and shown in Table 3.4. Further reduction of V_{GE} was not desired

below this value to show active region operation and current limiting effectiveness.

Table 3.4. V_{GE}=10 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=2 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1000	10	3447	1256	2707*
1000	6.25	3195	1268	2680
1400	10	4234	1266	2825*
1600	10	4580	1278	2870*

During this test series, a 6.25 μs test was conducted with the system voltage at 1000 V, and desaturation protection was not observed. The IGBT conducted for the full duration of the gating signal, and was turned off as the positive gate voltage was removed. In all other tests, the IGBT was turned off due to desaturation protection. In the final 1600 V test, the MOV and SCR voltages diverge from IGBT voltage during the IGBT on-state and require further testing to completely understand the behavior and is shown in Figure 3.11. This phenomenon is observed in later tests and will not be discussed further in this thesis.

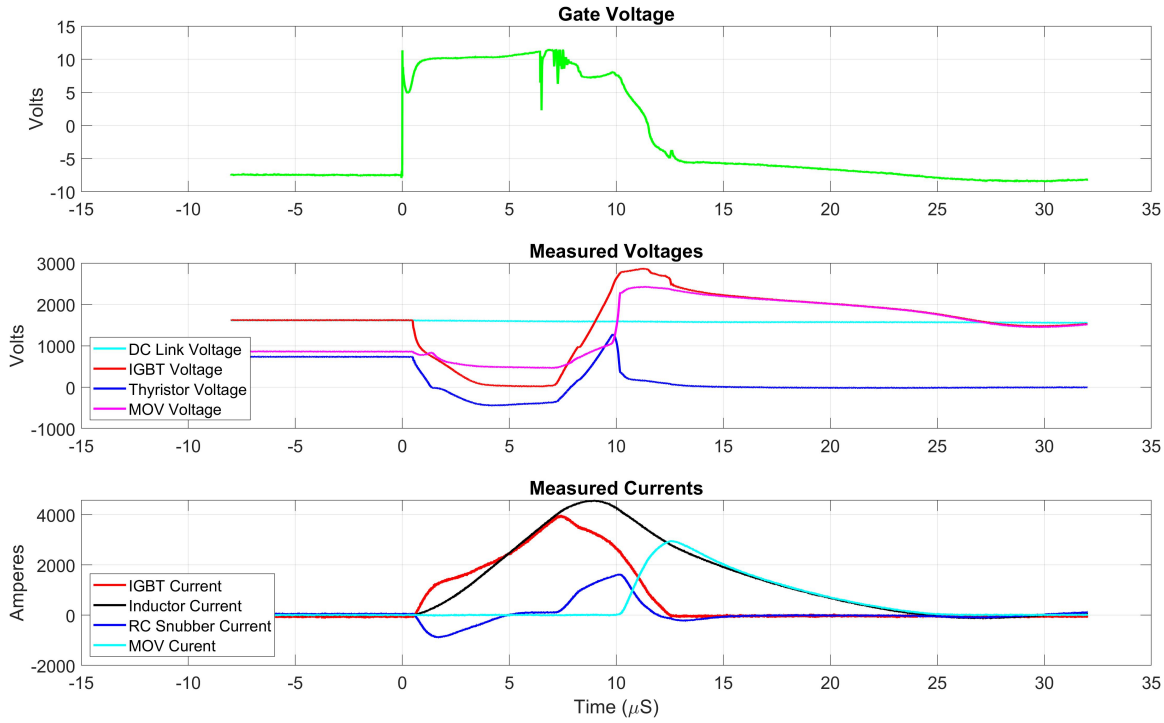

Figure 3.11. Full Switch Test Zoomed In Transient Response, V_{sys}=1600 V, V_{GE}=10 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=2 μH

This transient details the same result of the RC snubber discharging through the IGBT when current conduction is initiated resulting in higher than system current values. The IGBT returns to follow system current after the RC snubber is fully discharged. The desaturation protection of the IGBT occurred around 7 μs after it was turned on, and active region operation was not apparent in the IGBT as the current rise remained nearly linear until the IGBT was turned off. After the SCR was triggered and the MOV began commutating the system current, the MOV voltage was clamped at around 2400 V after 10 μs from test initiation. The IGBT stopped conduction from a peak current of 3993 A to 0 A in 5 μs.

The following reduced gate voltage tests were conducted in a similar fashion, but the system inductance was reduced to a minimum by tightly connecting the capacitor bank to the SSCB and the results are shown in Table 3.5. The calculated system inductance was approximately 1 μH during this test. By reducing system inductance further, the system current rate of

change would be sufficient to achieve a high enough I_C to expose a change in operating behavior from the saturation region to the active region.

Table 3.5. V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
200	10	2145	No trigger	1130
400	10	2888	No trigger	1660
600	10	4041	1251	2344*
800	10	4991	1253	2584*
1000	10	5693	1255	2680*
1200	10	6233	1263	2751*

During this test, the BOD circuitry did not trigger in the first two tests as the SSCB voltage did not rise to a sufficient value based on the voltage divider ratio. As noted in earlier tests, the IGBT entered desaturation in nearly all tests. Further testing was not conducted beyond the 1200 V test due to the peak current levels and the 1000 V test is shown in Figure 3.12. Apparent active region operation was not observed during these tests.

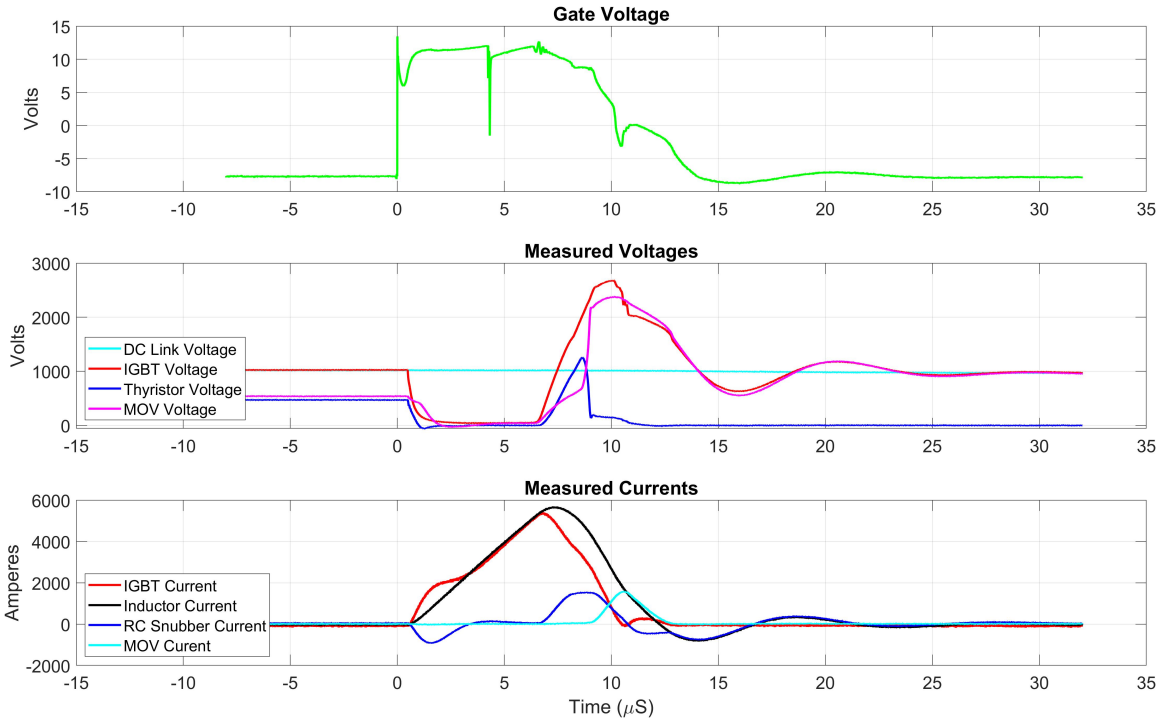

Figure 3.12. Full Switch Test Zoomed In Transient Response, V_{sys}=1000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

Figure 3.12 shows the transient waveforms during the switching of the SSCB at V_{sys} 1000 V. The applied gate signal of 10 μs was interrupted by desaturation protection after 6 μs. The IGBT current fell from the peak to 0 A within 4 μs. Nominal SSCB component operations were observed with the BOD breakover and SCR triggering initiating MOV current as well as the MOV voltage response. The clamped voltage for the MOV during the test was approximately 2400 V before rapidly dropping toward system voltage. The duration from peak clamped voltage to the first system voltage crossing was only 4 μs, which was substantially quicker than the approximately 15 μs in the previous test, due to lower system voltage as well as tighter cabling and reduced power loop inductance. A clear indication of active region operations is not apparent during this test. In addition to other factors, low system voltage and early desaturation protection prevented the active region operation shift to become visually apparent.

The same test with a direct, tight connection between the capacitor bank and the SSCB was conducted with a gate voltage of 10 V and shown in Table 3.6. This test was conducted to observe clear indication of active region operations. Due to the lower gate voltage, peak currents would be reduced allowing for testing at higher voltages, as well as lowering the current threshold for transition from saturation region to active region operation.

Table 3.6. V_{GE}=10 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{peak} (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
200	10	2005	No trigger	1081
400	10	2670	No trigger	1581*
600	10	3266	1244	2073*
800	10	3467	1249	2340*
1000	10	3565	1247	2473*
1200	10	3756	1259	2586*
1400	10	3900	1251	2668*
1600	10	4022	1255	2745*
1800	10	4181	1256	2894*
2000	10	4332	1261	3064*

During this test, the BOD circuitry failed to trigger in the first two tests as the SSCB voltage failed to rise to a sufficient value based on the voltage divider ratio. As noted in earlier tests, the IGBT entered desaturation protection in nearly all tests. This test is the first to show the IGBT apparently entering active region operation at higher voltages, shown in Figure 3.13 in the 2000 V test.

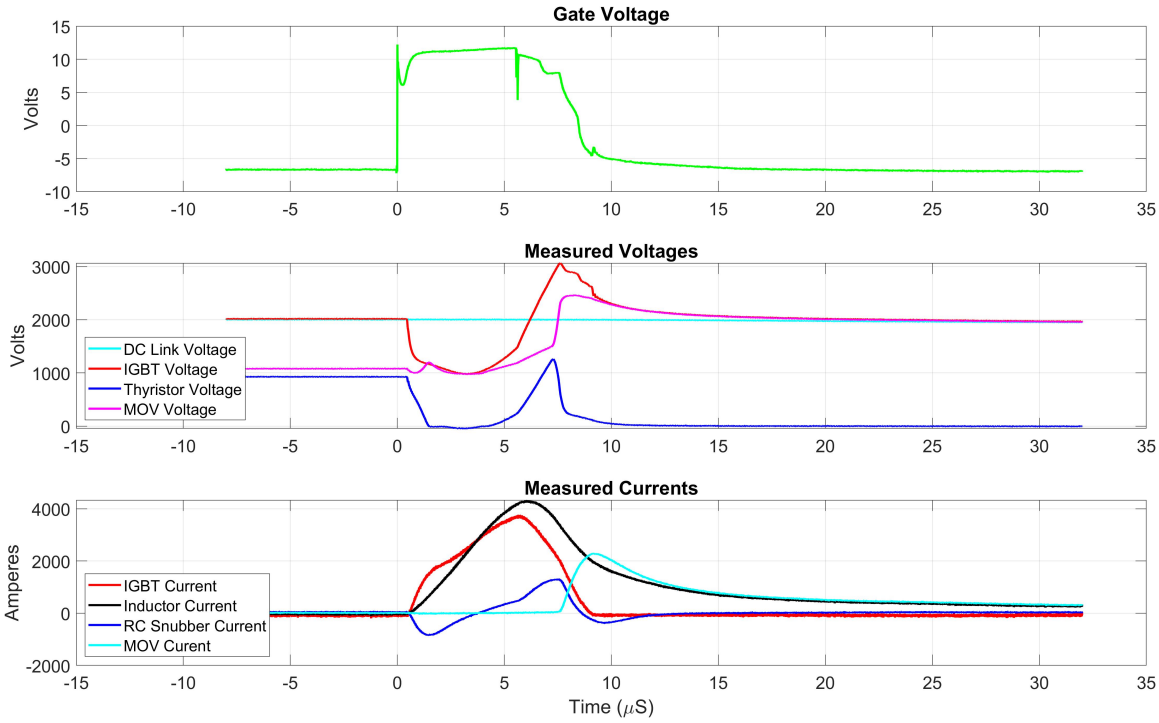

Figure 3.13. Full Switch Test Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=10 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

The desaturation protection signal turned off the IGBT before the gate command ends. However, the active region operation was apparent, as shown by the V_{CE} not approaching zero during conduction. In fact, the voltage stayed above 1000 V during the test, which is a clear indication of active region operation discussed in Subsection 2.2.1 and shown in Figure 2.4. This behavior reduced the peak current during the fault transient, and the peak IGBT current was less than 4000 A during this test. This test shows the ability of a reduced operating V_{GE} to contain the fault current, reducing the size and weight of the SSCB components. However, the gate voltage is likely too low for operational relevance and may introduce more losses than are acceptable. The turn off time for the IGBT in this test was only 3 μs as the reduced conduction channel and lower peak current required less time to interrupt. Due to higher system voltage, compared with the previous case shown in Figure 3.12, a longer duration was noted for the MOV voltage to meet system voltage during current commutation, transitioning from 2400 V at max clamping voltage to 2000

V system voltage in approximately 12 μs.

Testing with a direct cable connection between the capacitor bank and SSCB did not expose apparent current saturation or active region operation behavior unless the gate voltage was reduced to as low as 10 V. In addition, the saturation current value appeared to deviate from the short circuit current, I_{SC}, specified in the IGBT datasheet provided by the manufacturer. Therefore, a closer look into aspects which could impact the short circuit behavior became necessary. Among these aspects, bus bar size and power cable termination location were found to be especially relevant.

3.2.3 Bus Bar Connection Configurations

Following the benchmark tests determining the operating behavior of the SSCB at V_{GE} of 15, 12, and 10 V, a test was performed to evaluate the current distribution behavior of the IGBT through different bus bar configurations and connection points. During earlier testing with different manufacturers of IGBT modules, it was noted that the size and shape of the collector and emitter bus bars, as well as the external cable termination point at the bus bars, would have different effects on the SSCB operating characteristics. This test was designed and focused on how emitter bus bar size and shape and power cable connection location could affect the current distribution to the IGBT module chips and the current and voltage profiles during the switching transients, thus determining the best method to ensure even current distribution throughout the IGBT module and its short circuit behavior as specified by the IGBT module manufacturer.

Narrow Copper Bus Bar

The narrow copper bus bar, as shown in Figure 3.14, was used in all the tests described in the previous subsections. For this test, the positive emitter connection to the SSCB remained constant, while the negative emitter bus bar connection was tested at each connection location. These locations are labeled “Hole #1,” “Hole #2,” and “Hole #3.” t_{on} for each test was 10 μs and V_{GE} was 12 V.

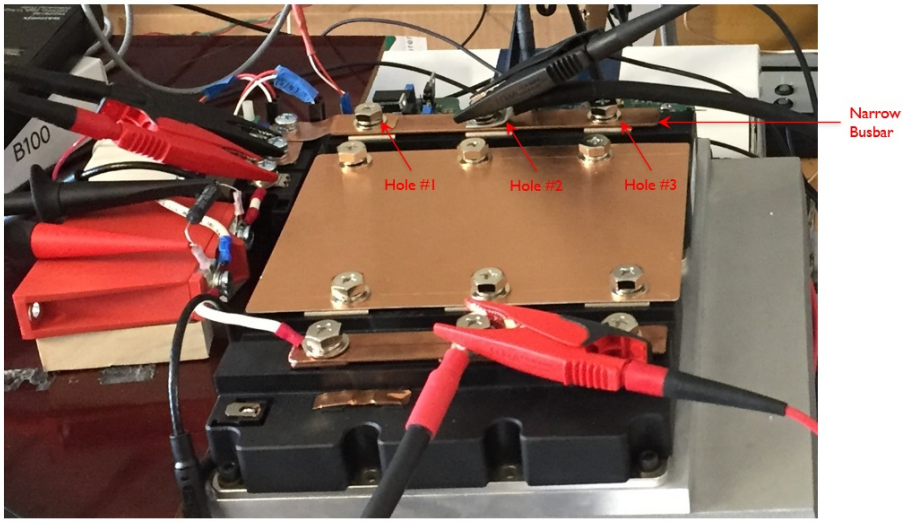

Figure 3.14. SSCB Configuration with Narrow Emitter Bus Bar

The hole closest to the IGBT auxiliary terminals was labeled "Hole #1" and the one furthest was labeled "Hole #3." The power cable termination at the emitter bus bar was moved from each hole location, and the short circuit tests performed in a similar fashion to the benchmark testing initially performed. Tests with an asterisk in Table 3.7 are ones in which the IGBT entered desaturation, caused by the rapid rise of I_C during the short circuit fault condition. Each test was conducted with a tight, direct cable connection from the capacitor bank to the SSCB with an estimated inductance of 1 μH.

Table 3.7. Narrow Bus Bar, "Hole #1," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1400	4527	3922	1245	2764*
1600	4662	3980	1247	2889*
1800	4827	4080	1256	3019*
2000	4976	4204	1260	3135*

Previous tests on this IGBT module had not been conducted using "Hole #1" and there is no direct comparison to be made. However, higher voltages were safely tested at this test location than previous tight, direct connected switching tests. The test shown in Table 3.5 never exceeded 1200 V due to high current conditions experienced and was similarly conducted in "Hole #2" as that was the common connecting point in previous tests. The test shown in Table 3.8 suggests a dependence upon terminal location in the IGBT module through the narrow bus bar, and a nonuniform current distribution into the IGBT chips inside the module through the narrow bus bar.

Table 3.8. Narrow Bus Bar, "Hole #2," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
800	4978	4805	1258	2555*
1200	6230	5888	1261	2739*
1400	6691	6169	1264	2790*
1600	7037	6365	1271	2847*
1800	7290	6354	1273	2891*
2000	7238	6148	1276	2938*

The dramatic increase in current through the IGBT and system when compared with the "Hole #1" test can be seen above. The "Hole #2" termination appeared to allow more current through the device and connection, indicative of strong interaction between the power circuit and gate drive circuit, most pronounced when the bus bar cannot guarantee an even current distribution among the IGBT chips inside the module. Therefore, this test further supports a dependence upon terminal location in the IGBT module through the narrow bus bar. Table 3.9 test results continue to show a dependence on the terminal location.

Table 3.9. Narrow Bus Bar, "Hole #3," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1400	7689**	7613	1265	2898*

Only one test was performed in "Hole #3" due to the apparent saturation of the Rogowski coil, denoted by the double asterisk in the peak system current column. This phenomenon had not been noted before during any previous testing. The current rating for the coil is listed as 6 kA but usually can measure current up to about 120% of the rating at reduced fidelity and accuracy. The coil had not saturated in previous tests where peak currents had exceeded the rated current values. Furthermore, the rapid rise in current through the IGBT and the system showed a significant increase from the "Hole #1" and "Hole #2" tests previously conducted. Further testing was not deemed necessary nor worthwhile at this location at increased voltages. This test further supports a strong dependence of the IGBT module short circuit current profile upon terminal location in a narrow bus bar. The "Hole #2" transient response is shown in Figure 3.15.

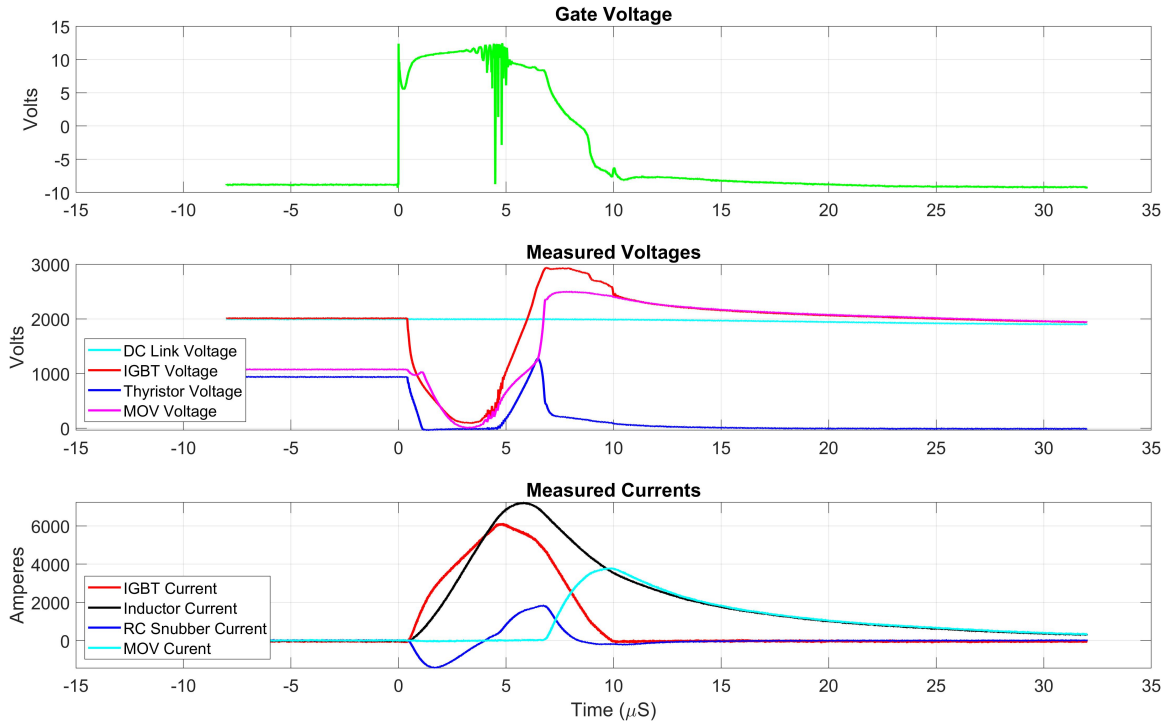

Figure 3.15. Narrow Bus Bar, "Hole #2" Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω L_{sys}=1 μH

Peak current through the SSCB was at 7238 A, a peak IGBT current at 6148 A, and desaturation protection of the IGBT are shown. This is the first test where 12 V_{GE} achieves an apparent current saturation behavior of the IGBT module and operations in the active region. The voltage profile for the transient begins to approach that in Figure 2.8 where the IGBT V_{CE} is at a value higher than the typical values seen during saturation region operations. V_{CE} during the period of active operation was approximately 200 V in this test case. The BOD, SCR, and MOV behavior are all comparable to previous testing done. The time for the IGBT to stop conducting during the test was 5 μs from a peak of 6148 A to 0 A. The MOV peak clamp voltage was approximately 2500 V and took approximately 25 μs to decay to system voltage.

This test showed a current profile strongly dependent on which hole was used for cable termination. The narrow bus bar was unable to provide a uniform voltage field and conduct

a uniform current density from the cable into the IGBT. This behavior was also noted and reproduced by collaboration partners at Clemson University.

Z-Shaped Bus Bar

The narrow bus bar was replaced with a z-shaped bus bar, shown in Figure 3.16, to provide a more even current distribution to the IGBT module by allowing a more uniform voltage field at the IGBT module chips. The same test procedure was used with "Hole #1," "Hole #2," and "Hole #3." t_{on} for each test was 10 μs and V_{GE} was 12 V. Only the negative emitter bus bar was modified for this test, the other emitter bus bar remaining in the narrow configuration and terminated at "Hole #2." Note that the non-triggered IGBT module is not actively gated and only the freewheeling diode inside that module is utilized for current conduction, and therefore the impact of bus bar shape and cable termination there is not significant for this test. Also, a wide, flat copper bus is used to connect the collectors of the two IGBT modules, further reducing any impact the emitter bus bar and power cable termination at the unswitched IGBT module might have on the SSCB switching performance under evaluation.

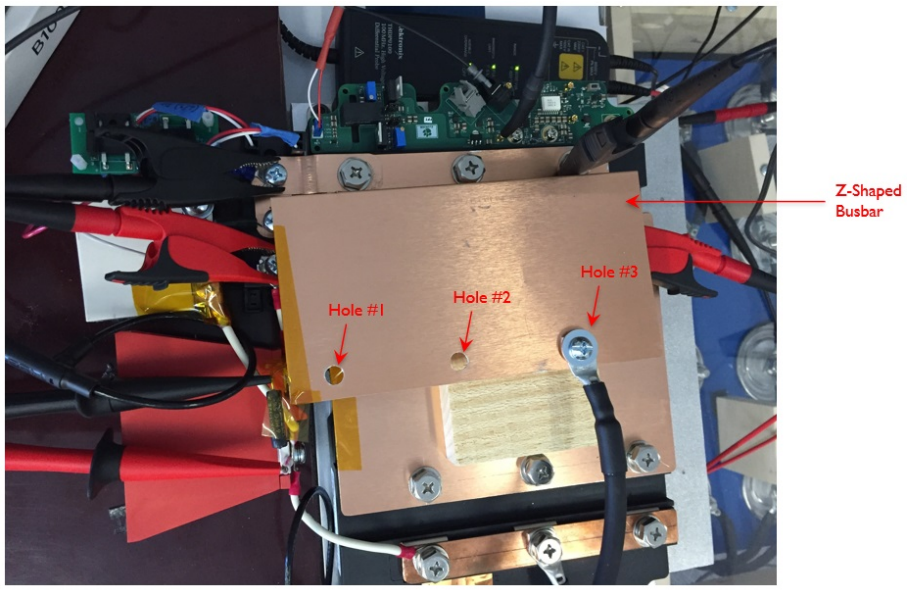

Figure 3.16. SSCB Configuration with Z-Shaped Emitter Bus Bar

A wood block was used to provide mechanical support to the copper bus bar to minimize the mechanical stresses on the angled bar and IGBT module power terminals from the cable termination. Tests indicated with an asterisks in Table 3.10 are where desaturation protection occurred.

Table 3.10. Z-Shaped Bus Bar, "Hole #1," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	5308	4930	1256	2732*
1600	5327	4663	1252	2901*
2000	5817	4962	1256	3126*

The effects of the larger bus bar were immediately obvious. Compared to the "Hole #1" test with a narrow bus bar, a higher current through the IGBT module was observed during the conduction period. For a nearly identical peak voltage during the 2000 V test, an additional 750 A was carried through the IGBT. "Hole #2" test results are shown in Table 3.11.

Table 3.11. Z-Shaped Bus Bar, "Hole #2," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
800	4616	4466	1254	2543*
1000	5126	4903	1259	2648*
1200	5479	5145	1255	2748*
1400	5771	5232	1254	2848*
1600	5878	5152	1253	2939*
1800	5801	5002	1254	3024*
2000	6101	5213	1253	3191*

Compared to the "Hole #2" test with a narrow bus bar, the total current through the IGBT and system was less with the z-shaped bus bar. The total current values conducted through "Hole #2" were almost 20% greater in the narrow bus bar configuration. Compared with the narrow bus bar test, more current was conducted in the "Hole #1" case, while a lower current was measured in the "Hole #2" case. It is also noted that with the z-shaped bus bar, the current difference between the "Hole #2" case and "Hole #1" case is much less, the peak current at the 2000 V test point being only 5% higher than that in the "Hole #1" case. The test in "Hole #3" is shown in Table 3.12.

Table 3.12. Z-Shaped Bus Bar, "Hole #3," R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	5069	4723	1250	2721*
1600	5101	4389	1250	2891*
2000	5553	4744	1254	3120*

Compared to the “Hole #3” test with a narrow bus bar, “Hole #3” on the z-shaped bus bar was able to carry a nominal level of fault current that did not exceed system design parameters at operating system voltage. It is also noted that with the z-shaped bus bar, the current developed in the “Hole #3” case is lower than that in the “Hole #1” case. The peak current was about 5% less than that observed in the “Hole #1” test. The dependence upon which termination location used with a wider bus bar is far less pronounced than with the narrow bus bar. “Hole #2” transient response is shown in Figure 3.17.

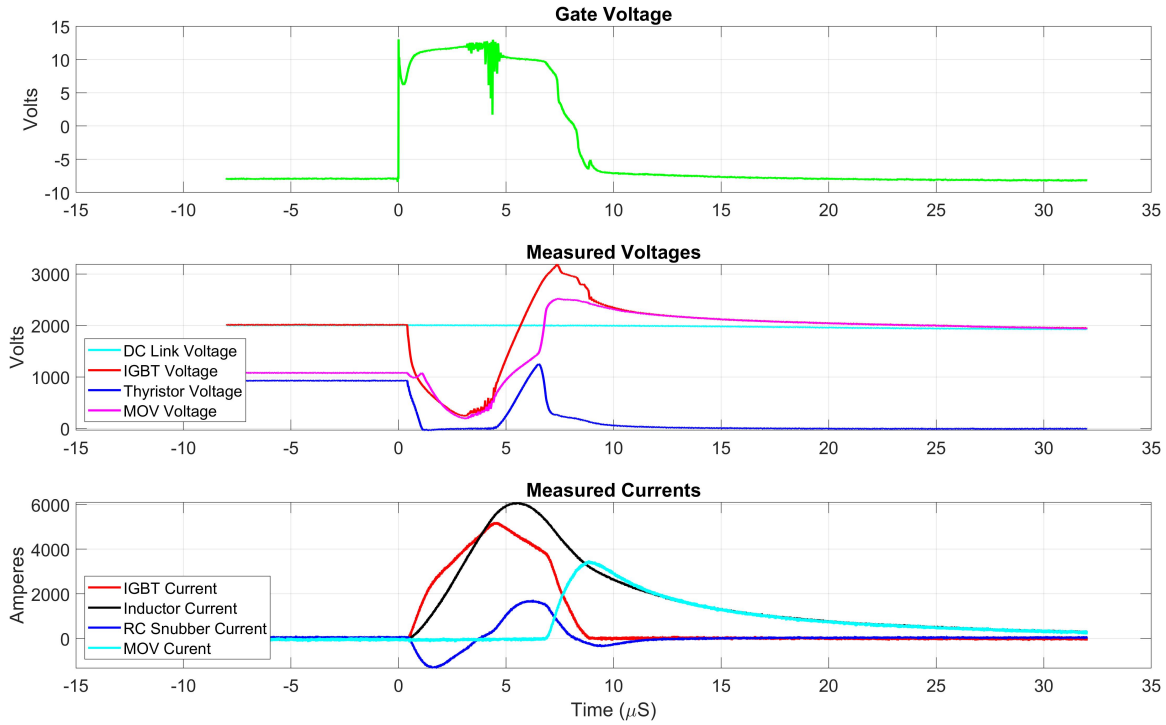

Figure 3.17. Z-Shaped Bus Bar, “Hole #2” Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=6800 pF, R_{STO}=4 Ω, R_{off}=4 Ω, L_{sys}=1 μH

Peak current through the SSCB was at 6101 A, a peak IGBT current at 5213 A, and desaturation protection of the IGBT are shown. With all the other conditions staying the same, the short circuit current was about 1000 A less than when conducted through the narrow bus bar. The IGBT demonstrates active mode of operation with a V_{CE} of 250 V during this period. This current self-limitation behavior again approaches what is shown

in Figure 2.8. All other SSCB components functioned as expected. The IGBT stopped conduction in 5 μs and the time for the MOV to achieve system voltage from a clamp voltage of 2500 V was 20 μs.

This test showed that the IGBT current profile was weakly affected by the cable termination location with a larger bus bar. However, a dependence on the termination location was still observed, and all further tests were conducted from "Hole #2" or "Hole #3" and were labeled as such to provide a continuity for comparison and reproducible results. The narrow bus bar was no longer used for testing as the voltage and current dependence on termination location had a noticeably negative impact on system performance.

3.2.4 Desaturation Tuning

The majority of the testing of the SSCB to this point had caused desaturation protection of the IGBT to initiate current interruption and fulfill the typical functions required of a circuit breaker. Desaturation protection is determined by the gate driver board, and is able to be tuned through components built into the gate drive board. By carefully tuning $C_{blanking}$ and R_{STO}, the SSCB is able to achieve consistent performance, striking the best compromise among protection sensitivity, switching time, device thermal stress and transient voltage containment. Improper tuning of $C_{blanking}$ and R_{STO} can cause damage to the IGBT as desaturation protection is the method of short circuit protection for the IGBT itself, separate from external circuitry. The blanking capacitor, $C_{blanking}$, is used to determine when the gate circuitry begins to monitor for an over current condition. A longer blanking time can be achieved by increasing $C_{blanking}$, making the current saturation or active region operation more apparent at a V_{GE} of 12 V. R_{STO} is used to determine the rate at which the IGBT turns off when triggered by desaturation protection. The turn-off resistor, R_{off}, on the other hand, determines the turn-off rate of the IGBT upon a normal gating command issued by the operator or upper level controls. R_{on} determines how rapidly the IGBT turns on. R_{on} has stayed at 0.3 Ω in all the tests reported in this thesis.

The desaturation protection components, $C_{blanking}$ and R_{STO}, were tuned in an iterative process and the final desaturation test is detailed in Table 3.13. The final capacitance value for $C_{blanking}$ was 13400 pF and R_{STO} was 10 Ω.

Table 3.13. V_{GE}=12 V, "Hole #3," R_{on}=0.3 Ω, R_{off}=4 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, L_{sys}=1 μH, t_{on} 10 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	5807	5245	1215	2578*
1600	6079	5308	1216	2788*
2000	6493	5654	1221	2983*

Comparing the post-tuning test to the previous "Hole #3" test with the z-shaped bus bar, the IGBT carries more current prior to fault interruption due to the longer delay time provided through a higher $C_{blanking}$. This allows more time for the fault current develop before desaturation protection activates. Consequently, this gives the IGBT more opportunity to become current saturated, demonstrating active region operation. On the 2000 V test, shown in Figure 3.18, compared with the 2000 V case detailed in Table 3.12, almost 1000 A additional current was carried through the system and IGBT during the transient. However, peak voltage across the SSCB was 140 V less, indicating the R_{STO} tuning resulted in a smaller di/dt, and thus less inductive voltage. The desaturation tuning process was sufficient for allowing desaturation protection to occur at very low system inductance while utilizing the reduced I_C active region initiation from a reduced V_{GE}.

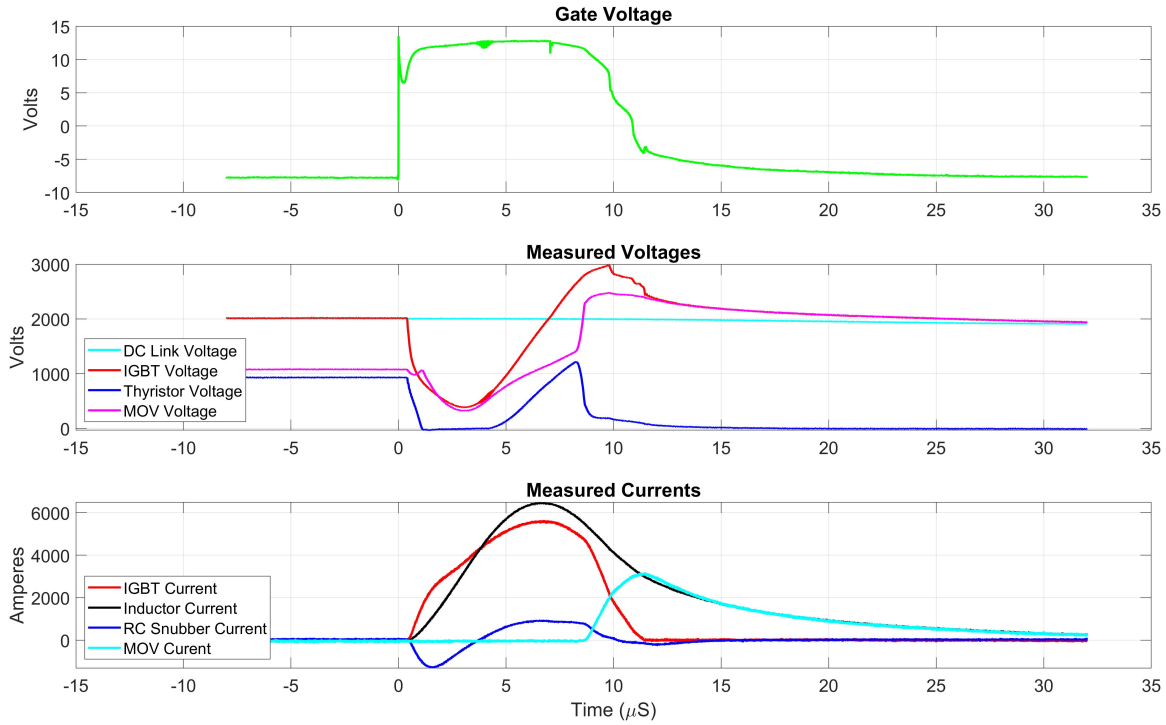

Figure 3.18. "Hole #3," V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, R_{off}=4 Ω, L_{sys}=1 μH

I_C maximum was 5654 A, I_{sys} peaked at 6493 A and the IGBT turned off by desaturation protection as shown. Peak V_{SSCB} occurred at 2983 V. Importantly, the IGBT can be seen entering active mode operation as V_{CE} drops from system voltage to approximately 350 V. This was a higher active region voltage than seen previously in Figure 3.17. The IGBT current falling rate of change is noticeably lower during the turn-off, due to increased R_{STO}. The SCR, BOD, and MOV voltage and current waveforms all reflect the typical operating behavior of the circuit prior to desaturation tuning. The MOV peak voltage is 2500 V and decays to system voltage after 20 μs. The desaturation tuning process was effective for achieving the desired SSCB operation at low system inductances while still providing for short circuit protection and maintaining peak current through the IGBT less than 6 kA.

The post-tuning transient responses are shown in Figure 3.19 and Figure 3.20 for increasing system inductance. The IGBT does not enter active region operation similar to previous tests at higher system inductance.

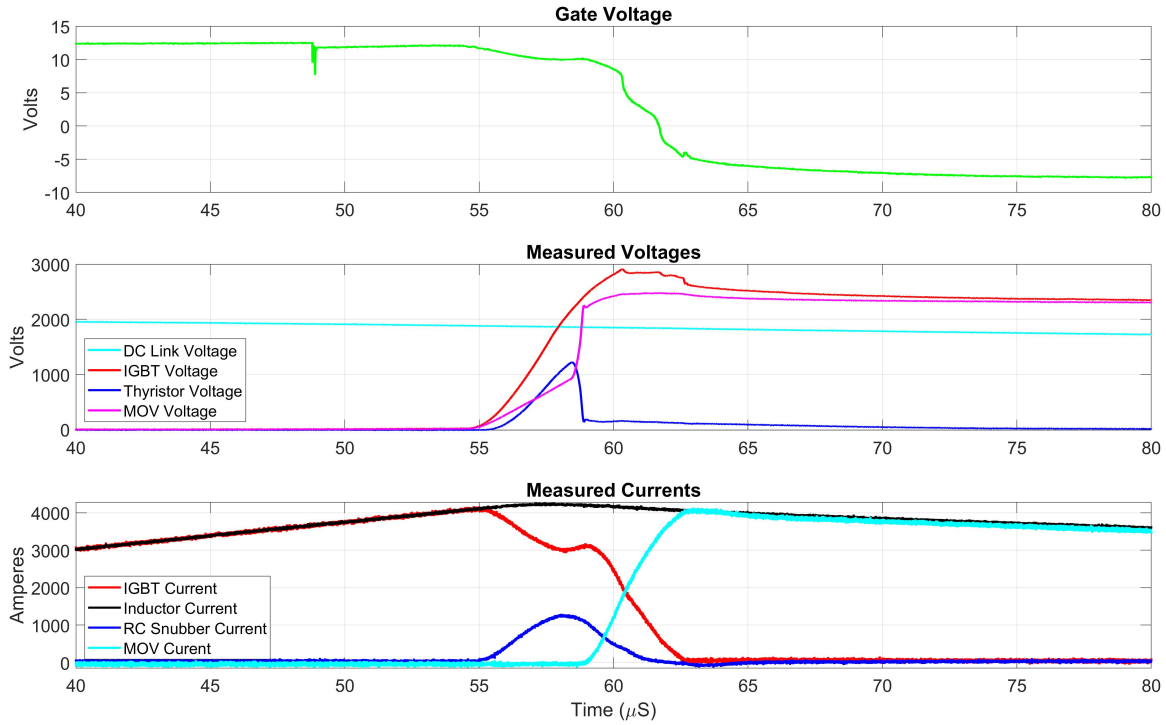

Figure 3.19. "Hole #3," V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, R_{off}=4 Ω, L_{sys}=25 μH

I_C maximum was at 4175 A, I_{sys} peaked at 4281 A and the IGBT was turned off by desaturation protection. Peak V_{SSCB} occurred at 2910 V. Due to a higher system inductance, the IGBT current is not sufficient to drive the IGBT into active region operation, as V_{CE} remains relatively low during the conduction period. Additionally, due to the higher amounts of energy within the system, the MOV conduction time is significantly longer, with V_{MOV} remaining above system voltage for about 160 μs. The IGBT current fall time is approximately 7 μs. The gate voltage slowly lowers from 12 V to 10 V, resulting in an active region operation momentarily from 55 μs to 59 μs during the transient test before the gate is completely removed, about 4 μs later.

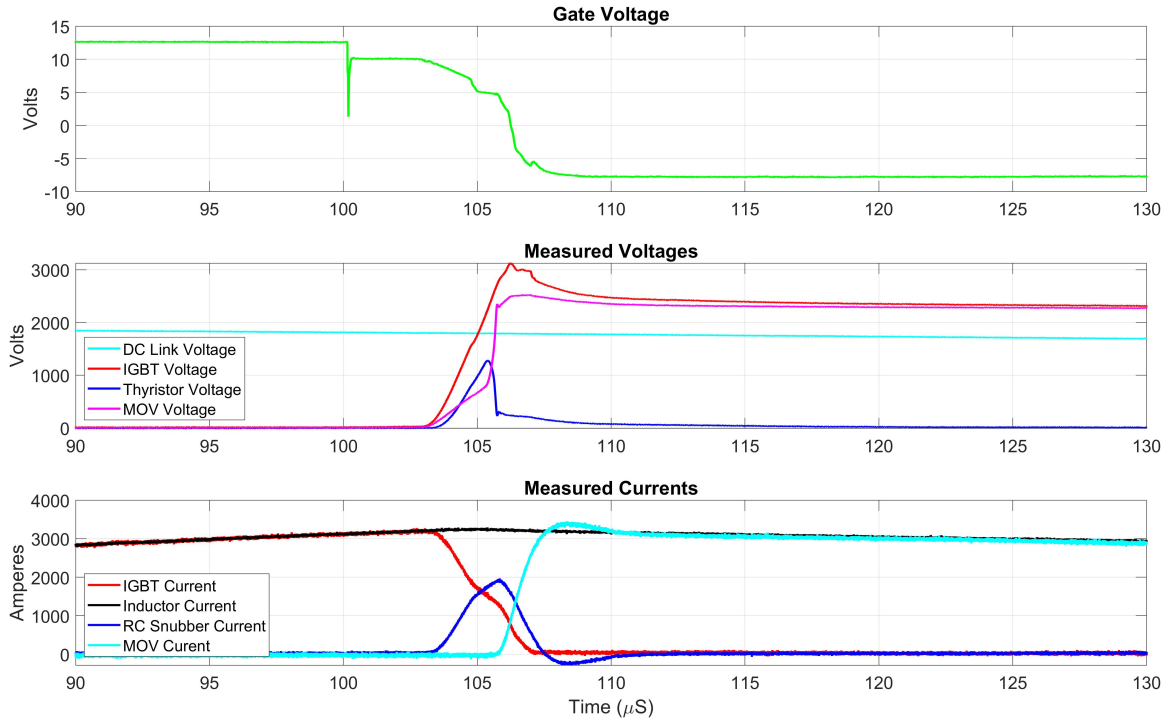

Figure 3.20. "Hole #3," V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, R_{off}=4 Ω, L_{sys}=50 μH

Figure 3.20 shows IGBT turned off by the gate command at 100 μs rather than desaturation protection, with I_C maximum occurring at 3276 A, I_{sys} peak at 3290 A and peak V_{SSCB} occurring at 3125 V. Due to a higher system inductance, the IGBT current is not sufficient to drive the IGBT into active region operation, as V_{CE} remains relatively low during the conduction period. In this test, the peak current values are more than 2000 A lower than the minimal inductance tests. The di/dt reduction from the higher system inductance provides sufficient reduction in the current rate of change that the IGBT desaturation protection circuitry does not trigger with the given on-state pulse length of 100 μs, and the IGBT is turned off when V_{GE} is driven negative after 100 μs. The IGBT current fall time is approximately 3 μs, which is shorter due to the lower resistance value of R_{off} compared with R_{STO}. MOV voltage reaches a peak clamping voltage of 2500 V and decays to system voltage 250 μs after the turn-off transient is initiated.

As a further test step, the location of the capacitor bank was adjusted following the previous

tests to realize the lowest system inductance the test configuration was able to achieve and shown in Figure 3.21. The capacitor bank was raised on a platform and set as close to the SSCB as possible. The connect leads were cut as short as possible and twisted together to minimize the cabling inductance.

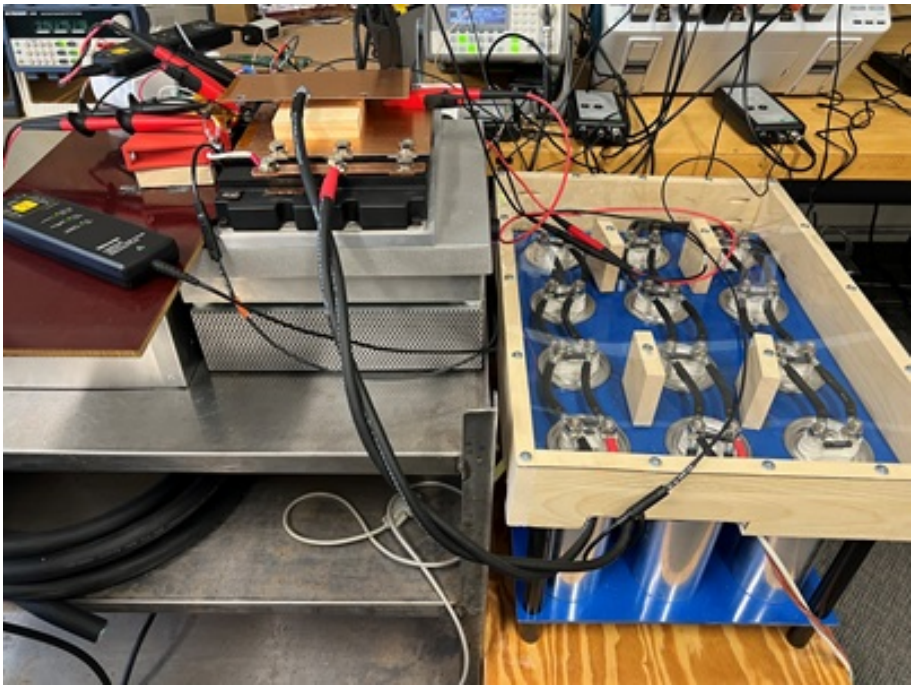

Figure 3.21. Minimizing Total Inductance by Relocating Capacitor Bank, L_{total} 0.65 μH

The power cables were twisted together to minimize the cabling inductance, resulting in a total inductance, $L_{\text{total}} = L_{\text{sys}} + L_{\text{CB}}$, to an calculated 0.65 μH. As L_{sys} was sufficiently reduced, L_{CB}, which arises from the power circuit connections within the SSCB, begins to have a noticeable effect on system response and is included in the inductance calculations. Additionally, the terminating connection was made in "Hole #2" and remained in this location for all following tests. All other parameters were the same as in previous desaturation tuned tests and the results are shown in Table 3.14.

Table 3.14. V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, R_{off}=4 Ω, L_{total}=0.65 μH, t_{on} 10 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1000	5528	4906	1205	2122*
1200	5610	4889	1206	2306*
1600	6022	5221	1209	2637*
2000	6301	5498	1213	2922*

Although the total inductance was reduced, the peak currents and voltages experienced during the transients were slightly less than those when compared with the "Hole #3" test results shown in Table 3.13, due to relocating the termination point in "Hole #2" as well as tightened power cabling between the capacitor bank and the SSCB. This shows the slight dependence upon the hole location for current and voltage profiles, but the change remains minimal when compared to the narrow bus bar and can be seen in Figure 3.22.

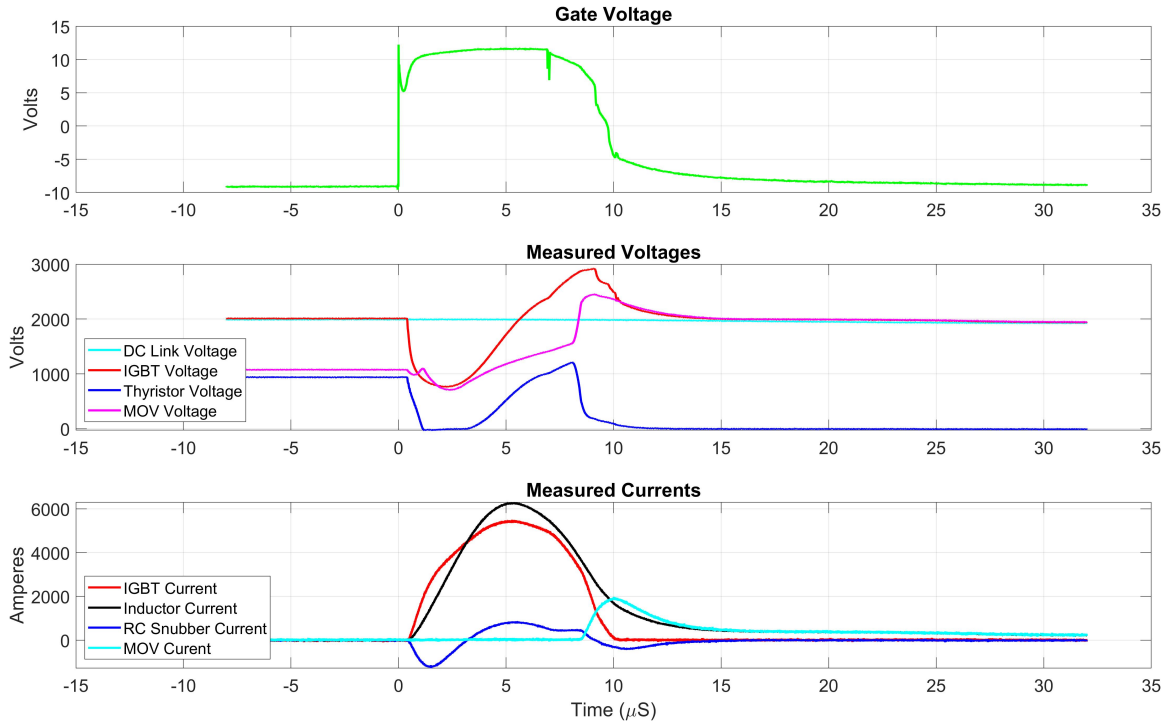

Figure 3.22. V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=10 Ω, R_{off}=4 Ω, L_{total}=0.65 μH

The lower system inductance resulted in an active region of operation of the IGBT with V_{CE} never dropping below 750 V for the final 2000 V test. The distortion to the IGBT current di/dt also points to the active region operation. The tuned desaturation circuitry and reduced gate voltage, along with the z-shaped bus bar, have all contributed to achieving the desired SSCB behavior, including IGBT current saturation under fault condition and contained transient voltage during current interruption, thus maintaining peak voltage and peak currents within the nominal specification parameters and component limits.

3.2.5 High Temperature Switching Test

Room Temperature Baseline

To further optimize the SSCB operation, additional modifications to the gate drive board were made following the initial tuning of R_{STO}. R_{STO} was increased to 22 Ω and the turn-off

resistance, R_{off}, was increased from 4 Ω to 10 Ω. Raising R_{STO} and R_{off} was to further reduce the peak SSCB voltage during a turn-off transient by reducing the turn-off rate, at the cost of longer turn-off delay and turn-off time. These tests became the baseline for comparison when testing the SSCB and IGBT at "operational" temperatures. The 0.65 μH inductance test is shown in Table 3.15.

Table 3.15. Room Temperature, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{total}=0.65 μH, t_{on}=10 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	5567	4850	949	1911*
1600	5968	5207	1039	2343*
2000	6269	5473	1131	2830*

During these tests, the BOD voltage did not rise to the breakover level and therefore the electronic MOV did not participate in the turn-off transient. This is due to the reduced turn-off rate and lower transient voltage across the SSCB. With R_{STO} at 22 Ω, the electrically tight connection between the SSCB and capacitor bank as well as the RC snubber branch result in well contained IGBT voltage during turn-off, insufficient to activate the electronic MOV branch and can be seen in Figure 3.23. This is not a problem since safe device operation can be achieved without the electronic MOV participation. As the system inductance increases, typical switching waveforms with electronic MOV action returns.

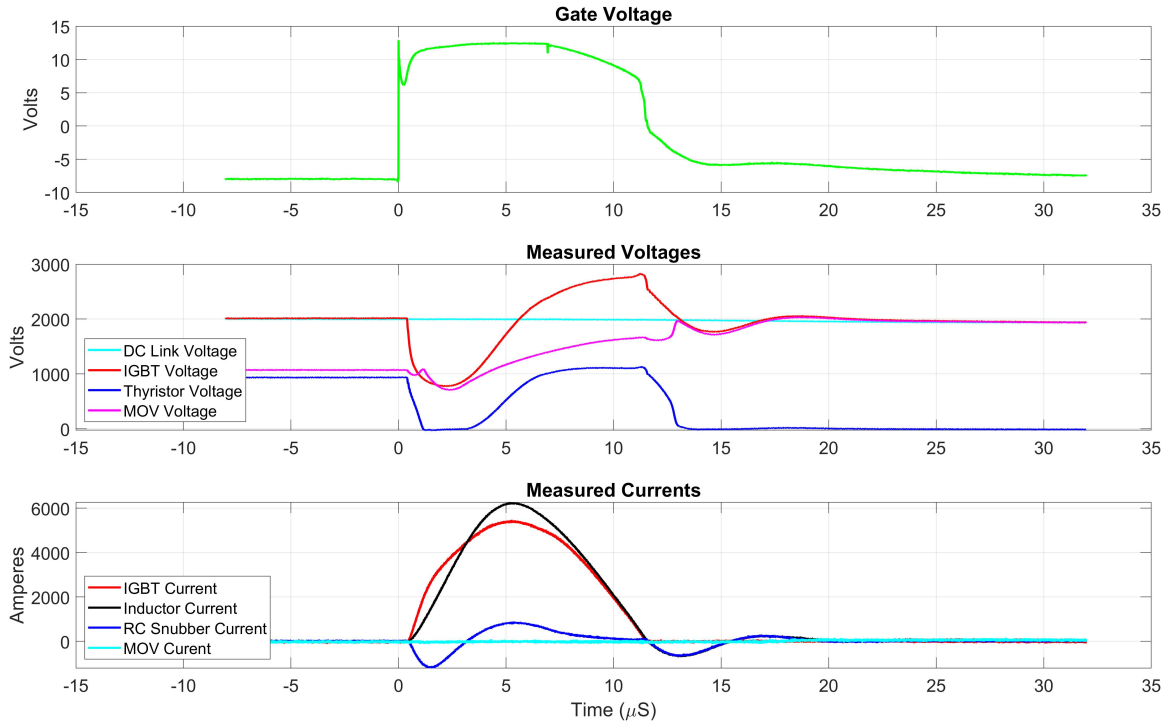

Figure 3.23. Room Temperature, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{total}=0.65 μH

With the higher R_{STO}, the peak current values were almost identical to the previous test at 2000 V, but the peak system voltage was nearly 100 V lower. As described above, in the tests at this minimal system inductance, the triggering of the SCR did not occur. Active region operation behavior is apparent upon the short circuit initiation, with the IGBT voltage showing a minimum at approximately 750 V and increasing with I_C. The IGBT current saturated operation is sufficient to limit the fault current through the IGBT to less than 6000 A at the minimal system inductance.

System inductance was incremented up to 25 μH to continue characterizing the system performance with the tuned desaturation protection circuitry. With a gate pulse width of 100 μs, desaturation continued to occur, and active region operation was no longer observed at higher system inductance. Table 3.16 presents the test results.

Table 3.16. Room Temperature, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH, t_{on}=100 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	4221	4167	1202	2688*
1600	4461	4348	1203	2747*
2000	4661	4477	1202	2823*

As noted earlier, BOD and SCR behavior returned to expected at a higher system inductance. The SSCB waveforms are shown in Figure 3.24 for the 2000 V test.

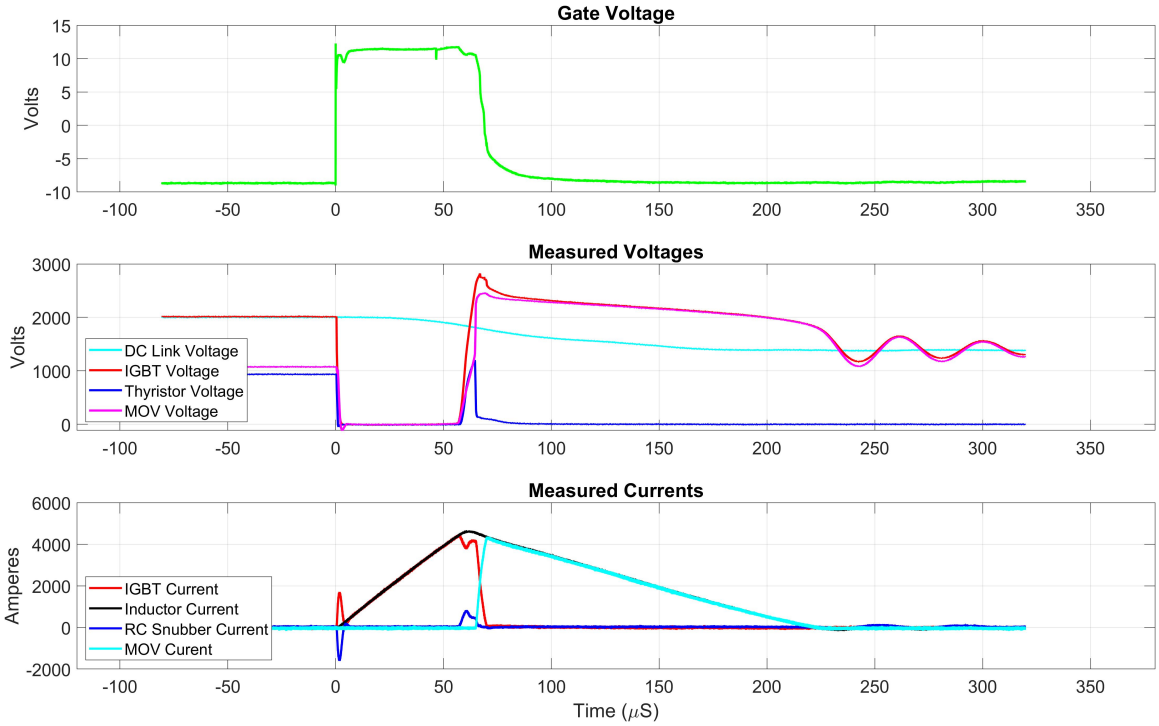

Figure 3.24. Room Temperature, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH

Compared to the previous test at the same operating parameters where "Hole #3" was used, the peak current values are 200 A to 300 A higher. The higher R_{STO} causes a longer turn-off duration, allowing the fault current to rise to a higher peak value. The dependence on hole selection for the terminal connection is minuscule with L_{sys} at 25 μH. As noted earlier, the SCR triggering process from the BOD breakover point functions as expected, and the characteristic MOV voltage clamping behavior is observed. The zoomed in transient response is shown in Figure 3.25.

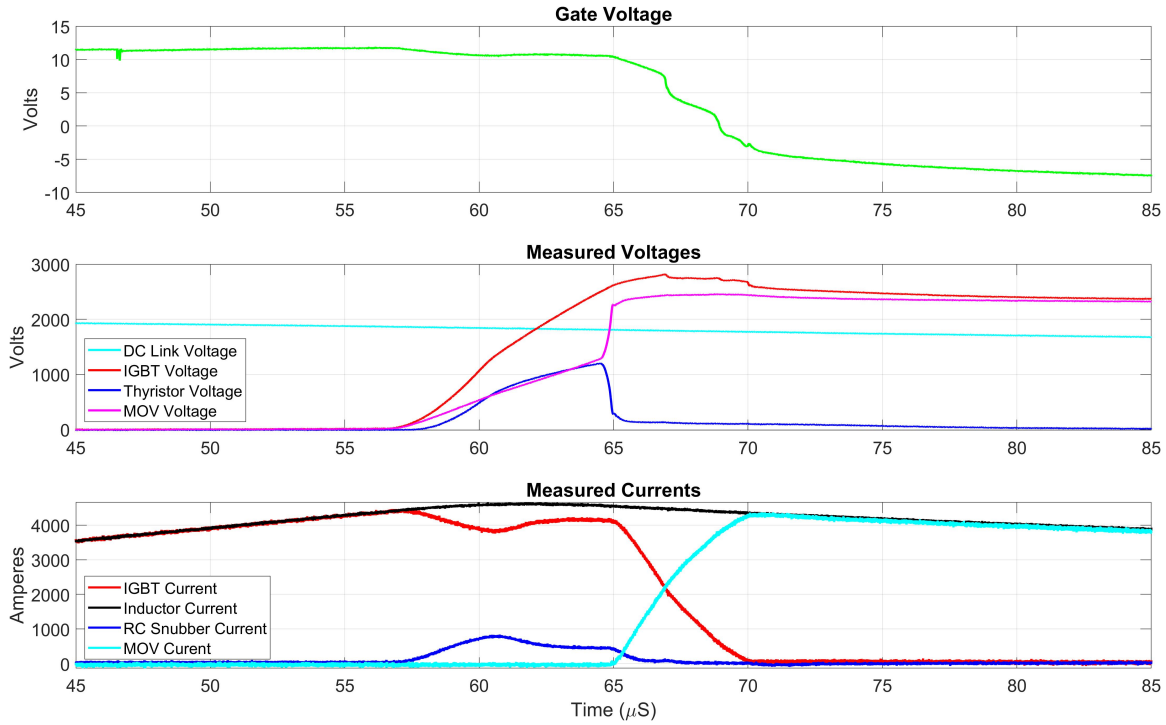

Figure 3.25. Room Temperature Zoomed In Transient Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH

During the conduction period, the rise in current through the IGBT is nearly linear until the IGBT is turned off due to desaturation protection. Upon desaturation detection, there is a delay before the gate voltage starts to reduce from 12 V to 10 V, where the current barely changes from 57 μs to 65 μs. This is the time interval when the Miller capacitance is charged up, during which the IGBT voltage V_{CE} rises while the IGBT current I_C changes

little. After the so-called Miller plateau, the gate voltage decreases rapidly together with the IGBT current I_C, which lasts for approximately 5 μs. The total duration from the desaturation detection to complete commutation of the IGBT current is about 24 μs. A higher R_{STO} accounts for the longer transient duration.

For the 50 μH test conducted below in Table 3.17, the time duration of the gating signal for the first test was 100 μs and the second test was conducted for 167 μs. The longer test was necessary to activate the desaturation protection of the IGBT.

Table 3.17. Room Temperature, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=50 μH

DC Bus Voltage (V)	t_{on} (μs)	I_{sys} Peak (A)	I_{IGBT} Peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
2000	100	3483	3433	1236	2866
2000	167	4141	4064	1211	2766*

The 100 μs transient is shown in Figure 3.26. The gating signal is seen to be removed after 100 μs, as commanded.

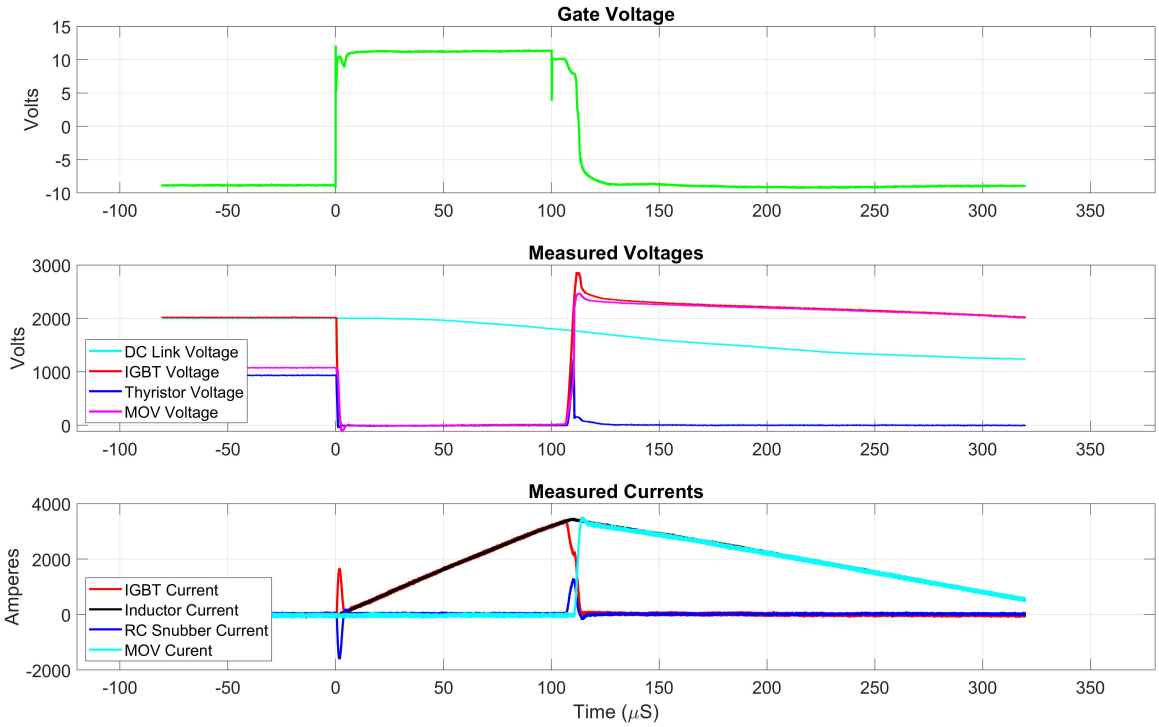

Figure 3.26. Room Temperature, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=50 μH

During the turn-off, the SCR triggering behavior from the BOD performed as expected. The MOV voltage response is as expected with the rapid rise from SCR trigger initiating the current flow through the MOV to the max clamping voltage. The IGBT current fall time is about 6 μs, a longer duration compared with the case where R_{off} is 4 Ω.

100 °C Switching Transient

After the room temperature baselines were recorded, the IGBT module mounted on the hot plate was heated and the temperature was raised to 100 °C. The previous tests were conducted at this higher temperature to observe the change in IGBT behavior and the results shown in Table 3.18. A "softer" response is expected due to the IGBT positive temperature coefficient and a slightly longer duration for turn-off to occur.

Table 3.18. T_j 100 °C, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{total}=0.65 μH, t_{on}=10 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	4657	3973	833	1803*
1600	4928	4188	904	2219*
2000	5160	4410	988	2649*

Similar to the room temperature tests, the BOD voltage did not rise to the breakover level and therefore the electronic MOV did not participate in the turn-off transient. The SSCB response waveforms are shown in Figure 3.27.

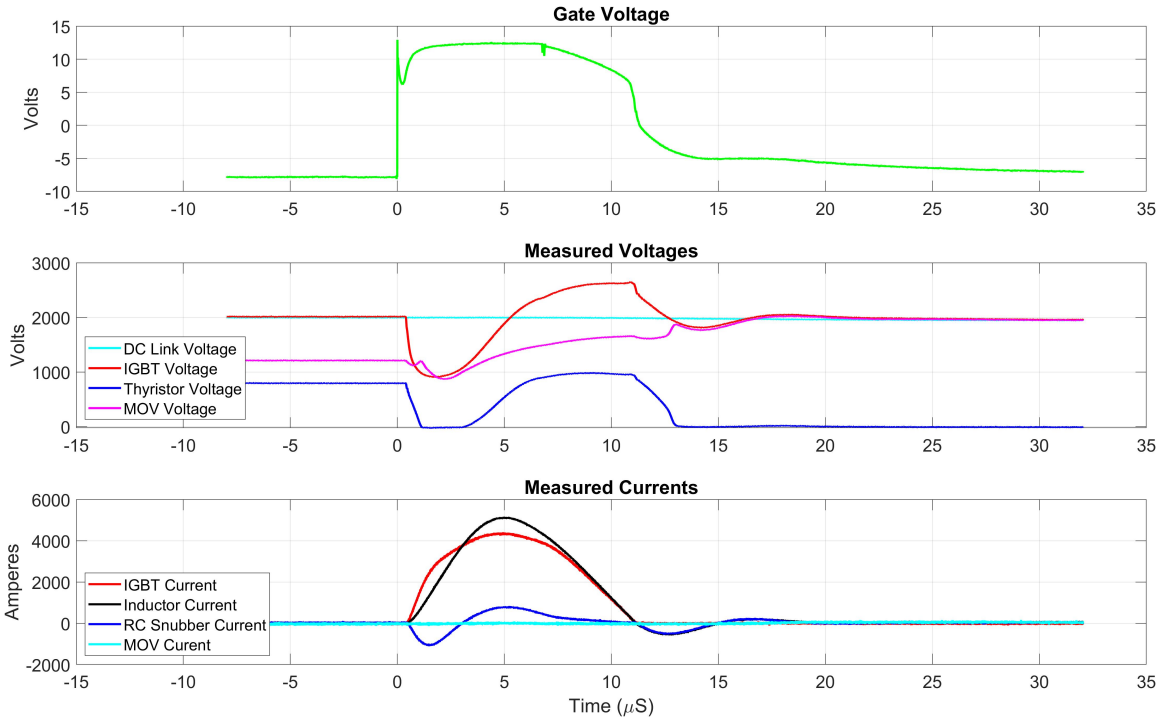

Figure 3.27. T_j 100 °C, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{total}=0.65 μH

Compared to the room temperature tests, the elevated temperature tests experienced lower peak voltages and currents. The active region voltage was higher. These effects are attributable to the positive temperature coefficient discussed in Subsection 2.2.1. Active region operation continued to be observed at the nominal system voltage. The minimum V_{CE} during the test was approximately 900 V whereas the room temperature test had a minimum voltage of 750 V. The SCR was not triggered during the test, due to insufficient voltage rise across the BOD during the turn-off process. The active region of operation in the IGBT was sufficient to limit fault current through the SSCB and peak I_C, at 5160 A and 4410 A, respectively, compared with 6269 A and 5473 A, respectively, observed in the short circuit test at the room temperature.

The test was repeated as the inductance was incremented from an absolute minimum through 25 μH to 50 μH and are shown in Table 3.19 and Table 3.20.

Table 3.19. T_j=100 °C, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH, t_{on}=100 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
2000	4168	3900	1204	2750*

Only one data point was collected at a system inductance of 25 μH due to observed performance at minimum system inductance showing lower device voltage and current stresses at elevated temperature. Behavior at elevated temperatures continues to show a lower peak current and voltage value when compared to room temperature operation. Additionally, the higher system inductance continues to limit the current rate of change sufficiently to maintain the IGBT operating in the saturation region instead of the active region experienced at very low system inductance. BOD and SCR behavior returned to expected as noted earlier in the section. Figures 3.28 and 3.29 present the waveforms captured during the high temperature test with L_{sys}=25 μH, and the zoomed-in portion showing the turn-off details, respectively.

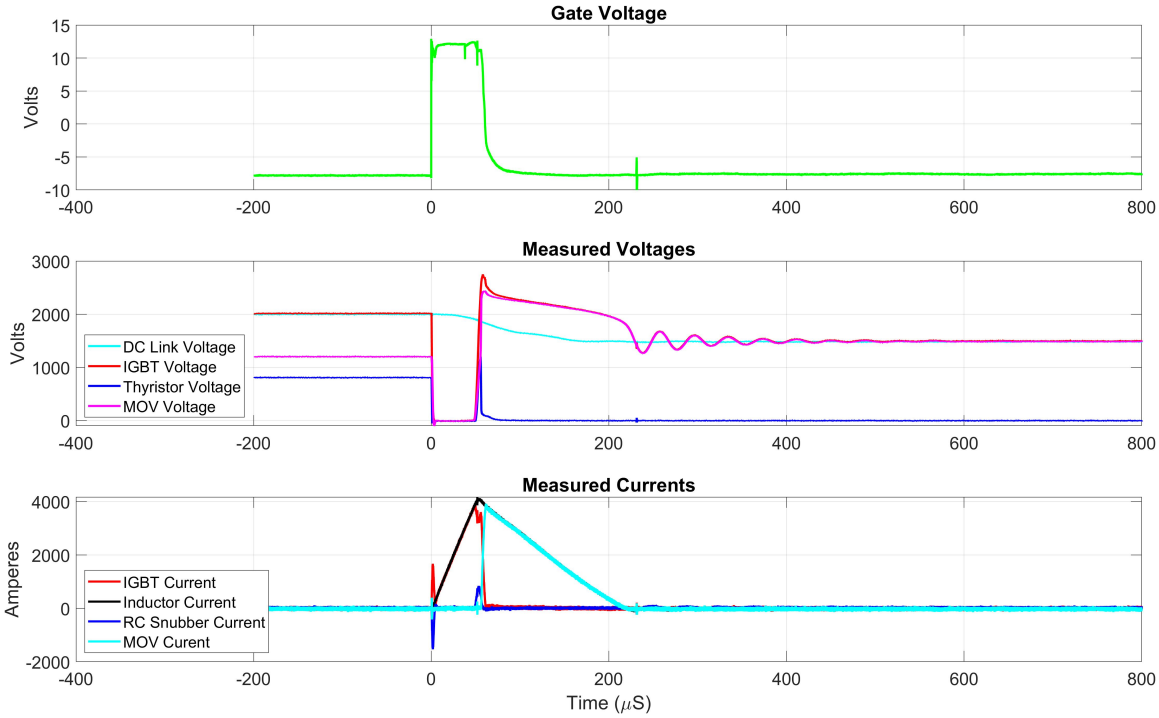

Figure 3.28. T_j=100 °C, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH

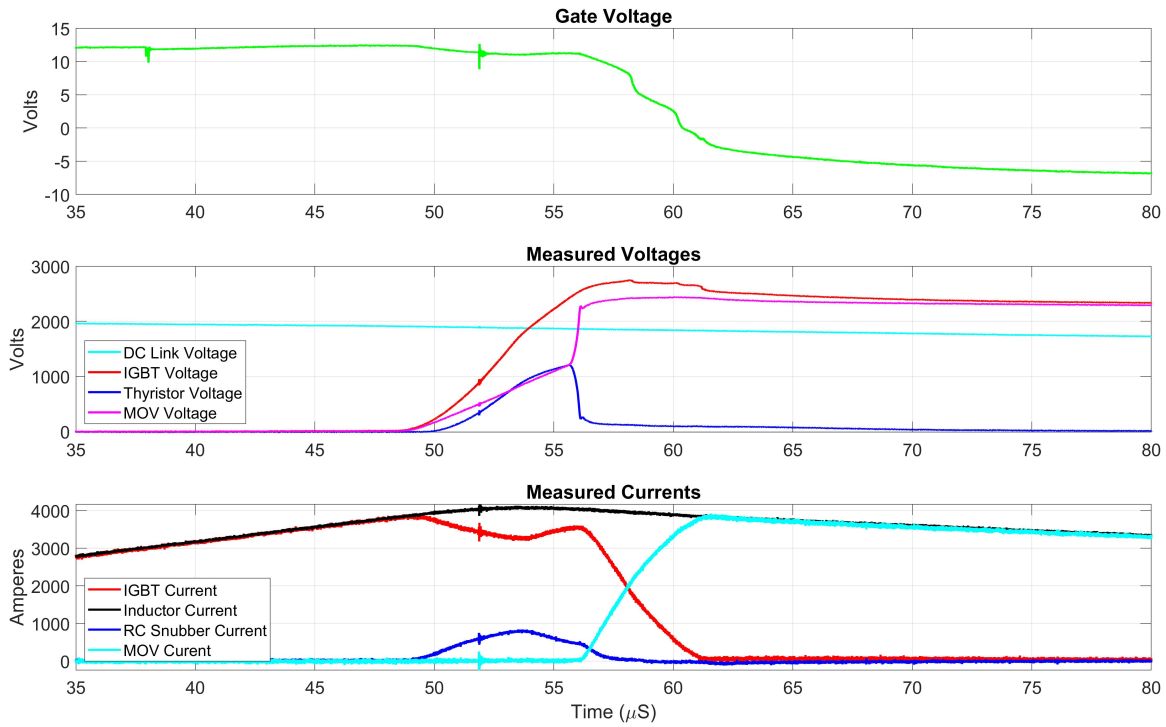

Figure 3.29. Zoomed In Transient Response, T_j=100 °C, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH

The turn-off transient at elevated temperatures shows lower peak voltages and currents and a smoother transition from the room temperature tests. The time for the IGBT to switch to carrying no current is 13 μs whereas the room temperature test only required 11 μs. Peak MOV clamping voltage is approximately 2450 V. Nominal SCR behavior was observed as the BOD trigger turned on the SCR and current initiated through the MOV in less than 1 μs. A full system inductance test was conducted and is shown in Table 3.20.

Table 3.20. T_j=100 °C, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=50 μH, t_{on}=100 μs

DC Bus Voltage (V)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1200	2197	2087	1241	2752
1600	2859	2744	1243	2847
2000	3667	3516	1211	2711*

The test with the DC bus voltage at 2000 V shows that the SSCB operates with a peak current approximately 500 A less than at room temperature, and peak voltage approximately 50 V less than at room temperature. The operational temperature tests continue to show a "softer" performance of the SSCB and IGBT during fault transient operations at elevated temperatures and can be seen in Figure 3.30.

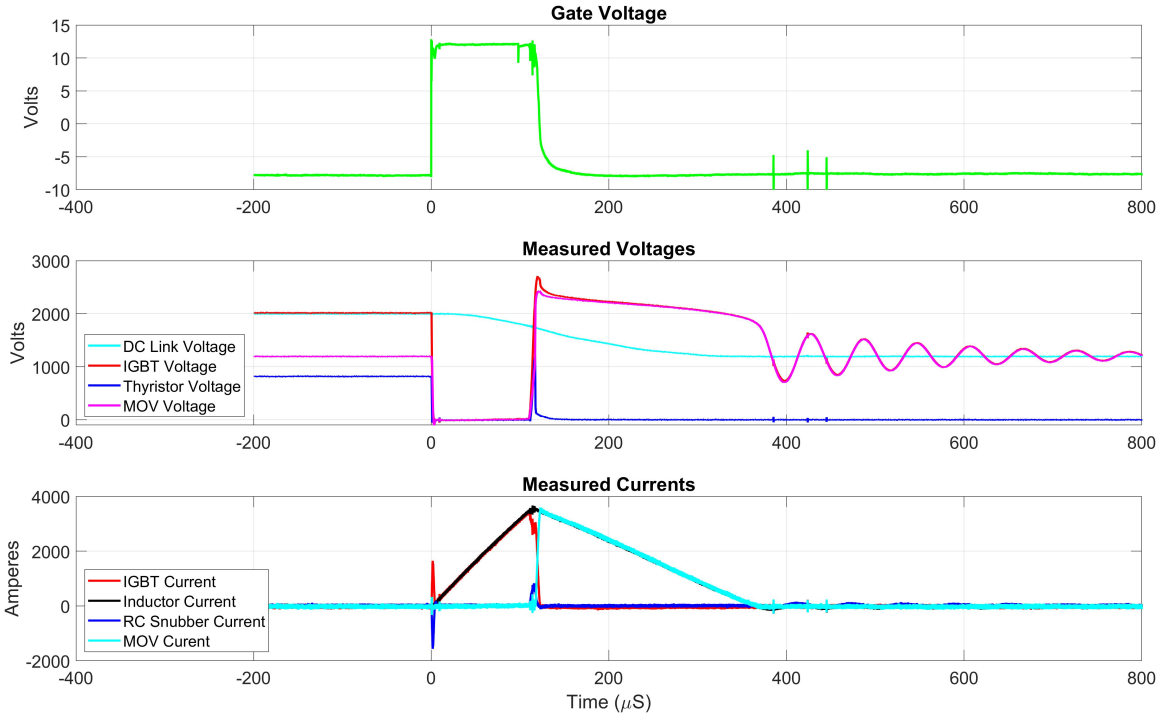

Figure 3.30. T_j=100 °C, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=50 μH

The total time to dissipate all inductive energy within the system was about 800 μs. The peak voltages and currents experienced during the operational temperature test were noticeably lower than those from the room temperature test. Additionally, the IGBT turn-off time is slightly longer.

The thermally affected response of the IGBT and SSCB was as expected with reduced peak voltage and current values, a longer transient response, and an increased margin to design parameters and device operating limits.

3.2.6 MOV Performance Improvements

Changes to the SSCB transient response can be made by adjusting the MOV characteristics, especially the clamping voltage. In addition to energy dissipation capability sufficient for the specified system inductance and fault current rating, an ideal MOV should have sufficiently low clamping voltage up to the maximum fault current that might flow through the SSCB, while a sufficiently low leakage current at the nominal DC system voltage. These specifications usually are in conflict, and the MOV manufacturers typically have a limited range of parts. Therefore a compromise has to be made prioritizing leakage current or clamping voltage. Another consideration is the mechanical form factor of the MOV, which affects the SSCB internal component layout and the insulation performance.

After several trials with various configurations using commercially available MOVs from the same manufacturer, the MOV configuration was refined by replacing the "BA" body style MOV with a "DB" body style. The "DB" body style is preferred for mechanical layout and insulation considerations. It has lower current and energy ratings than the "BA" style MOV, and therefore such MOVs need to be used in parallel. By the series connection of two MOVs of about half the voltage rating, the resulting configuration could allow a better compromise between the clamping voltage and leakage current. The resulting new configuration utilized two MOV sets in parallel, and two MOVs in series in each set, as shown in Figure 3.31. This configuration is called the 2P2S configuration.

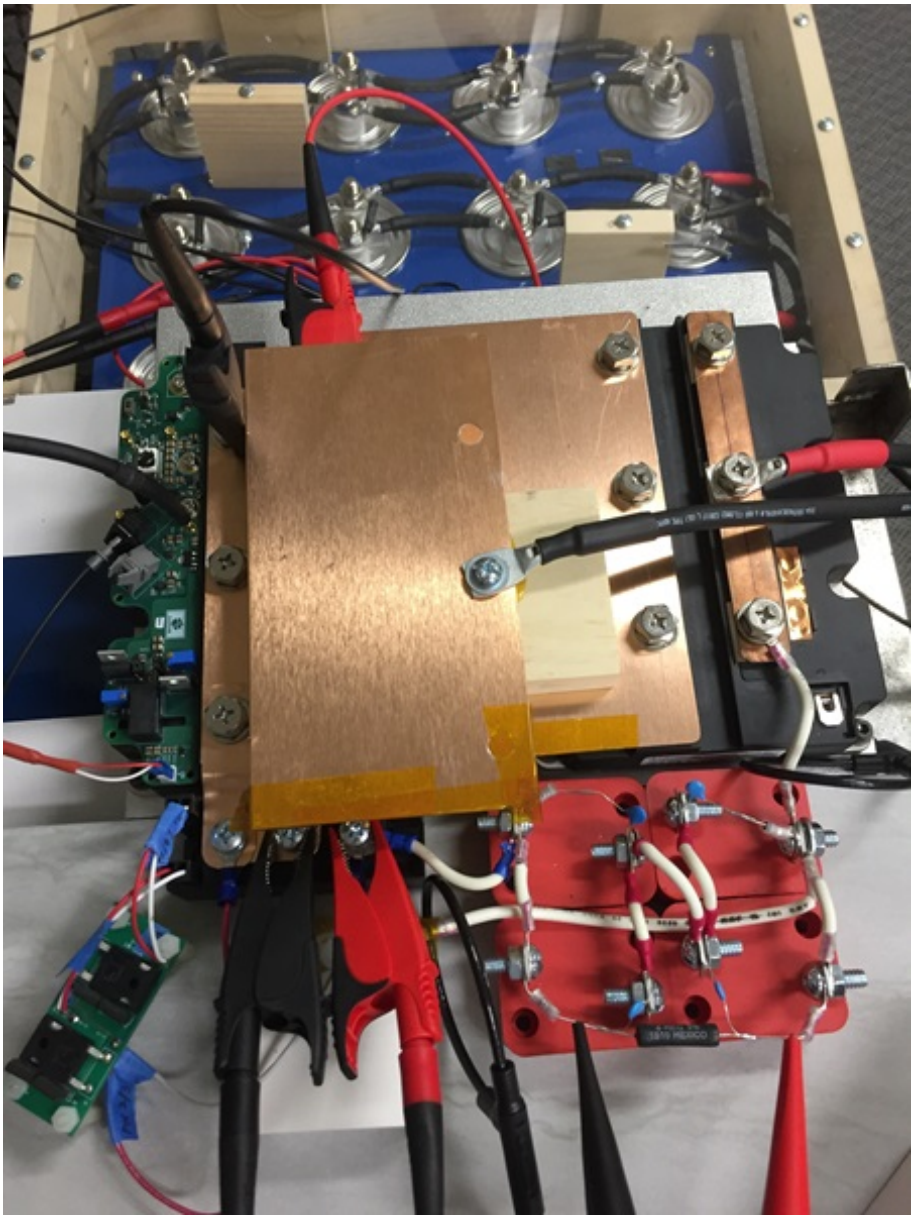

Figure 3.31. Four MOVs in 2P2S Configuration

This 2P2S configuration does introduce more inductance through the electronic MOV branch as there are more wire connections between the MOVs. This will slightly increase the peak voltage during transient operation but will be sufficiently low as to not affect total system design. The gain by optimizing the MOV configuration outweighs the penalty of

increased wiring inductance. In addition, a dedicated printed circuit board can be designed to facilitate the electrical connections and minimize the electronic MOV branch inductance.

Finally, a 3300 pF capacitor was selected to connect in parallel with each MOV to achieve an improved electronic MOV response during the turn-off of the IGBT. The capacitor was added to enhance the parasitic capacitance of MOV, allowing faster voltage buildup across the BOD during IGBT turn-off. As a result, the BOD control circuitry fires earlier in the transient, commutating current through the MOV sooner than previous tests. In addition to the MOV configuration changes, the turn-off resistor, R_{off}, was increased from 10 Ω to 22 Ω to further contain the peak IGBT voltage during turn-off. These modification were performed through an iterative process. Test results with the final configuration are shown in Table 3.21.

Table 3.21. 2P2S MOV configuration, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=22 Ω, L_{sys}=25 μH, C_{MOV}=3300 pF

DC Bus Voltage (V)	t_{on} (μs)	I_{sys} peak (A)	I_{IGBT} peak (A)	BOD Trigger Voltage (V)	SSCB V_{peak} (V)
1600	25	2729	2549	1181	2918
1800	25	3072	2868	1169	2960
2000	20	3063	2788	1203	2971
2000	25	3395	3144	1203	2996

Direct comparisons cannot be made to the similar test conducted at room temperature for the thermal performance baseline measurements due to the different gate pulse duration. However, iterations of the MOV improvements included a configuration of two series connected “BA” body style MOVs, termed as 1P2S, with test results for the same gate pulse duration. Shown below in Figure 3.32 and Figure 3.33 are the direct comparison waveforms for gate pulse of 20 μs and 25 μs, respectively.

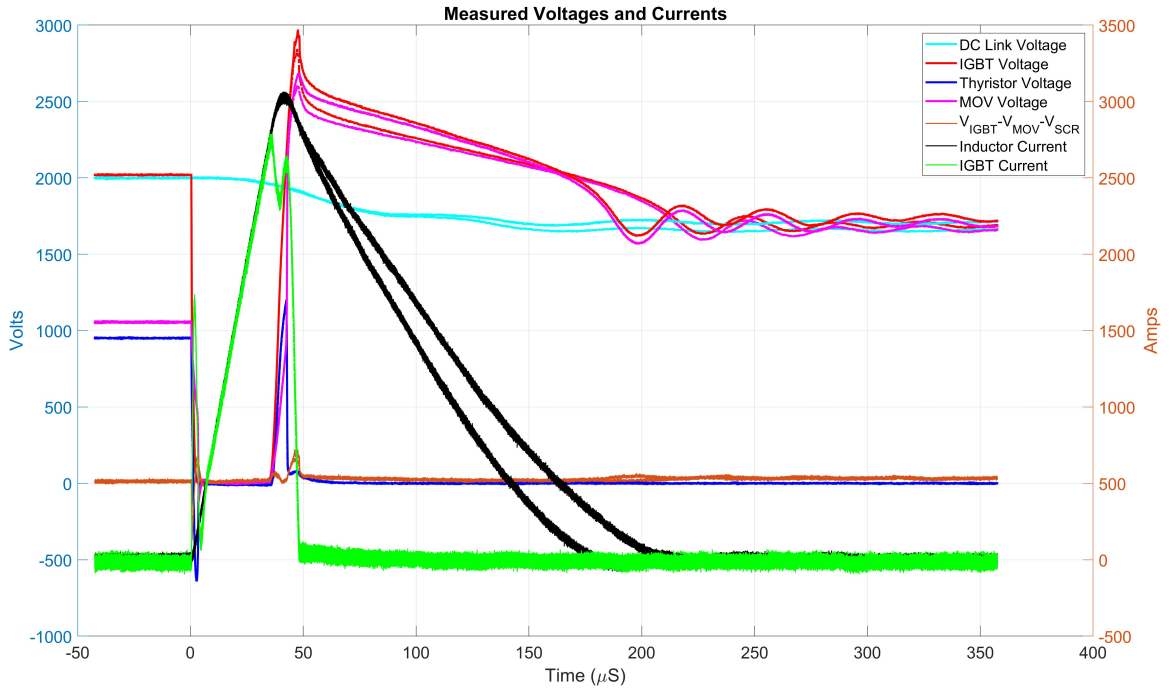

Figure 3.32. 2P2S Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH, C_{MOV}=3300 pF, t_{on}=20 μs

Figure 3.32 shows the comparison between the 1P2S configuration with 'BA" body style MOVs and the 2P2S configuration with 'DB" body style MOVs. The solid red line indicates the 2P2S configuration and reaches a peak voltage of approximately 100 V higher than the 1P2S configuration. Accordingly, faster energy dissipation can be observed. Other SSCB components experienced nearly identical peak current and voltage values, as well as turn-off performance of the IGBT.

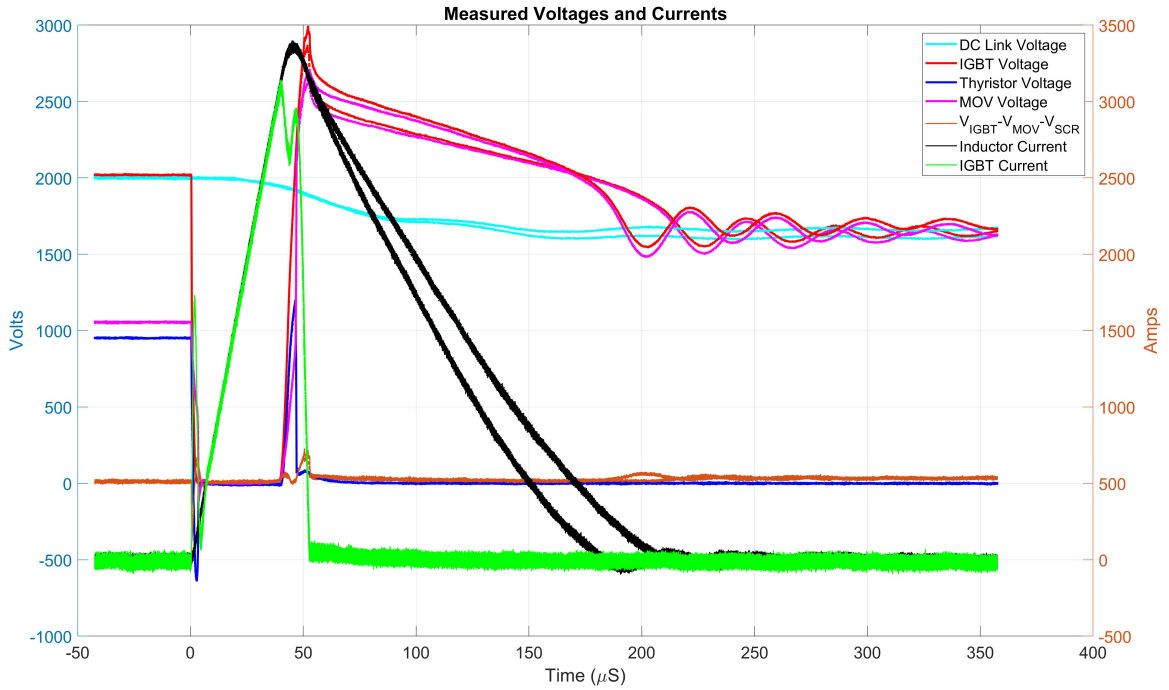

Figure 3.33. 2P2S Response, V_{sys}=2000 V, V_{GE}=12 V, R_{on}=0.3 Ω, $C_{blanking}$=13400 pF, R_{STO}=22 Ω, R_{off}=10 Ω, L_{sys}=25 μH, C_{MOV}=3300 pF, t_{on}=25 μs

Figure 3.33 shows the comparison between the 1P2S configuration and the 2P2S configuration with a longer gating pulse and higher current to interrupt. Similar to the 20μs case, the solid red line indicates the 2P2S configuration of MOVs and reaches a peak voltage of approximately 100 V higher than the 1P2S configuration, and faster energy dissipation is observed. Other SSCB components experienced nearly identical peak current and voltage values, as well as turn-off performance of the IGBT.

By careful selection of the MOV body style and compensating for differences in clamping voltage, pulse current and energy, and leakage current ratings, the MOV circuitry was able to be optimized for improved system performance and increased margins to design limits.

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CHAPTER 4:
Thermal Performance Test

4.1 Test Setup

In addition to satisfactory switching performance, the SSCB should have acceptable thermal behavior during the load current carrying steady state. The thermal dissipation inside the SSCB occurs mostly in the IGBT modules. The dissipation results in IGBT temperature rise and impacts the SSCB efficiency. A thermal performance evaluation therefore is critical to verifying the heat sink and cooling loop design and determining the operating efficiency of SSCB. A single IGBT module is placed under test and the cold plate and coolant loop interface closely mimics that of the complete SSCB. Both the IGBT conduction mode and freewheeling diode conduction mode require evaluation, since in a complete SSCB and system design the load current flows through two IGBTs and two freewheeling diodes. Other than the comparatively insignificant loss incurred in the power bus bars and cable terminations, the thermal losses come entirely from conduction losses within the IGBT or diode chips. A constant, nominal cooling flow was provided by a chiller to remove heat generated to ensure the cooling system and IGBTs would maintain nominal temperature parameters during periods of maximum loading. The instrumentation necessary to monitor system variables, the low-voltage high-current power supply, and the bench top control power supply were also included and can be seen in Figure 4.1. Each component of the setup was selected to meet or exceed required values of NASA FLASH SSCB design.

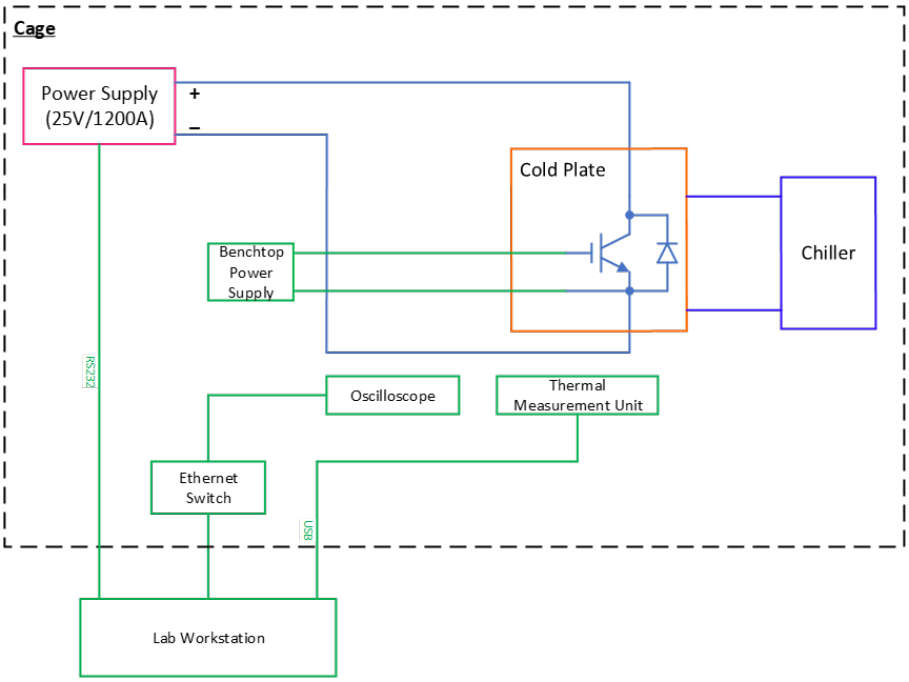

Figure 4.1. Nominal Thermal Test Configuration Including Hardware, Instrumentation, and Controls

The test was designed to measure and record the device voltage drop and chip temperature over the complete load current range. These data would be used to calculate the thermal resistance, the conduction loss, and the SSCB efficiency.

4.1.1 Hardware Selection

The only necessary SSCB component to conduct the thermal test was the IGBT module under test. In order to monitor the internal chip temperatures, a hole was drilled at one of the bus bar connection plates as shown in Figure 4.2.

Figure 4.2. IGBT Module with Modified Bus Bar Connection Plate

With the bus bar connection plate removed, the IGBT and diode chips can be seen. These chips, shown below in Figure 4.3 and Figure 4.4, are the points where the temperatures would be measured.

Figure 4.3. IGBT Module with Bus Bars Connection Plate Removed, Chips Exposed

Figure 4.4. IGBT Module Chip Closeup

The flat wide copper bus bars shown in Figure 4.5 were used in the thermal test for power cable termination at the IGBT module collector and emitter terminals. The bar connected to the IGBT collector terminal had a small hole drilled to allow a fiber optic temperature probe to be inserted through the bus bar, the modified connection plate, and into the silicon gel layer covering the IGBT and diode chips to touch the surface of the Si die. In the completed assembled arrangement shown in Figure 4.5, the fine yellow fiber optic cable can be seen passing through the copper bus bar through a small hole.

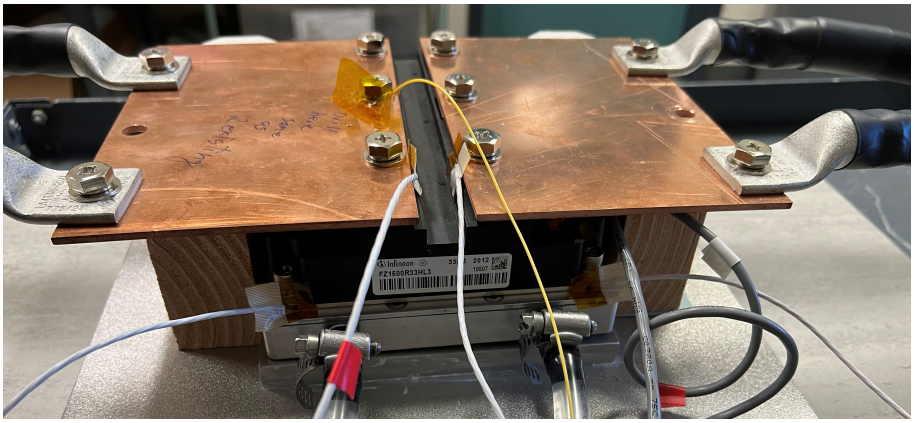

Figure 4.5. Chip Temperature Measurement with Fiber Optic Temperature Probe

Figure 4.6 shows the modification necessary to the collector bus bar. The small hole drilled in the bus bar allows insertion of a temperature probe into the IGBT module to monitor the IGBT and diode chip temperatures and was positioned with the bus bar template overlaid on top of the IGBT module mechanical model in computer software.

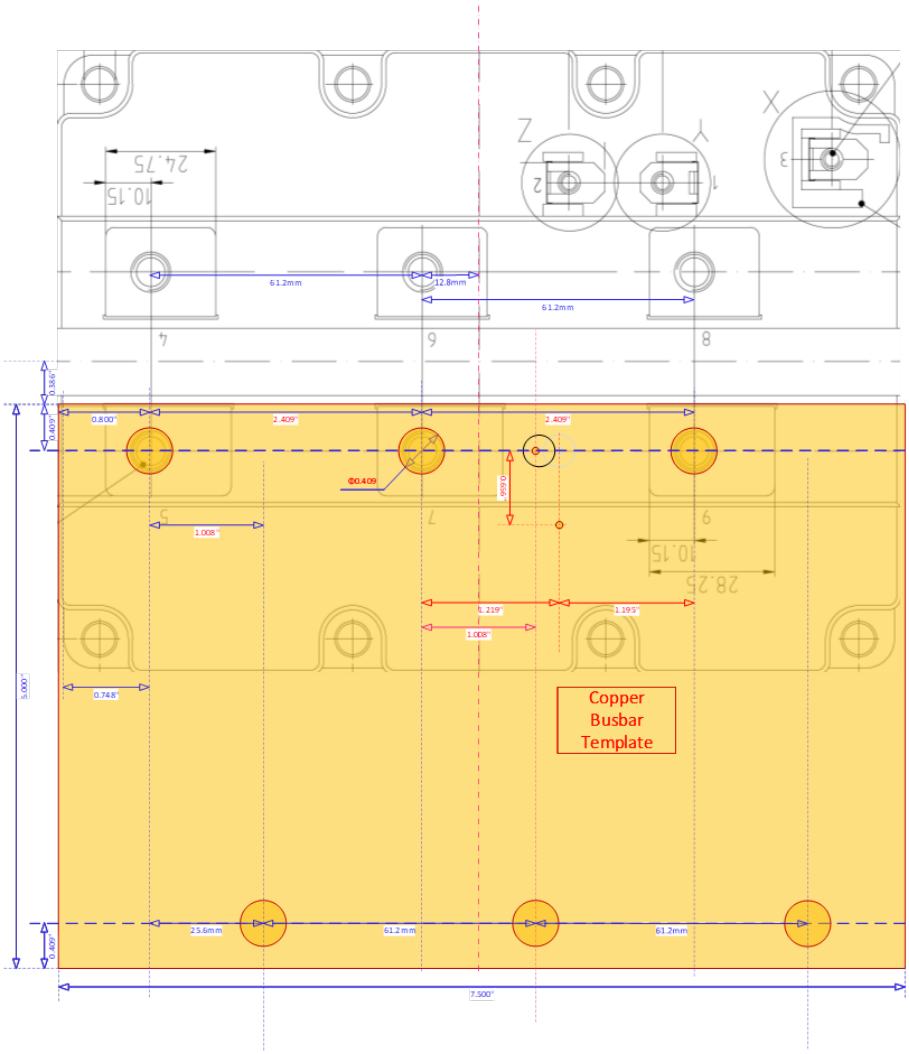

Figure 4.6. IGBT Collector Bus Bar Hole Placement

Once the bus bar was designed for placement on the module, the template image was superimposed over the chip placements, shown in Figure 4.7, from an Infineon 2000 A module, which previous tests were conducted on prior to thermal test of the 1500 A module. However, the IGBT and diode chip placement is similar, with the 1500 A IGBT module having four diode chips per section, instead of the three diode chips per section shown in the 2000 A module.

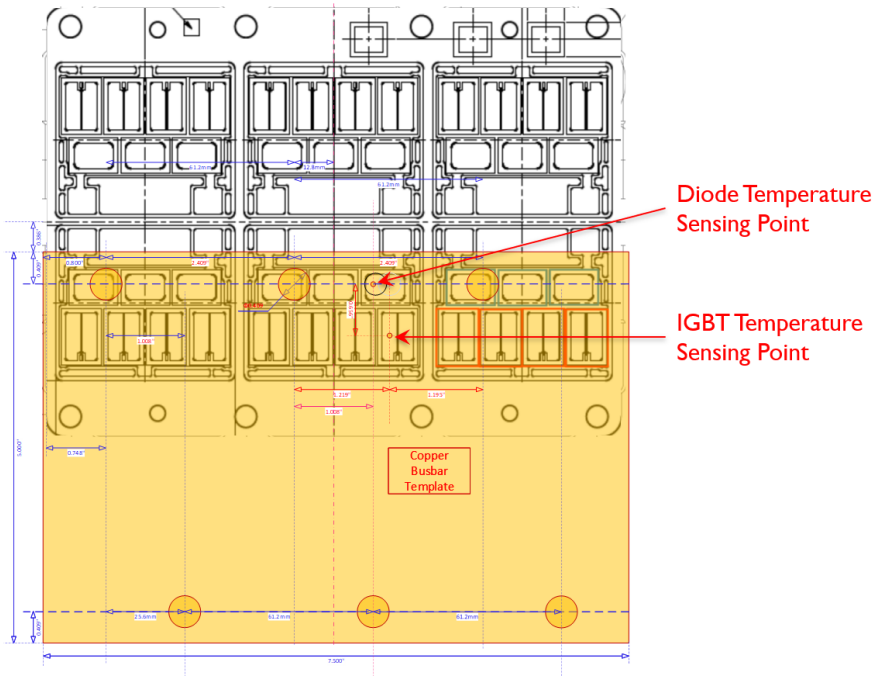

Figure 4.7. IGBT Modified Collector Bus Bar and IGBT Chip Placement

To carry the current necessary for the test, two 313 kCMIL DLO cables rated for 2 kV were used to carry 600 A each, totaling the 1200 A necessary for the full-load thermal test. The current source selected for the thermal test was a 25 V, 1200 A Magna-Power DC Power Supply. This model allowed for remote control and monitoring from the lab station as well as programmable protections that were adjustable during operations [38]. To provide the heat transfer capabilities, an ATS cold plate was selected that allowed for modification to support the IGBT module foot print [39]. The advantage of using this particular model is that the holes to attach the IGBT to the cold plate can be drilled and tapped to any design specification. The chiller selected for the thermal test was the SMC HRS060 Thermo Chiller [40]. This model was selected due to the operational temperature range and cooling flow capabilities which met or exceeded the FLASH specifications. Specifically, the chiller can maintain 3 Gallons per Minute (GPM) flow rate with a cooler outlet temperature of 15 °C. The simulated heat load from the IGBT module also falls well within the cooling capabilities of the chiller. To achieve and maintain a 3 GPM flow rate, a bypass line was installed between the chiller inlet and outlet in parallel with the cooling loop. The valve

within the bypass line was normally open, and throttled shut to achieve the desired flow rate. Within the cooling loop, a flow meter was installed that coupled to an oscilloscope [41]. The flow meter pulses were converted to a flow rate according to the individual model rating and manufacturer calibration. To maximize conduction between the IGBT base plate and the cold plate, T-Global TG-N909 thermal grease was selected for the superior thermal conductivity of 9 kW/m-K [42]. Finally, although not included in the test, a stencil was fabricated to ensure a uniform application of the thermal grease to the IGBT base plate and shown in Figure 4.8 and Figure 4.9.

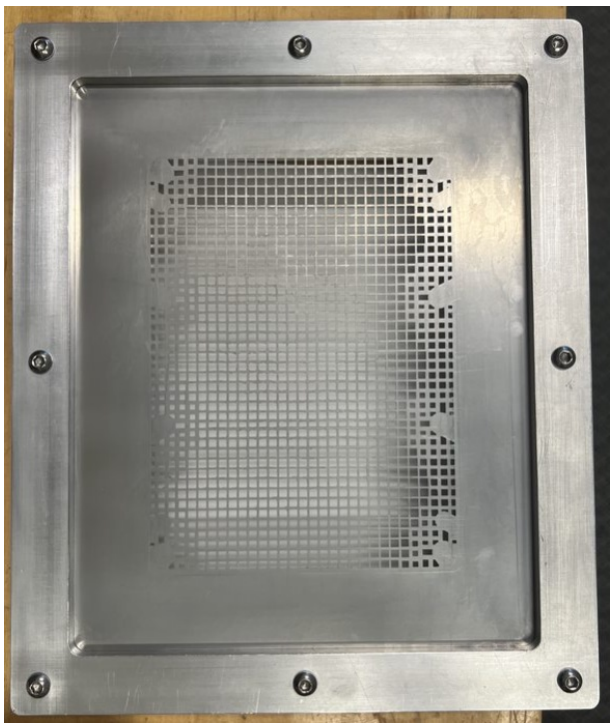

Figure 4.8. Thermal Grease Stencil - Back View for Grease Application

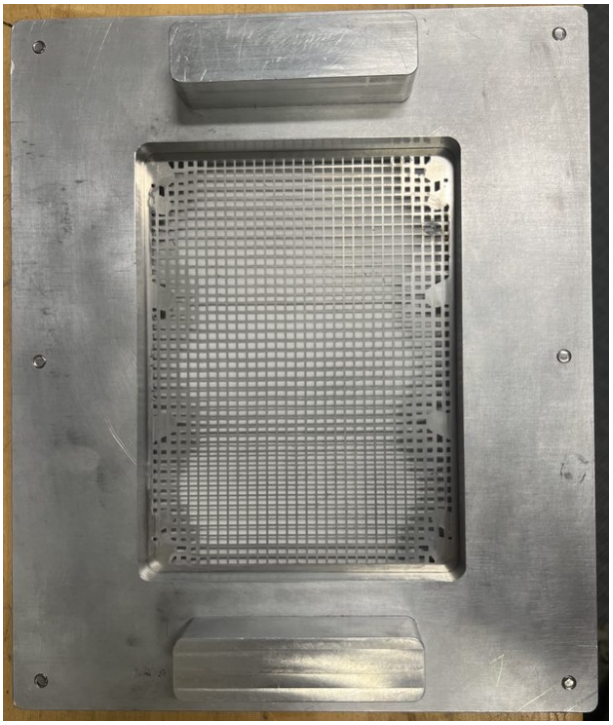

Figure 4.9. Thermal Grease Stencil - Front View for Aligning IGBT Module

The stencil included a cut out on the front side for placing and holding the IGBT module along with protrusions to hold the screen against a flat surface. On the reverse side, the stencil had a raised edge to assist in guiding the tools used to apply thermal grease evenly to the surface of the IGBT module.

4.1.2 Instrumentation Selection

Within the flow path, pressure gauges were installed to monitor inlet and outlet pressure to the cold plate. However, these sensors did not have remote capabilities and were only used during initial flow testing to verify the pressure drop across the cold plate. Additionally, these gauges were used when initiating system flow to monitor for system anomalies. To monitor the chip temperatures within the IGBT, a fiber optic temperature sensor was necessary. This allowed for a non-conductive measurement as close to the semiconductor junctions as possible. The Neoptix Fiber Optic Temperature Probe was used along with the Neoptix T-Guard Link Signal Conditioning Module [43]. This system was selected

for remote monitoring at the lab station via a serial link from the module. Additionally, the fiber optic temperature probe operates free from RF interference, has a high operating temperature range, and high accuracy. Additional temperature measurements were taken to monitor for heat generated by conduction. Resistance Temperature Detectors (RTDs) [44] were placed on the IGBT emitter and collector bus terminals, and another pair was placed on the IGBT base plate to monitor the base plate temperatures close to the inlet and outlet of the cold plate, respectively. To monitor the current supplied to the IGBT, a DC current meter was necessary. The Hioki CT6877 AC/DC current sensor was selected for this purpose [45]. This probe had a sufficient opening to allow passage of two current carrying cables from the power supply to the IGBT. This allowed for monitoring total system current with one pass-through probe instead of monitoring both lines simultaneously and summing the currents. At the time of testing for the thesis, the remote temperature monitoring devices for coolant inlet and outlet temperature were not received and therefore there is no outlet coolant temperature provided. The inlet temperature was controlled by the chiller and was kept at 15 °C for the duration of the thermal tests and was readable from the front of the operational chiller. Figure 4.10 shows the layout of the test instrumentation for the thermal performance test.

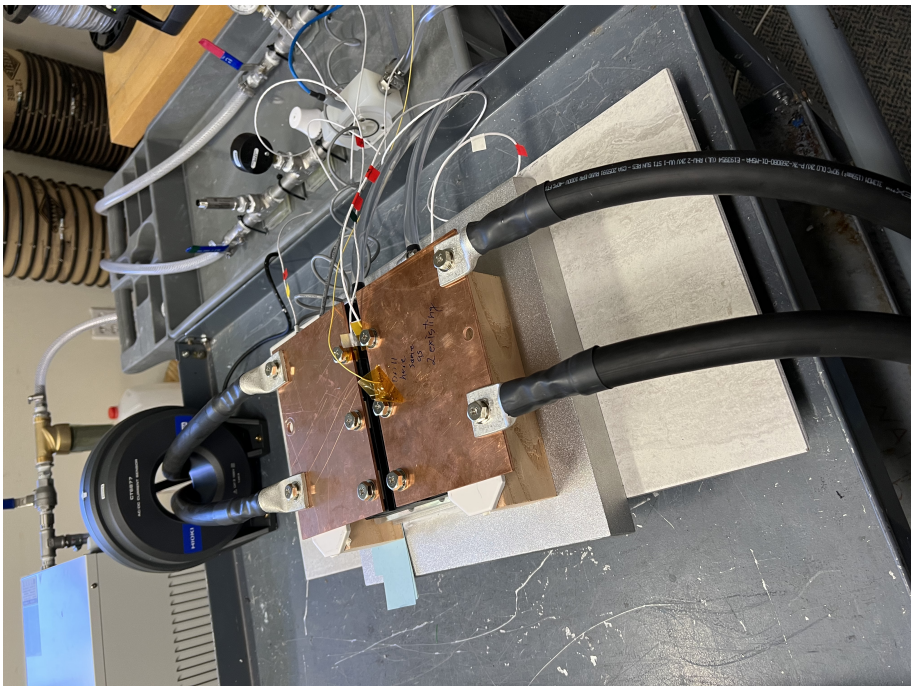

Figure 4.10. Instrumentation Configuration for Thermal Performance Test

4.1.3 Thermal Test Layout

Figure 4.11 shows the assembled layout for the proposed thermal test setup. Similar to the switching performance test, this test is conducted inside an interlocked safety cage due to high currents. A single IGBT module is used in this test setup, while both the IGBT conduction mode and freewheeling diode conduction mode are evaluated. Since the high current power supply is unipolar, power cabling needs to be swapped when the current flow direction through the IGBT module changes. A benchtop DC power supply was connected to the gate to supply a 12 V gate to turn on the IGBT for forward current conduction and a -8 V gate force the IGBT off for reverse current conduction through the freewheeling diode. The current through the IGBT module was incremented from a low value towards the full load current of 1200A. The temperature readings were allowed to reach steady state at each current value before being incremented to the next test point. The data acquisition units record the data of interest in this process, including the device voltage drop and temperatures at points detailed in Subsection 4.1.2.

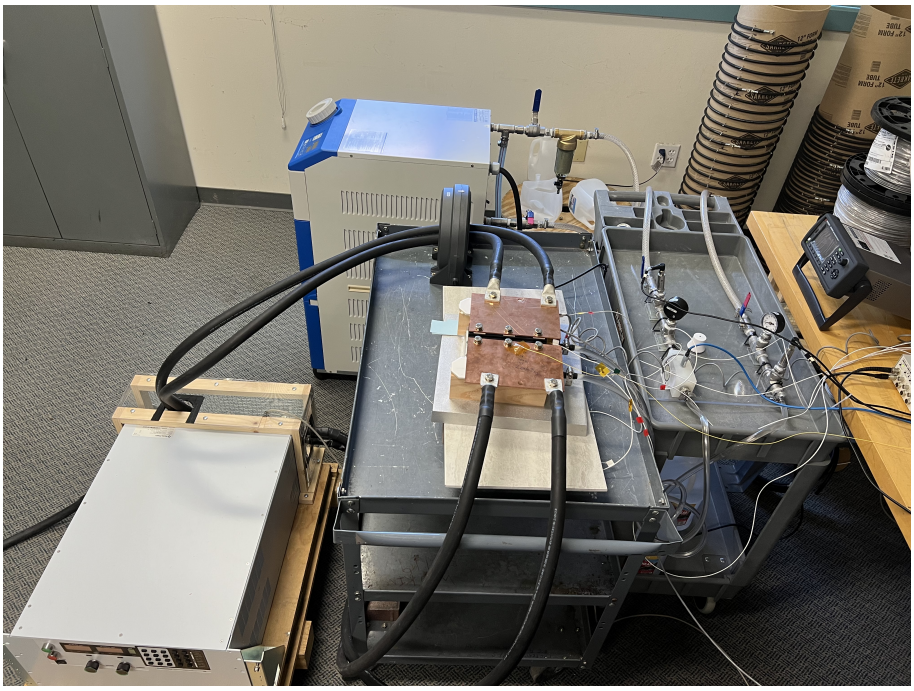

Figure 4.11. Hardware Assembled Testing Setup for Thermal Performance Test

4.2 IGBT Thermal Test

4.2.1 15 V V_{GE} Benchmark Test

A benchmark thermal performance test was performed on the 1500 A IGBT module with current flowing through the IGBT chips with an applied V_{GE} of 15 V and results shown in Table 4.1. Current was incremented from 100 A to 1200 A, the rated current of the SSCB. The fiber optic temperature probe measured the IGBT chip temperature near the middle of the IGBT module, and RTDs were placed to measure the base plate temperatures near the cooling inlet and outlet. A voltmeter integral to the Keysight data acquisition unit was used to measure V_{CE} during the test. The voltmeter was connected to the IGBT modules Kelvin terminals, measuring voltage from the emitter to collector. Therefore a negative voltage reading indicates that the IGBT is in the on-state and forward conducting, as shown in Figure 4.12. In Table 4.1, however, the voltage reading is negated to avoid

confusion. Coolant inlet temperature was 15 °C throughout the duration of the test. Due to the inability to see where the temperature probe was actually located within the IGBT module, the measured chip temperature is not necessarily that of the hot spot on the hottest chip. Therefore the temperature profile of the IGBT chip needed sufficient margin from the maximum allowed temperature to ensure satisfactory performance of the chip and the cooling system.

Table 4.1. IGBT Thermal Test, V_{GE}=15 V, I_C=100-1200 A

V_{CE} Voltage (V)	I_C (A)	IGBT Temperature (°C)	Baseplate Inlet Temperature (°C)	Baseplate Outlet Temperature (°C)
1.18	100	16.1	17.8	17.8
1.36	200	18.4	18.6	18.7
1.49	300	21.0	19.5	20.1
1.61	400	24.2	20.5	21.6
1.71	500	27.5	21.8	23.0
1.81	600	31.1	23.0	24.7
1.92	700	35.1	24.4	26.5
2.02	800	39.7	26.0	28.5
2.12	900	44.5	27.7	30.7
2.22	1000	50.0	29.5	33.1
2.33	1100	55.7	31.4	35.4
2.45	1200	62.0	33.9	38.4

The final emitter bus terminal temperature at the conclusion of the test was 50.8 °C. Although this temperature was not used in any further calculation, it was monitored for an understanding of the thermal behavior of the IGBT module power terminal. Additionally, the base plate RTD temperatures measured are used to calculate the thermal resistance from the IGBT chip to the base plate. These measurements also show the temperature gradient across the IGBT module base plate. The data set for the benchmark thermal performance test was plotted and is shown in Figure 4.12.

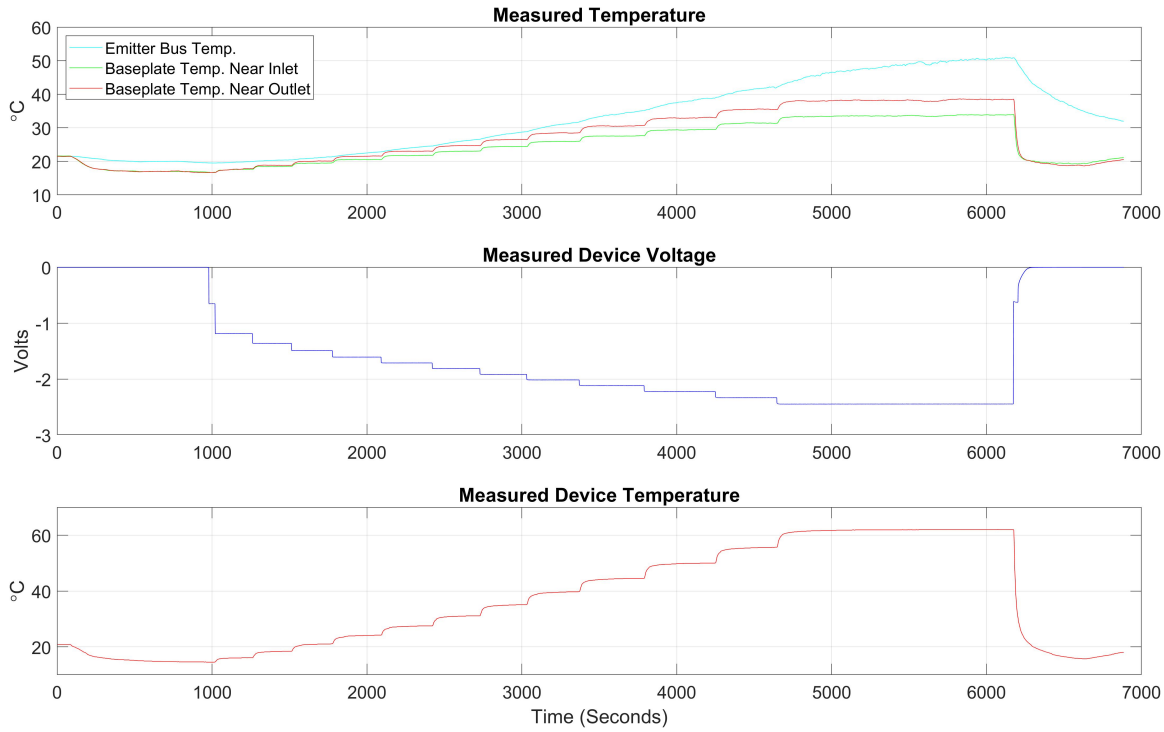

Figure 4.12. V_{GE}=15 V IGBT Thermal Performance Test Recorded Data

This plot shows how the base plate temperature gradient was developed as higher current was driven through the IGBT chips. The conduction loss in the IGBT and cooling provided through the flow path in the cold plate caused a 4.5 °C gradient from the inlet to the outlet side of the IGBT base plate at 1200 A. The emitter bus terminal temperature profile was more pronounced as it is not actively cooled by the cold plate and its cooling depends on thermal conduction through the copper bus bar and power cable as well as convection and radiation to the ambient air. The final IGBT chip temperature was well below the threshold temperature of 100 °C, with sufficient margin to account for slight inaccuracies in measuring due to temperature probe placement uncertainties.

Calculating the conduction loss of the IGBT at 15 V V_{GE}, at full power, the current through the IGBT is 1200 A and the voltage drop across the IGBT, V_{CE}, is 2.45 V. This equates to a power loss of 2940 W. This baseline is compared against the selected 12 V_{GE} for an operational IGBT in the SSCB. The thermal resistance of the IGBT is derived from the measured data, and shown in Figure 4.13.

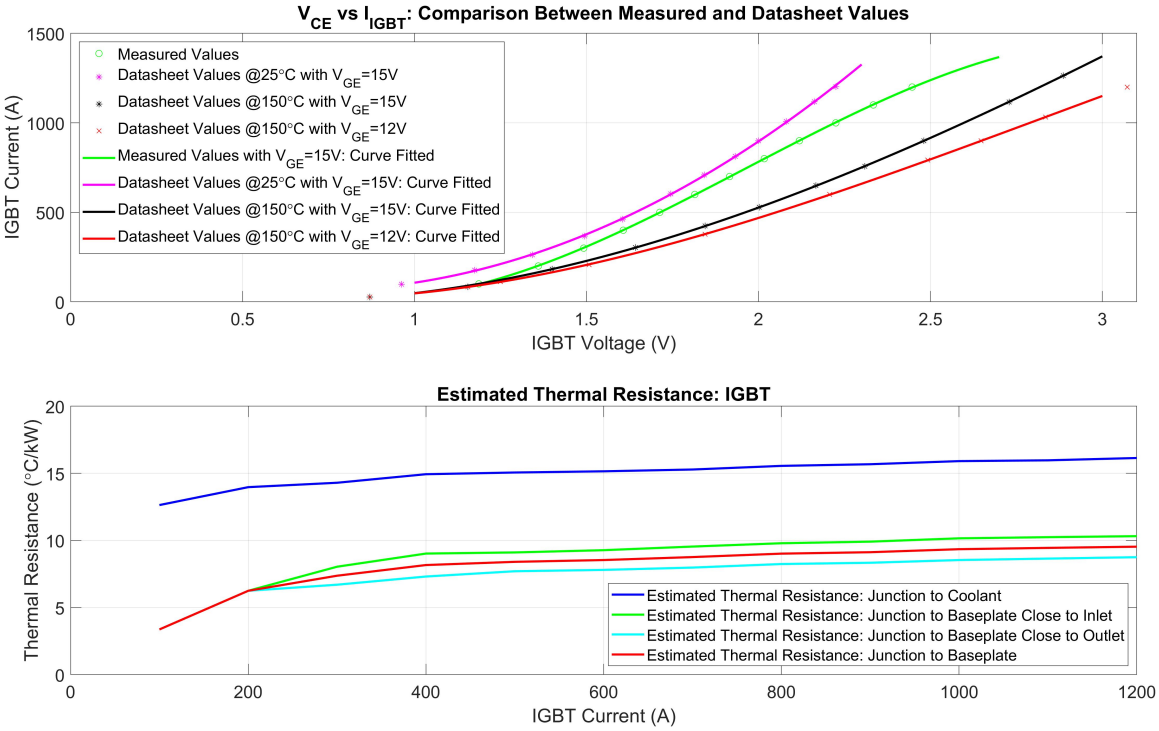

Figure 4.13. V_{GE}=15 V IGBT Thermal Performance Test Postprocessed Data

The mathematical models developed from manufacturer data and measured data are shown in Figure 4.13. The green line in the top graph represents the measured values of I_C vs. V_{CE}. A best fit curve is generated from the data set. This is plotted against the manufacturer provided data for different operating gate voltages and operating temperatures. This data is also compared against Figure 2.5, where this IGBT demonstrates positive temperature over the entire current range. As the IGBT junction temperature increases, its voltage drop becomes higher for the same amount of collector current. As apparent from the measured data, as the IGBT junction temperature increased during the test, the data points are seen to begin moving away from the manufacturer data set in magenta at 25 °C and toward the manufacturer data set in black at 125 °C. After I_C of 600 A, the data sets begin to diverge from the 25 °C set at an increasing rate, showing the effect of positive temperature coefficient of the IGBT.

From the manufacturer data sheet, the thermal resistance from the IGBT chip junction to the

base plate is 7.35 K/kW. The average estimated from the IGBT chip to the base plate was approximately 9.5 K/kW. This calculated value has some error introduced from uncertainty on the fiber temperature probe placement on the IGBT chip. But more importantly, this is due to the fact that the RTDs measuring base plate temperatures cannot be positioned directly underneath the IGBT chip, and the resulting readings are lower than what should be used in the calculation of thermal resistance, resulting in higher calculated value. The estimated junction-to-coolant thermal resistance is approximately 16 K/kW and is derived using the coolant inlet temperature of 15 °C and would be higher than actual, since the coolant temperature is expected to rise from the inlet to outlet, especially in high dissipation conditions. Any offset in the temperature probe or RTDs can also introduce inaccuracy in calculated thermal resistance, especially in low dissipation conditions.

4.2.2 12 V V_{GE} Operational Test

This test was conducted to measure the SSCB performance at the proposed operating gate voltage of 12 V and results are shown in Table 4.2. This test provides the most relevant thermal performance data with the IGBT module driven as it would inside the SSCB. Otherwise the test setup and instrumentation arrangement are identical to that in the 15 V V_{GE} benchmark test described in Subsection 4.2.1.

Table 4.2. IGBT Thermal Test, V_{GE}=12 V, I_C=100-1200 A

V_{CE} Voltage (V)	I_C (A)	IGBT Temperature (°C)	Baseplate Inlet Temperature (°C)	Baseplate Outlet Temperature (°C)
1.20	100	16.1	17.0	17.0
1.38	200	18.6	17.8	18.2
1.53	300	21.4	19.0	19.7
1.65	400	24.8	20.5	21.4
1.77	500	28.3	21.9	23.1
1.89	600	32.3	23.6	25.2
2.01	700	37.0	25.5	27.3
2.13	800	41.8	27.5	29.7
2.25	900	47.4	29.5	32.2
2.38	1000	53.3	31.5	34.7
2.52	1100	60.0	33.8	37.6
2.66	1200	67.2	36.5	40.7

The final bus bar temperature at the conclusion of the test was 53.0 °C, higher than that in the 15 V V_{GE} benchmark test. The other RTD measured temperatures and the IGBT chip temperature were also higher due to higher IGBT voltage drop and conduction loss at reduced V_{GE}. The temperature profile results are shown in Figure 4.14.

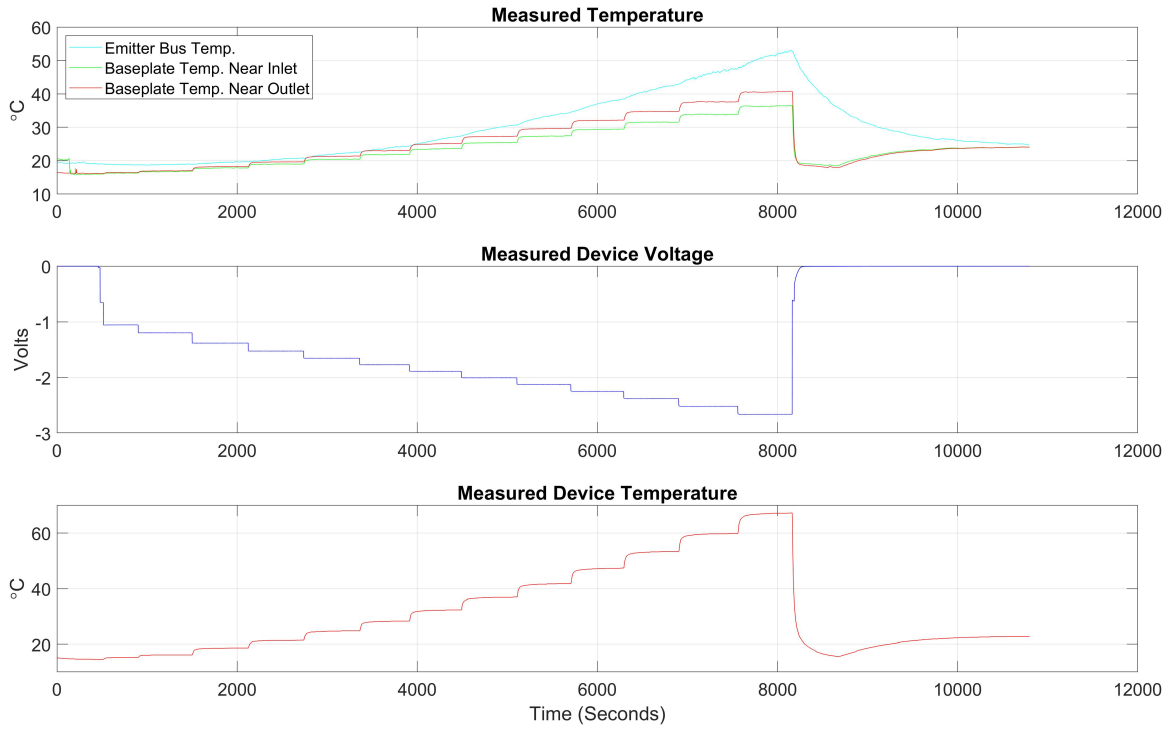

Figure 4.14. V_{GE}=12 V Thermal Performance Test Recorded Data

Calculating the conduction loss of the IGBT at 12 V V_{GE}, at full power, the current through the IGBT is 1200 A and the voltage drop across the IGBT, V_{CE}, is 2.66 V. This equates to a power loss of 3192 W. This is an increase of less than 8% from the 15 V V_{GE} conducted above. For the 2.4 MW SSCB, this increase in power loss is only 0.01%. This additional loss is negligible against the desired efficiency of 99.5% for the SSCB. The thermal resistance of the IGBT is derived from the measured data, and shown in Figure 4.15.

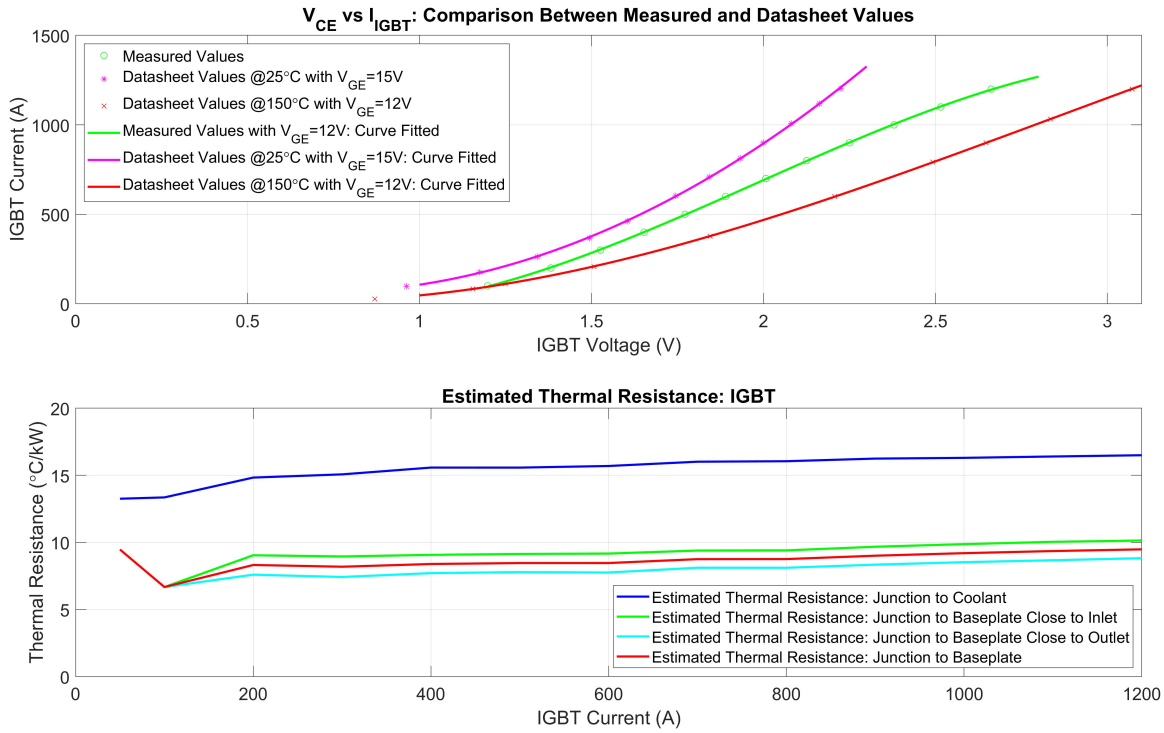

Figure 4.15. V_{GE}=12 V Thermal Performance Test Postprocessed Data

The mathematical models developed from manufacturer data and measured data are shown in Figure 4.15. The green line in the top graph represents the measured values of I_C vs. V_{CE}. A best fit curve is generated from the data set. This is plotted against the manufacturer provided data for different operating gate voltages and operating temperatures. Since the manufacturer datasheet does not provide the IGBT output characteristic at 25 °C for V_{GE} of 12 V, the 25 °C characteristic for 15 V V_{GE} is used in Figure 4.15. As the IGBT junction temperature increased during the test, the data points are seen to begin moving away from the manufacturer data set in magenta at 25 °C for V_{GE} of 15 V and toward the manufacturer data set in red at 125 °C for V_{GE} of 12 V. After I_C of 400 A, the data sets begin to diverge from the 25 °C set at an increasing rate, showing the effect of positive temperature coefficient of the IGBT.

The estimated thermal resistance from the IGBT chip to the base plate was approximately 9.5 K/kW, while the estimated junction-to-coolant thermal resistance is approximately 16 K/kW. These results match very well with those calculated from the 15 V V_{GE} benchmark test data.

This data consistency is expected and is an indication of proper test setup, instrumentation, and data acquisition and processing.

4.3 Diode Thermal Test

A single thermal test was conducted on the 1500 A IGBT module to evaluate its performance with the load current flowing through the diode chips. The applied V_{GE} is -8 V to have the IGBT negatively biased. The power cabling between the low-voltage high-current power supply and the IGBT module is reversed for the intended current flow. Current was incremented from 100 A to 1200 A, the rated current capacity during normal operations for the system. The fiber optic temperature probe measured the diode junction temperatures near the middle of the IGBT module, and RTDs were placed to measure the base plate temperature near the cooling inlet and outlet. A voltmeter was used to measure V_{diode} during the test. The voltmeter was connected emitter to collector and indicates a positive voltage when the diode is forward biased and conducting. Coolant inlet temperature was 15 °C throughout the duration of the test. Due to the inability to see where the temperature probe was actually located within the IGBT module, the temperature profile of the diode chip needed sufficient margin from a threshold temperature to ensure satisfactory performance of the chip and the cooling system. The test results shown in Table 4.3.

Table 4.3. Diode Thermal Test, V_{GE}=-8 V, I_F=100-1200 A

V_{diode} Voltage (V)	I_C (A)	Diode Temperature (°C)	Baseplate Inlet Temperature (°C)	Baseplate Outlet Temperature (°C)
1.18	100	17.0	17.3	17.3
1.34	200	19.9	17.6	17.6
1.47	300	23.4	18.3	18.3
1.58	400	27.4	19.0	19.0
1.67	500	31.4	19.3	20.0
1.76	600	36.0	19.9	20.9
1.84	700	40.7	20.6	21.9
1.92	800	45.9	21.4	23.0
1.99	900	51.4	21.9	24.0
2.06	1000	57.2	22.6	25.0
2.13	1100	63.5	24.0	26.6
2.19	1200	70.1	25.0	28.0

The final bus bar temperature at the conclusion of the test was 49.0 °C, lower than that observed during the IGBT thermal test. This may be due to the lower forward drop of the freewheeling diode compared with the IGBT saturation voltage while conducting the same amount of current. Additionally, the RTD was not tightly adhered to the emitter bus terminal, resulting in lower readings than expected and can be seen through the noisy measurements in Figure 4.16. The other RTD measured temperatures and the diode chip temperature were recorded and processed to derive the thermal resistance values. The temperature profile results are shown in Figure 4.16.

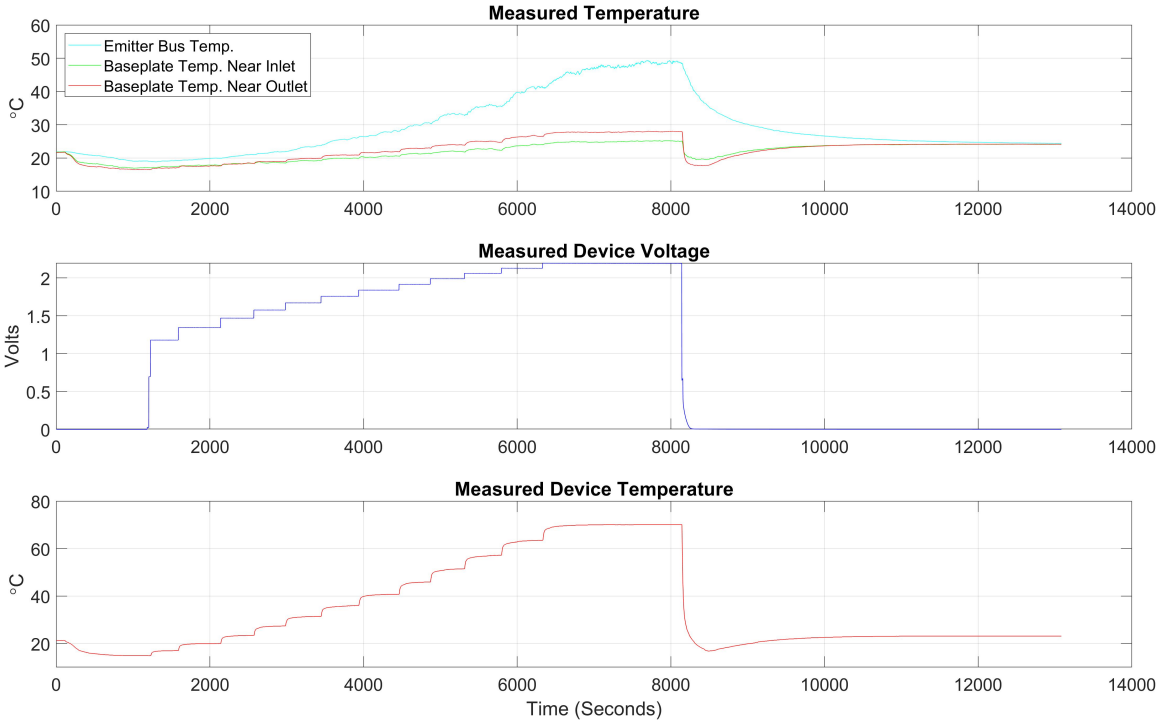

Figure 4.16. V_{GE}=-8 V Diode Thermal Performance Test Recorded Data

Calculating the conduction loss of the diode at full power, the current through the diode is 1200 A and the voltage drop across the diode was 2.19 V. This equates to a power loss of 2628 W. The thermal resistance of the diode is derived from the measured data, and shown in Figure 4.17.

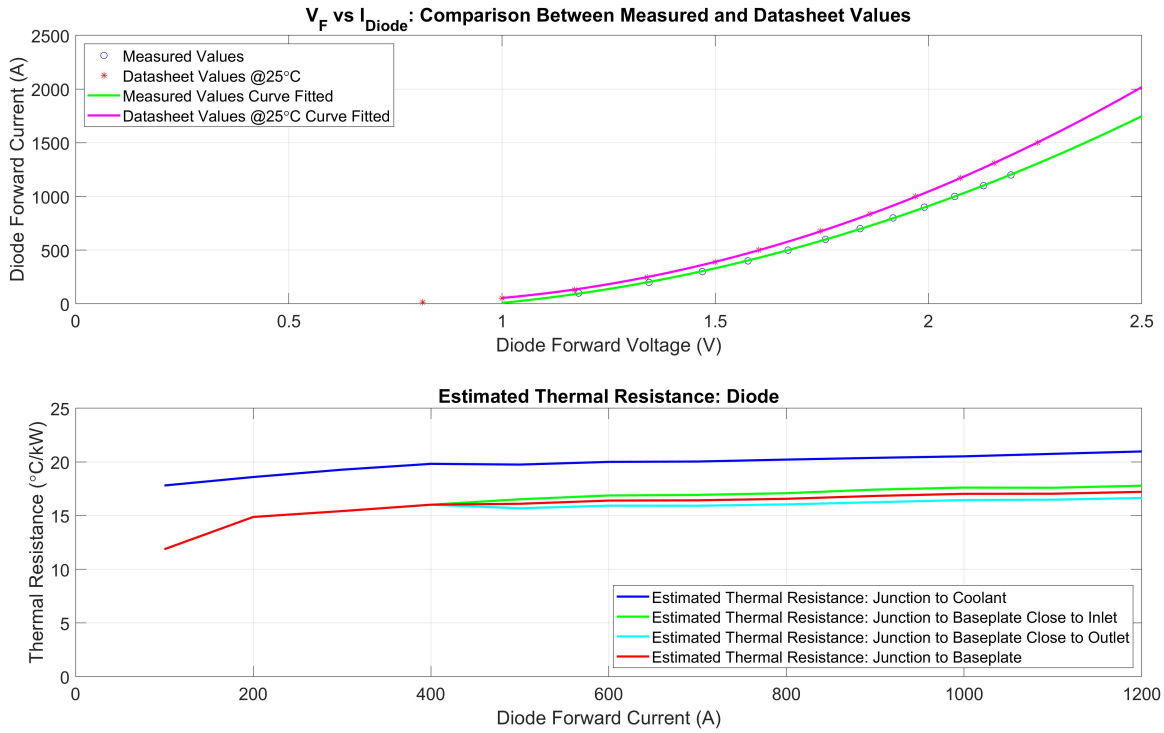

Figure 4.17. V_{GE}=-8 V Diode Thermal Performance Test Postprocessed Data

The mathematical models developed from manufacturer data and measured data are shown in Figure 4.17. The green line in the top graph represents the measured values of I_{diode} vs. V_{diode}. A best fit curve is generated from the data set. This is plotted against the manufacturer provided data for the diode forward characteristic. This data is also compared against Figure 2.5. The manufacturer data sheet shows that in the normal steady-state operating range of SSCB, the freewheeling diode has a negative temperature coefficient. As the temperature in the diode increases, a lower voltage drop is expected for conducting the same amount of current. However, as the diode junction temperature increased during the test, the data points were seen to begin moving away from the manufacturer data set in magenta at 25 °C. This line is expected to approach, and eventually cross, the 25 °C reference line from manufacturer data corresponding to the diode I-V curve in Figure 2.5 as the diode junction temperature rose throughout the test. This is likely due to the fact the diode forward drop characteristic has a wide range, as indicated by the significant difference between the typical and maximum values specified in the data sheet. The actual performance might vary

noticeably depending on the production batch.

From the manufacturer data sheet, the thermal resistance from the diode chip to the base plate is 13.0 K/kW. The estimated thermal resistance from the IGBT chip to the base plate was approximately 17 K/kW. This calculated value has some error introduced from uncertainty on the fiber temperature probe placement on the diode chip. In addition, the RTDs measuring base plate temperatures cannot be positioned directly underneath the diode chip, and the resulting readings are lower than what should be used in the calculation of thermal resistance, yielding in higher calculated value. The estimated diode junction-to-coolant thermal resistance is approximately 21 K/kW and is derived using the coolant inlet temperature of 15 °C and would be higher than actual, since the coolant temperature is expected to rise from the inlet to outlet, especially in high dissipation conditions. Any offset in the temperature probe or RTDs can also introduce inaccuracy in calculated thermal resistance, especially in low dissipation conditions.

The total voltage drop across one SSCB with the load current flowing through one forward biased diode and one 12 V V_{GE} IGBT was a combined 4.85 V at full operational current and nominal cooling flow. This voltage drop was consistent with manufacturer data and the model estimates. The total power loss through one SSCB at operational voltages and temperatures is 5820 W, for a total power loss of two SSCBs of 0.485% from the rated 2.4 MW system design. This exceeds the 99.5% efficiency requirement as detailed in Chapter 2.

CHAPTER 5:
Conclusions and Future Work

5.1 Conclusions

The rapid development and implementation of components in the MVDC distribution network will be essential for continued application and expansion of this promising distribution system. The SSCB is a key enabling component for ultra-fast, highly reliable circuit protection and current interruption in the MVDC network. This thesis studies the performance of a high-density, high-efficiency inductorless SSCB based on IGBT devices, focusing on its switching characteristics and thermal behavior.

5.1.1 Switching Performance Characterization

The switching characteristics of the SSCB has been thoroughly investigated. A setup was constructed to test one pole of the SSCB, with the layout of components closely mimicking that in a fully packaged SSCB. The 3.3 kV, 1.5 kA Infineon IGBT module was selected as the primary candidate for SSCB implementation after multiple IGBT modules of the same form factor were evaluated. Improvements to the component layout were made based on the findings from the tests. The switching characteristics were evaluated under all the relevant operating conditions to facilitate the tuning of the gate drive component values. The current saturation behavior of the IGBT at reduced gate voltage was thoroughly examined and exploited for fault current containment in an inductorless SSCB. Another focal point is the electronic MOV branch which allows more compact and efficient SSCB design. The functional behavior of the electronic MOV branch was meticulously investigated to guarantee reliable suppression of the peak voltage across the IGBT during current interruption. The following conclusions can be drawn based on the switching characterization test results:

- The electronic MOV branch should be placed as close as possible to the IGBT modules to minimize the loop inductance.
- At a reduced gate voltage of 12 V, IGBT current saturation and active region operation can safely limit the short circuit fault current under an acceptable level, thus

eliminating the need of a current-limiting inductor.

- Wide bus bars must be used for power cable termination at the SSCB to guarantee predictable current profile and even current distribution upon short circuit with very low system inductance.
- The peak IGBT voltage during turn-off can be mitigated by increasing the turn-off resistance, at the cost of slower turn-off process and longer-lasting current. This is an acceptable trade off in the SSCB design, since the switching loss is not a concern.
- In the electronic MOV branch, the parasitic capacitance of the MOV and SCR cannot always guarantee repeatable and desirable transient voltage distribution. An additional ceramic capacitor added in parallel with the MOV can remove this uncertainty and improve the SSCB performance.
- There is a compromise between the MOV clamping voltage and leakage current. Use of multiple MOVs in parallel and/or series connection can help to reach an optimized MOV equivalent. However, limited range of available MOVs from the manufacturer makes the optimization challenging.

In summary, the switching characterization test verifies that the SSCB can meet the design specifications, with the exception of the DC system voltage. At the nominal 2000 V DC system voltage, the MOV leakage current is higher than the SCR holding current, thus preventing the turn-off of the SCR. With the present available MOVs, the system voltage cannot exceed 1700 V to 1800 V.

5.1.2 Thermal Performance Evaluation

The thermal test was carried out with the IGBT module mounted on a cold plate identical in performance to that to be used in the fully packaged SSCB. The test showed satisfactory thermal performance. The measured IGBT module static characteristics match closely those on the data sheet. The conduction loss data confirms that the SSCB can achieve the efficiency specification. The temperature measurement data shows that both the IGBT and freewheeling diode has sufficient thermal margin with the selected cold plate and coolant flow. The various thermal resistance values derived from the measured data reasonably match those in the data sheet.

5.2 Future Work

A MOV or a network of MOVs with desired clamping voltage and leakage current specifications for safe deployment of the SSCB at the nominal DC system voltage of 2000 V still is to be found. Another path worth exploring is the high power Transient Voltage Suppressor (TVS) diode. The TVS diode tends to have insufficient energy capability for the SSCB application. However, high power TVS diodes deserve an in-depth evaluation, considering their advantageous characteristics such as flat clamping voltage over a wide range of current and extremely low leakage current.

The transient voltage distribution between the MOV and SCR in the electronic MOV branch is worth further investigation. A deeper look into the component physics will be helpful to quantify the transient voltage profiles across the MOV and SCR, and to predict potential variation in component characteristics and its impact on the SSCB reliability.

This SSCB is aimed for aviation applications. Therefore, its safe operation at high altitude and low air pressure without partial discharge is a critical requirement. Verification test of the SSCB operation at high altitude needs to be conducted in a vacuum chamber.

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List of References

[1] L. Qi, P. Cairoli, Z. Pan, C. Tschida, Z. Wang, V. Ramanan, L. Raciti, and A. Antoniazzi, "Solid-state circuit breaker protection for DC shipboard power systems: Breaker design, protection scheme, validation testing," *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 952–960, 2019.

[2] D. Bosich, A. Vicenzutti, R. Pelaschiar, R. Menis, and G. Sulligoi, "Toward the future: The MVDC large ship research program," in *AEIT International Annual Conference*, 2015, pp. 1–6.

[3] U. Javaid, D. Dujić, and W. Van Der Merwe, "MVDC marine electrical distribution: Are we ready?" in *41st Annual Conference of the IEEE Industrial Electronics Society*, 2015, pp. 823–828.

[4] J. Kuseian, T. McCoy, and K. McCoy, "Naval power systems technology development roadmap PMS 320," Naval Sea Systems Command, 2013.

[5] J. Langston, K. Schoder, M. Sloderbeck, M. Steurer, and A. Rockhill, "Testing operation and coordination of DC solid state circuit breakers," in *44th Annual Conference of the IEEE Industrial Electronics Society*, 2018, pp. 445–452.

[6] S. Kim, G. Ulissi, S.-N. Kim, and D. Dujic, "Protection coordination for reliable marine DC power distribution networks," *IEEE Access*, vol. 8, pp. 813–823, 2020.

[7] T. B. Sledge, "Modeling and control of a modular multilevel rectifier," M.S. thesis, Monterey, CA; Naval Postgraduate School, 2022.

[8] D. T. Kinney Jr, "Modeling and topology evaluation for rectifier circuits in medium voltage direct current system," M.S. thesis, Monterey, CA; Naval Postgraduate School, 2021.

[9] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 364–377, 2020.

[10] S. Nandakumar, I. V. Raghavendra, C. M. Ajmal, S. N. Banavath, and K. Rajashekara, "A modular bidirectional solid state DC circuit breaker for LV and MVDC grid applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2022.

[11] D. Zhang, Y. Xu, J. Brandt, Z. Zhang, D. Qin, and D. Dong, "A solid-state circuit breaker without current limiting inductor," in *IEEE Transactions on Power Electronics*, to be published.

[12] D. Zhang, J. He, D. Pan, M. Schutten, and M. Dame, "High power density medium-voltage megawatt-scale power converter for aviation hybrid-electric propulsion applications," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 582–588.

[13] P. Channegowda, B. Liu, B. Riar, and X. Wu, "Testing solid state DC circuit breakers for electrified aircraft applications," in *IEEE Transportation Electrification Conference & Expo (ITEC)*, 2022, pp. 123–127.

[14] Office of Naval Research, "High power solid state circuit protection for power distribution and energy storage ONRBAA13-016 22 MAY 2013," Office of Naval Research, US Navy, Tech. Rep. TR-576, 2013 [Online]. Available: https://govtribe.com/file/government-file/onrbaa13016-onrbaa13-016-dot-pdf

[15] P. Cairoli, R. A. Dougal, U. Ghisla, and I. Kondratiev, "Power sequencing approach to fault isolation in DC systems: Influence of system parameters," in *IEEE Energy Conversion Congress and Exposition*, 2010, pp. 72–78.

[16] P. Cairoli, I. Kondratiev, and R. Dougal, "Ground fault protection for dc bus using controlled power sequencing," in *Proceedings of the IEEE SoutheastCon*, 2010, pp. 234–237.

[17] N. Doerry and J. Amy, "The road to MVDC," in *ASNE Intelligent Ships Symposium*, 2015, vol. 5.

[18] N. Doerry and R. Ashton, "Auctioneering diodes: Pros and cons," in *IEEE Electric Ship Technologies Symposium*, 2019, pp. 409–415.

[19] N. Doerry and J. V. Amy, "System inductance for MVDC circuit breakers," in *IEEE Electric Ship Technologies Symposium (ESTS)*, 2021, pp. 1–7.

[20] N. H. Doerry, "Preliminary interface standard, medium voltage electric power, direct current," Naval Sea Systems Command, US Navy, Tech. Rep., 2020.

[21] D. P. DeToma, "Shipboard voltage source inverter control system to meet MIL-STD-1399-300 limits for pulsed power loads," M.S. thesis, Monterey, CA; Naval Postgraduate School, 2020.

[22] J. Zhu, Q. Zeng, X. Yang, M. Zhou, and T. Wei, "A bidirectional MVDC solid-state circuit breaker based on mixture device," *IEEE Transactions on Power Electronics*, 2022.

[23] D. Zhang, “Fast light-weight altitude-ready solid-state circuit breaker for hybrid electric propulsion (flash),” National Aeronautics And Space Administration (NASA) Glenn Research Center, 2019.

[24] Infineon, *IHM-B module with Trench/Fieldstop IGBT3 and emitter controlled 3 diode*, FZ1500R33HL3 Datasheet, 2021 [Online]. Available: https://www.infineon.com/dgdl/Infineon-FZ1500R33HL3-DataSheet-v01_10-EN.pdf?fileId=db3a304314dca389011527dbd30811c0

[25] L. Ravi, D. Zhang, D. Qin, Z. Zhang, Y. Xu, and D. Dong, “Electronic MOV-based voltage clamping circuit for DC solid-state circuit breaker applications,” *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 561–565, 2022.

[26] TDK, *Film Capacitors - Power Electronic Capacitors*, Series/Type: FilterCap MKD-AC - Single Phase Datasheet, 2019 [Online]. Available: https://4donline.ihs.com/images/VipMasterIC/IC/TDKC/TDKC-S-A0009778449/TDKC-S-A0009778449-1.pdf?hkey=CECEF36DEECDED6468708AAF2E19C0C6

[27] KEPCO, *KEPCO’S HIGH VOLTAGE BHK-MG SERIES*, Half Rack, 2003 [Online]. Available: https://www.kepcopower.com/1461923.pdf

[28] Southwire, *2kV HDFPC-DLO, RHH/RHW-2 & RW90*, SPEC 44020 , 2021 [Online]. Available: https://assets.southwire.com/ImConvServlet/imconv/3f0f2d32490ad0b44711e4312b93b83af7c13e83/origin?assetDescr=SPEC44020

[29] IXYS, *Thyristor Module*, Phase leg MCC200-18io1 Datasheet, 2019 [Online]. Available: https://www.mouser.com/datasheet/2/240/MCC200-18io1-1549231.pdf

[30] Littlefuse, *Metal-Oxide Varistor (MOVs)*, Industrial High Energy Terminal Varistors > BA/BB Series Datasheet, 2020 [Online]. Available: https://www.mouser.com/datasheet/2/240/Littelfuse_Varistor_BA_BB_Datasheet_pdf-769954.pdf

[31] KEMET, *IGBT direct mount power film capacitors*, C4BS, 850-3000VDC/550-750VAC Datasheet, 2022 [Online]. Available: https://www.mouser.com/datasheet/2/212/1/KEM_F3048_C4BS-2064381.pdf

[32] TT Electronics, *Vitreous enamelled wirewound resistors*, W20 series Datasheet, 2021 [Online]. Available: https://www.mouser.com/datasheet/2/414/W20-1528338.pdf

[33] Thermo Fisher Scientific, *HOT PLATE Operation Manual and Parts List Series 237*, Model Numbers HPA2230M HPA2234M HPA2235M HPA2238M HPA2235M-13 HPA2230M-26, [Online]. Available: https://www.thermofisher.com/order/catalog/product/HPA2245MQ

[34] Tektronix, *Isolated Measurement Systems*, TIVP1, TIVP05, TIVP02 Datasheet, 2022 [Online]. Available: https://www.tek.com/en/datasheet/isolated-measurement-systems-tivp1-tivp05-tivp02-datasheet

[35] Power Electronic Measurements, *CWT Mini*, CWT MiniHF CWT Mini, 2020 [Online]. Available: http://www.pemuk.com/Userfiles/CWTmini/CWT_Mini_DS_Feb_2020.pdf

[36] Tektronix, *High-voltage Differential Probes*, TMDP0100, 2021 [Online]. Available: https://www.tek.com/en/datasheet/high-voltage-differential-probes

[37] Tektronix, *5 Series MSO*, Mixed Signal Oscilloscope Datasheet, 2022 [Online]. Available: https://www.tek.com/en/datasheet/5-series-mso

[38] Magna-Power Electronics, *TS Series*, MagnaDC Programmable DC Power Supplies Datasheet, 2021 [Online]. Available: https://magna-power.com/assets/files/datasheets/datasheet_ts_4.5.0.pdf

[39] Advanced Thermal Solutions, *DIY Cold Plates*, ATS-CP-1001-DIY, 2019 [Online]. Available: https://media.digikey.com/pdf/Data%20Sheets/Advanced%20Thermal%20Solutions%20PDFs/ATS-CP-1001-DIY.pdf

[40] SMC Corporation, *Circulating Fluid Temperature Controller Thermo-chiller Compact Type*, Series HRS, 2011 [Online]. Available: https://www.smcpneumatics.com/pdfs/HRS.pdf

[41] Seametrics, *S-Series*, SPT, SPX Low Flow Meters, 2022 [Online]. Available: https://www.seametrics.com/wp-content/uploads/LT-65650049r2.2-20220524-S-Series-Specs.pdf

[42] TGlobal Technology, *TH-N909*, Non-silicone Thermal Grease, 2020 [Online]. Available: https://www.tglobaltechnology.com/wp-content/uploads/2019/07/TG-N909-1.pdf

[43] Neoptix, *Neoptix T1 Probe*, Fiber optic temperature probe, 2019 [Online]. Available: https://www.environmental-expert.com/downloads/neoptix-t1-fiber-optic-temperature-probe-brochure-393912

[44] Omega, *Easy-To-Use Surface RTD*, SA1-RTD-B Series, 2008 [Online]. Available: https://assets.omega.com/spec/SA1-RTD-B-series_spec.pdf

[45] Hioki, *AC/DC Current Sensor*, CT6877A CT6877A-1, 2021 [Online]. Available: https://www.hioki.com/global/support/download/manuals?keyword=CT6877

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