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ABSTRACT

Conformable, flexible, and stretchable thin film transistors hold promise for ubiquitous and low-cost electronics. As part of the research endeavor toward this goal, the challenges associated with compatible materials and growth processes have been intensely studied. What is seldom considered, however, is how device electrostatics change as the physical form of devices change. In this report, we study how one would expect the current–voltage characteristics of thin film transistors to change as they are deformed on the surface of a sphere. We derive analogous equations to those derived in the gradual channel approximation to relate current to applied voltage for various spherical geometries. Combined with a finite-difference strategy to evaluate geometric capacitance, example current–voltage characteristics are calculated. The results demonstrate for certain deformations in this geometry, the behavior deviates from what one would expect using just the gradual channel approximation. For flexible electronics to be commercially viable, it must be predictable in any physical form. These results represent some of the first steps in a broader effort to quantify the relationship between device geometry and electrical behavior.

I. INTRODUCTION

Flexible electronics is a technology that holds potential for a diverse range of applications[1] and promises a world where electronics is low cost and ubiquitous.[2] The challenges to such a vision are twofold. First, traditional, silicon-based electronics are too mechanically rigid and physically incompatible to fulfill the requirements of low-cost, large areas deposition.[3] This has led to a large research effort over the past few decades into new semiconductor systems compatible with large area deposition and mechanically flexible substrates.[4] Second, when considering electronic devices which could potentially have limitless variation in geometry and shape,[5–7] a re-assessment of our existing device modeling paradigms is needed. In particular, the assumption that electronics is always flat, static, and that charges travel in straight lines must be re-assessed.

While extensive progress has been made in the development of innovative, low-cost manufacturing methods[2] and the use of novel, solution processable materials[8] such as metal oxides,[9] organic semiconductors,[10] carbon nanotube networks,[11] metal halide perovskites,[12] and chalcogenides,[13] the electrostatic models for analyzing such devices remains broadly similar to existing, traditional, and linear electronics.[14] We have previously made a first attempt at generalizing models to consider non-planar devices by evaluating current–voltage characteristics for transistors on the surface of cylinders.[15] In this work, we broaden this strategy to consider transistors on the surface of a sphere.

The gradual channel approximation (GCA) is a commonly employed strategy to quantify the electronic behavior of transistors.[16] Specifically, it enables one to predict current as a function of applied gate and drain voltages and is widely employed in the thin film transistor (TFT) community to predict behavior and quantify performance.[17–19] In the GCA, capacitance is derived by solving Gauss' law for an infinite flat plane.[20] One of the main results of the GCA is the relationship between source–drain current (I_D), gate (V_G), drain (V_D), and threshold (V_T) voltages for a device with a certain charge carrier mobility (μ), dielectric capacitance per unit area (C_i), and channel width (W)/length (L)

ratio,

$$I_D = \frac{W}{L}\mu C_i \left[(V_G - V_T)V_D - \frac{V_D^2}{2} \right].\qquad(1)$$

While a good approximation for conventional, linear transistors, the assumptions made in the derivation of Eq. (1) may not hold for electronics based on flexible, curvilinear substrates, where the dimensions of curvature are comparable to device dimensions.[15] In such cases, a more general model is required to take into account the curvature and geometry of the device itself. While effects of mechanical strain[14] and film fracture[21] as a result of device deformation have been well studied, an in depth look into the effect of deformation on the electrostatics itself is less common.[15,22] We have previously reported deviations in dielectric capacitance and transfer characteristics for a thin film transistor on a cylindrical substrate.[15]

In this work, we look at another non-planar geometry, that of a transistor on the surface of a sphere. We analyze two unique device configurations, differing in the orientation of the source and drain, and derive transfer characteristics for these configurations. Our results show once again that significant deviations in device characteristics are expected when deformations occur over length scales comparable to the device dimensions.

## II. EVALUATION OF CURRENT–VOLTAGE CHARACTERISTICS

The capacitance per unit area of the dielectric layer (C_i) term from Eq. (1) is derived for traditional, planar, TFT's by assuming the gate electrode as an charged plane with infinite extent and applying Gauss' law,[16] resulting in electric field lines perpendicular to the plane.[20] When we are dealing with a curvilinear substrate, however, this approximation is not valid, and we must resort to more exact, numerical methods to evaluate the C_i term for our specific device geometry. Such an approach also allows us to study the effect of the curvature on the C_i term itself. Here, we apply finite-difference methods to evaluate C_i. This process is analogous to our previous strategy used to evaluate the dielectric capacitance of a transistor on the surface of a cylinder[15] and is described in more detail in the Sec. I in the supplementary material.

Once we have a strategy established to evaluate the mutual capacitance between the metal–semiconductor layers, our next step is to derive an equation for current–voltage characteristics for our geometry, analogous to that resulting from the GCA. Depending on how the source and drain electrodes are positioned, there are many ways one can construct a transistor on the surface of a sphere. For the purposes of this report, we consider two example device configurations, which we designate configuration 1 and configuration 2, described in more detail shortly. While such devices are unlikely to be of any practical use on their own, especially with the length scales considered here, we hope to illustrate in this manuscript how current–voltage characteristics will change as transistors are deformed from planar to spherical. Such deviations are not encapsulated in the current models for TFTs and hence represent deviations from expected behavior.

The strategy described in this report focuses exclusively on considerations arising from changes in geometry and is hence highly idealized. For example, we have not considered any changes to the electronic/dielectric properties as a result of physical deformation. It is well known that stress and strain can affect electronic properties,[14] indeed pressure sensors are based on this principle.[23] Additionally, we have neglected the role played by traps in these devices. Again, traps play a decisive role in thin film electronic devices, especially when layers are deposited using relatively crude growth techniques such as solution-based methods.[24] In real flexible devices, it is likely that the density and properties of traps will change as films are deformed. Strain and compression are known to lead to film cracking in certain cases which, again,[25] is a phenomenon neglected for the purposes of this study.

Similarly, we will here consider extreme deformations only; those with bending radii comparable to device dimensions. This is in order to demonstrate appreciable changes in electrical characteristics. We have simulated devices with widths on the order of ~mm, which are not likely to be technologically relevant for applications requiring high device density, for example, displays, circuits, and so on.[26] However, devices with extreme bending ratios have been demonstrated experimentally,[27] and it is hoped that this work serves as a first step toward a more general mathematical framework for characterizing and predicting the behavior of electronics of any physical form.

All layers of the thin film transistors considered here will be stacked vertically onto the surface of a sphere, which will be assumed to be highly electrically insulating (e.g., glass), as depicted in Fig. 1. The bottom layer will be a metallic gate, followed by an insulating layer, and a semiconductor on top of the insulator. The distance between the center of the sphere and the metal–semiconductor interface is defined as r_1, and the distance from the center of the sphere and semiconductor–insulator interface is defined as r_2.
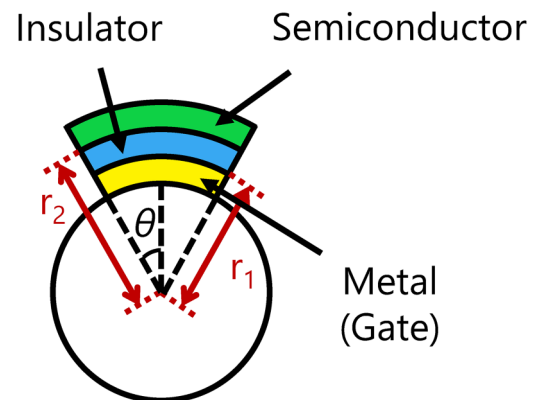
FIG. 1. Illustrative cross-sectional diagram of the layers which makeup a thin film transistor on the surface of a sphere. The distance between the center of the sphere and the metal–semiconductor interface is defined as r_1, and the distance from the center of the sphere and semiconductor–insulator interface is defined as r_2. The angle θ is used to define the size of the device on the surface of the sphere.

Our strategy is based on analogous steps we would use to evaluate the current–voltage characteristics in a planar device.[16] The procedure is as follows:

(1) Identify the direction of charge carrier flow. We assume that charge will flow between the source and drain via the shortest path through the semiconductor.
(2) Identify and discretize the space through which the charge is flowing into a number of differential volume elements (DVEs). Define the volume of each DVE as dv, and the sheet area of each DVE as dA. dA is the differential area of the semiconductor–dielectric interface where charge resides. Note, we use lowercase v to represent volume throughout this report to avoid confusion with voltage (which is denoted as uppercase V).
(3) Write an expression for two key parameters associated with each DVE, the area of cross section through which our charge passes and the volume of the DVE itself.
(4) For each such DVE, we also identify and write an expression for the sheet area, essentially the area of the semiconductor–dielectric interface where our mobile charge resides.
(5) Express dv and dA in spherical-polar coordinates.
(6) Use our strategy for mutual capacitance, derived in Sec. I in the supplementary material, to evaluate carrier concentration.
(7) Use Ohm's law to express the source–drain current I_D, in terms of carrier concentration.
(8) Finally, we integrate our expression between the electrodes in our transistor to evaluate the transfer characteristics.

A. Configuration 1

The first type of spherical transistor we will consider is depicted in Fig. 2. In this case, one of the source/drain electrodes is at one of the poles while the other is a band around the equator. While in Fig. 2, the device is depicted with finite electrode sizes (for clarity), the electrodes in these calculations are all assumed to be infinitesimal in size. This is to ensure that effective device area, equivalent to width/length ratio in planar transistors, does not change unexpectedly with deformations.
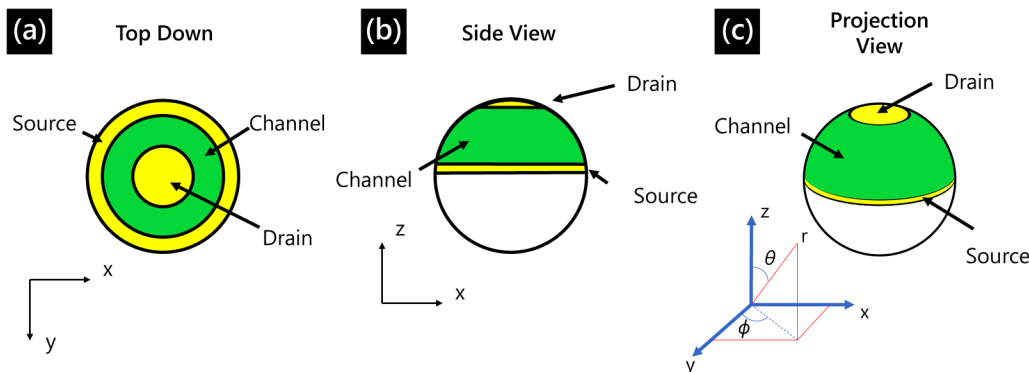

FIG. 3. Side view schematic diagrams of thin film transistor on the surface of a sphere, in what we have designated "configuration 1" for values of θ (a) equal to 90° and (b) less than 90°.

Figure 2 depicts a device defined by a polar angle of $\theta = 90°$. This means the device occupies an area between $\theta_D = 0°$ (i.e., the north pole at the drain) to $\theta_S = 90°$ (i.e., the source at the equator) on the surface of the sphere. If the device were defined by an angle smaller than 90°, it would instead be defined between $\theta_D = 0°$ and $\theta_S = \theta$. This is illustrated in Fig. 3. As $\theta \to 0°$, it is clear that the device tends to a flat, circular, and transistor.

As in a planar TFT, we use the definition of capacitance per unit area, C_i, to evaluate the mobile charge density per unit area, Q_{mob}, induced in the semiconductor for a given gate voltage V_G when the drain voltage is zero: $V_D = 0$. This is given by Eq. (2), where V_T is the threshold voltage,

$$Q_{\text{mob}} = C_i(V_G - V_T). \tag{2}$$

The application of a drain voltage leads to an additional potential at the semiconductor–dielectric interface in a TFT, depending on position in the channel: $V(r, \theta, \phi)$. For our spherical transistors, we can exploit certain aspects of spherical symmetry to simplify our formalism. Being on the surface of a sphere, the

FIG. 2. Schematic diagrams of thin film transistor on the surface of a sphere, in what we have designated "configuration 1." While the electrodes are depicted here with a finite area, for the purposes of this study all electrodes are considered infinitesimal in size.
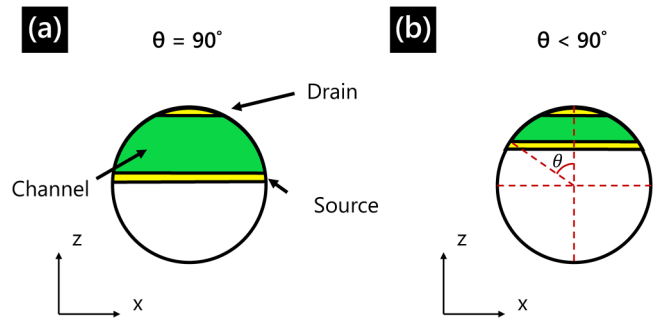
radius, r, is constant for all positions in the channel. For configuration 1, we define the charge to flow between the source and the drain, as depicted in Fig. 4(a), implying that the potential will also be independent of the azimuthal angle, ϕ, and that we can hence parameterize the voltage due to the drain as a function of just the zenith angle, θ, i.e., $V(r, \theta, \phi) \rightarrow V(\theta)$.

We can then define the mobile carrier density with an applied drain voltage as follows:

$$Q_{mob} = C_i(V_G - V_T - V(\theta)). \tag{3}$$

For this derivation, we will assume we are dealing with an n-type TFT; one where the current is due to the injection and transport of electrons only. Our procedure is equally valid for a p-type TFT with appropriate adjustments in sign and notation. For an ambipolar[28] TFT, a more elaborate formalism would be required, and ambipolar behavior is not encapsulated in this model. For a n-type TFT, the conductivity, σ, can be expressed in terms of the average electron mobility in the channel, μ, the three-dimensional electron density, n, and the magnitude of the fundamental unit of charge, e, as follows:

$$\sigma = e\mu n. \tag{4}$$

The charge density, and hence σ, will depend on location in the channel. We can approximate the current as flowing through a series of differential volume elements, with σ depending on θ, as depicted in Fig. 4(b). The volume of the differential element, dv, is given by Eq. (5),

$$dv = 2\pi \left(\frac{r_2^3 - r_1^3}{3} \right) \sin(\theta)d\theta. \tag{5}$$

Here, r_1 is the radius from the center of the sphere to the interface between the gate electrode and gate dielectric, and r_2 is the distance from the center of the sphere to the interface between the gate dielectric and the semiconductor. Hence, the thickness of the dielectric is $r_2 - r_1$.
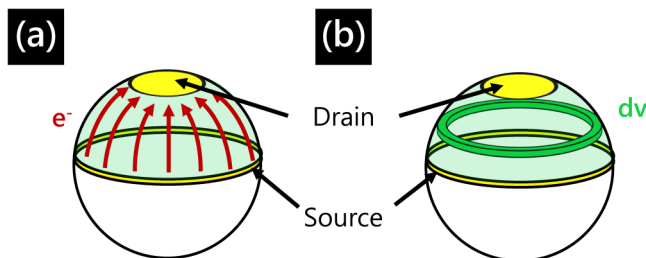
FIG. 4. Schematic diagrams of thin film transistor on the surface of a sphere in "configuration 1." (a) Illustration of the direction of electrical charge flowing between source and drain electrodes. (b) Illustration of differential volume element, dv, used in evaluation of current–voltage characteristics in this configuration.

The definition of three-dimensional number density is $n(\theta) = N(\theta)/dv$, where $N(\theta)$ is the total number of mobile charge carriers in our differential volume element. We can hence write $eN(\theta)$ as $Q'_{mob}(\theta)$, the total mobile charge in our differential volume element (where the prime denotes this is an absolute charge, not a charge density). We relate total charge to two-dimensional (areal) charge density via Eq. (6),

$$Q_{mob}(\theta) = \frac{Q'_{mob}(\theta)}{dA}, \tag{6}$$

where dA is the sheet area or the surface area of the semiconductor–dielectric interface of our differential volume element, where the mobile charge resides,

$$dA = 2\pi r_2^2 \sin(\theta)d\theta. \tag{7}$$

Hence,

$$Q'_{mob}(\theta) = 2\pi r_2^2 \sin(\theta)d\theta Q_{mob}(\theta). \tag{8}$$

Substitution into Eq. (4) allows us then to define the conductivity of the volume element,

$$\sigma(\theta) = \frac{3\mu r_2^2}{r_2^3 - r_1^3} Q_{mob}(\theta). \tag{9}$$

To evaluate the source–drain current, we need to consider the sample dimensions, which we do via resistance. The resistivity of a medium is defined as $\rho = RA/L$, where A is the cross-sectional area of the medium in the direction of charge movement, L is the distance the charge travels, and R is the resistance of the object. Both these parameters will vary depending on the zenith angle coordinate,

$$L = r_2(\theta), \tag{10}$$

$$A = \pi \sin^2(\theta)(r_2^2 - r_1^2). \tag{11}$$

Combined with the definition of resistivity, R, we can say

$$\sigma = \frac{1}{\rho} = r_2 \frac{d\theta}{dR\pi\sin^2(\theta)(r_2^2 - r_1^2)} \tag{12}$$

and

$$dR = r_2 \frac{d\theta}{\sigma(\theta)\pi\sin^2(\theta)(r_2^2 - r_1^2)}. \tag{13}$$

Substitute $\sigma(\theta)$ from Eq. (9) into Eq. (13),

$$dR = \frac{r_2^3 - r_1^3}{r_2^2 - r_1^2} \frac{1}{\pi\sin^2(\theta)} \frac{d\theta}{3\mu r_2 Q_{mob}(\theta)}. \tag{14}$$

We can use the differential form of Ohm's law, $I_D = dV/dR$, to define source–drain current in the device. We can evaluate the

current by integrating over the device's dimensional and operational limits,

$$\int_{\theta_S}^{\theta_D} I_D \frac{d\theta}{\sin^2\theta} = \frac{3\pi\mu r_2 C_i (r_2^2 - r_1^2)}{r_2^3 - r_1^3} \int_0^{V_D} (V_G - V_T - V(\theta))dV. \quad (15)$$

Here, θ_S and θ_D denote the zenith angle of the source and drain electrodes, respectively. This is our analogous version of Eq. (1) for a transistor on the surface of a sphere, constructed as in Fig. 2. This equation allows us to determine how source–drain current depends on the device dimensions θ_S, θ_D, r_2, and r_1.

B. Configuration 2

For our second spherical transistor, the source and drain electrodes are semicircles on the side of the sphere, as depicted in Fig. 5. This could be more representative of a real deformation in a flexible transistor. For example, by pushing through from below a previously flat transistor on a flexible substrate.

Figure 5 depicts a device defined by a polar angle of $\theta = 90°$. This means the device occupies an area on the surface of the sphere between the north pole (0°) and the equator (90°). For a device defined with $\theta < 90°$, it is perhaps less intuitive than configuration 1 (where the electrodes were at the pole and equator) what this means. In the case of configuration 2, θ defines the angle where the semiconductor channel starts. This is depicted in Fig. 6. As $\theta \to 0°$, it is clear that the device tends to a flat, linear transistor.

As before, we assume here an n-type TFT, but the derivation is valid for a p-type device with the appropriate changes of sign. The direction of charge flow from source to drain for this configuration is shown in Fig. 7(a).

The initial expression for the mobile charge per unit area at our semiconductor–dielectric interface as a result of an applied gate and drain voltage is equivalent to that used for configuration 1, but the voltage due to the applied drain voltage now depends on both the zenith and azimuthal angles: $V(\theta, \phi)$. As before, the TFT is on the surface of a sphere and hence carrier density is not a
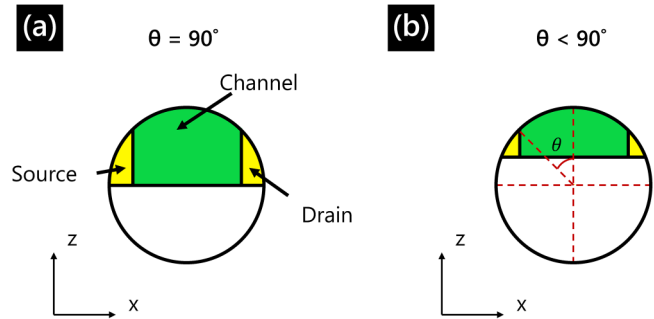

FIG. 6. Side view schematic diagrams of thin film transistor on the surface of a sphere, in what we have designated "configuration 2" for values of θ (a) equal to 90° and (b) less than 90°.

function of radial distance from the center of the sphere,

$$Q_{\mathrm{mob}} = C_i(V_G - V_T - V(\theta, \phi)). \quad (16)$$

The differential element through which our charge passes this time is depicted in Fig. 7(b). The area of cross section through which current passes is given by Eq. (17),

$$A_{cross} = \phi\sin^2\theta(r_2^2 - r_1^2). \quad (17)$$

The sheet area of our differential element is then,

$$\partial A = \left(\frac{\phi}{\pi}\right) \int_{-\phi}^{\phi} \int_{\theta}^{\theta+d\theta} (r_2\sin(\theta)d\phi)(r_2 d\theta). \quad (18)$$

Therefore,

$$\partial A = 2r_2^2 \phi\sin(\theta)d\theta\left(\frac{\phi}{\pi}\right). \quad (19)$$
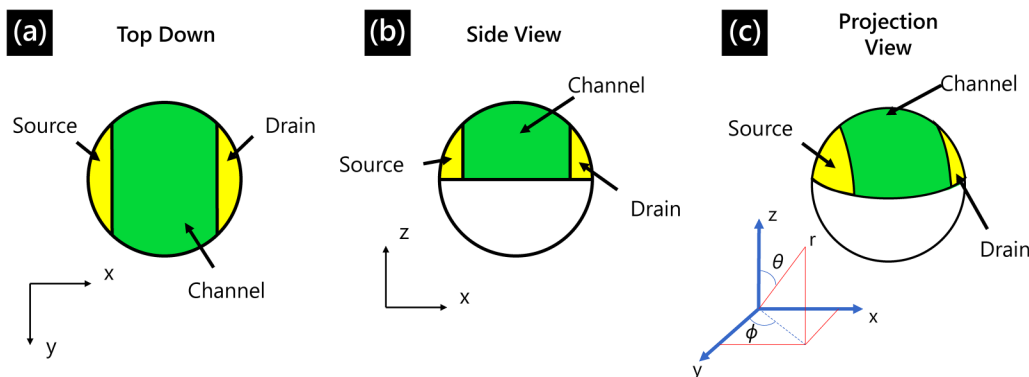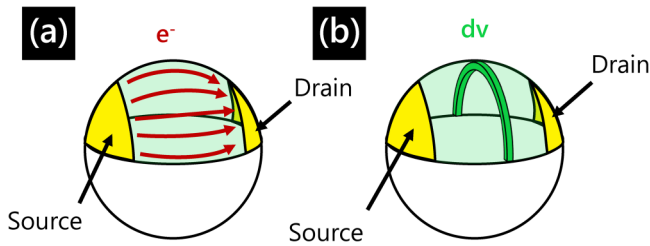

FIG. 5. Schematic diagrams of thin film transistor on the surface of a sphere, in what we have designated "configuration 2." While the electrodes are depicted here with a finite area, for the purposes of this study all electrodes are considered infinitesimal in size.

FIG. 7. Schematic diagrams of thin film transistor on the surface of a sphere in "configuration 2." (a) Illustration of the direction of charge flowing between source and drain electrodes. (b) Illustration of differential volume element, dv, used in evaluation of current voltage characteristics in this configuration.

The volume of our differential element is

$$\partial v = \left(\frac{\phi}{\pi}\right) \int_{\theta}^{\theta+d\theta} \int_{-\phi}^{\phi} \int_{r_1}^{r_2} r\sin(\theta)d\phi(rd\theta)dr = 2\frac{r_2^3 - r_1^3}{3}\phi\sin(\theta)\left(\frac{\phi}{\pi}\right)d\theta.$$

(20)

We can combine Ohm's law in one dimension, $j = ne\mu_n E$, with A_{cross} through which the charge passes [Eq. (18)] to provide current,

$$I_D = n\phi\sin^2\theta(r_2^2 - r_1^2)e\mu_n E ,$$

(21)

where n is the charge carrier concentration per unit volume for our differential element. If n_s is the sheet charge (areal) carrier concentration at the semiconductor–dielectric interface for our differential element, then we can say $n_s dA = ndV$. Combining this definition with the induced charge density in a capacitor [Eq. (16)] and our equation for source–drain current [Eq. (21)] gives

$$\int_{\theta_S}^{\theta_D} I_D \frac{d\theta}{\sin^2\theta} = 3r_2^2\frac{r_2^2 - r_1^2}{r_2^3 - r_1^3}C_i\mu\frac{\phi}{r_2}\int_0^{V_D}(V_G - V_T - V(\theta))dV.$$

(22)

This is our analogous version of Eq. (1) for a transistor on the surface of a sphere, constructed as in Fig. 5.

III. RESULTS

By evaluating the capacitance as described in Sec. I in the supplementary material, and then applying Eqs. (15) and (22), it is possible to evaluate how the current–voltage characteristics change with the deformation of the device for both device configurations analyzed in Secs. II A and II B. The objective is to demonstrate how current–voltage characteristics of transistors deformed in this way can be expected to change. Specifically, we vary the parameter θ, the extent of the surface of the sphere covered by the device, while keeping other length scales constant. In this context, θ can be considered a metric for deformation from flat, because as $\theta \rightarrow 0$,

we should approach the case of a flat transistor and hence recover behavior described by conventional models.

It is clear from Fig. 1 that to maintain a spherical geometry with deformation, at least one of the following three parameters must change: outer arc length, $r_2\theta$ (the length of the semiconductor–dielectric interface), inner arc length, $r_1\theta$ (the length of the gate–dielectric interface), and the dielectric thickness, $r_2 - r_1$. Because changing the outer arc length $r_2\theta$ is equivalent to changing the device length in a flat TFT, we expect this deformation to lead to obvious changes (lower current as $r_2\theta$ increases). Therefore, we consider the two possible deformations which maintain a constant effective channel length (the outer arc $r_2\theta$),

(1) Keeping both the outer and inner arc lengths, constant. In this case, r_1 and r_2 will decrease as our angle of curvature increases. The dielectric thickness $r_2 - r_1$ will also decrease.
(2) Keeping the outer arc length and dielectric thickness constant, in this case, $r_2 - r_1$ and as $r_2\theta$ are held constant, but $r_1\theta$ can vary to accommodate the deformation.

In reality, the deformation will depend on the mechanical properties of the respective layers of the device. For example, the relative values of Young's moduli and thicknesses will determine the extent of bending and cracking in each of the layers.[14] On inspection of Fig. 1, it is clear that a clean stack, with all material edges aligned and perpendicular to the substrate, is not possible with these deformations. However, because of the way the capacitance is calculated (see the supplementary material), the consequences of edge effects and loss of direct contact is going to be minimal in our calculations.

To evaluate current as a function of voltage, we choose some representative values, as given in Table I. These are meant to approximate what one could expect when employing metal oxide semiconductors in flexible electronics.[18] For transistors on the surface of spheres, there no longer exists simple values for L and W, in the same way as there is for linear transistors. The distance between the source and drain ($L_{S\rightarrow D}$) electrodes is the same for all positions and is a function of θ. $L_{S\rightarrow D} = r_1\pi\theta/180$, where θ is in degrees. For the case of $\theta = 90°$, $L_{S\rightarrow D} = 0.79$ cm, and for $\theta = 10°$, $L_{S\rightarrow D} = 0.09$ cm, for example.

The analog of the gate width (the distance perpendicular to the direction of current flow) is not constant as a function of position

TABLE I. List of parameters used in current–voltage calculations.

Parameter	Name	Value
r_1	Distance from center of sphere to metal–dielectric interface	0.5 cm
$r_2 - r_1$	Thickness of the dielectric layer	100 nm
V_D	Source–drain voltage	10 V
V_T	Threshold voltage	0 V
V_G	Gate voltage (range)	0–100 V
θ	Angle of curvature (range)	10–80°
μ	Electron mobility	100 cm²/Vs
ε_r	Dielectric constant of dielectric	3.9

for configuration 1 or configuration 2. In configuration 1, this parameter would increase from 0 at the drain to $2\pi r_1 \sin\theta$ at the source. In configuration 2, this parameter would increase from 0 (assuming infinitesimal contacts) at both contacts to $\pi r_1 \sin\theta$ at the point halfway between the contacts. The dielectric thickness depends on the type of deformation but is defined as 100 nm for $\theta = 10°$.
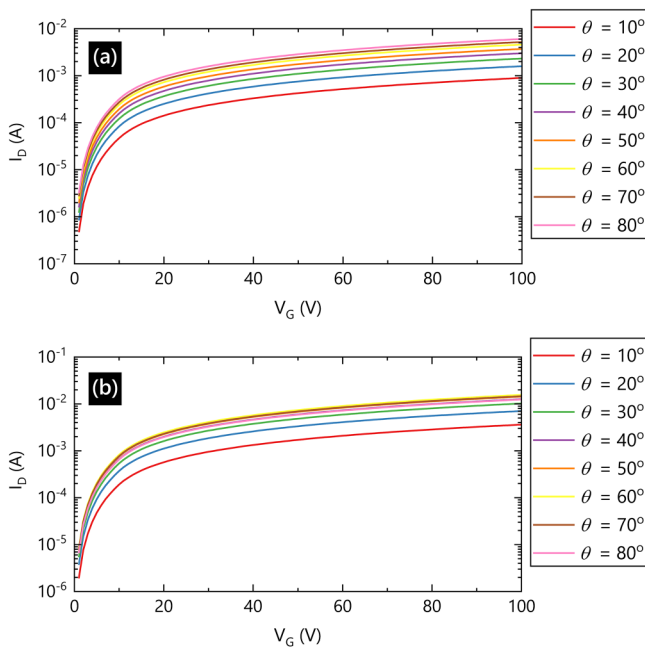
Figure 8 shows transfer characteristics (source–drain current, I_D, as a function of gate voltage, V_G) for a transistor on the surface of a sphere, for various values of θ. Figure 8(a) shows the results for a transistor in configuration 1 (i.e., Fig. 2). In this case, as θ increases, the current also increases. To accommodate this deformation, the dielectric thickness must change as θ does. This requirement can be visualized by imagining the cross-sectional blue slice in Fig. 1 being bent from an almost flat rectangle to a semicircular block arc, with the condition that the inner and outer arc lengths remain constant. In three-dimensions, the blue section is of course a spherical cap not a rectangle. If we started with a true flat circle ($\theta = 0$), any such restricted deformation would be impossible; however, since we consider only $\theta \geq 10°$, the arc lengths can be kept constant by allowing the dielectric thickness to change.

The data in Fig. 8 illustrate that the strategy for evaluating current works as expected, and that conventional transfer curves are obtained.[14] In both configurations, the current increases as the device is deformed from close to flat ($\theta = 10°$) toward a device on a hemisphere ($\theta = 80°$). Because the path length of carriers remains

constant (by definition), the increase here can be attributed to the increase in C_i resulting from the decrease in the dielectric thickness. The differences in magnitude of current between the two geometries are because of the different effective width/length ratios.

Figure 9 shows transfer characteristics of transistors on the surface of a sphere, undergoing similar deformations, but in this case, the outer arc length (i.e., along the semiconductor–dielectric interface) and the dielectric thickness are kept constant, and the inner arc length is allowed to vary to accommodate the deformation. In this case, we see that the changes are much less significant, especially for configuration 1. The effects of this deformation are slightly more subtle, as it does not involve changes to the thickness of the dielectric medium. The changes observed in Fig. 9 are more a result of changes in electrostatics and edge effects, resulting from the change in geometry. The effect appears more pronounced for the case when the field resulting from the source–drain voltage goes across the device (configuration 2) rather than radially from the center of the device (configuration 1). For both deformations, and both configurations, we have demonstrated non-negligible phenomena which are not encapsulated by the traditional GCA.

One thing to note in our model is that we have assumed the dielectric constant of the oxide layer remains constant with mechanical deformation, which may not necessarily be the case.[29] In reality, the effect of curvature on the I–V characteristics of a flexible TFT will depend on a lot of other properties of the device and material

FIG. 8. Calculated transfer characteristics (source–drain current, I_D, as a function of gate voltage, V_G) for a thin film transistor on the surface of a sphere being deformed as a function of θ for (a) configuration 1 and (b) configuration 2. In this case, both the outer and inner arc lengths are kept constant, and the dielectric thickness $r_2 - r_1$ is allowed to vary to accommodate the deformation. All parameters used in this calculation are from Table I.
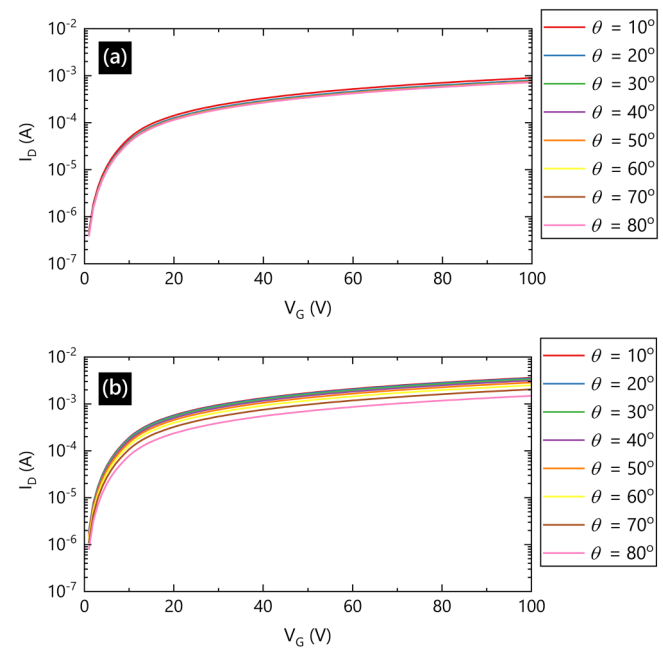
FIG. 9. Calculated transfer characteristics (source–drain current, I_D, as a function of gate voltage, V_G) for a thin film transistor on the surface of a sphere being deformed as a function of θ for (a) configuration 1 and (b) configuration 2. In this case, both the outer arc length and dielectric thickness are kept constant, and the inner arc length was allowed to vary to accommodate the deformation. All parameters used in this calculation are from Table I.

design, such as the Young's moduli. However, this study does illustrate that changes in curvature is expected to cause a noticeable deviation in the I–V characteristics based on the geometry alone.

IV. CONCLUSION

Using the finite-difference method, we calculated the mutual capacitance between two surfaces with arbitrary geometry. As compared to approaches used to model areal capacitance in planar transistors, which typically assume an infinite flat sheet of charge for the gate, this approach enabled us to accurately calculate the capacitance of the dielectric layer sandwiched between two surfaces of arbitrary shape. We generalized the gradual channel approximation (GCA) to a thin film transistor on the surface of a sphere and used this model to analytically derive current–voltage characteristics for two discrete device configurations, distinguished by the relative orientation of the source and drain electrodes with respect to each other. Combining the two approaches, we were able to evaluate transfer characteristics (source–drain current as a function of gate voltage) for a transistor on the surface of a sphere. We observed non-negligible changes in the current levels for these devices as the extent of curvature was varied. Our results illustrate that certain non-planar transistors cannot be characterized by the conventional GCA, and that traditional models cannot be used to accurately predict behavior.

Combined with our previous work elucidating a similar approach to the simpler case of a transistor on the surface of a cylinder,[15] this work is a logical step toward a generalized model for any arbitrary transistor geometry. Quantitative models that can accurately predict the current–voltage characteristics are an important prerequisite before flexible electronic devices can truly become commercial.

SUPPLEMENTARY MATERIAL

See the supplementary material for details of how capacitance was evaluated.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

J.G.L. conceived the project. S.C. developed the model and carried out calculations. Both authors discussed the results and contributed to the writing of the paper.

Shirsopratim Chattopadhyay: Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (supporting). **John G. Labram:** Conceptualization (lead); Funding acquisition (lead); Project administration (lead); Resources (lead); Supervision (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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