Effects of post oxidation of SiO_2/Si interfaces in ultrahigh vacuum below 450 °C

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ABSTRACT

Growing SiO_2 layer by wet-chemical oxidation of Si surfaces before growth of another insulating film(s) is a used method to passivate Si interfaces in applications (e.g., solar cell, photodiode) at low temperatures (LT) below 450 °C. We report on potential of LT ultrahigh-vacuum (UHV) treatments combined with the wet-chemical oxidation, by investigating effects of LT-UHV oxidation after the wet-chemical growth of SiO_2 and before growing Al_2O_3 film on top of SiO_2/Si. This method modifies the SiO_2/Si and is found to (i) decrease defect-level density, (ii) increase negative fixed charge density, and (iii) increase carrier lifetime for Al_2O_3/SiO_2/p-Si, as compared to state-of-the-art SiO_2/p-Si reference interfaces without LT-UHV. X-ray photoelectron spectroscopy shows that the LT-UHV treatment decreases amount of Si^{+3} oxidized atoms in chemically grown SiO_2 and also amount of carbon contamination. In order to pave the way for further tests of LT-UHV in silicon technology, we present a design of simple UHV instrument. The above-described benefits are reproduced for 4-inch silicon wafers by means of the instrument, which is further utilized to make LT-UHV treatments for complementary SiO_2/Si interfaces of the native oxide at silicon diode sidewalls to decrease the reverse bias leakage current of the diodes.

1. Introduction

The SiO_2/Si interface defects cause electrical and optical losses as well as malfunctions in the current and future Si-based devices. Although the Si passivation is undoubtedly the most investigated and advanced procedure among different semiconductor materials and passivation methods, the Si surfaces still form one limiting part for the Si devices performance when the size of device components decreases, and the components integration level increases all the time [e.g., Refs. [1–5]].

The high temperature (HT) treatment above 700 °C has been traditionally one key step of the passivation process for the Si-based technology in order to decrease the defect-level densities (D_{it}) down to

$1 \cdot 10^{10}$ levels/(eVcm²) in the Si band-gap area for the SiO_2/Si, HfO_2/SiO_x/Si, and Al_2O_3/SiO_x/Si device interfaces [6–8]. However, the HT annealing step cannot be used, or is not preferred in many cases. For example, hybrid materials integrated with the Si platform do not necessarily tolerate HT without material degradation. HT treatments increase also energy consumption and the risk for materials contamination via increased diffusion of many elements like Cu and Ni.

The low-temperature (LT) methods to passivate Si surfaces below 450 °C become more and more relevant to develop various Si-based devices, e.g., solar cells, sidewalls of three dimensional structures, and hybrid structures integrated with the Si transistor platform [9–23]. Two common LT methods to passivate the Si interfaces are: wet-chemical oxide growth [11,12,16–19] of SiO_2 before the deposition of another

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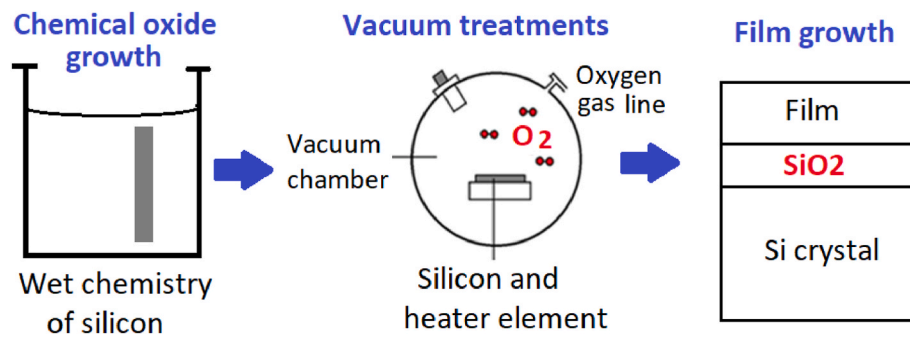
Fig. 1. Scheme for combining the wet-chemical oxide growth of SiO_2 and the ultrahigh vacuum treatments before a film deposition (e.g., ALD of Al_2O_3).

insulator(s), and the hydrogen passivation [2,8,13,22] via the forming gas anneal after insulator deposition. Often these two methods are combined like in the case of the traditional HT approach, where the hydrogen passivation is still performed after the HT annealing step of SiO_2/Si or $HfO_2/SiO_x/Si$. Silicon oxidation is a strongly exothermic reaction, so it occurs anyway at some stage(s) of the device processing. Thus, a clear benefit of the wet-chemical oxide growth of SiO_2 is that the method allows a control of the Si oxidation at low temperatures. The post-annealing after the insulator deposition (e.g., during hydrogen passivation) activates often another type of the Si-insulator interface passivation: the field-effect passivation. Here the fixed (or static) charges of an insulator film cause an internal electric field, which repels electrons or holes from the defect-rich SiO_2/Si interface region. Both the decreasing of D_{it} (i.e., so-called chemical passivation) and the field-effect passivation can simultaneously affect the electrical properties.

In this work, we have addressed the issue whether it is still useful to modify the wet-chemically grown SiO_2 by means of ultrahigh vacuum (UHV) treatments at low temperatures (<450 °C), at which the wet-chemically grown silicon oxide is not desorbed/removed. The combination of LT heating and controlled oxidation of the wet-chemically grown SiO_2/Si in UHV conditions before atomic layer deposition (ALD) of Al_2O_3 is demonstrated to decrease D_{it} as well as to increase the carrier lifetime for p-Si, as compared to the state-of-the-art wet-chemical oxide SiO_2/p-Si interfaces [16,17] with top Al_2O_3 without LT-UHV. X-ray photoelectron spectroscopy (XPS) and scanning-tunneling-microscopy (STM) characterizations are used to study factors behind the found differences in electrical properties. Finally, despite that UHV is currently used in some industrial scale processes, UHV has not been widely utilized in the Si processing. Therefore, in this work, we have also built up and tested a simple prototype UHV instrument, which is scalable and allows treating wafers and separate processed components.

2. Materials and methods

Full wafers for electrical measurements were 4-inch planar or black p-type silicon wafers, which had a wet-chemically grown layer of SiO_2 as surface finish. Black silicon wafers were prepared by using reactive ion etching (RIE) with SF_6/O_2 plasma for 7 min at a pressure of 10 mTorr and at a temperature of − 120 °C resulting in formation of nanostructures on the surface [24]. Black-silicon nanostructures, in addition to the planar surfaces, provide a strict reference [16,17] as well as a test of three-dimensionally structured surfaces for the method of this work.

Two different UHV systems were used for heating and oxidizing the 4-inch wafers. One was a UHV multichamber equipped with reflection high energy electron diffraction (RHEED), while the other instrument is introduced below in Section 3.2. The planar and black silicon wafers were inserted into the UHV system through a glove box filled with nitrogen. The wafers were heated at 350 °C for 30 min in UHV pressure of 10^{-8} mbar followed by 200-Langmuir (L) oxidation at the same

temperature (350 °C). After cooling down to room temperature under UHV condition the samples were transferred into the nitrogen glove box connected to the UHV system and were packaged in double sealed clean room bags with nitrogen. Then samples were transferred to the Aalto university within 4 h. The wafers were unpackaged in ambient condition in an ISO4 clean room and inserted into the ALD system within 3–4 min. ALD (Beneq TFS500) system was utilized for growing 22 nm Al_2O_3 using trimethylaluminium (TMA) and water precursors. Then the wafers were still annealed at 400 °C in N_2 gas for 30 min. The interface defect density (D_{it}) and fixed charge density (Q_{tot}) were measured by Corona Oxide Characterization Of Semiconductor (COCOS) method [25,26]. Minority carrier lifetime was also measured using Sinton Lifetime (Sinton Instruments, WCT-120).

Also, separate samples with wet-chemically grown SiO_2/n-Si were prepared by the RCA-based recipe without a final HF dip for XPS, STM and scanning-tunneling spectroscopy (STS) measurements. In the used RCA recipe, the samples were cleaned by acetone and methanol sonication for 3 min. Then samples were inserted into H_2SO_4(95–97%): H_2O_2(30%) (3:1) for 15 min at room temperature. After rinsing with deionized (DI) water, the samples were inserted into NH_4OH(28–30%): H_2O_2(30%):H_2O (1:1:5) at 80 °C for 10 min followed by DI water rinsing and immersion into HCl(37%):H_2O_2(30%):H_2O (1:1:6) at 80 °C for 10 min. The samples were inserted into UHV system after rinsing with DI water. Resistivity of deionized water was 21.1 MΩcm. Even if these small surface-science samples did not contain exactly the same SiO_2/Si as the wafers used in the electrical measurements, they provided a model system to clarify the properties of wet-chemically grown SiO_x/Si before and after LT-UHV.

Two different XPS instruments were used in this work: in-situ and ex-situ with base pressure of 10^{-9} (or lower) and low 10^{-7} mbar during measurements respectively and 0° electron emission angle from the surface normal. In both XPS instruments, measurements were performed without any sputtering-etch prior to analysis. In-situ XPS has MgKα radiation source (non-monochromatized), with analyzed area diameter of 3–4 mm, without any charge compensation. Ex-situ XPS has mono-chromatized AlKα radiation source equipped with dual mode charge compensation with X-ray spot size of 200 μm. The STS current-voltage curves were measured with the grid mode, and afterwards were averaged over a chosen surface area and derivated numerically.

Transmission electron microscopy (TEM) was performed at the University of Tartu. FEI Helios Nanolab 600 DualBeam scanning electron microscope (SEM) equipped with Ga focused ion beam (FIB) was used to make lamellae for scanning transmission electron microscopy (STEM). FEI Titan Themis 200 STEM with Cs corrector was used to investigate lamellae. Special sample of $Al_2O_3/SiO_2/Si$ was prepared for STEM to study how much oxygen can be incorporated into the material at the low temperatures. After cleaning of Si(100) by the flash heating at 1200 °C, the surface was oxidized by the 200-L oxygen exposure (5·10^{-6} mbar) at 350 °C in similar way as described above. Then the sample was transferred via UHV to ALD unit connected to the UHV system. After Al_2O_3-ALD, the sample was not post heated to avoid any annealing-

Table 1

Defect densities (D_{it}) and negative charge densities (Q_{tot}) for p-type planar Si wafers with Al_2O_3 film (22 nm) on the top of SiO_2/p-Si. Reference includes the preparation of chemically grown SiO_2/Si before Al_2O_3-ALD without any LT-UHV treatment [16,17]. Values represented in parentheses show the repeated measurement results for a different sample prepared with same treatment using the instrument constructed (Sec. 3.2.).

	Reference sample with chemically grown silicon oxide	Chemically grown silicon oxide + LT-UHV treatments
D_{it} ($eV^{-1}cm^{-2}$) for planar p-Si	$2.6 \cdot 10^{11}$ ($4.1 \cdot 10^{11}$)	$1.5 \cdot 10^{11}$ ($2.2 \cdot 10^{11}$)
Q_{tot} (q/cm^2) for planar p-Si	$-1.7 \cdot 10^{12}$ ($-1.6 \cdot 10^{12}$)	$-2.3 \cdot 10^{12}$ ($-2.3 \cdot 10^{12}$)

induced Si oxidation, because the aim was to understand effects of LT-UHV oxidation by STEM. A Pt film was deposited on Al_2O_3 to prepare lamellae.

Commercial Si diode components with metal contacts were used to study LT-UHV treatment effects on complementary SiO_2/Si interfaces, namely, the native oxides formed at the sidewalls of cut diodes in air exposure. Section 3.2 below presents a photograph from the diode which is a Si cube with a side length of 2.35 mm. The p and n faces include Ag/Ni/Ti/Si metal contacts covering the whole faces. These diodes were first heated in UHV at 350 °C for 30 min and after that, the diodes were oxidized at 350 °C for 60 min in O_2 background of $5 \cdot 10^{-6}$ mbar, corresponding to $18 \cdot 10^3$ L.

3. Results and discussion

3.1. Interface characterization

Fig. 1 presents a scheme for the studied passivation method where the UHV technology is combined with the wet chemistry. Various wet-chemical recipes are known for growing a SiO_2 film on Si. For instance, the traditional RCA treatment of Si provides the oxidized Si surface when the last HF-based etching step is not performed. Also, nitric acid chemicals (so-called NAOS) are used to grow SiO_2 at low temperatures [11,12]. In this work, the previously tested passivation recipe [16,17] for wet-chemical growth of silicon oxide has been used for 4-inch wafers. Also, the RCA-based recipe for preparing SiO_2/Si (details provided in the materials and methods section) has been used for smaller surface-science samples (6 mm × 12 mm). These wafers were treated with LT-UHV method as explained in materials and methods section in a post-treatment manner. For each sample with LT-UHV treatment, a reference sample was prepared and measured. Reference samples were the same as LT-UHV treated samples, but without LT-UHV treatment.

Table 1 presents the interface defect-level density (D_{it}) and the fixed (or static) charge density (Q_{tot}), measured by the COCOS method [25, 26]. It can be seen that D_{it} decreases due to the LT-UHV treatment (Table 1). In contrast, Q_{tot} increases, and therefore the field-effect passivation is expected to improve for p-Si because the negative fixed charge repels the electron minority carriers away from the SiO_2/p-Si interfaces. Indeed, the minority-carrier lifetime results in Table 2 are consistent with this hypothesis. The results show that LT-UHV treatment at 350 °C increases the minority carrier lifetime, while higher

temperature (450 °C) LT-UHV treatment decreases the minority carrier lifetime. Recently it has been shown that origin of the negative fixed charge lies in the SiO_2 interlayer between silicon and insulating passivation layer of Al_2O_3 or HfO_2 [27]. Therefore, it is reasonable that the described LT-UHV procedure has an effect on the Q_{tot} formation as well.

Separate surface-science samples were measured by XPS. Fig. 2 shows Si 2p spectra for the sample with the wet-chemically RCA-oxidized Si(100) before and after the LT-UHV treatment. XPS results indicate that the amount of partially oxidized Si atoms (i.e., Si^{+3}) [28] decreases due to LT-UHV. This spectral difference is relatively small, and therefore we have repeated the experiment with more samples and another XPS instrument and found the same difference. Also, separate results shown below support that this difference in Si 2p is significant. The literature also presents that similar spectral differences can be
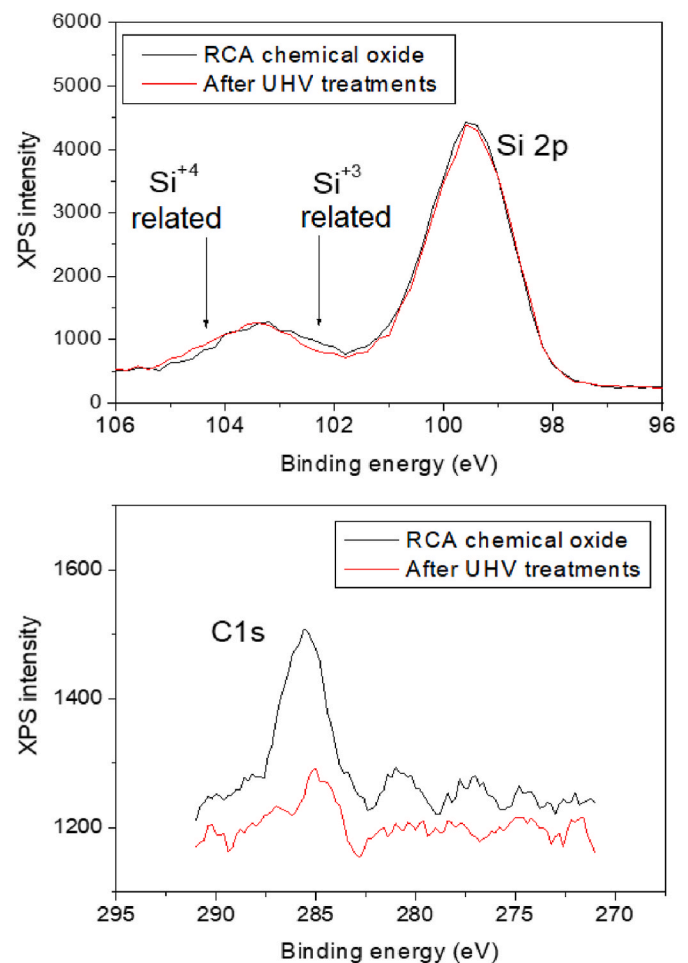

Fig. 2. In-situ XPS characterizations of the RCA wet-chemical oxide of Si(100) before and after low-temperature ultrahigh vacuum (LT-UHV) treatment. LT-UHV treatment after the chemical oxide growth of SiO_2/Si decreases amount of lower oxidation states, Si^{+3} around 103 eV binding energy.

Table 2

Minority carrier lifetimes (τ) for Al_2O_3/SiO_2/p-Si wafers with the planar or black-silicon structure with and without LT-UHV. Wafers include the preparation of chemically grown SiO_2/p-Si before 22-nm Al_2O_3-ALD. Values represented in parentheses show the repeated measurement results for a different sample prepared with same treatment using the instrument constructed (Sec. 3.2.).

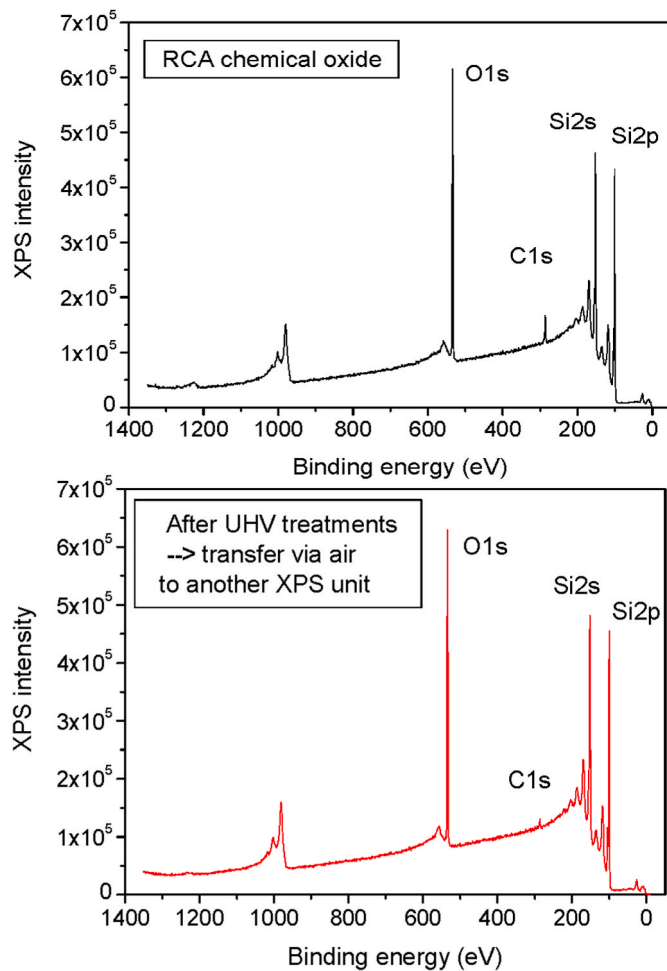|	Reference sample with chemically grown silicon oxide	Chemically grown silicon oxide + LT-UHV treatments at 350 °C	Chemically grown silicon oxide + LT-UHV treatments at 450 °C
τ for planar Si	2.2 ms	2.9 ms	1.0 ms
τ for black Si	0.9 ms (1.0 ms)	2.4 ms (2.1 ms)	0.7 ms

Fig. 3. XPS survey spectra of the RCA wet-chemical oxide of Si(100) before and after low-temperature ultrahigh vacuum (LT-UHV) treatment. An ex-situ XPS unit is used here. Thus, the sample with LT-UHV was transferred via air to another XPS after the UHV vacuum treatments.
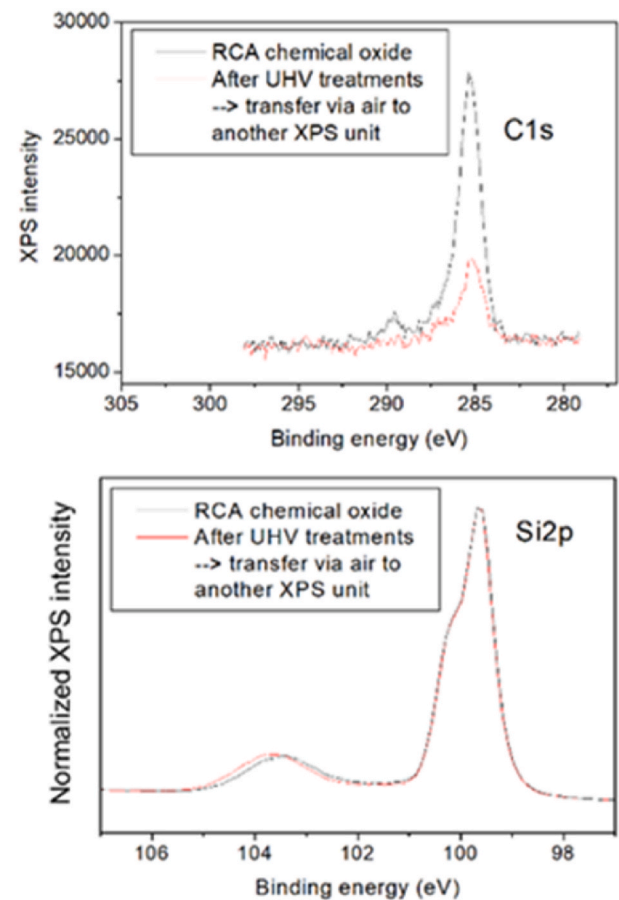

Fig. 4. XPS comparison (C 1s and Si 2p) of the RCA wet-chemical oxide of Si (100) before and after low-temperature ultrahigh vacuum (LT-UHV) treatment. An ex-situ XPS unit was used here. Thus, both samples with and without LT-UHV were transferred via air to another XPS after the UHV vacuum treatments.

significant, when the analysis is done carefully [e.g. Refs. [29,30]].

Furthermore, Fig. 2 reveals that amount of carbon contamination decreases due to LT-UHV. We did not use C 1s binding energy to calibrate the energy axis because previously such C 1s calibration has been found to be problematic [31]. In contrast, we adjusted manually the Si $2p_{3/2}$ peaks of the bulk crystal at the same energy, 99.6 eV [1], because in this work we are interested in the SiO_2-induced core-level shifts.

We used two different XPS instruments in this work. Figs. 3 and 4 present the ex-situ results obtained after transferring the LT-UHV treated sample via air to XPS. In other words, the LT-UHV treatments were done in the same UHV system, as the in-situ XPS measurements (Fig. 2) were performed, and after that the LT-UHV sample was still transferred via air to the second XPS instrument. Figs. 3 and 4 show that the amount of carbon contamination is still lower for the LT-UHV sample after the air transfer. This indicates that the carbon contamination arises mainly from the wet chemistry in these experiments. Fig. 4 shows also the Si 2p spectra measured for samples with and without LT-UHV treatment after the air transfer. Fig. 5 shows the peak analysis of Si 2p spectra shown in bottom panel of Fig. 4 indicating Si^{+4} to Si^{+3} ratio is 5.0 and 3.0 for samples with and without LT-UHV treatment respectively. These Si 2p results are consistent with the above results in Fig. 2, supporting that the amount of partially oxidized Si atoms (i.e., Si^{+3}) decreases, and the amount of Si^{+4} increases due to LT-UHV. In this Si 2p comparison, it is very relevant that the bulk crystal peaks overlap exactly between the different spectra. Therefore, small differences in the SiO_2 emission are

significant. The line shape of O 1s spectra (not shown) did not vary between the different samples, but the intensity of O 1s (i.e., peak area) increased 5% due to the LT-UHV oxidation.

Fig. 6 presents STM images together with the line profile before and after LT-UHV treatment. The surface is covered more uniformly by flat-top islands after LT-UHV as compared to the surface before LT-UHV. The STS results (Fig. 6) indicate that LT-UHV increases the surface band gap by decreasing the valence-band features (black peaks in Fig. 6) that can be associated with Si^{+3}, consistent with the above XPS results.

It is now possible to interconnect the surface science results to the observed decrease in D_{it}. Before that it might be useful to discuss a typical XPS resolution of 0.5–5 atomic % ($\sim10^{12}$ to 10^{13} atoms/cm^2) and the D_{it} values ($\sim10^{11}$ levels/eVcm^2). In other words, it is difficult to observe directly by XPS the Si atoms that have broken bonds (i.e., dangling bonds) if the dangling bond density is less than 10^{12} cm^{-2}. Here we also expected that the dangling bond would change the Si 2p binding energy via different electron distribution around the atom, as compared to the normal tetrahedral bonding configuration. Therefore, it is difficult to resolve a XPS spectral change, which would directly arise from the Si atoms causing the defect levels if the defect density is low. However, the spectral changes can be linked to the reduced D_{it} as follows. The partially oxidized areas (i.e., Si^{+1}-Si^{+3}) at SiO_2/Si can increase the number of unsaturated Si dangling bonds at the interface region, which often cause the defect levels in the Si band gap area. Thus, in the atomic environment around one Si dangling bond, there might be several Si atoms with the partial oxidation state, which cause a
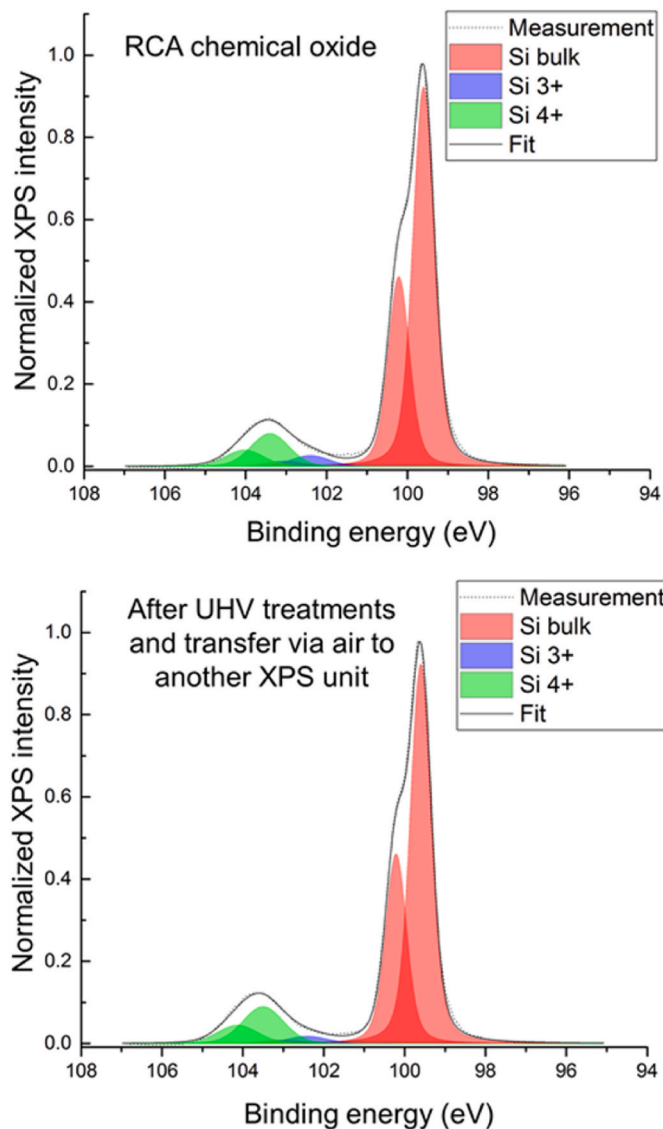
Fig. 5. Peak analysis of Si 2p spectra measured for samples with and without LT-UHV. The analysis indicate that Si^{4+}/Si^{3+} ratio has been increased after LT-UHV treatment compared to the sample without LT-UHV treatment.

resolvable difference in the XPS spectrum. In other words, the LT-UHV treatment can decrease the amount of oxygen-vacancy related defects [32,33] in the wet-chemically grown silicon oxide film.
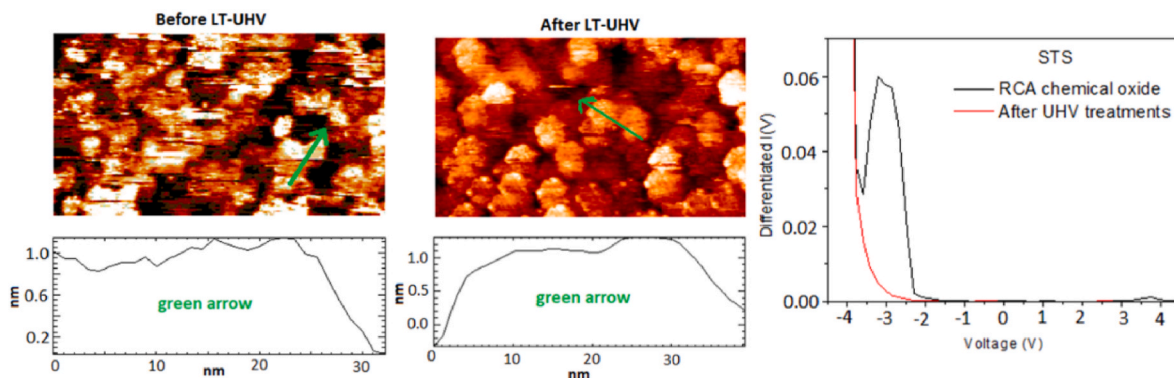
Because the SiO_2/Si interface has been one of the most studied material systems, many detailed investigations during several decades have improved our understanding of the formation and properties of SiO_2/Si (e.g., Refs. [32–36]). The different oxidation states of Si do not necessarily arise from the graded (or diffused) SiO_2/Si interface structure but can also arise from local areas with oxygen vacancies. However, the SiO_2/Si interface structure hardly is sharp concerning its chemical and physical properties. In contrast, the affected layer in the Si side can contain several atomic layers. The temperature during the oxidation or/and the post heating is known to enhance significantly the diffusion of Si and O elements across the interface. On the other hand, a graded oxygen concentration at the interface should enhance accommodation of the structural strain between Si and SiO_2, decreasing the strain-relaxation induced defect density.

In this work, we have used the relatively low temperatures to oxidize Si, and thus one crucial question is to which depth oxygen is able to diffuse at the low temperatures. Although the recent study [37] supports that the LT-UHV oxidation can have a significant effect, no TEM image was reported in that study. Therefore, we have prepared here a separate $Al_2O_3/SiO_2/Si$ sample for TEM (Sec. 2). The STEM images in Fig. 7 show that a significant Si oxidation appears already at the 200-L oxygen exposure at LT. Thickness of this oxidized layer is at least 1 nm, supporting the above results that the LT-UHV oxidation can modify the wet-chemically oxidized Si.

3.2. Instrumentation

The UHV technology has been so far utilized in specific industrial processes of the current semiconductor technology, particularly, in molecular-beam-epitaxy growth and UHV-based chemical vapor deposition of semiconductor device heterostructures [37–39]. Potential of UHV to develop various material systems and applications, including graphene and metal-semiconductor contacts, has been also demonstrated [e.g., Refs. [40–43]]. The benefit of UHV is obviously very clean environment for processing materials, which should naturally decrease contamination-induced point-defect densities for instance. On the other hand, the UHV technology is often considered a complex method. UHV has not been widely used in silicon industry although UHV-based CVD and rapid thermal annealing (UHV-RTA) instruments belong to an available arsenal of the commercial Si processing tools. To contribute to opening a different way for testing UHV benefits in the Si technology, we present one option in Fig. 8.

This UHV system includes a stainless steel (304) cylindrical chamber with diameter of 406 mm and total height of 443 mm. The main chamber height is 254 mm, and a long port is connected to it to insert the heating element stage (Fig. 8). Since the chamber is small, heating of the chamber walls due to large size of the heater element (compared to laboratory heating element for small samples) becomes an issue, in
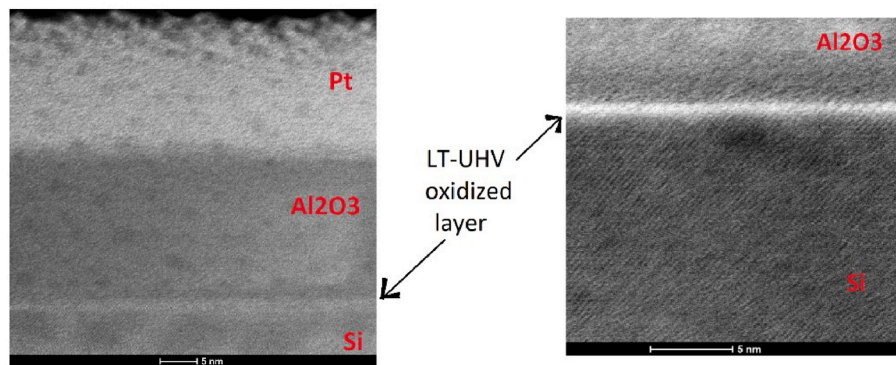

Fig. 6. STM images indicate that LT-UHV enhances the formation of flat top islands. Line profiles are taken along the green arrow. STS curves indicate that amount of surface phases of Si^{+2} or/and Si^{+3} with smaller band gap (i.e., black feature around −2 V and −3 V) decreases due to LT-UHV.

Fig. 7. STEM images $Al_2O_3/SiO_2/Si$ of which Si surface was pre-oxidized with the same LT-UHV parameters as described in Methods Section. The SiO_2 layer with the thickness of 1 nm is resolved. The Pt film was deposited on Al_2O_3 during lamella preparation process.
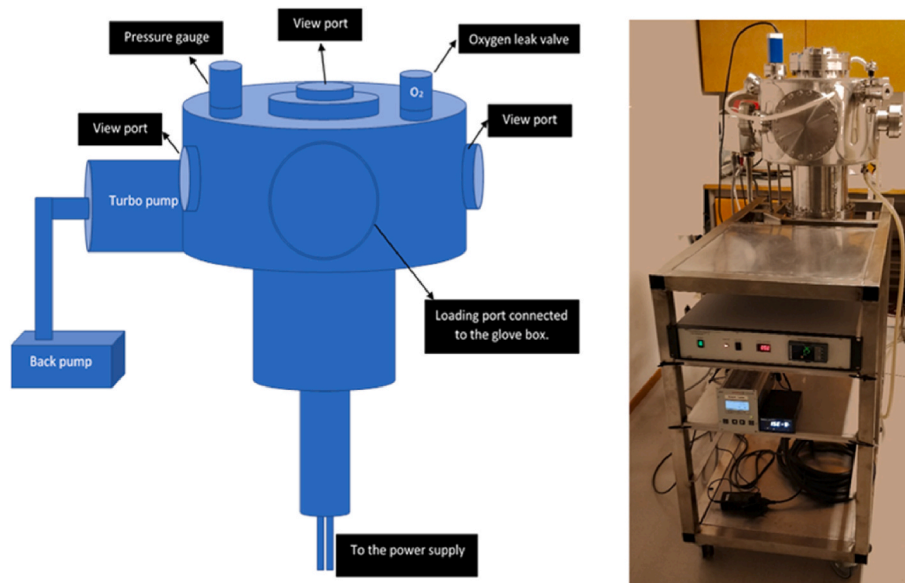

Fig. 8. (a) Scheme of the UHV system. (b) Picture of the instrument and its controllers.

particular, when elevated temperatures are used. Therefore, the chamber was designed with integrated water-cooling system, where the water circulates within chamber walls during heating and oxidation at flow rate of 4 l/min and temperature of water is 17 °C.

A cold cathode gauge is connected to the system to measure the vacuum and oxygen partial pressure during oxidation. Cold cathode gauge was chosen among the large variety of UHV and high vacuum (HV) gauges to satisfy the system and procedure requirements: to measure the vacuum down to 10^{-9} mbar. Also, the cold cathode gauge is not damaged when exposed to air while it is power on, in contrast to e.g., hot ion gauge where the gauge filament burns even at low vacuum levels.

An all-metal regulating leak valve connects the system to an oxygen cylinder through a DN16CF port, which is used for increasing oxygen partial pressure within the chamber when sample is heated. System is connected to a molecular turbo pump, which is connected to a rotary back pump. View ports window material is UV sapphire, which can work at temperatures as high as 450 °C.

Heating system is a solid silicon carbide heater element mounted on a manipulator with the possibility of adjusting operating height through a manually actuated bellows-sealed linear shift mechanism of 150 mm insertion/retraction. An Inconel cradle is connected to the manipulator on top of heater element with height adjustment of 25 mm to facilitate wafer mounting and unmounting. The heater element is mounted on a

DN200CF stainless steel flange and is inserted into the UHV chamber from bottom port so that the heater element is facing up. A combined temperature controller (suitable for K-type thermocouple) and DC power supply (96 V, 31 A) is connected to the heater element utilizing feedthroughs. Temperature of the wafer is measured with a K-type thermocouple mounted on the stage and it was calibrated utilizing a pyrometer with emissivity of 0.60.

The sample can be inserted into the chamber using top or side DN150/160CF compatible ports. An additional benefit of the system is that it provides the possibility to treat very small samples that are not suitable to be mounted on standard sample holders. These small samples can be put on the heater element utilizing a Si wafer template or molybdenum plate put on cradle.

The system is connected to a nitrogen venting line that is used to vent system. A nitrogen glove box or bag is connected to the port of which the sample is inserted into/taken out from the system to minimize the contamination of system and sample. A sealing system is inside the glove box for packaging samples in clean room bags.

This instrument was used to repeat the above described LT-UHV treatments. The obtained results are well consistent with the benefits described in Tables 1 and 2 The described instrument is scalable as heater elements for wafers larger than 4-inch are available. On the other hand, we admit that future development is needed to use the LT-UHV method to treat many wafers quickly for example for solar panels.
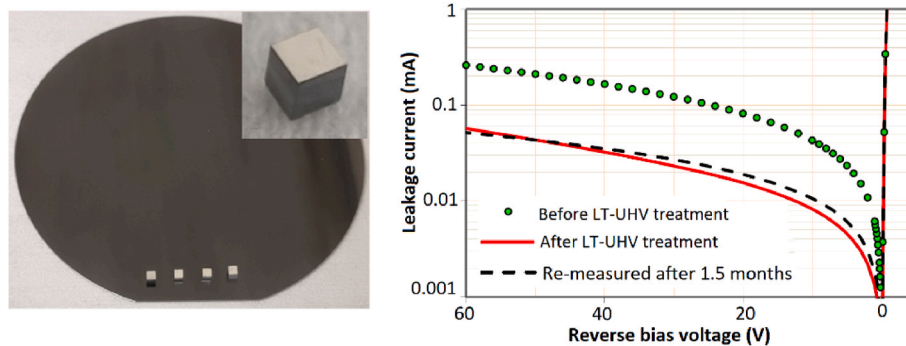
Fig. 9. Left: Photograph of four Si diodes on the top of 4-inch Si wafer, and zoom-in for one diode. Right: Leakage current of diode as a function of the reverse bias voltage before and after LT-UHV treatments. The measurement of LT-UHV treated diode was repeated after 1.5 months, which shows stability of the treatment effect.

Finally, the instrument was tested to perform the LT-UHV oxidation of separate diode components, of which native oxides at the sidewalls provide simultaneously a complementary SiO$_2$/Si system, as compared to the above wet-chemically grown SiO$_2$/Si. These cube-like components were put on the top of 4-inch Si wafer such that the face of another metal film (which covered the whole face) was in the contact with the template Si wafer. These diodes are thicker than the common wafers (Fig. 9), and therefore, the four sidewalls form a significant area, which is expected to affect the leakage current of diode at the reverse-bias voltages. The leakage current can arise from an increased thermal excitation of carriers via the band-gap defect levels at the sidewalls [44]. Furthermore, if the defect-level density is high, the levels near sidewalls might even cause a separate hopping channel which lies along the sidewalls parallel to the bulk p-n junction, which resembles the hopping channel of amorphous silicon due the gap levels.

Above we have seen that the LT-UHV oxidation of 200 L decreases D$_{it}$ of the wet chemically grown SiO$_2$/Si. Moreover, it can be also expected that the native SiO$_2$/Si includes initially a higher D$_{it}$ than the wet chemically grown material. Therefore, it is consistent that the LT-UHV decreases the leakage current at least by the factor of 5, as exemplified in Fig. 9.

4. Conclusions

We have demonstrated that a simple LT-UHV procedure is a potential method to develop further the current Si passivation method of the wet-chemical oxide growth of SiO$_2$ layer on Si. The LT-UHV heating and oxidation at 350 °C has been found to decrease D$_{it}$ and to increase Q$_{tot}$ as well as the carrier lifetime at Al$_2$O$_3$/SiO$_2$/p-Si interfaces, as compared to the state-of-the-art device interfaces without LT-UHV oxidation. XPS measurements show that the LT-UHV oxidation decreases the amount of the Si^{+3} sites and also the amount of carbon contamination, which can be linked to the found decrease in D$_{it}$. To contribute to lowering a step for testing UHV in the Si technology, we have built up and tested a simple UHV chamber instrument for LT-UHV of the 4-inch Si wafers. This instrument was also tested to modify the native oxides of SiO$_2$/Si at the sidewalls of separate Si diodes. The LT-UHV oxidation decreased the reverse-bias leakage current of diodes, which can be explained by a decreased D$_{it}$ at SiO$_2$/Si sidewalls.

CRediT authorship contribution statement

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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