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Shoot-through protection for an inverter consisting of the next-generation IGBTs with gate impedance reduction

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Abstract

Attention has been paid to the next-generation IGBT toward CMOS compatible wafer processes, which can be driven by a 5-V logic level due to its low threshold gate voltage. This low threshold voltage makes the so-called shoot-through fault severer. Even though the switching speed of the IGBT is intentionally reduced, the shoot-through fault can happen. This paper presents shoot-through protection for an inverter consisting of the next-generation IGBTs with gate impedance reduction. Theoretical analysis reveals the criterion of the gate impedance with taking parasitic parameters of the inverter into account.

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1. Introduction

Power semiconductor devices used in high-power conversion systems such as utility-grid and industrial applications always face a significantly long operating time and thus have to be highly reliable [1]. Attention has been paid to reliability-oriented issues of power semiconductor devices to prevent or predict their open- or short-circuit failures [2-6] including the so-called shoot-through fault [7-13].

Gate-drive circuits for insulated-gate bipolar transistors (IGBTs) usually provide a negative turn-off gate voltage to ensure the IGBTs against the shoot-through fault because the negative voltage not only increases the safety margin of gate voltage but also significantly reduces the reverse transfer capacitance C_{CG} of the IGBT [12]. Reduction in C_{CG} chokes a noise current path to the gate terminal [11].

Although the negative gate-voltage improves the reliability of IGBTs, a bipolar voltage source is necessary for the gate-drive circuit. This makes the circuit complex and brings a high manufacturing cost. A gate-drive circuit with a unipolar voltage source is cost-effective and easy to be integrated.

Microfabrication techniques for the next-generation IGBT toward CMOS compatible wafer processes with 3D scaling have been developed [14, 15]. This IGBT can be driven by a 5-V logic level with a scaling factor k of three [15], so that its gate-drive circuit can consist of a CMOS integrated circuit with the unipolar voltage source. It is, however, more sensitive to the noise voltage on its gate terminal because its threshold gate voltage is inversely proportional to the scaling factor. The shoot-through fault, therefore, will be severer.

The authors of this paper have investigated the relation between the shoot-through fault and parasitic parameters of an inverter [11], which indicates that not only junction capacitances of the IGBT but also stray inductances in the inverter have a strong influence on the criterion of the shoot-through fault. This also suggests that the fault can be more critical due to the existence of stray inductances.

This paper provides a theoretical analysis of the shoot-through fault with focusing on the gate impedance between the IGBT and its gate-drive circuit as well as on the switching speed of the IGBT.

2. Mechanism of shoot through in inverter

Fig. 1 shows an inverter leg consisting of high- and low-side IGBTs, Q_H and Q_L, including stray inductances. Turning on Q_H brings a high *dv/dt* waveform and then results in a surge voltage between the collector and emitter of Q_L, in which an amount of high-frequency displacement current flows into the gate through the reverse transfer capacitance C_{CG} and thus the gate voltage varies unless the gate impedance is zero. The gate voltage v_G may exceed its threshold

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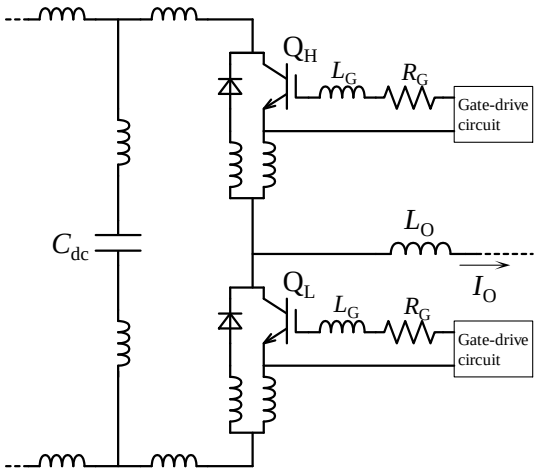
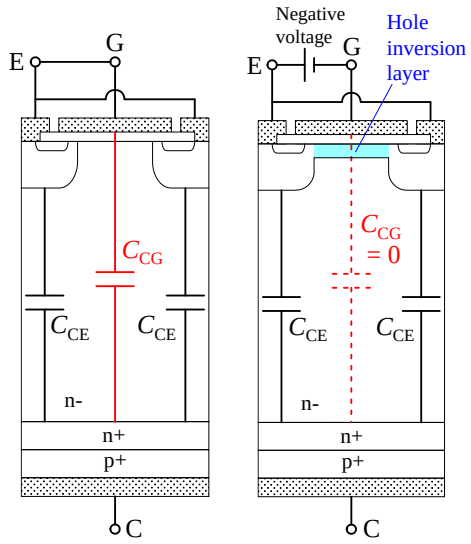


Fig.1 An inverter leg including stray inductances.



(a) V_{GE} = 0 V (b) V_{GE} < 0

Fig. 2 Device structure of an IGBT along with the gate voltage.

voltage and result in the shoot-through fault.

The ways to prevent the fault are classified into the followings:

- Reducing the reverse transfer capacitance C_{CG}.
- Reducing the surge voltage
- Reducing the gate impedance

The first one is achieved by a negative voltage as discussed in the next subsection. Since this paper focuses on the positive gate driving, it provides an intensive discussion on the others.

2.2 Gate shielding by a negative gate voltage

Fig. 2 shows the device structure of an IGBT along with the gate voltage. An amount of reverse transfer capacitance C_{CG} exists when the gate voltage is zero as shown in Fig. 2(a), whereas the negative gate voltage results in no net reverse transfer capacitance C_{CG} as shown in Fig. 2(b) because a hole inversion layer is formed between the N-base layer and gate oxide interface. It shields the reverse transfer capacitance C_{CG} from the gate terminal [12]. Thus, the negative gate voltage prevents the shoot-through fault.

Table I Circuit parameters of the inverter shown in Fig. 3.

DC-link voltage	V_{DC}	600 V
Stray inductance	L_{BUS}	200 nH
Junction capacitance of D_L	C_{AK}	390 pF
Output capacitance of Q_L	C_{CE}	55 pF
Reverse transfer capacitance of Q_L	C_{CG}	25 pF
Gate capacitance of Q_L	C_{GE}	4700 pF

2.3. Circuit modeling of inverter

Since the shoot-through fault happens between high- and low-side switches, this paper deals with a single inverter leg for circuit modeling.

Fig. 3 shows equivalent circuits of the inverter and its IGBTs and free-wheeling diodes (FWDs) for analysis, where the output current flows out of the low-side FWD Q_L in the initial state and then the high-side IGBT Q_H is going to turn on. Table I summarises circuit parameters for analysis and simulation, where a 1200-V Si-IGBT and a SiC Schottky barrier diode as the free-wheeling diode (FWD) are assumed. Note that the junction capacitance of the low-side FWD, Q_L is relatively large because this paper focuses on the analysis shortly after Q_L turning off and hence the voltage across the Q_L is much lower than the rated voltage. The dc-link capacitor has no influence on the circuit modeling except for its equivalent-series inductance, for its capacitance is much larger than junction capacitances of IGBTs and FWDs. The capacitor is, therefore, replaced by a voltage source V_{DC}. L_{BUS} is the sum of all the stray inductances in the loop that is formed from C_{dc}, the high-side arm, and the low-side arm. The output current I_O is replaced by a current source because the output inductor L_O is relatively large, through which no high-frequency current flows.

The high-side IGBT Q_H acts as a switch or a ramp voltage if its *dv/dt* is considered, whereas the high-side FWD D_H is open because no current flows into it. The low-side FWD is replaced by its junction capacitance C_{AK} after turning off.

Since the low-side IGBT Q_L is a turn-off state, it acts as a capacitor network consisting of its output

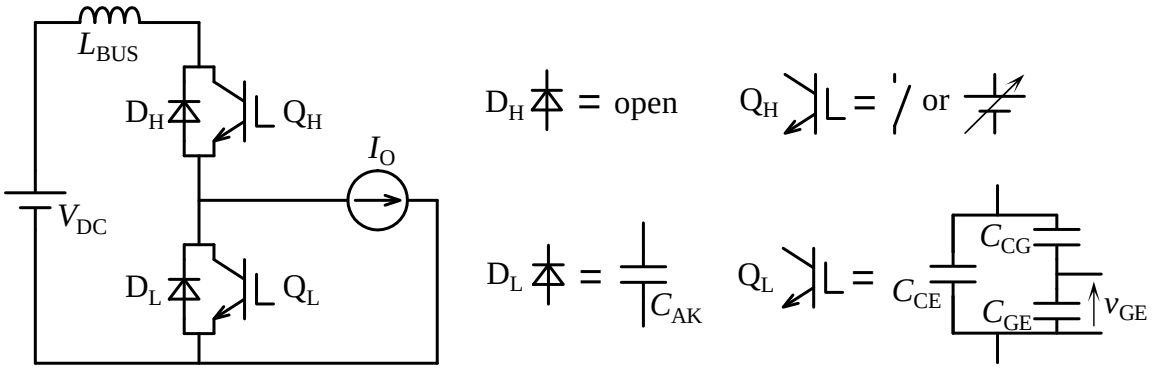


Fig. 3 Equivalent circuit of the inverter for analysis

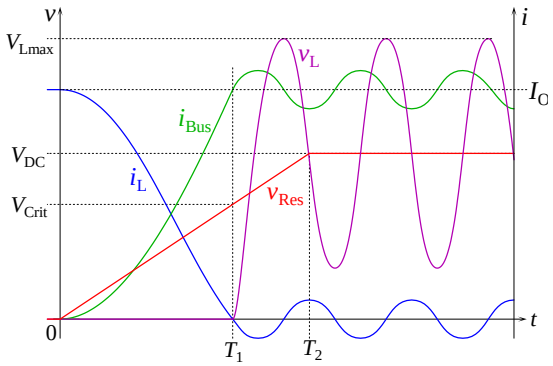
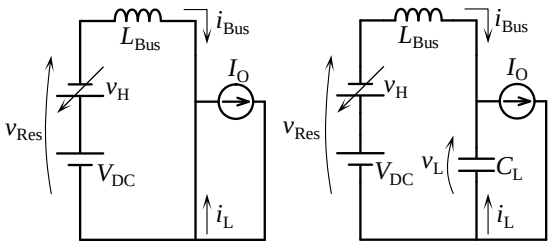


Fig. 4 Theoretical waveforms when focusing on switching speed.



(a) Mode 1 ($0 \le t \le T_1$) (b) Mode 2 ($T_1 < t$)

Fig. 5 Two modes of the equivalent circuit when focusing on switching speed.

capacitance C_{CE}, reverse transfer capacitance C_{CG}, and gate capacitance C_{GE}. This paper focuses on the gate-emitter voltage v_{GE} in the capacitor network because it is the indicator of the shoot-through fault.

3. Relation between switching speed *dv/dt* and shoot-through fault

3.1 Theoretical Analysis

The switching speed of the IGBT can be intentionally controlled by the gate resistance and is also a function of the temperature. It should be taken into account in either case.

This section introduces the ramp voltage to the high-side IGBT Q_H and analyses the surge voltage across the collector and emitter terminals of Q_L, v_L because the gate-emitter voltage is in proportion to the collector-emitter voltage if the gate terminal is open as follows:

$$v_{GE} = \frac{C_{CG}}{C_{GE}+C_{CG}} \times v_L \tag{1}$$

Fig. 4 illustrates theoretical waveforms. Fig. 5 shows two modes of the equivalent circuit; the low-side FWD D_L conducts in Mode 1, whereas D_L turns off and behaves as only the capacitance C_{AK} in parallel with Q_L in Mode 2, in which C_L is given by

$$C_L = C_{AK} + C_{CE} + \frac{C_{CG}C_{GE}}{C_{CG}+C_{GE}} \tag{2}$$

The voltage across Q_H, v_H is expressed by

$$v_H = \begin{cases} V_{DC} - kt & (0 \le t \le T_1) \\ 0 & (T_1 < t) \end{cases} \tag{3}$$

where k is a constant corresponding to *dv/dt* as follows:

$$\frac{dv_H}{dt} = -k \ \ (k > 0) \tag{4}$$

v_{Res} means the series connection of V_{DC} and v_H as follows:

$$v_{Res} = V_{DC} - v_H \tag{5}$$

Substituting (3) into (5) gives

$$v_{Res} = \begin{cases} kt & (0 \le t \le T_1) \\ V_{DC} & (T_1 < t) \end{cases} \tag{6}$$

In $0 \le t \le T_1$, the current flowing out of L_{BUS} into Q_H, i_{BUS} is given by

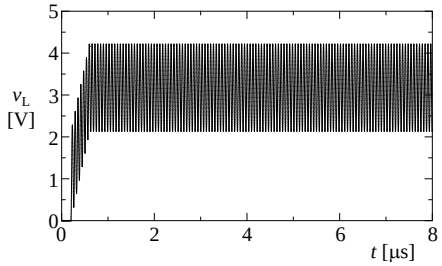
$$i_{BUS} = \frac{1}{L_{BUS}} \int_0^t v_{Res} dt \tag{7}$$

Substituting (6) into (7) results in

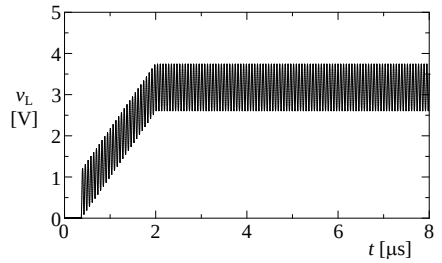
$$i_{BUS} = \frac{1}{L_{BUS}} \int_0^t kt dt = \frac{k}{2L_{BUS}} t^2 \tag{8}$$

T_1 is the time at which i_{BUS} equals I_O and the circuit mode is changed from Mode 1 to Mode 2, which is given by

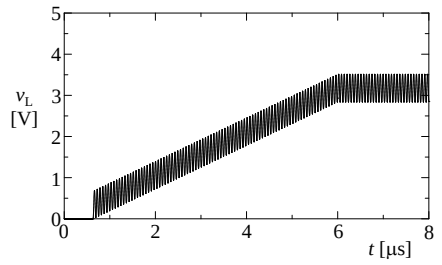
$$T_1 = \sqrt{\frac{2L_{BUS}I_O}{k}} \tag{9}$$



(a) $k = |dv/dt|$ = 1000 A/μs



(b) $k = |dv/dt|$ = 300 A/μs



(c) $k = |dv/dt|$ = 100 A/μs

Fig. 6 Simulated waveforms of the gate voltage v_{GE} with different k.

V_{crit} is the voltage at which D_L turns off and begin to become only the junction capacitance, which is given by

$$V_{\text{crit}} = v_{\text{Res}}(T_1) = kT_1 \quad (10)$$

Substituting (9) into (10) yields

$$V_{\text{crit}} = \sqrt{2L_{BUS}I_O k} \quad (11)$$

At $t = T_1$, the resonance circuit consisting of L_{BUS} and C_L is in parallel with V_{crit}. This means the resonance circuit is connected to a step voltage and resonance occurs. The amplitude of the resonance is equal to that of the step voltage, which is the same as V_{Crit}. After $t = T_1$, v_{Res} still increases until V_{DC} and the resonance maintains. Thus, the maximum voltage of v_L, V_{Lmax} is given by the following equation:

$$V_{Lmax} = V_{DC} + V_{Crit} = V_{DC} + \sqrt{2L_{Bus}I_O k} \quad (12)$$

Substituting (1) into (12) gives the maximum gate voltage V_{GEmax} as follows:

$$V_{GEmax} = \frac{C_{CG}}{C_{GE}+C_{CG}} \times \left(V_{DC} + \sqrt{2L_{Bus}I_O k}\right) \quad (13)$$

These equations suggest that reducing k, making the switching speed slow, reduces V_{GEmax}. Hence, the possibility of the shoot-through fault decreases. Even if k equals zero, V_{GEmax} cannot be reduced below the following:

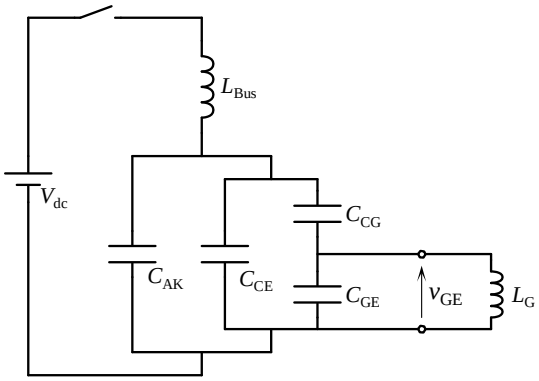


Fig. 7 Equivalent circuit along with gate inductance L_G for analysis

$$V_{GEmax}(k = 0) = \frac{C_{CG}}{C_{GE}+C_{CG}} \times V_{DC} \quad (14)$$

If this voltage exceeds the threshold gate voltage, reducing the switching speed k does not prevent the shoot through fault. As a result, reducing the switching speed helps prevent the shoot-through fault, but does not guarantee it.

3.2 Simulated results

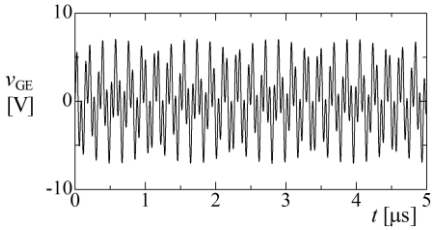
Fig. 6 shows simulated waveforms of v_L with three different switching speeds k, where a software package of "plecs" is used. The output current I_O 100 A. From Eq(14), $V_{GEmax}(k = 0)$ equals 3.2 V. The maximum voltages at k = 1000, 300, 100 A/μs are 4.2 V (133% of $V_{GEmax}(k = 0)$), 3.7 V (118%), and 3.5 V (111%), respectively, which agree with theoretical values obtained from Eq (13).

The voltages across the Q_L, v_L corresponding to the three switching speed are analogous to Fig. 5(a), (b), and (c), and their maximum voltage are 800 V (133% of V_{dc}), 707 V (118%), and 664 V (111%), respectively.

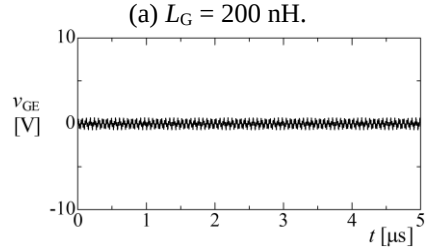
4. Protection against shoot-through fault with gate impedance reduction

4.1 Theoretical analysis

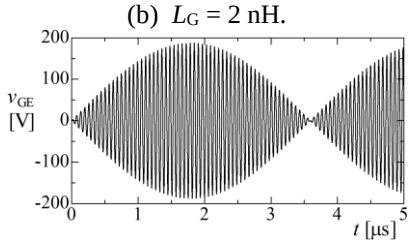
Even though the gate-drive circuit is directly connected to the gate terminal, there is an amount of stray inductance between the circuit and terminal. This is a constraint on reducing the gate impedance. This paper analyses the criterion of the gate inductance that protects the shoot-through fault.



(a) L_G = 200 nH.



(b) L_G = 2 nH.



(c) L_G = 20 nH, where resonance happens.

Fig. 8 Gate-emitter voltage v_{GE} with different gate inductances.

Fig. 7 shows the modelled circuit of the inverter leg for this analysis. The combination of the dc-capacitor voltage and Q_H is replaced by that of the dc voltage source and a switch when the switching speed is enough fast. The gate-drive circuit is replaced by a pure inductor because the it provides 0 V during the off state. The output current path is discarded because it has a large amount of inductance, through which no net high-frequency current flows. When the gate terminal is open-circuited, the gate voltage v_{GE} is given by [11]

$$v_{GE} = \frac{C_{GC}}{C_{GC}+C_{GE}} \times V_{dc}(1 - \cos \omega_{bus} t) \qquad (15)$$

where ω_{bus} is given by

$$\omega_{\mathrm{Bus}} = \frac{1}{\sqrt{L_{\mathrm{Bus}} C_{\mathrm{L}}}} \qquad (16)$$

The current flowing into C_{GE} has to commutate into the gate inductance L_G in order to reduce the peak voltage, which is achieved by satisfying the following equation:

$$\frac{1}{\omega_{\mathrm{bus}} C_{\mathrm{GE}}} \gg \omega_{\mathrm{bus}} L_{\mathrm{G}} \qquad (17)$$

Substituting (16) into (17) results in the requirement of L_G as follows:

$$L_G \ll L_{total} \times \frac{C_{\mathrm{L}}}{C_{\mathrm{GE}}} \qquad (18)$$

Note that L_G and C_{GE} form a resonant circuit, the resonant frequency of which is given by

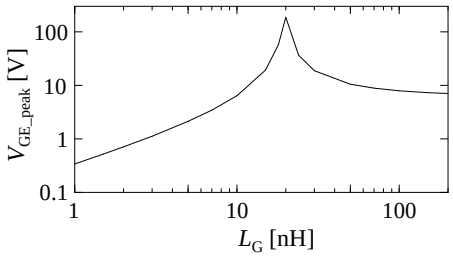


Fig. 9 Relation between the peak gate-emitter voltage V_{GE_peak} and gate inductance L_G.

$$\omega_{\mathrm{G}} = \frac{1}{\sqrt{L_{\mathrm{G}} C_{\mathrm{GE}}}} \qquad (19)$$

4.2 Simulated results

The resonant frequency comprising L_{bus} and C_L, $f_{bus} = \omega_{bus}/2\pi$ = 16.4 MHz.

Fig. 8 shows the gate-emitter voltage waveforms with different gate inductances. In Fig. 8(a), L_G = 200 nH does not satisfy Eq (18), where the peak gate voltage V_{GE_peak} is 7 V that is almost determined by Eq (15). In Fig. 8(b), L_G = 2 nH meets Eq (18), so that V_{GE_peak} is reduced to 0.7 V. In Fig. 8(c), L_G = 20 nH results in the resonance, i.e., ω_G equals ω_{bus}, and thus V_{GE_peak} greatly increases to 180 V. Note that this analysis gives the possible peak voltage even though some amount of gate resistance R_G exists.

Fig. 9 shows the relation between the gate inductance and peak gate voltage V_{GE_peak} obtained from simulation. As a result, the gate inductance L_G should be much lower than 20 nH to guarantee the IGBT not to accidently turn on.

5. Conclusion

This paper has presents shoot-through protection for an inverter consisting of the next-generation IGBTs that can be driven by a 5-V logic level. Theoretical analysis reveals that reducing the surge voltage by making the switching speed slow helps withstand the shoot-through fault but cannot always prevent it. Gate impedance reduction is mandatory to guarantee the shoot-through fault not to happen. Theoretical analysis also clarifies the criterion of the gate inductance to achieve the protection with considering parasitic parameters of the inverter.

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