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Title:
Reflected wave phenomenon in inverter-fed machines with fast-switching (high dv/dt) wide bandgap power converters
causes, consequences and solutions

Reflected Wave Phenomenon in Inverter-fed Machines with Fast-Switching (high dv/dt) Wide Bandgap Power Converters: Causes, Consequences and Solutions

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A thesis submitted to the University of Bristol in accordance with the requirements of the degree of Doctor of Philosophy in Electrical Engineering.

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June 2022

Abstract

Power density, efficiency and reliability are key design drivers and central concerns for adjustable speed drive systems in a plethora of applications including industrial automation and robotics, and transportation systems. The commercially available of Wide Bandgap (WBG) power semiconductors such as Silicon Carbide (SiC) MOSFETs with extremely fast switching speed are pushing the boundaries of power converter performance to meet the aggressive power density and efficiency targets (e.g., 25kW/kg, 99% +) for existing and emerging applications.

However, these steep voltage transients (high dv/dt) of SiC inverters are expected to accelerate the degradation of the connected motor stator winding insulation, which significantly affects the reliability and lifetime of the motor drive system. In a typical SiC-based cable-fed motor drive system, the fast-fronted Pulse-Width Modulation (PWM) voltage pulses generated by the SiC inverter make cables act like transmission lines, with waves travelling along the cables back and forth. Since the characteristic impedance of the motor is much higher than that of the cable in the motor drive system, the inverter PWM voltage pulses experience reflections at motor terminals, leading to excessive overvoltage oscillations that can be twice the inverter voltage. This phenomenon is known as the reflected wave phenomenon (RWP). The resultant overvoltage stress adversely affects the reliability and lifetime of the motor by accelerating the motor stator winding insulation ageing through the inception of partial discharges, progressively yielding to the degradation of motor winding insulation, while raising the Electromagnetic Interference (EMI) problems.

The aim of this PhD thesis is to investigate the RWP in SiC-based cable-fed motor drive systems and explore the overvoltage mitigation techniques without compromising the benefits of SiC switching devices. The RWP is systematically investigated in both the time domain and frequency domain, providing the foundation for developing the active waveform shaping techniques. The impact of parasitic of SiC switching devices on the motor terminal overvoltage due to the RWP in a three-phase motor drive system is investigated and experimentally verified. Moreover, two active waveform shaping techniques, i.e., the Quasi-Three-Level (Q3L) PWM scheme and the voltage slew-rate (dv/dt) profiling, are proposed to address the motor terminal overvoltage oscillations in SiC-based long cable-fed motor drive systems. The proposed active waveform shaping

techniques are supported by theoretical analysis and experimental verification. The essence of the overvoltage mitigation mechanism of the proposed active waveform shaping techniques is crystallized in both the time domain and frequency domain. The philosophy used here is addressing the motor terminal overvoltage oscillations at the source by actively mitigating the excitation source for the overvoltage oscillations. The theoretical and experimental results indicate that when the dwell time for the Q3L PWM scheme is set as $2t_p$ (t_p is the wave propagation time), the motor terminal overvoltage oscillations can be attenuated since there is no excitation source invoking the overvoltage oscillations. In addition, the proposed Q3L PWM using the SiC module-parallel inverter can extend the switching devices' current capacity. The proposed voltage slew rate (dv/dt) profiling is implemented on the SiC Auxiliary Resonant Commutated Pole Inverter (ARCPI) to verify its effectiveness. The theoretical analysis and experimental results show that the ARCPI can entirely mitigate the motor terminal overvoltage oscillations when the rise and fall times of the PWM voltage pulses are shaped as $4t_p$. Also, the voltage slew rate profiling inherits the advantages of the soft-switching inverter including high power efficiency and EMI performance.

Dedicated to my parents

Acknowledgements

I would like to thank and acknowledge the people who contributed to this research both directly and indirectly.

First and foremost, I would like to thank my supervisors, Prof. Xibo Yuan and Prof. Phil Mellor for their invaluable advice, guidance, and timely technical input. I could not have completed this work without their unwavering support. I greatly appreciate their contribution.

I would like to acknowledgement my PhD viva committee members: Prof. Andrew Forsyth and Dr Christian Klumpner, and Dr David Drury for their support, comments, and suggestions.

I would like to thank Dr. Mohamed Diab for his constant support, and technical discussion throughout the PhD work.

I would also like to thank the UK Research and Innovation (UKRI) and the University of Bristol for funding my PhD project.

I am grateful to all my colleagues and friends in the EEMG for their support and help, and to all my friends in Bristol whose help got me to the end of this arduous but enriching journey.

Special thanks are owed to my parents, my sister and my partner Pangya for their steadfast support, encouragement, and kindness.

Declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

SIGNED: ..... DATE:.....

Memorandum

The accompanying thesis "Reflected Wave Phenomenon in Inverter-fed Machines with Fast-Switching (high dv/dt) Converters: Causes, Consequences and Solutions" is based on work carried out by the author in the Department of Electrical and Electronic Engineering of the University of Bristol.

The main contributions claimed by the author are as follows:

1. Investigated the reflected wave phenomenon in SiC-based cable-fed motor drive system.

    1) Crystallized the underlying cause of motor terminal overvoltage oscillations in both the time domain and frequency domain, providing foundations for developing overvoltage mitigation techniques through active waveform shaping.
    2) Investigated the impact of switching devices' parasitic on motor terminal overvoltage. Systematically analysed and experimentally verified the switching commutation processes for a three-phase SiC-based cable-fed motor drive system, considering the impacts of parasitic elements of the switching devices and load current during the switching transitions.

2. Addressed the motor terminal overvoltage oscillations at the source by using the active waveform shaping technique, i.e., the quasi-three-level (Q3L) PWM scheme.

    1) Revealed the essence of the overvoltage mitigation mechanism of the Q3L PWM in both the time domain and frequency domain.
    2) Investigated the impact of the parasitic of switching devices of the Q3L PWM T-type inverter on the mitigation of motor terminal overvoltage oscillations.
    3) Proposed the Q3L PWM using the module-parallel inverter to mitigate the motor terminal overvoltage and extend the switching devices' current capacity.
    4) Experimental implemented the Q3L PWM scheme on a SiC-based T-type inverter and a SiC-based module-parallel inverter, respectively.

3. Addressed the motor terminal overvoltage oscillations at the source by using the active waveform shaping technique, i.e., soft-switching voltage slew rate (dv/dt) profiling, without sacrificing the benefits of SiC devices.

1) Proposed and derived the optimum rise and fall times of the PWM voltage pulses for entirely mitigating the motor terminal overvoltage.
2) Revealed the essence of the overvoltage mitigation mechanism of the voltage slew rate profiling in both the time domain and frequency domain.
3) Experimental implemented the voltage slew rate profiling concept with a soft-switching inverter, i.e., the SiC Auxiliary Resonant Commutated Pole Inverter (ARCPI).

Publications

Journal Articles

1. **W. Zhou**, M. Diab, X. Yuan and C. Wei, "Mitigation of Motor Overvoltage in SiC-Based Drives using Soft-Switching Voltage Slew-Rate (dv/dt) Profiling," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9612-9628, Aug. 2022, doi: 10.1109/TPEL.2022.3157395.

2. **W. Zhou**, M. Diab and X. Yuan, "Impact of Parasitic and Load Current on the Attenuation of Motor Terminal Overvoltage in SiC-Based Drives," *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 2229-2241, March-April 2022, doi: 10.1109/TIA.2022.3141703.

3. **W. Zhou** and X. Yuan, "Experimental Evaluation of SiC MOSFETs in Comparison to Si IGBTs in a Soft-Switching Converter," *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5108-5118, Sept.-Oct. 2020, doi: 10.1109/TIA.2020.2999440.

4. M. Diab, **W. Zhou**, C. Emersic, X. Yuan and I. Cotton, "Impact of PWM Voltage Waveforms on Magnet Wire Insulation Partial Discharge in SiC-Based Motor Drives," *IEEE Access*, vol. 9, pp. 156599-156612, 2021, doi: 10.1109/ACCESS.2021.3129266.

5. X. Yuan, J. Wang, I. Laird and **W. Zhou**, "Wide-Bandgap Device Enabled Multilevel Converters With Simplified Structures and Capacitor Voltage Balancing Capability," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 414-423, 2021, doi: 10.1109/OJPEL.2021.3094713.

Conference Proceedings

1. **W. Zhou**, M. Diab and X. Yuan, "Impact of Parasitics and Load Current on the Switching Transient Time and Motor Terminal Overvoltage in SiC-Based Drives," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 225-232, doi: 10.1109/ECCE44975.2020.9235417.

2. **W. Zhou**, M. Diab and X. Yuan, "Mitigation of Motor Overvoltage in SiC-Device-Based Drives using a Soft-Switching Inverter," in *2020 IEEE Energy Conversion*

Congress and Exposition (ECCE), 2020, pp. 662-669, doi: 10.1109/ECCE44975.2020.9236099.

3. **W. Zhou**, X. Yuan and I. Laird, "Performance Comparison of the Auxiliary Resonant Commutated Pole Inverter (ARCPI) using SiC MOSFETs or Si IGBTs," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 1981-1987, doi: 10.1109/ECCE.2019.8912876.

4. **W. Zhou**, X. Yuan and I. Laird, "Elimination of Overshoot and Oscillation in the Auxiliary Branch of a SiC Auxiliary Resonant Commutated Pole Inverter (ARCPI)," in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, 2019, pp. 1-7, doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8797163.

5. M. Diab, **W. Zhou** and X. Yuan, "Evaluation of Topologies and Active Control Methods for Overvoltage Mitigation in SiC-Based Motor Drives," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 4867-4873, doi: 10.1109/ECCE47101.2021.9595730.

6. M. Diab, **W. Zhou**, C. Emersic, X. Yuan and I. Cotton, "Impact of PWM Waveforms on Partial Discharge in SiC-Based Motor Drives," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1-7, doi: 10.1109/IECON48115.2021.9589431.

7. C. Wei, X. Yuan, **W. Zhou** and J. Wang, "Derivation of Flying-Type Multilevel Converter Topologies with a Voltage-Level Extension Method," in *2021 IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia)*, 2021, pp. 688-695, doi: 10.1109/ECCE-Asia49820.2021.9479046.

8. J. Wang, I. Laird, X. Yuan and **W. Zhou**, "A 1.2 kV 100 kW Four-level ANPC Inverter with SiC Power Modules and Capacitor Voltage Balance for EV Traction Applications," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5202-5209, doi: 10.1109/ECCE47101.2021.9595038.

9. J. Wang, C. Wei, **W. Zhou** and X. Yuan, "Capacitor Voltage Balancing Algorithm with Redundant Level Modulation for a Five Level Converter with Reduced Device Count," in *2020 IEEE 9th International Power Electronics and Motion*

Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 1758-1764, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367875.

10. X. Yuan, C. Wei, **W. Zhou** and G. Wang, "A Novel Five-Level Converter for Medium-Voltage Power Conversion Systems," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, 2019, pp. 4953-4958, doi: 10.1109/IECON.2019.8927260.

Other Publications

1. **W. Zhou**, M. Diab and X. Yuan, "Comparison of Motor Neutral Point Overvoltage Oscillation in SiC-Based Adjustable Speed Drives using Two-Level and Three-Level Inverters," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022. (Accepted)

2. **W. Zhou**, M. Diab and X. Yuan, "Mitigation of Motor Overvoltage and Extending Switching Devices' Current Capacity with Module Parallel Power Converter in SiC-Based Adjustable Speed Drives," (in preparation)

3. **W. Zhou**, M. Diab and X. Yuan, "Evaluation of Active Control Methods for Mitigation of Antiresonance Overvoltage Phenomenon in SiC-Based Motor Drives," (in preparation)

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A	Voltage pulse amplitude
C_{ds}	Drain-source capacitance
C_{dg}	Drain-gate capacitance
C_{gs}	Gate-source capacitance
C_c	Cable per unit length capacitance
C_{oss}	Output capacitance
c_n, c_{n1}, c_{n2}	Fourier series coefficient
Γ_m	Reflection coefficient at the motor terminals
Γ_s	Reflection coefficient at the power inverter side
D	Duty ratio
f_{rwp}	Oscillation frequency
f_{osc}	Anti-resonance frequency
L_c	cable per unit length inductance
L_r	Resonant inductance
L_f	Filter inductance
i_A, i_B, i_C	Phase current
i_{Lr}	Resonant current
i_{phase}	Inverter output current
I_{load}	Load current

ω	Angular frequency
τ	Pulse width
t_{dead}	Deadtime
t_f, t_{fall}	Fall time
t_p	Propagation time
t_r	Rise time
t_{ramp}	Ramp up time
v	Wave propagation velocity
V_{AB}	Line voltage between phase A and B
V_{AB_inv}	Line voltage between phase A and B for inverter
V_{AB_laod}	Line voltage between phase A and B for load
V_{AN}, V_{BN}	Output voltage for phase A and B
V_{dc}	dc-link voltage
V_s, V_{s1}, V_{s2}	Inverter output voltage
V_m, V_{m1}, V_{m2}	Motor terminal voltage
Z_c	Cable characteristic impedance
Z_{cm}	Common mode impedance
Z_m	Motor characteristic impedance
Z_s	Inverter characteristic impedance

List of Abbreviations and Acronyms

AC	Alternating Current
ARCPI	Auxiliary Resonant Commutated Pole Inverter
CM	Common Mode
DC	Direct Current
DM	Differential Mode
DPT	Double Pulse Test
EMI	Electromagnetic Interference
HVDC	High-Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistors
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PD	Partial Discharge
PDIV	Partial Discharge Inception Voltage
PWM	Pulse-Width Modulation
Q3L	Quasi-Three-Level
RWP	Reflected Wave Phenomenon
SiC	Silicon Carbide
VSI	Voltage Source Inverter
WBG	Wide Bandgap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 Background and Motivation

Power electronics converters are core elements in a plethora of applications including industrial automation and robotics [1], transportation systems [2], [3], and renewable energy [4], where they transform the electrical power, i.e., voltages and currents, from an available form to the desired form in a highly efficient and controllable manner. They are one of the critical enabling technologies for the electrification of automotive [5], railway [6], aerospace [7], and marine propulsion [8], and open the way for carbon footprint reduction, creating low emission and environment friendly transportation systems with high efficiency, flexible and smart control [9]. Furthermore, many emerging applications such as renewable energy [10], i.e., wind [11], solar [12], and tidal power generators [13], would not be possible without power electronics converters. In a nutshell, power electronics converters deeply permeate a huge range of industrial sectors, promoting remarkable technological progress as well as offering a green and sustainable development [14]–[17].

Power semiconductor devices, especially power switching devices, are at the heart of power converters to handle the electrical power conversion [18], [19]. Figure 1.1 shows the circuit diagram of a typical two-level three-phase Voltage Source Inverter (VSI) for the Direct Current (DC) to Alternating Current (AC) power conversion, where it consists of six switching devices [20]. These switching devices in the power inverter are operated in either the conduction state (on) or blocking state (off) to generate the required output voltages and currents. Since the switching devices have very low on-state and high off-state resistance [21], the main power loss of the VSI comes from the switching transients, which is known as the switching loss [22]. This can be explained by Figure 1.2 showing the voltage and current across the switching device in the VSI [23]. As can be noticed, the switching loss is determined by the time spend at switching transitions, where faster switching speed allows the switching loss reduction and power density improvement for the power inverter [24].

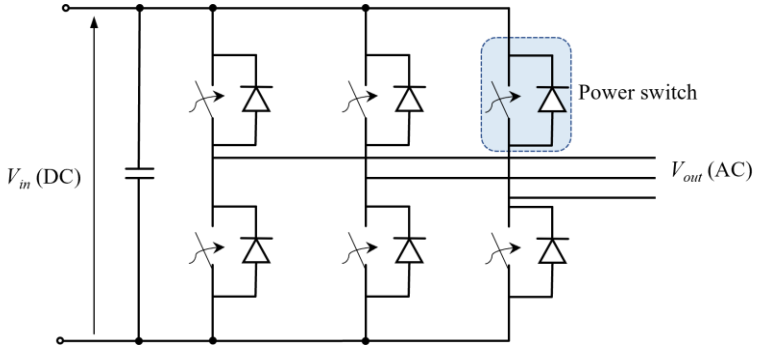


Figure 1.1 A two-level three-phase VSI.

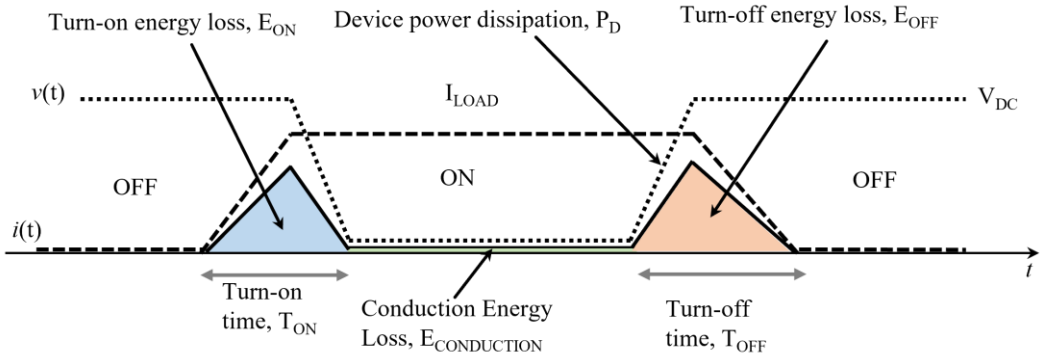


Figure 1.2 Voltage and current waveform of the switching device in a VSI during the switching transitions [23].

The commercial availability of fast-switching speed Wide-Bandgap (WBG) material based power semiconductor devices such as Silicon Carbide (SiC) Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) are pushing the boundaries of power converter performance to meet the aggressive power density and efficiency targets for existing and emerging applications [14]. WBG devices are considered to be the game-changing technologies, strongly contributing to all sectors of low-carbon industry, advancing transformative technological breakthorugh in highly compact and efficent power converter systems [25]. Compared with the conventional Silicon (Si) based switching devices, WBG devices are capable of switching at faster switching speeds, withstanding higher voltage level and operating at higher temperature [26]. Faster switching speed enables the switching loss reduction at a given switching frequencies which can reduce the cooling requirement or alternatively allows power converters operate at higher switching frequencies while maintaining high efficiency which can reduce the filter size [27]. Due to the reduction of passive components, the system's power density can be significantly improved. [28]. In addtion, the elavated temperature capabilities of WBG devices enable

the reduction of coolling requirement for power converters as well as working in harsh enviroments [29].

Though WBG power semiconductor switching devices offer an abundance of benefits, the fast-switching speed (high dv/dt) of WBG devices is expected to bring about a set of challenges for both the inverter and the connected electric motor in inverter-fed motor drive systems [14]. One of the serious issues is the motor overvoltage oscillations due to the Reflected Wave Phenomenon (RWP) caused by the high dv/dt and the impedance mismatch in the motor drive system [30]. In a typical WBG inverter-fed motor drive system, the fast-switched Pulse-Width Modulation (PWM) voltage pulses make power cables act like transmission lines [31]. Since the motor impedance is usually several times higher than the cable's, the inverter voltage pulses experience back and forth voltage reflections across the cables [32]. This results in overvoltage oscillations at motor terminals that can be twice the inverter voltage, as shown in Figure 1.3 [33].

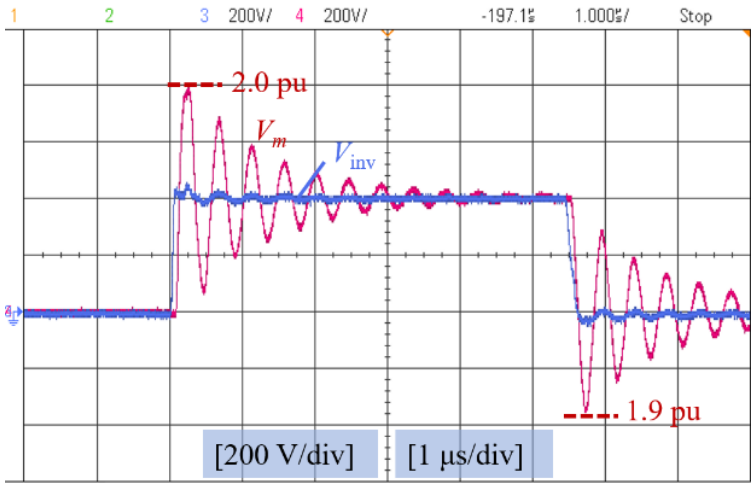


Figure 1.3 Voltages measured at the inverter side V_{inv} and motor terminals V_m when the motor is supplied by the fast-switching SiC inverter in a cable-fed motor drive system [33].

It is well established in the literature that fast-switched inverter voltage pulses result in the non-uniform voltage distribution within the motor stator winding turns with peak voltage stress across the first few turns close to the motor terminals [34]–[36]. This overstress is further exacerbated when long power cables are used to connect the inverter to the motor due to the RWP [37]. The resultant overvoltage stress across motor stator winding adversely affects the motor lifetime by accelerating the winding insulation aging through the inception of Partial Discharges (PDs) that progressively yield to the degradation and local heating of organic coatings of motor coils, which significantly affects the reliability

of the motor drive system [38]–[41]. Since PDs are frequency dependent, the occurrence of PD would increase with switching frequency [38]. According to an industrial survey, the additional voltage stresses at the motor stator windings in conventional Si based motor drive system accounted for 30%-40% of induction motor breakdown [42]. With the adoption of the fast-switching speed, high frequency WBG power inverter in motor drive systems, the motor winding insulation breakdown is predicted to increase significantly, which dramatically reduces the reliability and lifetime of the motor drive systems. In addition, the overvoltage oscillations due to the RWP and electromagnetic emissions due to the PDs further deteriorate the Electromagnetic Interference (EMI) performance which cannot satisfy the stringent requirement of many applications such as defence and aerospace [43], [44].

The above issues associated with the RWP due to the high dv/dt may hinder the application of WBG devices in motor drive systems. Therefore, it is necessary to devote more efforts to investigate the RWP in WBG inverter cable-fed motor drive system and explore potential mitigation techniques to effectively utilise WBG devices.

1.2 Research Objectives

The main goal of this PhD thesis is to investigate in-detail the RWP as well as to explore motor terminal overvoltage mitigation techniques without compromising the benefits of WBG devices in cable-fed motors with fast-switching SiC inverters. The research consists of both theoretical analysis and detailed experimental verification, which is focussed around four research objectives:

Research Objective 1: Gain deep understanding of the RWP and crystallize the underlying cause of motor terminal overvoltage oscillations in cable-fed motors using fast-switching SiC inverters, providing the foundation for developing overvoltage mitigation techniques through active waveform shaping.

RO 1.1 Investigate the RWP in time domain using a bounced diagram to visually illustrate the voltage reflection process in cable-fed motor drive systems, providing the foundation for developing active waveform shaping techniques to address the motor terminal overvoltage oscillations.

RO 1.2 Analyse the RWP in frequency domain to identify the motor terminal overvoltage oscillation frequency in cable-fed motor drive systems, providing the

foundation for revealing the overvoltage mitigation mechanism of the proposed active waveform shaping techniques.

RO 1.3 Assess how the motor terminal voltage is affected by the cable length and rise/fall times of the inverter voltage through simulation study.

Research Objective 2: Investigate the impact of parasitic capacitance of switching devices on motor terminal overvoltage in cable-fed motors using SiC inverters.

RO 2.1 Systematically analyse the switching commutation processes for a three-phase SiC based motor drive system, considering the impacts of parasitic elements of the switching devices and load current during the switching transitions.

RO 2.2 Experimental verification of the analysis.

Research Objective 3: Address the motor terminal overvoltage oscillations at the source by using the active waveform shaping technique, i.e., quasi-three-level (Q3L) PWM scheme.

RO 3.1 Reveal the essence of the overvoltage mitigation mechanism of the Q3L PWM in both the time domain and frequency domain.

RO 3.2 Investigate the impact of the parasitic capacitance of switching devices on the mitigation of motor terminal overvoltage oscillations using the Q3L PWM T-type inverter.

RO 3.3 Develop the Q3L PWM scheme using the SiC module-parallel inverter to mitigate the motor terminal overvoltage and extend the device current capacity.

RO 3.4 Experimental verification of the Q3L PWM scheme using SiC T-type inverter and SiC module-parallel inverter.

Research Objective 4: Address the motor terminal overvoltage oscillations at source using the active waveform shaping technique, i.e., soft-switching voltage slew rate (dv/dt) profiling without sacrificing the benefits of SiC devices.

RO 4.1 Derive the optimum rise and fall times for entirely mitigation of the motor terminal overvoltage.

RO 4.2 Reveal the essence of the overvoltage mitigation mechanism of the proposed slew rate profiling in both time domain and frequency domain.

RO 4.3 Experimental demonstration of the slew rate profiling concept with a SiC soft-switching inverter, i.e., the Auxiliary Resonant Commutated Pole Inverter (ARCPI).

1.3 Thesis Outline

This thesis consists of seven chapters. Following this introduction chapter (Chapter 1), **Chapter 2** presents a review of existing literatures relating to the PhD work. WBG power switching devices and their application in adjustable speed drive system are briefly introduced. The issues associated with the high dv/dt on the motors in WBG inverter-fed motor drive systems, and existing mitigation methods to address the RWP are described in this chapter. Moreover, the limitations of existing literature and research opportunities are summarised and discussed.

Chapter 3 investigates the RWP in both time domain and frequency, as well as assesses how the motor terminal voltage is affected by the cable length and rise/fall times of the inverter voltage through simulation study. This chapter is the foundation for developing active waveform shaping techniques including the Q3L PWM and the voltage slew rate (dv/dt) profiling to mitigate motor terminal overvoltage oscillations, as proposed in Chapters 5 and 6.

Chapter 4 investigates the motor terminal overvoltage oscillations in a three-phase motor drive system, considering the impacts of parasitic elements of the switching devices and load current during the switching transitions. Also, the analysis is experimentally verified in this chapter.

Chapter 5 develops the active waveform shaping technique, i.e., Q3L PWM scheme. The essence of overvoltage mitigation mechanism of the Q3L PWM scheme is crystallized in both the time domain and frequency domain. The impact of parasitic capacitance of switching device in SiC T-type inverter on the motor terminal overvoltage mitigation is analysed and experimentally verified. Furthermore, the Q3L PWM using module-parallel inverter is proposed to mitigate the motor terminal overvoltage as well as extend the switching devices current capacity. The SiC T-type inverter and the SiC module-parallel inverter are built to experimentally implement the Q3L PWM scheme.

Chapter 6 proposes the active waveform shaping technique, i.e., the voltage slew rate (dv/dt) profiling to address the motor terminal overvoltage. The essence of overvoltage mitigation mechanism of the voltage slew rate profiling is crystallized in both the time domain and frequency domain. The philosophy used here is addressing the motor terminal overvoltage oscillations at the source by actively mitigating the excitation source for the motor terminal overvoltage oscillations. The SiC ARCPI is used as an example of the soft-switching inverter to experimentally verify the effectiveness of the proposed approach.

Chapter 7 concludes the main findings of this PhD work and presents possible future research topics.

Chapter 2

Literature Review

2.1 Introduction

WBG devices due to their beneficial attributes such as the fast-switching speed have been widely adopted in a plethora of applications, offering transformative technological breakthrough in power electronics and adjustable speed drives [45]–[47]. However, the fast-switching speed (high dv/dt) of WBG devices is expected to result in excessive voltage stress on the connected motor stator windings due to the RWP, accelerating the degradation of motor windings insulation and causing premature failure of the motor drive system [9], [14], [48].

This chapter presents a review of existing literatures relating to the tittle of this PhD work. WBG power switching devices, i.e., SiC MOSFETs, and their application in adjustable speed drive system are briefly described. The issues associated with the high dv/dt of switching devices on the motors in inverter-fed motor drive systems, and existing mitigation methods including the passive and active approaches to address the RWP are presented in this chapter. Also, limitations of existing literature and research opportunities are summarised.

2.2 WBG Semiconductor Power Devices

2.2.1 Overview

In the past 60+ years, the continued rapid development of power electronics technology is driven by the advent of new generation power semiconductor devices [49], as demonstrated in Figure 2.1 [50], [51]. The invention of thyristor in 1957 elicited the deployment of High-Voltage Direct Current (HVDC) systems [52], the advent of Si based MOSFETs and Insulated-Gate Bipolar Transistors (IGBTs) in 1980s led to the PWM converters, advancing development of the modern adjustable speed drives and smart grid [53]–[59]. With the relentless research for more than 40 years, the conventional Si power semiconductor switching devices have become mature and are reaching their material performance limits [60]–[65].

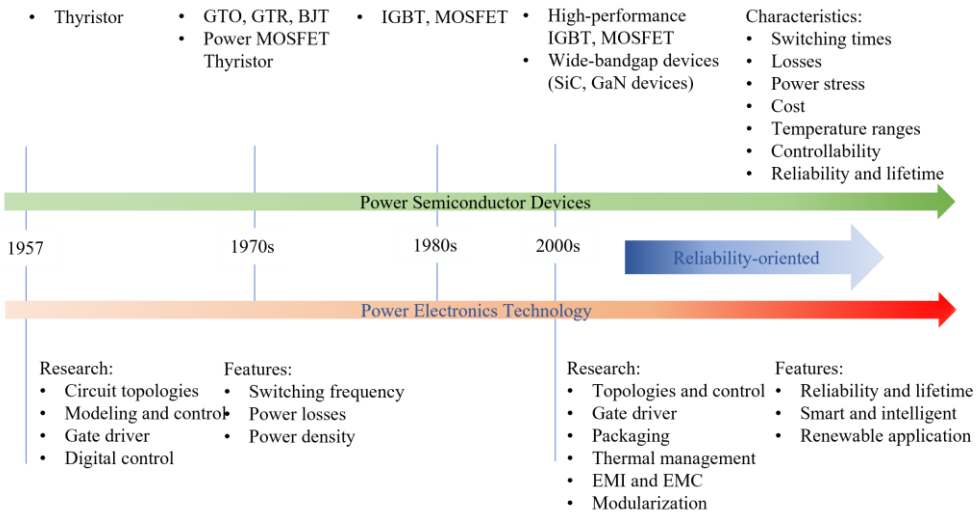


Figure 2.1 Development of power electronics and power electronics technology [50], [51].

The commercial availability of WBG materials based power semiconductor devices such as SiC MOSFETs is advancing transformative technological breakthrough in power electronics [66], [67]. WBG devices are considered to be the game-changing technologies, they are pushing the boundaries beyond the conventional Si based devices limits in power and switching frequency making it possible to dramatically increase the power density and efficiency for existing and emerging applications [14]. Compared with Si based switching devices, SiC MOSFETs can operate at faster switching speeds [68]–[70], higher voltage levels [67], [71], [72], and higher operating termperatues [73]–[75]. These enhanced performance of SiC MOSFETs are due to the superior material characteristics, as given in Table 2.1 [14], [61], [76], [77].

Table 2.1 The properties of Si and SiC material [14], [61], [76], [77].

	Si	**4H-SiC**	**Property**
Energy bandgap E_g	1.12 eV	3.26 eV	Operating temperature
Breakdown electric field strength E_{bk}	0.25 MV/cm	2.2 MV/cm	Breakdown voltage ON-resistance
Saturation Velocity V_s	1.0×10^7 cm/s	2.7×10^7 cm/s	Switching speed

Figure 2.2 compares the voltage and current waveforms of the conventional Si IGBT and SiC MOSFET at the turn-OFF switching transient measured in a double pulse test (DPT) experiment [78]. As shown, the switching speed of SiC MOSFET is about 10 times faster than that of Si IGBT, where the turn-OFF times of Si IGBT and SiC MOSFETs are about

500ns and 50ns, resepectively. Note that the switching speed at the turn-ON switching transient of SiC MOSFETs is much faster than Si IGBTs as well [27]. Since the power loss of the converter is mainly from the switching loss [79], the fast switching speed of SiC MOSFETs singnificantly reduces the switching loss and improves the efficiency of the power converters for a given switching frequency [80], as evidenced in Figure 2.3 [81]. This allows the reduction of cooling requirement and hence improve the power density of the power converter [82].

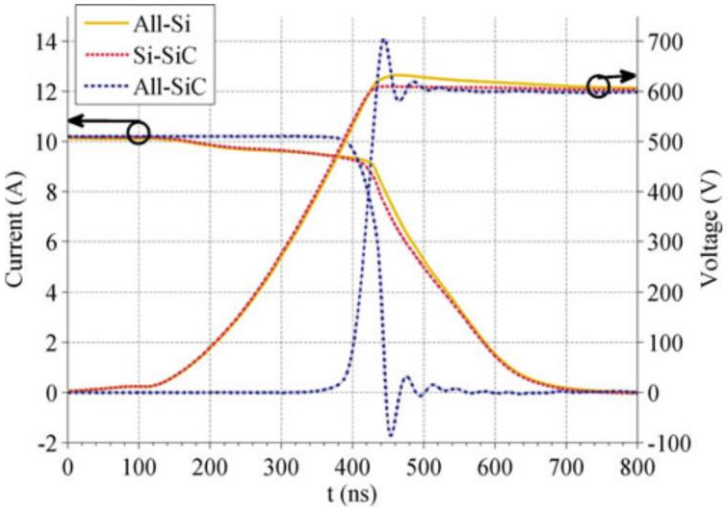


Figure 2.2 Comparison of the voltage and current waveform at the turn-OFF transient of SiC, Si-SiC and Si measured in a DPT experiment. The dc-link voltage is 600V and load current is 10A. All-Si represents Si IGBT and Si diode (Infineon IKW15T120, "IGBT3" and "EmCon HE" device generations), Si-SiC represents Si IGBT (IKW15T120) and SiC Schottky diode (SemiSouth SDA10S120) combination, All-SiC represents SiC MOSFET (Cree CMF20120D) and SiC Schottky diode (SemiSouth SDA10S120) combination [78].

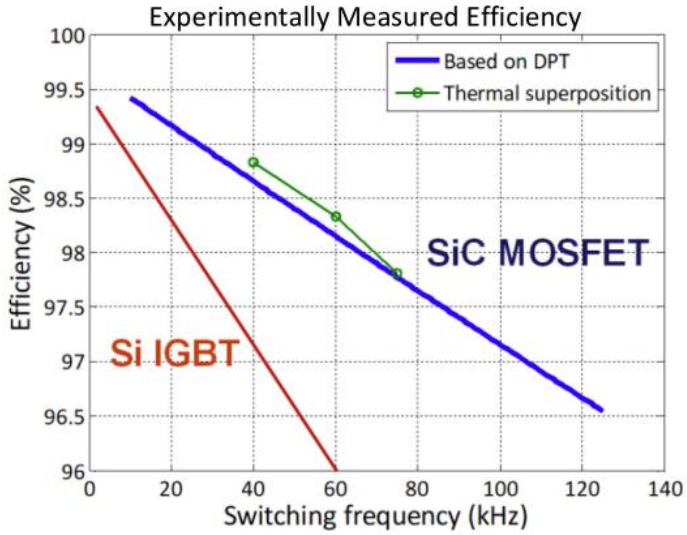


Figure 2.3 Efficiency comparison of the power converter using Si IGBT and SiC MOSFET at different switching frequency [81].

On the other hand, referring to Figure 2.3, with the switching loss reduction, the power converter can work at higher switching frequencies while maintaining the high efficiency. This can singinicantly shrink the size and reduce the weight of power converter as a result of the reduction of passive components [83], [84].

Furthermore, when the high frequency power converter is used to drive electric motors, several benefits can be achieved for the motor drive system [9], [14], [85]. For example, the increased switching frequeny enables higher control bandwidth and lower torque ripple, compared with Si counterpart. The increased switching frequency of the power converter leads to the reduction in current and voltage ripple [86], hence reduces the associated power loss due to the current ripple for the motors.

In terms of thermal performance, most of the commercial Si IGBTs operte below 150°C due to the limitation of material characteristics, while SiC MOSFETs can operate up to 250 °C or even high with the development of packaging techniques [14], [87], [88]. The elavated temperature capabilities of SiC MOSFETs enable the reduction of cooling requirement for power converters as well as working in harsh enviroments [89], [90].

2.2.2 Applications in Adjustable Speed Drive Systems

With relentless research in last 20 years, WBG power semiconductor switching devices have shown the technological readiness and are becoming the devices of choice to replace their Si predecessors in a growing number of power converters used to control electric motors in adjustable speed drive systems [14].

Mitsubishi Electric released the world's first all SiC 1.5kV dc, 180 kW tracton inverter in 2013, as shown in Figure 2.4 [91]. Mitsubishi claimed that compared with the Mitsubishi Electric's conventional the equivalently power-rating inverter system incorporating conventional Si IGBTs, the SiC power converter achieved about 55% reduction in switching loss.

In 2014, Toyota and Denso developed the SiC based power converter for use in automotive power control units in hybrid vehicles, as shown in Figure **2.5** [92]. Refering to Figure **2.5**, Compared to the conventional Si based power converter, the SiC based power control unit reduces the volume by 40% [92].

Figure 2.4 SiC-based traction inverter developed by Mitsubishia in 2013 [91].

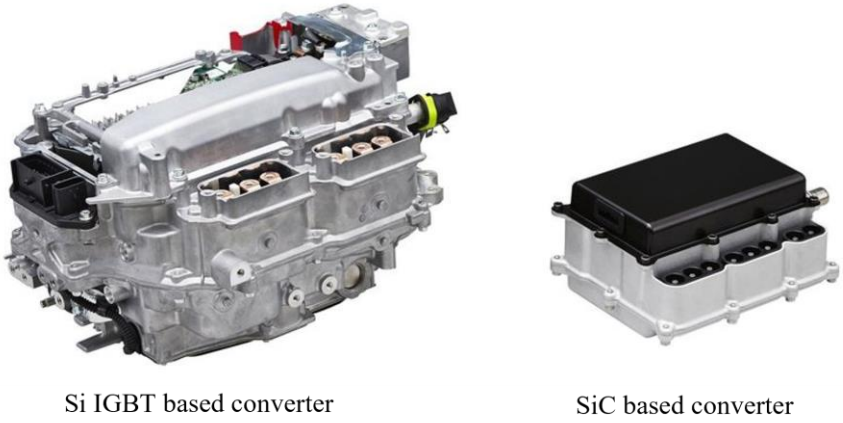


Figure 2.5 Inverter developed by Toyota for use in PCU in 2014 [92].

In 2018, Tesla used SiC MOSFETs in its Model 3 power converter for the motor drive system leading to more than 50% overall weight reduction when compared with conventional Si based power converter [93]. In addtion, the performance advantages of WBG power converter such as high-power density and low power loss, make it possible to integrate the power converter inside the motor housing, as shown in Figure 2.6, allowing further reductions in the cost, size, and improvements in fault tolerance of the motor drive system [93].

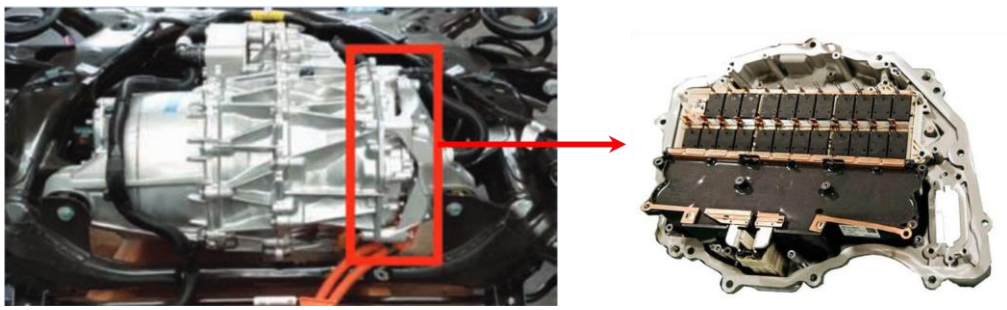


Figure 2.6 SiC Inverter developed by Tesla in 2018 [93].

In addition to the advantage of the fast-switching speed, SiC power converters benefit from the high operating temperature attribute of SiC MOSFETs [25], [94], [95]. Figure 2.7 shows the power converter prototype using Si IGBTs and SiC MOSFETs for hybrid-electric construction vehicles developed by John Deere in 2019 [96]. It is worth noting that the SiC power converter can operate at high temperature where the coolant temperature for SiC power converter can be 115°C due to the advanced internal cooling and packaging techniques which allows for full-power capabilities using engine coolant on even the hottest days. Referring to Figure 2.7, the size of power converter is reduced significantly when using SiC MOSFETs, where the power density for Si and SiC power converter are 11kW/L and 43kW/L, respectively.

Figure 2.7 John Deere 200 kW inverter prototypes [96].

Indeed, WBG power semiconductor devices are unfolding the technology revolution in inverter-fed motor drive systems. While the adoption of SiC power devices significantly improves the performance of power converters, the fast-switching speeds and high switching frequencies, resulting in several design challenges and technological issues, which will be described in next section.

2.3 Impact of the Fast-Switching WBG Converter on the Connected Motors in Adjustable Speed Drives

In addition to the design challenges for the converter itself, the fast-switching speed WBG converter is expected to significantly affect the reliability and lifetime of the connected electric motor in WBG based cable-fed motor drive systems [14]. Figure 2.8 summarises the main issues and challenges for motors when using the fast-switching speed WBG semiconductor in the inverter-fed motor drive systems.

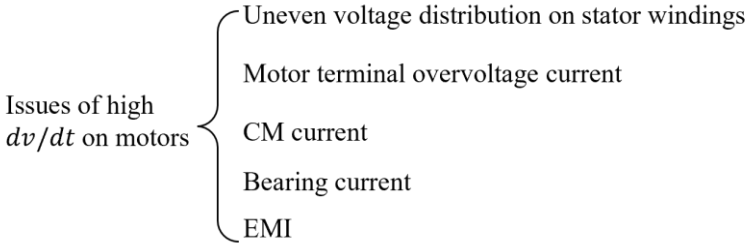


Figure 2.8 The main challenges of the high *dv/dt* on motors in WBG-based motor drive systems.

Since the PhD work aims to explore techniques to address the excessive voltage stress on the motor due to the fast-switching WBG inverter, the issues caused by the high dv/dt, i.e., uneven voltage distribution within the motor stator windings and the RWP will be reviewed in the following section.

2.3.1 Uneven Voltage Distribution within Motor Stator Windings

In inverter-fed motor drive systems, the fast-switched PWM voltage pulses result in uneven voltage distribution within motor stator windings [97]–[103]. In fact, the uneven voltage distribution arises from the propagation of the fast-switched PWM voltage pulses through the motor stator winding itself emulating the same effect of long cables. The faster the rise time, the more significant this effect and even greater the uneven voltage distribution along motor stator windings [104], [105]. As a consequence, the insulation failures most commonly occur in the first few turns of the first coil connected to the main terminals [106], [107].

Figure **2.9** shows the simulation result of the coil-to-core voltage when the motor is supplied by fast-switched PWM voltage pulses, where the dc-link voltage is 560V [105]. As can be noticed, the voltage distributes nonlinearly among the motor coils, where the voltage decreases from the first coil to the last coil in a monotonic manner. It is worth noting that the first coil endures the highest voltage stress among the stator winding coils, as shown in Figure 2.9.

Figure 2.10 compares the voltages across winding turns in the first coil of a motor stator measured in an experimental test [108]. As can be noticed, the voltage distributes unevenly among the motor stator winding turns, where the first several stator winding turns endure the higher voltages. Referring to Figure 2.10, the voltage across the first turn is about five times higher than that across the 20^{th} turn [108].

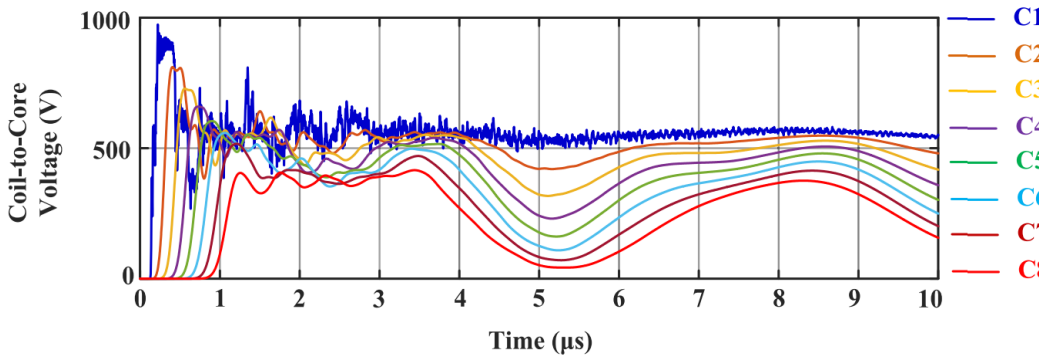


Figure 2.9 Simulation results of the coil-to-core voltage distribution when the motor is feed by high *dv/dt* voltage, the dc-link voltage is 560 V [105].

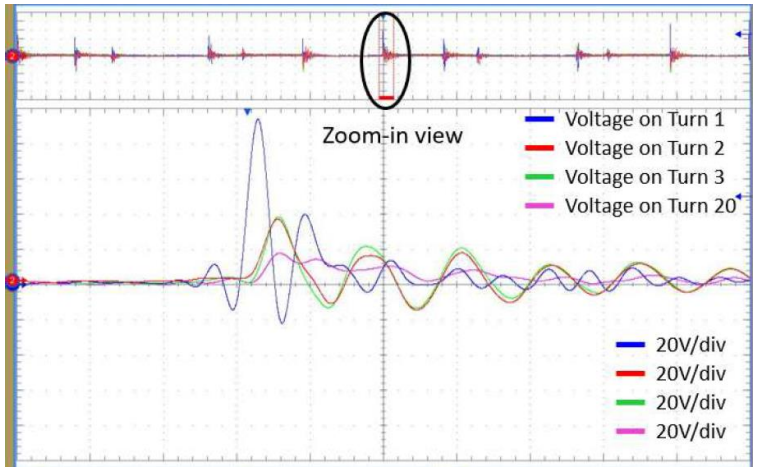


Figure 2.10 Experimental measured voltage distribution within winding turns of first coil of phase A winding when the motor is supplied by a two-level SiC power converter through 70-feet long cable. [108].

Note that the overstress across the first few winding turns closes to the motor terminals is further exacerbated when long power cables are used to connect the inverter to the motor due to the RWP in the motor drive system [32].

2.3.2 Motor Terminal Overvoltage Oscillations

In many harsh environments such as mining [109], oil exploration [110] and remote operated vehicle [111], the inverter and motor are installed at different locations connected through long power cables to provide better serviceability [112]–[114]. Figure 2.11 shows the circuit diagram of a typical inverter-fed motor drive system with long cables [48]. The cable length can be several meters to kilometers depending on the application [112].

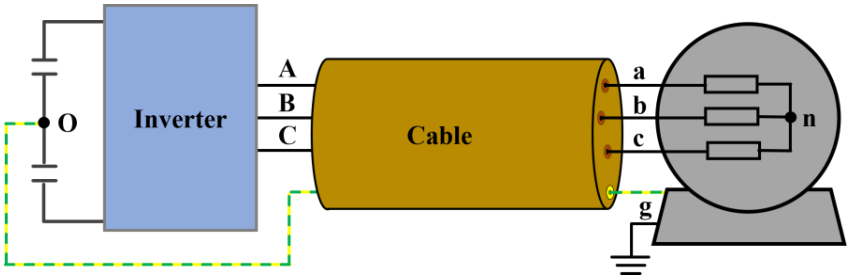


Figure 2.11 A typical WBG-based long cable-fed adjust speed drive system. The dotted yellow-green line represents the earth wire connecting the converter and the motor case.

Due to the distributed inductance and capacitance between cable conductors, the power cables in the motor drive system have similar behaviour to transmission lines, where the steep voltage (high dv/dt) pulses experience voltage reflections at motor terminals, resulting in serious overvoltage oscillations at motor terminals [30], [32]. This phenomenon is known as the RWP, caused by the high dv/dt and the characteristic impedance mismatch between the cable and motor [31]. The detailed model of the RWP will be presented in Chapter 3.

In fact, the RWP has been widely observed in Si based motor drive system when the long cable length is used, e.g., longer than 50m [115]. With the adoption of the fast-switched WBG inverter in motor drive systems, the RWP becomes more serious and complex [116]. On the one hand, the motor terminal overvoltage can be twice the inverter voltage with few meters power cable due to the fast-switching speed of WBG devices, as evidenced in Figure 2.12 [114]. On the other hand, the motor overvoltage can exceed twice the inverter voltage due to the undamped effects when the switching frequency of the WBG inverter is increased [117].

Figure 2.13 shows the voltage and current waveform measured at the inverter side and the motor terminals in a SiC-based 10 meters long cable-fed motor drive system. As shown, the motor terminal voltage is double of the inverter voltage due to the RWP in the motor drive system. Referring to Figure 2.13, the inverter output current is higher than that measured at the motor terminals. This is because the high dv/dt of the PWM voltage pulses charges or discharges the parasitic capacitance of the cable, resulting in high current spikes.

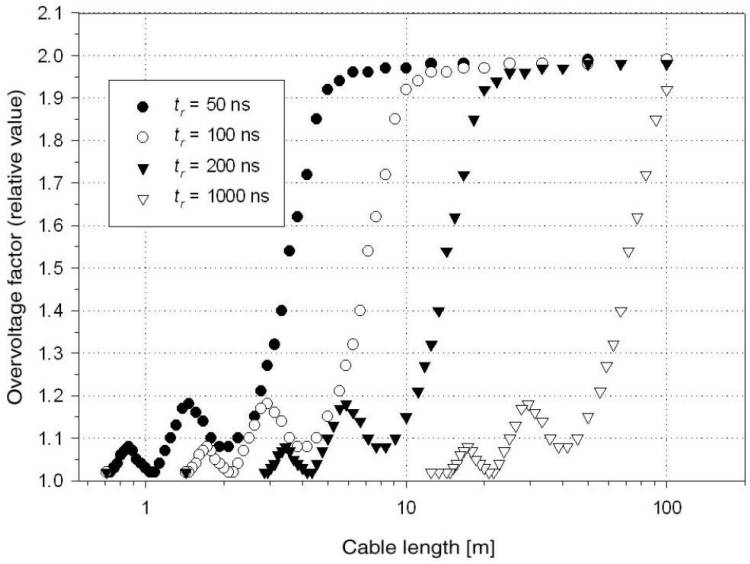


Figure 2.12 Motor overvoltage with the cable length and rise time [114].

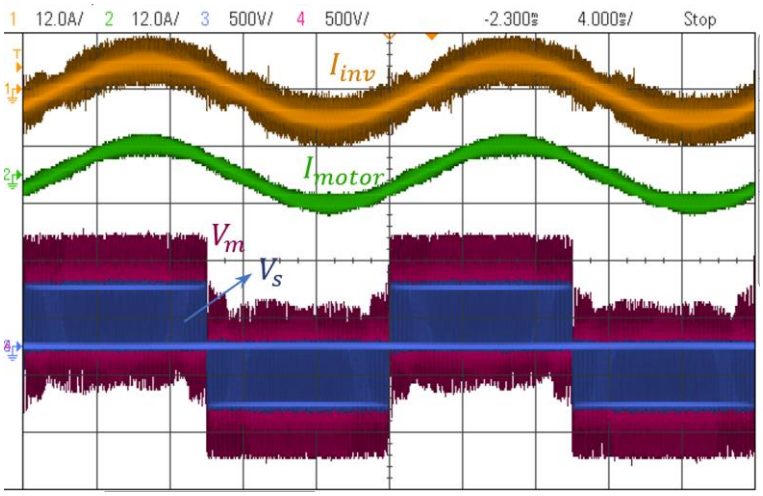


Figure 2.13 Voltage and current measured in a SiC-based 10m long cable-fed motor drive system for two fundamental cycles, I_{inv} and V_s are the current and voltage measured the inverter side, I_{motor} and V_m are the current and voltage measured the motor terminals. The dc-link voltage is 500V, voltage: 500V/div, current: 12A/div, time: 4ms/div.

Figure 2.14 shows the zoomed-in view at the switching transient, where the spike current shows the similar manner with the motor terminal overvoltage oscillations. The high current spikes may trigger the overcurrent protection of the inverter when they exceed the pre-set overcurrent level, leading to the unexpected shut down. Furthermore, the current spikes result in high power loss for the inverter and overheat the switching devices which reduce the power efficiency and reliability of the inverter [118].

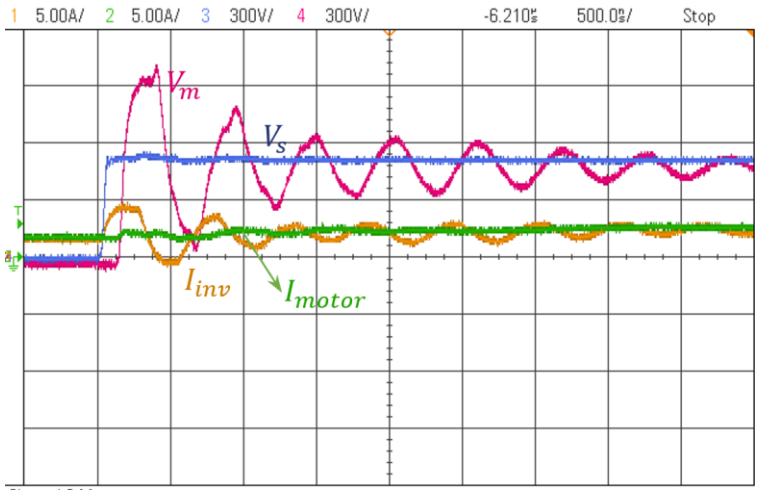
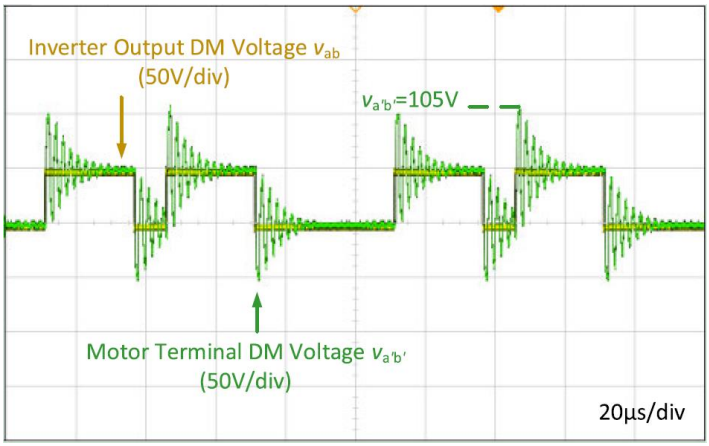
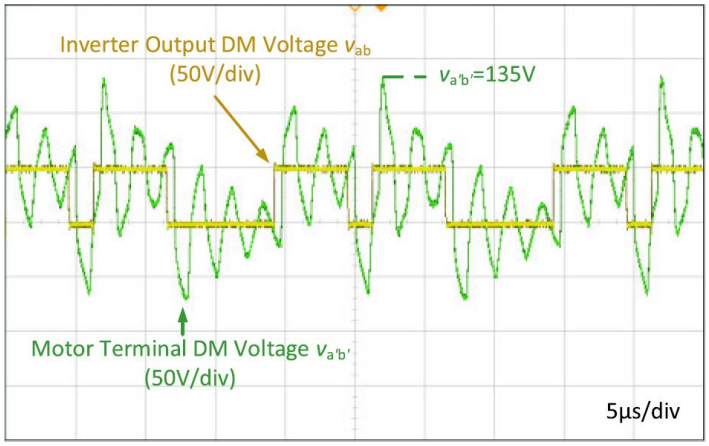


Figure 2.14 the zoomed-in view of the voltage and current measured in a SiC-based 10m long cable-fed motor drive system at switching transient, I_{inv} and V_s are the current and voltage measured the inverter side, I_{motor} and V_m are the current and voltage measured the motor terminals. The dc-link voltage is 500V, voltage: 300V/div, current: 5A/div, time: 0.5µs/div.

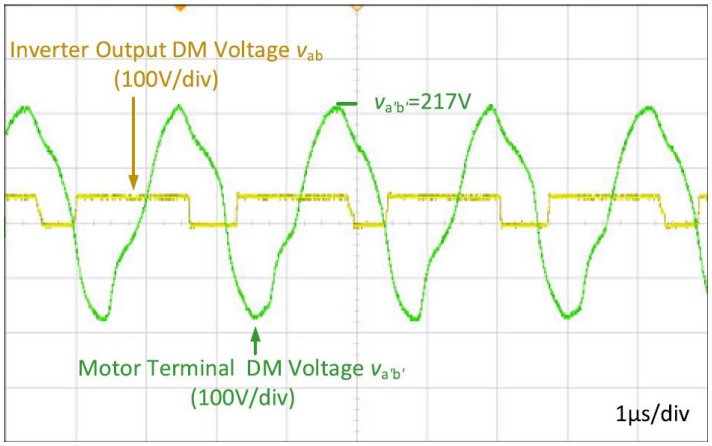
Figure 2.15 compares the voltages at the inverter side and motor terminals measured in a SiC-based cable-fed motor drive system when the inverter operates at different switching frequencies [30]. As shown in Figure 2.15 (a), when the inverter operates at the 10kHz, the motor terminal overvoltage is about twice the inverter voltage due to the RWP. However, with the switching frequency increasing, i.e., the two consecutive pulses are closed spaced, the motor terminal overvoltage is higher than twice the inverter voltage, as shown in Figure 2.15 (b) and (c). This is because the motor overvoltage caused by the first voltage pulses does not damp out before the second voltage pulse is generated [117], [119]–[121]. Referring to Figure 2.15 (b), the maximum motor terminal voltage is 139V when the switching frequency is 50kHz, i.e., the motor terminal overvoltage is about 2.8 times of the inverter voltage. It is worth noting that the motor terminal overvoltage can be even higher when the switching frequency of the inverter coincides with that of the overvoltage oscillation frequency [30]. Referring to Figure 2.15 (c), the motor terminal voltage is more than four times of the inverter voltage when the switching frequency is the same with that of the overvoltage oscillation frequency.



(a) switching frequency: 10kHz



(b) switching frequency: 50kHz



(c) switching frequency: 225kHz

Figure 2.15 Motor terminal voltage measured at different switching frequency in a SiC-based 70m long cable-fed motor drive system [30].

2.3.3 Issues Related to the Overvoltage Stress

In general purpose induction motors, the insulation material is not designed to resist such high overvoltage due to the RWP. When voltage stress across the motor stator windings exceeds the PD Inception Voltage (PDIV), it would increase the possibility to incept the PD [38]–[41], [100], [106], [122]. Therefore, the overvoltage stress across motor winding turns accelerates the winding insulation aging through inception of PDs that progressively yield to the degradation and local heating of random-wound motor coils [112], [114]. Figure 2.16 shows the PD activity in the motor stator windings due to the overvoltage stress [106]. The PDs are frequency dependent, the occurrence of PD would increase when the motor is supplied by the high switching frequency WBG inverter [30]. The accumulative effect of PD accelerate deterioration until the winding insulation breakdown, as shown in Figure 2.17 [107]. Also, the PDs deteriorate the EMI performance of the cable-fed motor drive systems due to the emitted high frequency electromagnetic energy [112], [123].

Figure 2.16 PD activity in motor stator windings [106].

Figure 2.17 An example of the insulation breakdown of motor stator windings [107].

2.4 Mitigation of Motor Terminal Overvoltage using Passive Filters

The motor terminal overvoltage oscillations due to the RWP is caused by the fast-fronted PWM voltage pulses travel along the long cables terminated by the motor, where the characteristic impedance of the motor is much larger that of the cable [30], [48]. The motor terminal overvoltage is affected by three main factors, i.e., the characteristic impedance of the cable and motor, the rise and fall times of the voltage feeding to the motor drive system, and the cable length [31], [116]. Accordingly, the motor overvoltage oscillations can be mitigated from three aspects: matching the impedance [124], adjust the rising and falling switching transitions [125], and reducing the cable length [93]. Several overvoltage mitigation strategies have been proposed in literature with different perspectives.

Figure 2.18 summaries the commonly used motor terminal overvoltage mitigation approaches. These strategies can be generally classified into passive, active, and other methods. The passive techniques employ passive filter networks installed either at the inverter side or the motor terminals, which will be reviewed in this section.

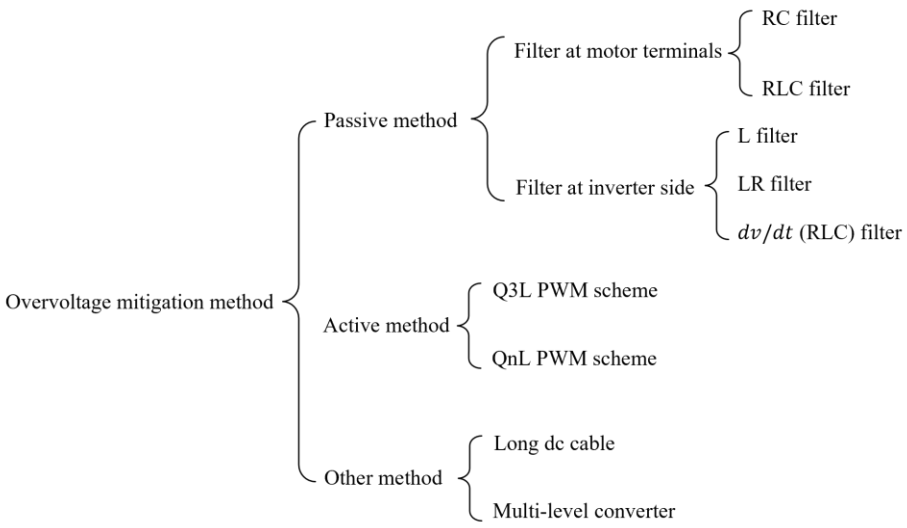


Figure 2.18 Summaries of the main motor terminal overvoltage mitigation methods.

2.4.1 Impedance Matching Filter Installed at Motor Terminals

Impedance matching filters mitigate the motor terminal overvoltage oscillations due to the RWP in long cable-fed motor drive system from the root cause, i.e., the characteristic impedance mismatch between the cable and motor [126]. Theoretically, when the equivalent characteristic impedance at the cable end is the same with the cable characteristic impedance, the fast-switched PWM voltage pulses will not be reflected at

motor terminals [116]. Therefore, impedance match filter can be installed at motor terminals where the filter is designed to match with the cable characteristic impedance. The impedance matching filter can be the RC filter [124], [126]–[128] and RLC filter [124], [126], [128], [129].

Figure 2.19 shows the circuit schematic of the RC impedance matching filter installed at motor terminals where the filter consists of a capacitor in series with a resistor for each phase [126].

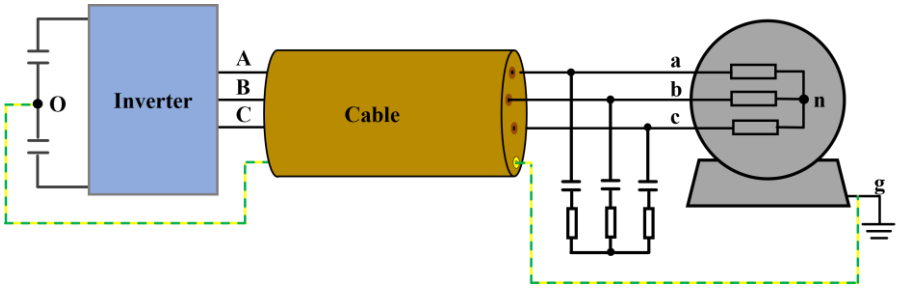


Figure 2.19 RC filter installed at the motor terminals in cable-fed motor drive system [126].

The filter impedance magnitude Z_{eq} is calculated as:

$$Z_{eq} = \sqrt{R_f^2 + \left(\frac{1}{j\omega_f C_f}\right)^2} \tag{2.1}$$

where R_f and C_f are the filter resistance and capacitance, ω_f is the angular frequency of the filter, respectively.

The filter parameters are designed to match the cable characteristic impedance Z_c, as given:

$$Z_{eq} = Z_c \rightarrow \sqrt{R_f^2 + \left(\frac{1}{j\omega_f C_f}\right)^2} = \sqrt{\frac{L_c}{C_c}} \tag{2.2}$$

where, L_c and C_c are the cable per unit inductance and capacitance, respectively.

To provide enough damping for the overvoltage, the resistance R_f should be designed to result in an overdamped circuit, as:

$$R_f > 2\sqrt{\frac{L}{C_f}} \tag{2.3}$$

where, L is the lumped cable inductance in the cable-fed motor drive system.

The RC filter, shown in Figure 2.19, has high power loss which limits its application [126]. To minimise the power loss of the RC filter, the second order RLC filter can be used, as shown in Figure 2.20 [126].

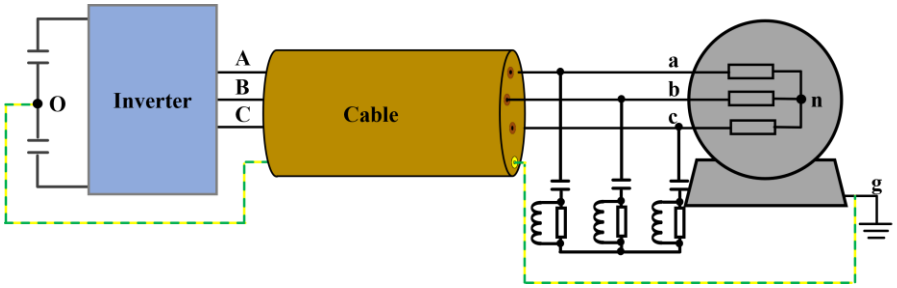


Figure 2.20 RLC filter installed at the motor terminals in long cable-fed motor drives [126].

The filter impedance magnitude Z_{eq} is calculated as:

$$Z_f = \sqrt{\left(\frac{R_f\omega_f^2 L_f^2}{R_f^2+\omega_f^2 L_f^2}\right)^2 + \left(\frac{R_f^2\omega_f L_f}{R_f^2+\omega_f^2 L_f^2} + \frac{1}{\omega_f C_f}\right)^2} \tag{2.4}$$

The filter parameters are designed to match the cable characteristic impedance Z_c, as given:

$$Z_{eq} = Z_c \rightarrow \sqrt{\left(\frac{R_f\omega_f^2 L_f^2}{R_f^2+\omega_f^2 L_f^2}\right)^2 + \left(\frac{R_f^2\omega_f L_f}{R_f^2+\omega_f^2 L_f^2} + \frac{1}{\omega_f C_f}\right)^2} = \sqrt{\frac{L_c}{C_c}} \tag{2.5}$$

The resistance R_f in the filter should be designed to result in an overdamped circuit, as:

$$R_f < \frac{1}{2}\sqrt{\frac{L_f}{C_f}} \tag{2.6}$$

In addition, the resonant frequency of the RLC filter should be larger than five times of the switching frequency [124].

While the filters at motor terminals can effectively mitigate the motor terminal overvoltage oscillations, the high dv/dt is still present at motor terminals [129], resulting in the non-uniform voltage distribution across the stator winding turns. This imposes high voltage stress across the first several turns close to motor terminals. Furthermore, the power loss of the filter increases the difficulty of the thermal management at the motor sides due to the limited installation space. Therefore, these disadvantages limit the application of the impedance matching filter.

2.4.2 L Filter Installed at Inverter Side

Another method to supress the motor terminal overvoltage is increasing the rise and fall times of the PWM voltage pulses applied to the long cable-fed motor drive system [118], [126], [130]. Passive filters such as L filter and LRC filter, are usually installed at the inverter side to limit the dv/dt of the inverter output voltage [126].

Figure 2.21 shows the output reactor installed at the inverter side in the long cable-fed motor drives, where the inductor L_f is in series with the power cable [126]. The L filter can reduce the dv/dt of output voltage [118]. Since the inductor is in series with the motor, the full load current flows through the inductor resulting in power loss and voltage drop across the filter. The motor terminal overvoltage mitigation is proportional to the inductance, a higher inductance reduces the effective voltage applied to the motor [116]. In addition, a higher inductance can increase the power loss in the installed inductor which may reduce the system power efficiency.

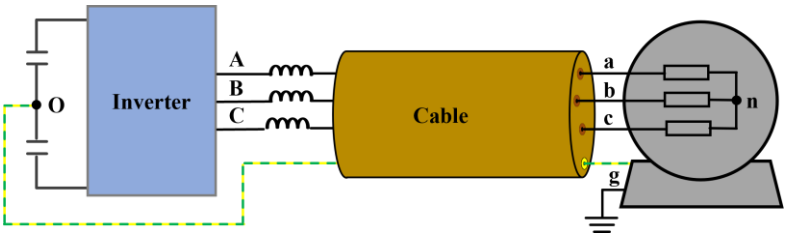


Figure 2.21 L filter installed at the inverter side in long cable-fed motor drives [126].

To reduce the power loss and voltage drop caused by the L filter, [131] proposes the LR filter as shown in Figure 2.22, where a parallel resistor is added to the inductor. While the LR filter can effectively mitigate the motor terminal overvoltage, the filter should be carefully designed due to the parasitic inductance of resistor which would result in an unpredicted high frequency overvoltage oscillation [132].

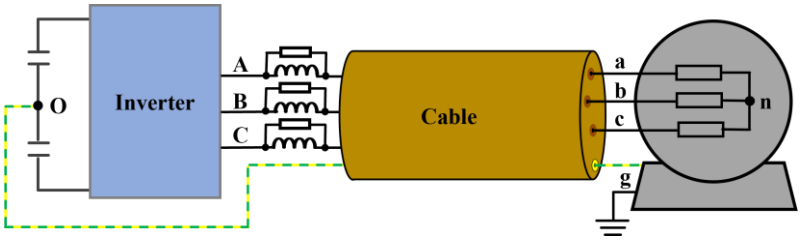
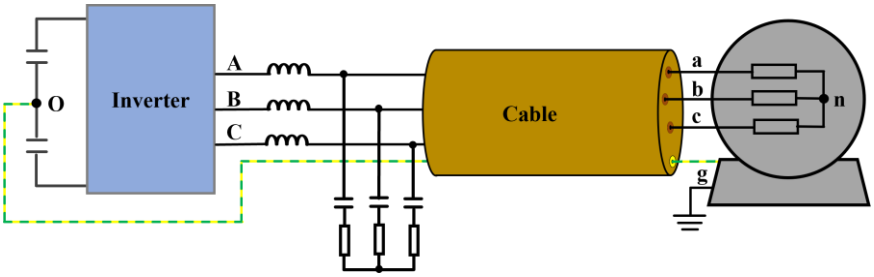


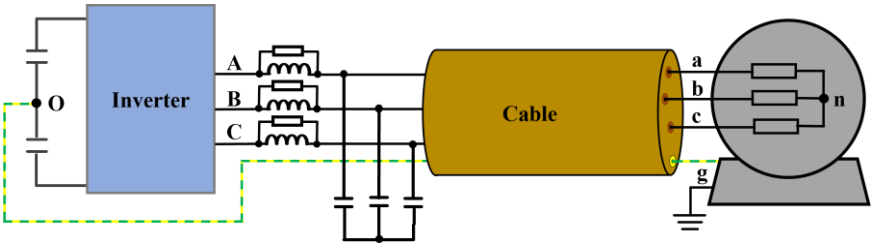
Figure 2.22 LR filter installed at the inverter side in long cable-fed motor drives [131].

2.4.3 Dv/dt Filter Installed at Inverter Side

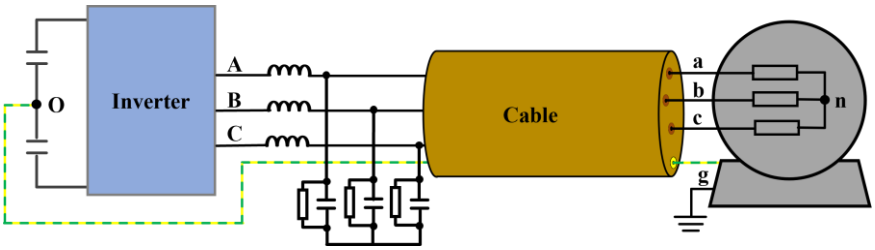
The dv/dt filters can be installed at inverter side to slow down the rising and falling transitions of the PWM voltage pulses feeding to the drive system [125]. It usually uses different combination the resistor, inductor, and capacitor, as show in Figure 2.23 [126].



(a) RLC dv/dt filter



(b) R//L+C dv/dt filter



(c) L+R//C dv/dt filter

Figure 2.23 RLC *dv/dt* filter installed at the inverter side in long cable-fed motor drives [126].

Taking the RLC filter shown in Figure 2.23 (a) as an example, the output dv/dt can be given as [133]:

$$\frac{dv}{dt} = \frac{V_{dc}}{\sqrt{L_f C_f}} \tag{2.7}$$

The resistance R_f in the filter should be designed to result in an overdamped circuit, as:

$$R_f > 2\sqrt{\frac{L_f}{C_f}} \tag{2.8}$$

To avoid the resonance with the inverter, the filter resonant frequency f_{res} should be set much higher than the switching frequency f_s as [133]:

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}} > f_{sw} \tag{2.9}$$

Figure **2.24** shows the voltage and current measured at the inverter output node and the filter output node of the dv/dt filter [33]. Note that to show the additional current introduced by the filter, the experimental results are measured at low/zero load condition. As shown, while the inverter output voltage is slowed down after the filter, the filter results in additional current for the inverter leading to high power loss for the inverter. Also, the dv/dt filter would reduce the effective voltage impose on the motor due to the voltage drop on the filter.

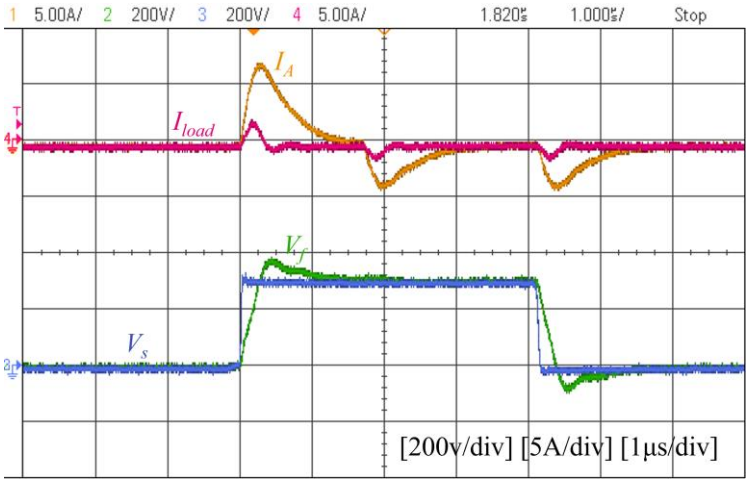


Figure 2.24 The inverter output voltage V_s and the filter output voltage V_f, the load current I_{load} and the inverter output current I_A measured in the inverter + *dv/dt* filter [33].

2.5 Mitigation of Motor Terminal Overvoltage using Active Mitigation Methods

Despite the effectiveness of filters on motor terminal overvoltage oscillations mitigation, they have disadvantages such as bulky and high-power loss, sacrificing the benefits of using WBG devices in adjustable speed drive systems [134]. To overcome the disadvantages of the filters, several active mitigation methods have been proposed in literature, which will be described in this section.

The key idea of the active mitigation method is propagating two or more consequence voltage segments separated with a proper time to the motor terminal, where the resultant motor terminal overvoltage due to these voltage segments can be counterbalanced or partial counterbalanced [135], [136]. Therefore, the overvoltage oscillations across the motor terminals can be limited to a safe level. This section reviews the Q3L PWM scheme [134], [135], [137]–[140], QnL PWM scheme [138], [141] from the overvoltage mitigation mechanism, adopted topology, etc.

2.5.1 Q3L PWM Scheme

Figure 2.25 shows an example of the widely adopted Q3L PWM scheme to mitigate the motor terminal overvoltage, where two consequence identical voltages (V_{s1} and V_{s2}) with an amplitude of $0.5V_{dc}$ are sent to the motor terminal [135].

Referring to Figure 2.25, the resultant motor terminal overvoltage V_{m1} and V_{m2} due to the two voltage segments V_{s1} and V_{s2} are counterbalanced. Therefore, the motor terminal overvoltage oscillations can be entirely mitigated. Since the rising and falling switching transitions of the actively shaped inverter voltage waveform has three voltage levels, the voltage waveform shown in Figure 2.25 is denotated as the Q3L PWM waveform.

The Q3L PWM scheme was first implemented and experimental verified on a Si IGBT based 100 m long cable-fed motor drive system when the motor is supplied by a three-phase T-type inverter [135], as shown in Figure 2.26. The middle voltage level, i.e., $0.5V_{dc}$, at the rising and falling switching transitions can be generated with the auxiliary branches. Referring to Figure 2.26, the output voltage of the T-type inverter is clamped to $0.5V_{dc}$ when the auxiliary branches are turned-ON.

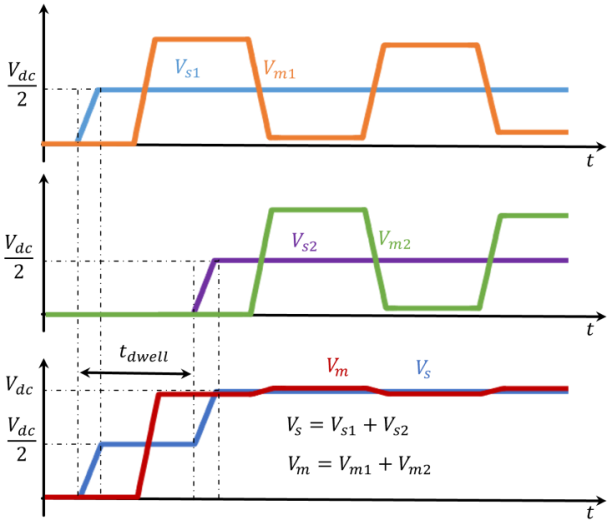


Figure 2.25 Q3L PWM Scheme.

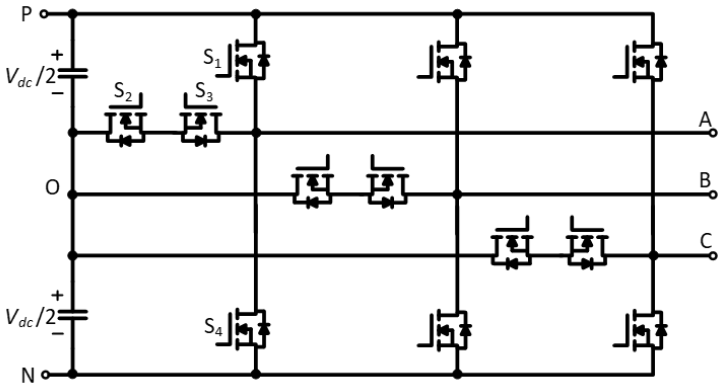


Figure 2.26 Three-phase T-type inverter.

In addition to the T-type inverter, many other inverter topologies can be used to generate the required Q3L PWM voltage waveform. For example, [134] uses a SiC-based H-bridge inverter to mitigate the motor overvoltage in a single-phase long cable-fed motor drive system, as shown in Figure 2.27.

Figure 2.28 illustrates how to generate the Q3L PWM using the single-phase H-bridge inverter [134]. Referring to Figure 2.28, a reference signal is compared with two identical triangle carrier waveforms carrier 1 and carrier 2 but separated with a dwell time, where the drive signals for S_1 and S_2 are generated by the comparison of carrier 1 and reference signal, and the drive signals for S_3 and S_4 are generated by the comparison of carrier 2 and reference signal. The experimental results show that the method proposed in [134] can

effectively mitigate the motor overvoltage oscillations. However, it can only be used in the single-phase long cable-fed motor drive system.

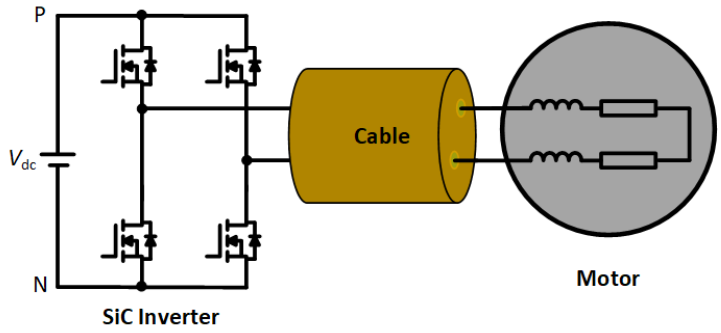


Figure 2.27 Single-phase inverter for the Q3L PWM [134].

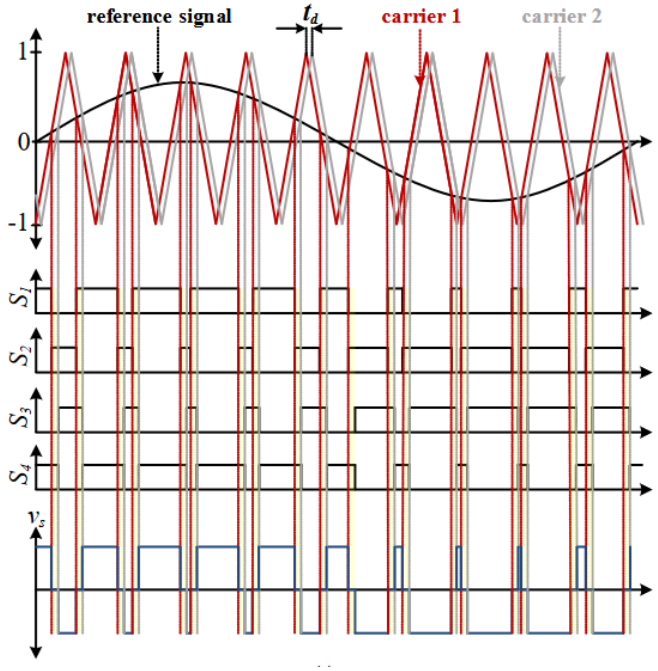


Figure 2.28 Q3L PWM generation in the single-phase inverter [134]

To implement the Q3L PWM in three-phase long cable-fed motor drive system, [137] proposes the Q3L PWM scheme with an open-end winding motor. Figure 2.29 (a) shows the circuit schematic of the long cable-fed open-end winding motor drive system, where the motor is supplied by two three-phase inverters. Instead of controlling the two inverters [142]–[144], i.e., VSI 1 and VSI 2, independently, the two inverters can be considered as a whole inverter. For each phase of the motor drive system, the Q3L PWM waveform can be obtained using the control approach shown in Figure 2.28. Despite its effectiveness in the

motor terminal overvoltage oscillations mitigation, it can only be implemented in the open-end winding motors.

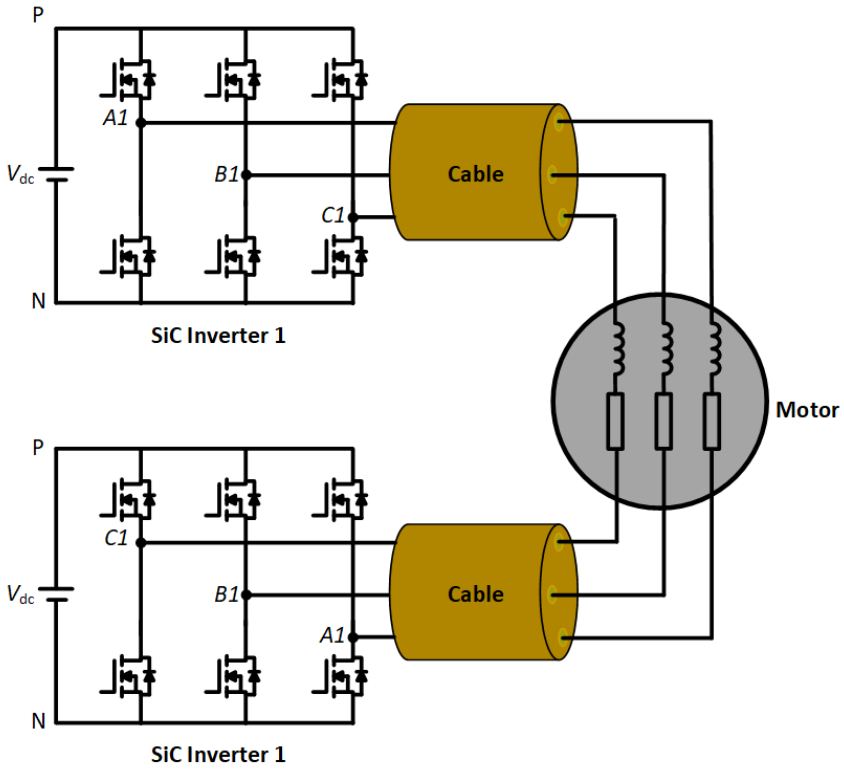


Figure 2.29 Open-winding motor for the Q3L PWM [137].

[139] proposes an active reflected wave canceller which consists of an external dc source, an H-bridge circuit and an inductor for each phase, to generate the Q3L PWM voltages for the motor terminal overvoltage mitigation, as shown in Figure 2.30. Since the proposed circuit uses 12 switches, three inductors, and external dc source, it would increase the system cost and limit its application.

[140] further optimised the active reflected wave canceller. Figure 2.31 shows the circuit schematic for the optimised active reflected wave canceller, where it is composed of two switching devices, two diodes and an inductor for each phase. Compared with Figure 2.30, the optimised ARWC reduces the cost because it uses two fewer switching devices and do not need the external dc.

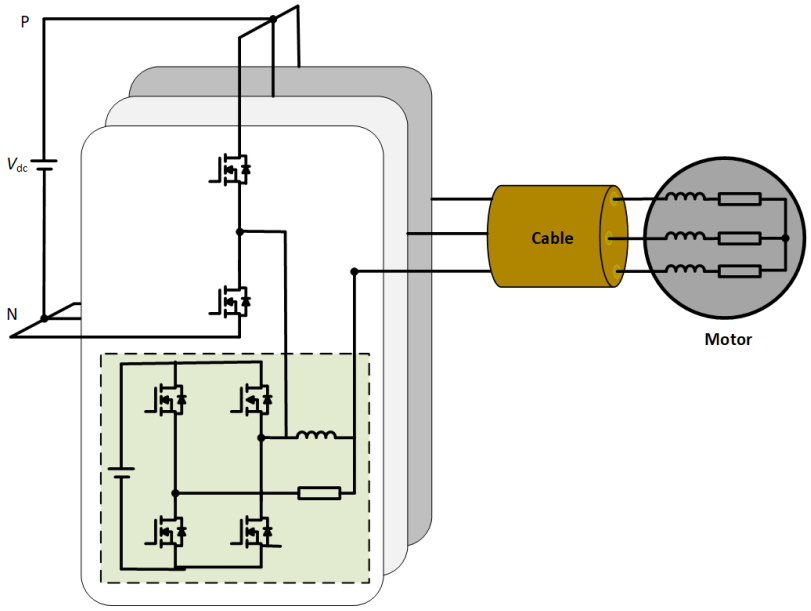


Figure 2.30 ARWC for Q3L PWM [139]

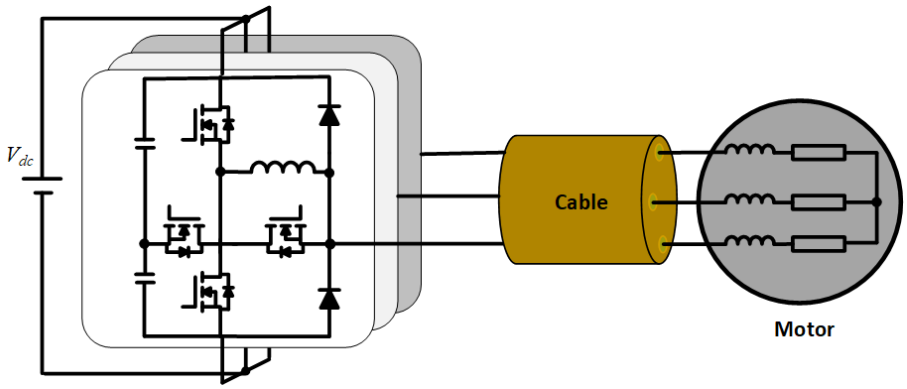


Figure 2.31 Optimised ARWC for Q3L PWM [140]

2.5.2 QnL PWM Scheme

The Q3L PWM can be further extended to QnL PWM, especially in medium and high voltage applications. Figure 2.32 illustrates the rising edge of the inverter output voltage waveform when the inverter is modulated under the QnL PWM scheme, where the rising switching transitions are shaped as multiple small voltage steps separated with a proper dwell time [141]. The overvoltage mitigation mechanism of the QnL PWM scheme is similar with that of the Q3L PWM, where the overvoltage oscillations across the motor terminals caused by the voltage steps can be counterbalanced.

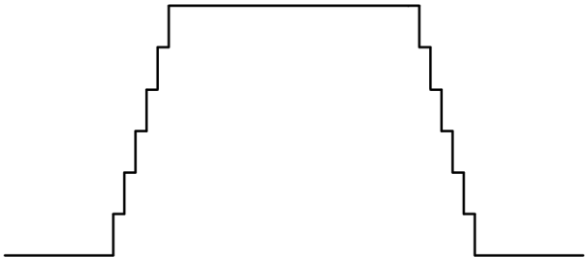


Figure 2.32 QnL PWM [141]

The QnL PWM scheme can be implemented using multilevel converters. For example, [138], [141], [145], [146] use the MMC to generate that QnL PWM to mitigate the motor terminal overvoltage oscillations in the long cable-fed motor drive system. Figure 2.33 depicts the circuit diagram of the MMC with long power cables, where each phase-leg consists of an upper arm, a lower arm, and a coupled arm inductor [146]. Compared with the MMC under the conventional multi-level operation mode, the MMC modulated under the QnL PWM scheme can reduces the size of the capacitor in the submodule but at the cost of increasing the THD of the current [141].

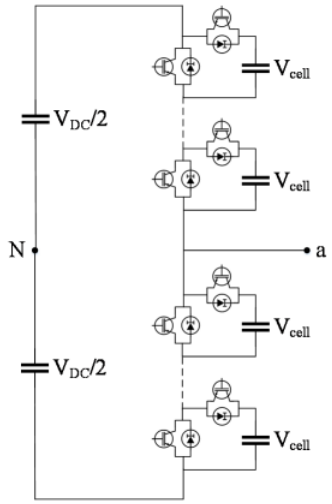


Figure 2.33 MMC for QnL PWM [138], [141], [145], [146].

2.6 Mitigation of Motor Terminal Overvoltage using Other Methods

In addition to the active and passive overvoltage mitigation methods, the motor terminal overvoltage can be mitigated using short cables and multilevel converters.

2.6.1 Long dc Cable + Integrated Motor

Since the motor terminal overvoltage is caused by the long cable, it is possible to mitigate the RWP without using the cable in the motor drive system. This can be achieved by using the long dc-cable, as shown in Figure 2.34 [147]. While this method can effectively mitigate the motor terminal overvoltage oscillations, it has several design challenges. For example, the inverter should be integrated with the motor, the thermal design, EMI filter would be more challenging.

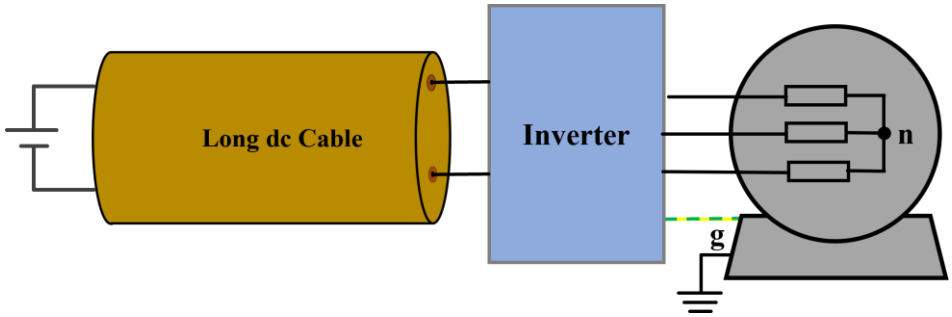


Figure 2.34 Long dc cable drive system [147].

2.6.2 Multilevel converter

Multilevel converter can be used to limit the motor terminal overvoltage due to the increased voltage steps for a given dc-link voltage. Figure 2.35 shows the motor terminal overvoltage when the motor is fed by a three-level inverter. As shown, the maximum motor terminal voltage is 1.5p.u [32]. However, this comes at the expense of employing increased component count incurring additional size, cost.

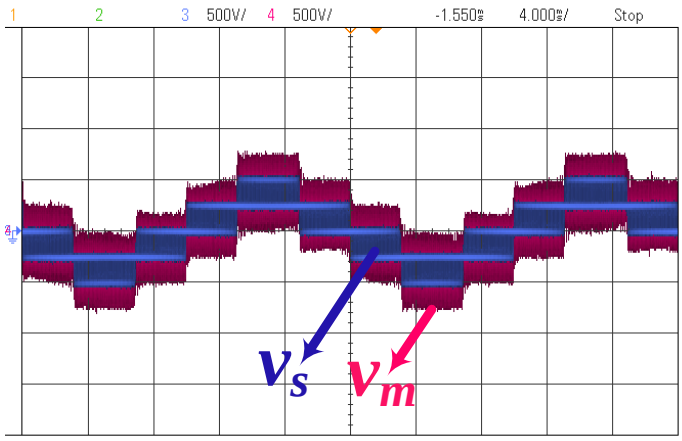


Figure 2.35 Motor terminal overvoltage when the motor is supplied by a three-level SiC inverter [32].

2.7 Limitations of the Literature and Research Opportunities

WBG devices are reaching the technological readiness and are becoming the devices choice to replace their Si predecessors in a growing number of power converters used to control electric motors in adjustable speed drive systems. The literature to date has proposed methods that seek to understand and address the challenges in motor drive system presented by fast-switching speed WBG semiconductor devices. However, these works are still limited, and research into the RWP and the corresponding mitigation methods to fully utilise WBG devices without compromising their benefits, is still requiring further work. The limitations of the literature and research opportunities are summarized as:

The Reflected Wave Phenomenon

- What is the root cause of the motor terminal overvoltage oscillations? Can we understand and crystallize the underlying cause of the RWP from the frequency domain?
- Do the parasitic elements of the switching devices affect the motor terminal overvoltage in the WBG-based cable-fed motor drive system?

Mitigation of the motor terminal overvoltage by slowing down the dv/dt

- As a rule of thumb, increasing the rise and fall times of inverter output voltages using dv/dt limiter is an effective method to suppress the motor terminal overvoltage oscillations. However, how to design the optimum rise and fall times for different cable length? What is the essence of the overvoltage mitigation mechanism by limiting the dv/dt?
- Slowing down the dv/dt using passive filters result in additional power loss and size of the motor drive system. Can we find a method to slow down the dv/dt without sacrificing the benefits of SiC?

Mitigation of the motor terminal overvoltage using Q3L PWM Scheme

- What is the overvoltage mitigation mechanism of the Q3L PWM scheme?
- Do the parasitic elements of the switching device in T-type inverter affect the effectiveness of the Q3L PWM on motor terminal overvoltage mitigation?
- Can we generate the Q3L PWM without using additional switching devices?

Chapter 3
Modelling of the Reflected Wave Phenomenon

This chapter aims to meet the Research Objective 1: Gain deep understanding of the RWP and crystallize the underlying cause of motor terminal overvoltage oscillations in cable-fed motors using fast-switching SiC inverters, providing the foundation for developing overvoltage mitigation techniques through active waveform shaping.

3.1 Introduction

The RWP has been observed in Si-based long cable-fed motor drive system in past several decades, where the cable length is usually longer than hundreds of meters [114]. This issue including the modelling and mitigation approaches, has been well studied in Si based motor drive system [112]. However, the emerging application of WBG semiconductor devices such as SiC MOSFETs in inverter-fed motor drive system with extremely fast switching speed makes the RWP more common and severe because it occurs in much shorter cables [30]. The motor terminal voltage can reach twice the inverter voltage with shorter cable length, i.e., only several meters, compared with those used in the equivalent rated Si counterparts [116].

Moreover, a greater than twice the inverter voltage can be observed at the motor terminals when the inverter is switched at very high switching frequency and/or modulation index, which is known as the double pulsing effect [117]. This is because the switching instants of inverter voltages are very closely spaced, where a subsequent voltage pulse is applied to the motor before the previous reflected motor terminal voltage is fully damped out [33]. Therefore, it is necessary to revisit the RWP and take this knowledge into account when designing a WBG-based adjustable speed drives to improve the reliability and lifetime of the motor drive system. In this chapter, the modelling of the RWP is presented briefly and factors that affects the motor overvoltage are investigated.

3.2 The Adjustable Speed Drive System with Long Cables

Figure 3.1 repeats the circuit schematic of a SiC-based long cable-fed adjustable speed drive system. As shown, the motor drive system consists of a dc power source, a PWM power inverter, a long power cable, and an electric motor. The inverter generates high-frequency fast-switched PWM voltage pulses, where the fast rise and fall times are generally within tens of nanoseconds depending on characteristics of the adopted switching devices, load conditions and gate drivers [48].

Referring to Figure 3.1, the inverter and the motor are connected through a four-core power cable, where the three output terminals i.e., A, B and C, of the inverter are connected to the motor terminals, i.e., a, b, and c, and the dc-link middle point (o) is connected to the motor chassis (g) [30]. Note that the dc-link midpoint (o) and the motor chassis (g) are assumed to be earthed, as shown in Figure 3.1. Thus, the inverter common mode (CM) voltage is imposed directly on the motor neutral point n.

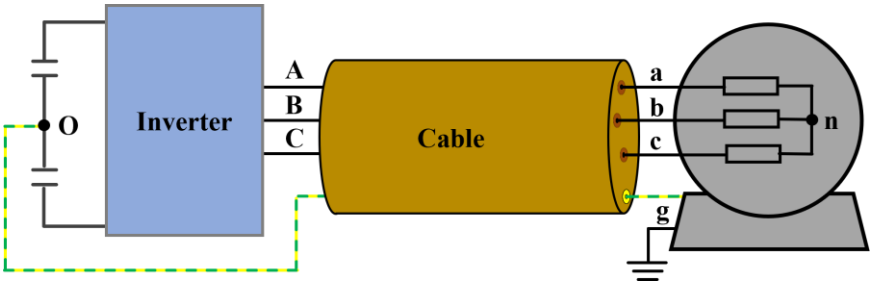


Figure 3.1 A typical WBG-based long cable-fed adjust speed drive system.

Fundamentally, the fast switched PWM voltage pulses experience the voltage reflection due to the characteristic impedance mismatch between two connected networks, i.e., an overvoltage oscillation can be excited at the connecting node when their impedance mismatch [32]. Therefore, three types of overvoltage can be observed in the motor drive system shown in Figure **3.1**, i.e., the differential mode (DM) overvoltage oscillations at the motor terminals (a, b, and c), the CM overvoltage oscillations at the motor terminals, and the CM overvoltage oscillations at the motor neutral point (n) [30]. The DM and CM motor overvoltage oscillations at motor terminals are excited by the DM and CM voltage, respectively. The motor neutral point overvoltage oscillations are excited by the CM voltage. This PhD work mainly focuses on the motor terminal overvoltage oscillations and their mitigation methods.

3.2.1 Motor Terminal Overvoltage Oscillations (DM & CM)

The PWM voltage pulses experience voltage reflection at motor terminals because the impedance of the motor is much higher than the cable. Therefore, the motor terminal overvoltage can be observed between the phases of the motor (DM) and between each phase and ground (CM). For simplify, only the terminal overvoltage between the phases, i.e., the DM overvoltage, will be analysed in the following part.

Figure 3.2 illustrates the equivalent differential mode circuit of any two phases of the cable-motor system that shown in Figure 3.1, where the characteristic impedance of the cable and motor are denoted as Z_c and Z_m, respectively. In general, the characteristic impedance of the cable is usually in the range of 20 Ω and 120 Ω depending the cable type [33]. By contrast, the characteristic impedance of the motor is much larger than that of the cable [48], where the motor characteristic impedance ranges between 500 Ω and 4000 Ω. As a rule of thumb, the characteristic impedance of the motor decreases with its power rating, i.e., the motor with lower power rating tends to have a higher characteristic impedance. Due to the characteristic impedance mismatch between the power cable and motor, the RWP arises at the motor terminals, leading to overvoltage oscillations. According to Figure 3.2, the motor terminal DM overvoltage is due to the DM voltage and the DM impedance mismatch in the motor drive system.

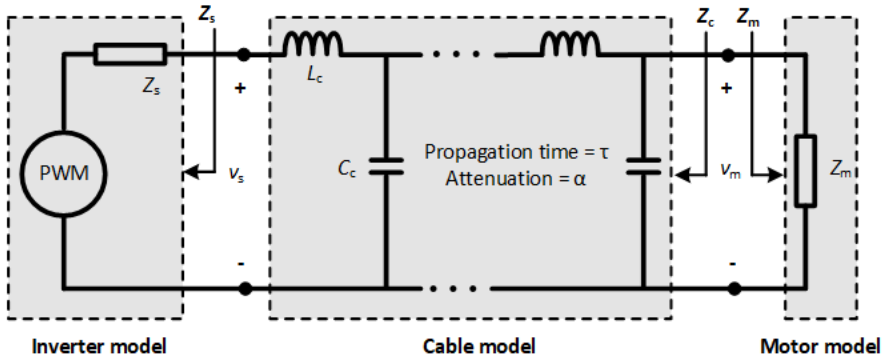


Figure 3.2 Equivalent differential mode circuit of the long cable-fed motor drive system.

Figure 3.3 compares the line voltages at the inverter side and motor terminal for one switching cycle in a cable-fed SiC-based motor drive system. As can be noticed, the motor terminals exhibit high frequency overvoltage oscillations in a damped manner as a result of the RWP, where the maximum motor terminal voltage is about 2.0 pu at both rising and falling edges.

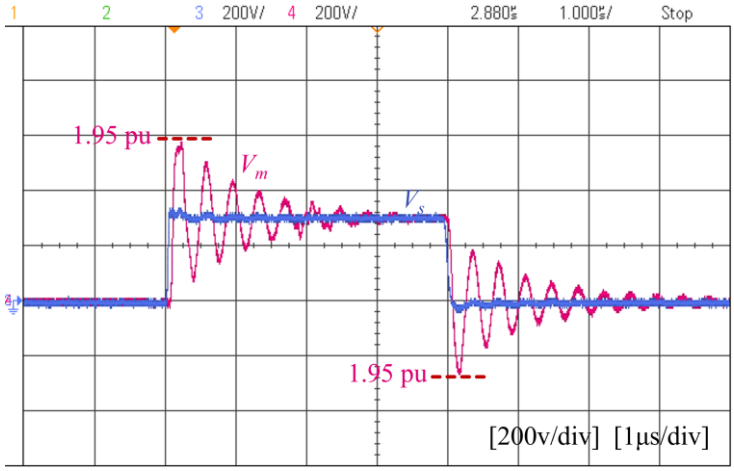


Figure 3.3 Experimental measured inverter line voltage V_s and motor terminal line volage V_m in SiC-based long cable-fed motor drive system. dc-link voltage: 300V; Cable: 12m long, 12 AWG, PVC cable; SiC MOSFET: Wolfspeed C2M0040120D; Motor: 3-phase 4-pole 2.2kW induction motor.

3.2.2 Motor Neutral Point Overvoltage Oscillations

Unlike the motor terminal overvoltage oscillations, the motor neutral point overvoltage oscillations are not caused by the long cables of the motor drive system. i.e., the motor neutral overvoltage oscillations can occur with short or even without connecting cables between the power converter and motor in the motor drive system [30], [32].

The motor neutral point overvoltage oscillations arise from the propagation of the CM voltage pulses through the motor stator winding itself which emulates the same effect of long cables [32]. With the motor neutral point being commonly floating, the inverter CM voltage pulses travelling through the motor stator winding encounter an infinite impedance between the neutral point and ground. The mismatch between the motor CM impedance and the neutral-to-ground infinite impedance causes the inverter CM voltage pulses to experience voltage reflection at the motor neutral point. This results in overvoltage oscillations that externally manifest at the motor neutral-to-ground voltage with peak voltage stress at the winding close to the neutral point [30], [104], [105].

Figure 3.4 illustrates the equivalent CM circuit of the long cable-fed motor drive system that shown in Figure 3.1. The total impedance of the cable Z_c and the motor Z_m can be lumped and detonated as the system CM impedance Z_{cm}. Note that the impedance between the neutral point n and ground g is considered to be infinite without considering the parasitic capacitance of windings to frame. Referring to Figure 3.4, the neutral point n and ground g are open circuit.

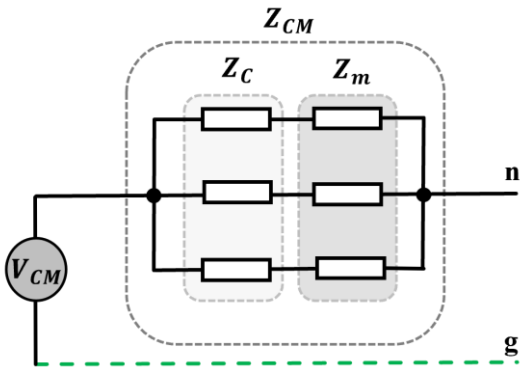


Figure 3.4 The equivalent CM circuit of the motor drive system.

Note that CM voltage of the inverter is also caused by and consists of PWM voltage pulses, depending on the inverter topology and modulation approach. Figure 3.5 shows an example of the CM voltage waveform of a standard three-phase two-level inverter modulated under the conventional PWM [121], [148], [149]. Referring to Figure 3.4, owing to the motor neutral point is facing an infinite impedance, the CM PWM voltage pulses will experience voltage reflections at the neutral point n, resulting in a double overvoltage of the inverter CM voltage.

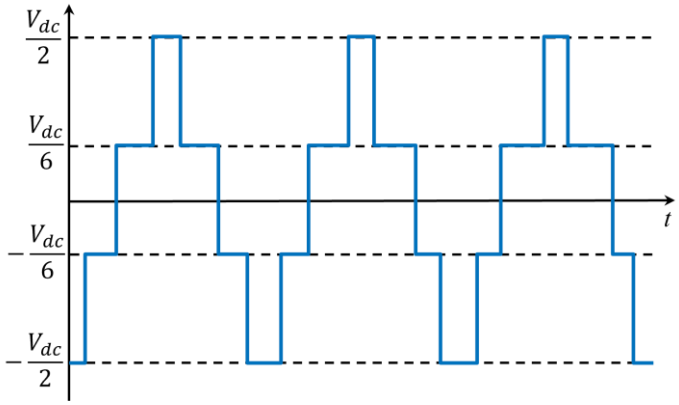


Figure 3.5 The CM voltage waveform of a three-phase 2L inverter modulated under conventional PWM.

Figure 3.6 shows the experimentally measured CM voltage of the inverter and the motor neutral point voltage when the motor is supplied by a two-level inverter under conventional PWM. As shown, the motor neutral point exhibits overvoltage oscillations as a consequence of the RWP, as previous analysed.

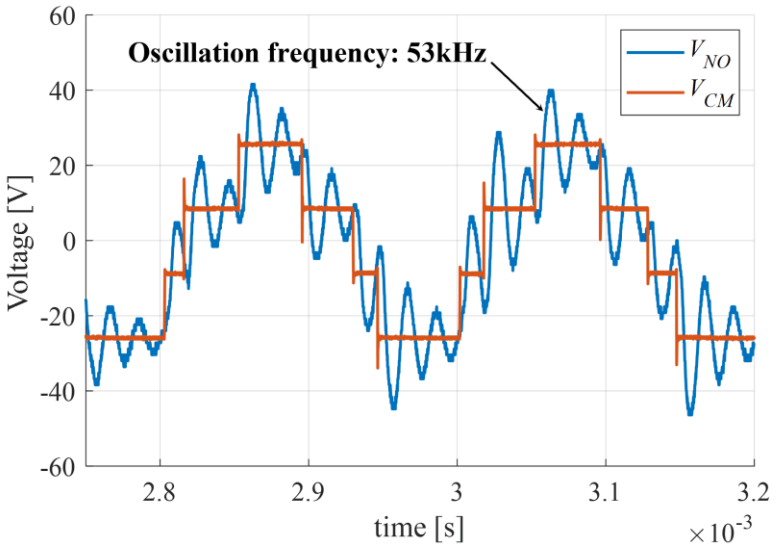


Figure 3.6 The inverter CM voltage V_{CM} and motor neutral point voltage V_{NO} when the motor is supplied by a three-phase two-level inverter at modulation index 0.2, switching frequency 20kHz, and dc-link voltage 50V. Cable: 12.5m long, four-core unshielded 13 AWG PVC cable; SiC MOSFET: Wolfspeed C2M0040120D; Motor: 3-phase 4-pole 2.2kW induction motor.

3.3 Analysis of the Reflected Wave Phenomenon

3.3.1 Analysis in Time Domain

The analysis of the RWP in adjustable speed motor drive system using the transmission line theory has been well studied in literature [30]. Several modelling techniques such as the snapshot [138], and the bounced diagram [33] are widely used to assist the analysis. To visually illustrate the voltage reflection process, the bounced diagram shown in Figure 3.7 is used for the analysis. Note that the wave propagation time t_p through the power cable from the inverter to the motor terminals, is assumed to be much longer than the rise and fall times t_r of the PWM voltage pulses feeding to the motor drive system [48].

The wave propagation velocity v through the power cable is calculated as:

$$v = \frac{1}{\sqrt{L_c C_c}} \tag{3.1}$$

where, C_c and L_c are the cable per unit length capacitance and inductance, respectively.

In general, these two parameters are not available in the cable's datasheets. L_c and C_c can be obtained from the impedance measurement based on the short-circuit and open circuit of the 1m long cable which is presented in the Appendix [33].

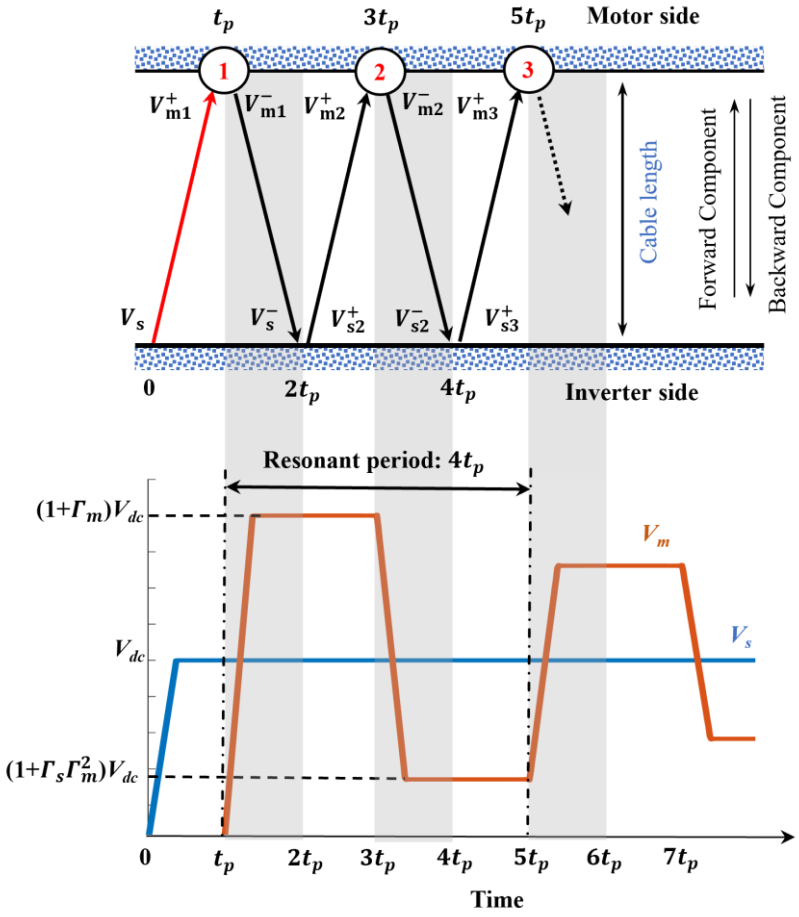


Figure 3.7 A bounced diagram for the reflected wave phenomenon in the long cable-fed motor drive system.

According to (3.1), for a given cable length l_c, the propagation time t_p is calculated as:

$$t_p = l_c\sqrt{L_c C_c} \tag{3.2}$$

The cable characteristic impedance Z_c is a function of the cable per unit length inductance L_c and capacitance C_c, as:

$$Z_c = \sqrt{L_c/C_c} \tag{3.3}$$

The reflection coefficient at the motor terminals Γ_m is determined by the characteristic impedance of cable Z_c and the motor Z_m, as:

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{3.4}$$

The reflection coefficient at the power inverter side Γ_s is determined by the characteristic impedance of cable Z_c and the inverter Z_s, as:

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \tag{3.5}$$

In general, the characteristic impedance of the motor is much higher than that of the cable ($Z_m \gg Z_c$), the typical inverter impedance is near zero ($Z_s \approx 0$). Therefore, according to (3.4) and (3.5) the reflection coefficients are unity, i.e., $\Gamma_m \approx 1$ and $\Gamma_s \approx -1$ [33]. Note that $\Gamma_m \approx 1$ means the voltage at the motor terminals is almost fully reflected with the same phase. While $\Gamma_s \approx -1$ means the voltage is almost fully reflected at the inverter side with the phase inverted.

Referring to Figure 3.7, the voltage reflection processes can be divided into four periodic intervals, which will be detailed in the following part.

Interval 1 ($0 < t \leq t_p + t_r$) The inverter output voltage transition V_s starts to travel from the inverter side to the motor terminals through the power cable at the time zero, as shown in Figure 3.7. The inverter output voltage V_s ramps from zero to the dc-link voltage V_{dc} within a rise time t_r. During the first propagation interval ($t < t_p$), the leading edge of V_s travels from the inverter to the motor terminals. Since the voltage V_s has not yet arrived at the motor terminals, the motor terminal voltage is zero. At the time t_p, the leading edge of PWM voltage pulse arrives at the motor terminals and experiences a voltage reflection to the inverter due to the characteristic impedance mismatch between the cable and motor. At the time $t_p + t_r$, the full inverter voltage transition V_s arrived at the motor terminals, the reflected voltage V_{m1}^- is calculated as:

$$V_{m1}^- = \Gamma_m V_s \tag{3.6}$$

Therefore, when accounting for the superposition of inverter voltage and the reflected voltage after $t_p + t_r$, the motor terminal voltage can be calculated as:

$$V_m = V_s + V_{m1}^- = (1 + \Gamma_m) V_s \tag{3.7}$$

Since $\Gamma_m \approx 1$, according to (3.7) the motor terminal voltage is almost twice the inverter voltage.

Interval 2 ($t_p + t_r < t \leq 2t_p + t_r$) After $t_r + t_p$, the reflected voltage transition V_{m1}^- propagates from the motor terminals back to the inverter side. At $t = 2t_p$, the front edge of the reflected voltage V_{m1}^- arrives at the inverter side and experiences a forward voltage reflection to the motor terminals, as shown in Figure 3.7. When $t = 2t_p + t_r$, the full reflected voltage pulse V_{m1}^- arrived at the inverter side. Therefore, the reflected voltage V_{s2}^+ can be calculated as:

$$V_{s2}^+ = \Gamma_s V_m^- \tag{3.8}$$

After the voltage transition reflection arrives, the inverter voltage can be calculated as:

$$V_s = V_{dc} + V_{s2}^+ = V_{dc} + (1 + \Gamma_s)V_m^- \tag{3.9}$$

Since $\Gamma_s \approx -1$, the voltage reflection does not affect the voltage at the inverter side.

Interval 3 ($2t_p + t_r < t \leq 3t_p + t_r$) After $t_r + 2t_p$, the reflected voltage V_{s2}^+ propagates from the inverter side to the motor terminals. The leading edge of the incident voltage V_{s2}^+ arrives at the motor terminals and experience another reflection to the inverter side at $t = 3t_p$, as shown in Figure 3.7. When $t = 3t_p + t_r$, the full reflected voltage V_{s2}^+ arrived at the motor terminals. Therefore, the reflected voltage V_{m2}^- can be calculated as:

$$V_{m2}^- = \Gamma_m V_{s2}^+ \tag{3.10}$$

Therefore, after the voltage reflection, the motor voltage can be calculated as:

$$V_m = (1 + \Gamma_m)V_s + V_{m2}^- = (1 + \Gamma_s\Gamma_m^2)V_{dc} \tag{3.11}$$

Since the $\Gamma_s \approx -1$, the voltage at the motor terminal decreases from $(1 + \Gamma_m)V_s$ to $(1 - \Gamma_m^2)V_{dc}$, as shown in Figure 3.7.

Interval 4 ($3t_p + t_r < t \leq 4t_p + t_r$) After $t_r + 3t_p$, the reflected voltage V_{m2}^- propagates from the motor terminals to the inverter side. At $t = 4t_p + t_r$, the reflected voltage V_{m2}^- arrives at the inverter side and experiences a forward voltage reflection to the motor terminals, as shown in Figure 3.7.

Thereafter, the voltage reflections at the inverter side and motor terminals repeat intervals 1-4. Note that reflection processes continue until the reflected voltage decades to zero due

to the loss in the power cables. Accordingly, the motor terminal voltage oscillates in a damped manner.

Referring to Figure 3.7, the oscillation frequency f_{rwp} of the motor voltage is determined by the wave propagation time t_p in the power cable, which can be calculated as:

$$f_{rwp} = \frac{1}{4t_p} \tag{3.12}$$

Note that, the motor terminals also experience the voltage reflections at the falling edges of the PWM voltage pulses due to the high dv/dt of the voltages and impedance mismatch in the cable-fed motor drive system, which can be analysed using the same bounced diagram shown in Figure 3.7.

Figure 3.8 shows the experimental measured voltages at the inverter side V_{ab} and at the cable terminals, where the cable length is 70m and the cable terminal is open circuit to emulate the unity reflection coefficient [30]. Note that the cable impedance is given in Figure 3.9.

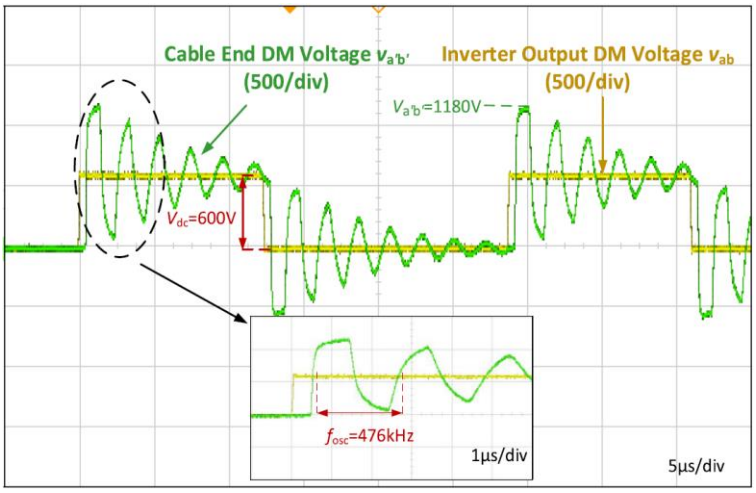


Figure 3.8 Voltages at the inverter side V_{ab} and the cable end $V_{a'b'}$ with a 70m long cable [30].

As can be noticed, the time shift between the two voltages is about 525ns, i.e., the wave propagation time $t_p = 525\text{ns}$. Referring to Figure 3.8, the overvoltage oscillation frequency is 475.7 kHz which is the same with the calculated frequency $1/4t_p$ based on the wave propagation time.

3.3.2 Analysis in Frequency Domain

While the time domain analysis can visually illustrate the RWP, it may not be straightforward to identifying the reflection frequency in a more complicated system [30]. Since the oscillation frequency is one of critical factors to design a proper motor overvoltage mitigation method [33], it is necessary to find a more straightforward method to predict the overvoltage oscillation frequency.

In fact, the motor overvoltage oscillations can be investigated from the perspective of the resonance, where the overvoltage oscillations are due to the resonance in the motor drive system caused by an excitation source. Therefore, the motor overvoltage oscillation frequency can be identified from the systems' anti-resonance frequency. Since the motor terminal overvoltage is trigged by the DM voltage, the motor terminal overvoltage oscillation frequency is determined by the anti-resonance frequency of the DM impedance. While the motor neutral point overvoltage is due to the CM voltage, the oscillation frequency can be identified from the anti-resonance frequency of the CM impedance.

Figure 3.9 shows the impedance of the 70 m long cable [30]. As shown, the anti-resonance frequency is 476 kHz for this cable, which matches with overvoltage oscillation frequency shown in Figure 3.8.

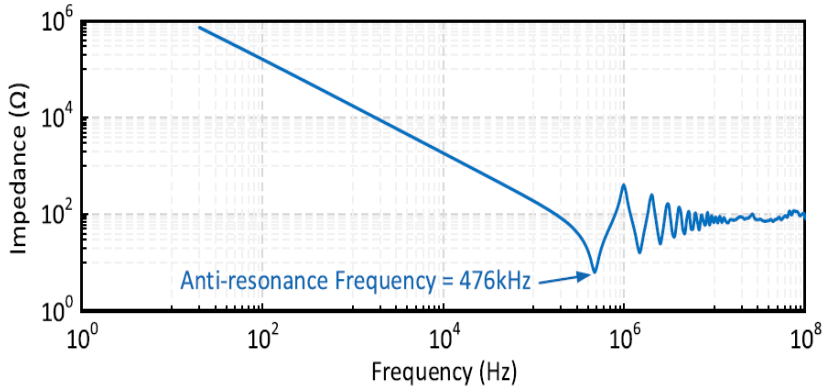
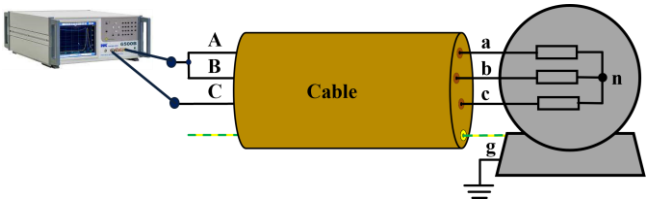
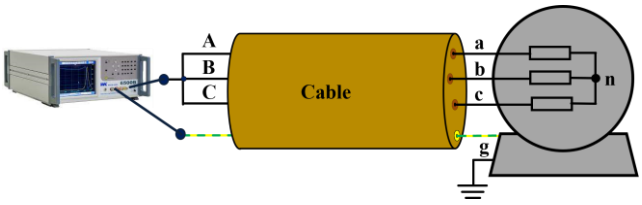


Figure 3.9 The 70m long cable impedance characteristics [30].

Figure 3.10 shows impedance measurement schematic in a long cable-fed motor drive system using an impedance analyser, where Figure 3.10 (a) and (b) show how to measure the DM impedance and CM impedance, respectively.



(a) DM impedance measurement



(a) CM impedance measurement

Figure 3.10 Impedance measurement for the long cable-fed motor drive system.

Generally, the long cable in the motor drive system is looped together to obtain the DM and CM impedance in the lab. Figure **3.11** compares the CM impedance of the straight cable and ring-coiled cable in a 12.5m long 13 AWG unshielded PVC cable-fed motor drive system, where the impedance is measured using the impedance analyser (WK6500B) from Wayne Kerr Electronics. As shown, while the impedance of the looped cable is slightly smaller than that of the straight cable, the anti-resonance frequency for both cases are the same. Therefore, there is no significant difference between the looped cable and straight cable.

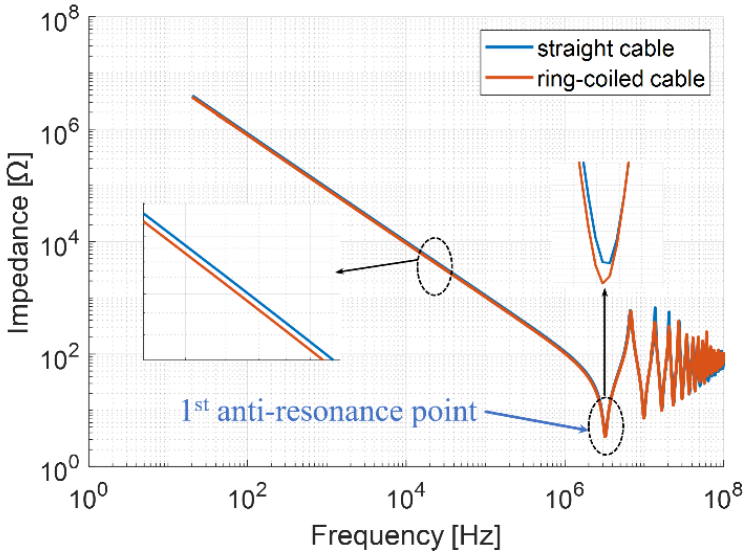


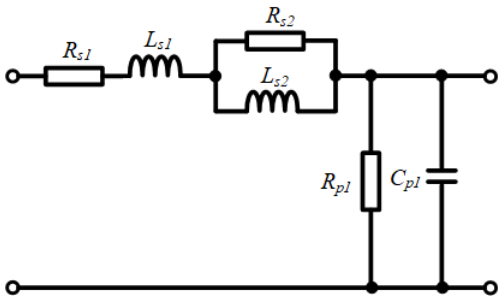
Figure 3.11 The impedance of ring-coiled cable and straight cable.

3.4 Simulation Study

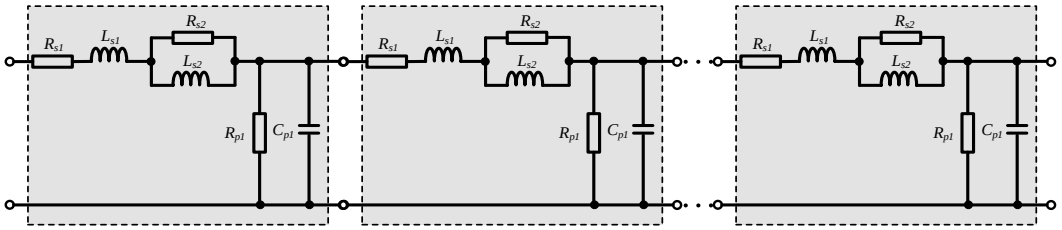
To predict the motor terminal overvoltage and investigate the impact of the cable length, rise time on the RWP, a simulation model is developed on MATLAB/Simulink.

3.4.1 Cable Model

Since the motor overvoltage oscillation frequency is more than hundreds of hertz, the high frequency cable model is needed. This PhD work uses the cable model proposed in [119] for the simulation study, where the model considers the skin effect, proximity effect and AC resistance. Figure **3.12**a shows the single-phase cable model for 1m long cable, where the cable model can precisely predict the reflected wave phenomenon [119]. Note that the long cable model can be obtained by cascading the 1m cable model multiple times depending on the required cable length, as shown in Figure **3.12**b. Note that to emulate the worst case of the RWP in the cable-fed motor drive system, i.e., the reflection coefficient is unity, the motor side is regarded as an open circuit. The cable parameters used for the simulation study are listed in Table **3.1** [33]. The simulation results are shown in Figures **3.13** and **3.14**. Since the cable model has been experimentally verified in [119], only the simulation results are provided in the following section.



(a) 1m cable model



(b) n meter cable model

Figure 3.12 The cable model proposed in [150].

Table 3.1 Main cable parameters of one meter cable [33].

Symbol	Value	Symbol	Value
R_{s1}	0.017 Ω	R_{s2}	0.143 Ω
L_{s1}	0.38 µH	L_{s2}	0.16 µH
R_{p1}	34.75 MΩ	C_{p1}	64 pF

3.4.2 Impact of the Rise Time and Cable Length

Figure **3.13** shows the simulation result of the motor terminal voltage at different cable lengths and rise times, where the results show good match with the theoretically calculated results in [114].

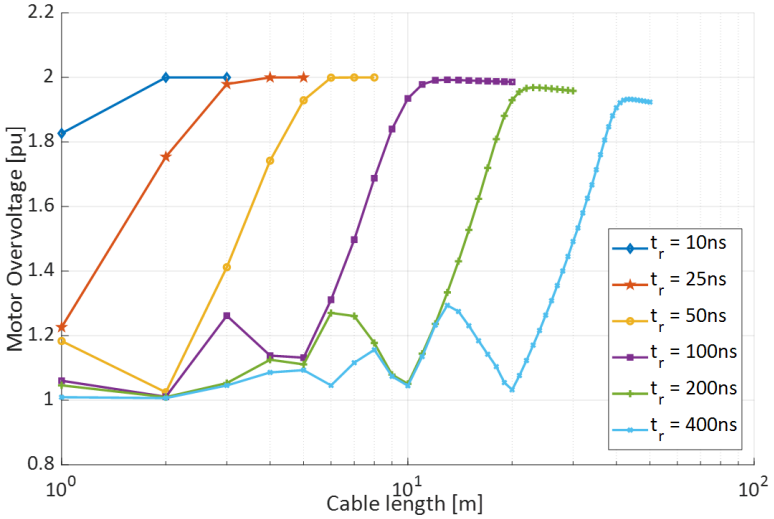


Figure 3.13 Motor terminal voltage at rise and fall times t_r, and different cable lengths in the long cable-fed motor drive system.

As shown, for a given cable length, the motor terminal voltage increases with the rise and fall times decreasing, where the maximum motor terminal overvoltage is 2 pu. For a given rise time, the motor terminal voltage increases with the cable length. Since the switching speed of SiC MOSFETs is usually less than 100 ns, the motor terminal overvoltage can reach to 2 pu within several meters of cable, as shown in Figure 3.13. Therefore, the motor terminal overvoltage is more common and severe in the fast-switching SiC-based cable-fed motor drive system.

3.4.3 Double Pulsing Effects

In the long cable-fed motor drive system, the double pulsing effect can be experimentally observed when the switching frequency and/or the modulation index are very high, i.e., the motor terminal overvoltage can reach greater than twice inverter voltage when the complementary voltage transition pulses of the inverter output voltage are closely spaced [33], [116], [117].

Figure 3.14 shows the simulation results for the double pulsing effect. As can be noticed, the first inverter voltage pulse propagates from the inverter side to the motor terminals through the cable, it experiences voltage doubling upon arrival at the motor terminals. Since there is not sufficient time for the oscillation decaying, the voltage doubling of the next incident inverter pulse accumulates with the undecayed oscillation (of the previous inverter pulse). With this cumulative effect, the motor terminal voltage exceeds two times the inverter voltage.

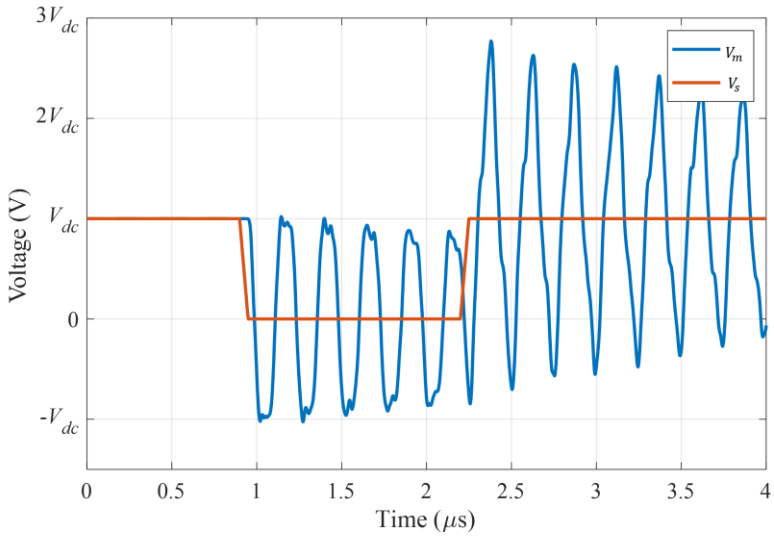


Figure 3.14 Double pulsing effect in adjustable speed drives.

3.5 Conclusion

This chapter has studied the RWP in WBG-based long cable-fed adjustable speed drives. The RWP has been analysed in time domain and frequency domain. The cable model and the effective factors on the motor terminal overvoltage have been presented. The conclusions of this chapter are the following:

- The motor overvoltage oscillations are due to the RWP in the long cable-fed motor drive system, caused by the high steep voltage PWM pulses (high dv/dt) and the impedance mismatch in the motor drive system. Two typical motor overvoltage can be observed, i.e., the overvoltage at the motor terminals and the overvoltage at the motor neutral point.
- The overvoltage oscillation frequency can be obtained by the wave propagation time t_p in the cable i.e., the frequency is $1/4t_p$.
- The motor overvoltage can be analysed in the frequency domain, i.e., the motor overvoltage oscillations are due to the resonance in the motor drive system caused by an excitation source, where the oscillation frequency can be identified from the anti-resonance frequency of the motor drive system.
- The motor overvoltage oscillations are more common and severe in SiC-based cable-fed motor drive system due to the fast-switching speed. With switching frequency and modulation index increasing, the motor terminal overvoltage would exceed two times the inverter voltage.

Chapter 4

Impact of Parasitic Capacitance of Switching Devices and Load Current on the Switching Transient and Motor Terminal Overvoltage Oscillations

This chapter aims to address the research objective 2: Investigate the impact of parasitic capacitance of switching devices on motor terminal overvoltage in cable-fed motors using SiC inverters.

The main content of this chapter has been published by the author in the following publication:

W. Zhou, M. S. Diab and X. Yuan, "Impact of Parasitics and Load Current on the Switching Transient Time and Motor Terminal Overvoltage in SiC-Based Drives," in *2020 IEEE Energy Conversion Congress and Exposition* (*ECCE*), 2020, pp. 225-232.

4.1 Introduction

For a given adjustable speed drive, the rising and falling transitions of the inverter output voltage is one of the critical factors affecting the motor terminal overvoltage oscillations due to the RWP [48]. Through a body of literature, the double pulse test (DPT) based on a half-bridge circuit has been widely used to investigate the RWP in SiC-based motor drive systems, where it solely focuses on the rising edge of the inverter output voltage waveform [31], [48]. However, it is not the case for the actual motor drive systems, where the motor is usually supplied by a three-phase power converter, i.e., the output voltage is synthesized by the two-phase legs rather than the half-bridge leg [48]. Therefore, the conventional method using the DPT to investigate the RWP is not accurate enough to reveal the actual case. The experimental results based on the DPT may overestimate or underestimate the motor terminal overvoltage oscillations, resulting in an inadequate design of the motor drive system. This chapter systematically investigates the motor terminal overvoltage

oscillations in a three-phase motor drive system, considering the impacts of parasitic elements of the switching devices and load current during the switching transitions.

4.2 Modelling of the Switching Transitions

The rise and fall times of the inverter output voltage are affected by the load current and the parasitic capacitance of the switching devices, i.e., the rise and fall times varies for the switching cycles in the fundamental cycles. In this section, the analysis of the switching transitions of the inverter output voltage is first carried out for a half-bridge inverter and then extended for a three-phase system.

Figure 4.1 shows the circuit schematic of a standard SiC-based half-bridge inverter employing two SiC MOSFETs, where P and N denote the positive and negative dc-link respectively. The parasitic capacitance of the switching devices, i.e., the drain-source capacitance (C_{ds}), the drain-gate capacitance (C_{dg}) and the gate-source capacitance (C_{gs}) are included. The current flowing out from the node A is defined as positive, as shown in Figure 4.1.

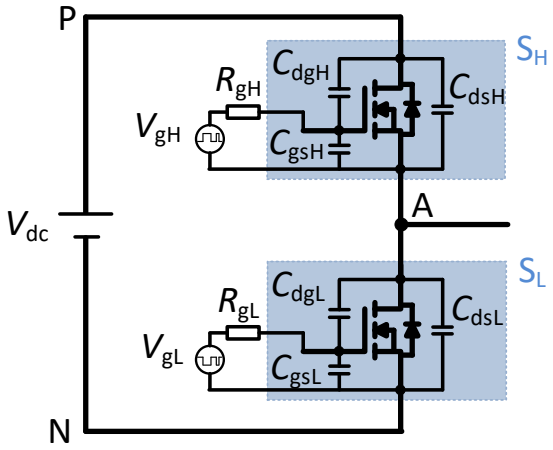


Figure 4.1 A SiC-based half-bridge circuit.

4.2.1 Switching Transitions of SiC MOSFETs in the Half-bridge Circuit

Figure **4.2** illustrates the detailed switching transitions of the half-bridge converter when the output current is positive, where Figure **4.2** (a)-(c) show the switching commutation from the lower switch S_L to the upper switch S_H characterized by intervals 1 and 2, while Figure **4.2** (e)-(f) show the opposite case characterized by intervals 3 and 4. Note that the phase current is considered constant during the switching transitions, the parasitic

capacitance of the switching devices is assumed to remain fixed. The parasitic inductance of the dc-link is not considered for the following analysis. The switching devices are assumed to be turn-ON/OFF simultaneously with the gate signal applied to them. In addition, the rising and falling times of the output voltage are assumed to be shorter than deadtime during the commutation process.

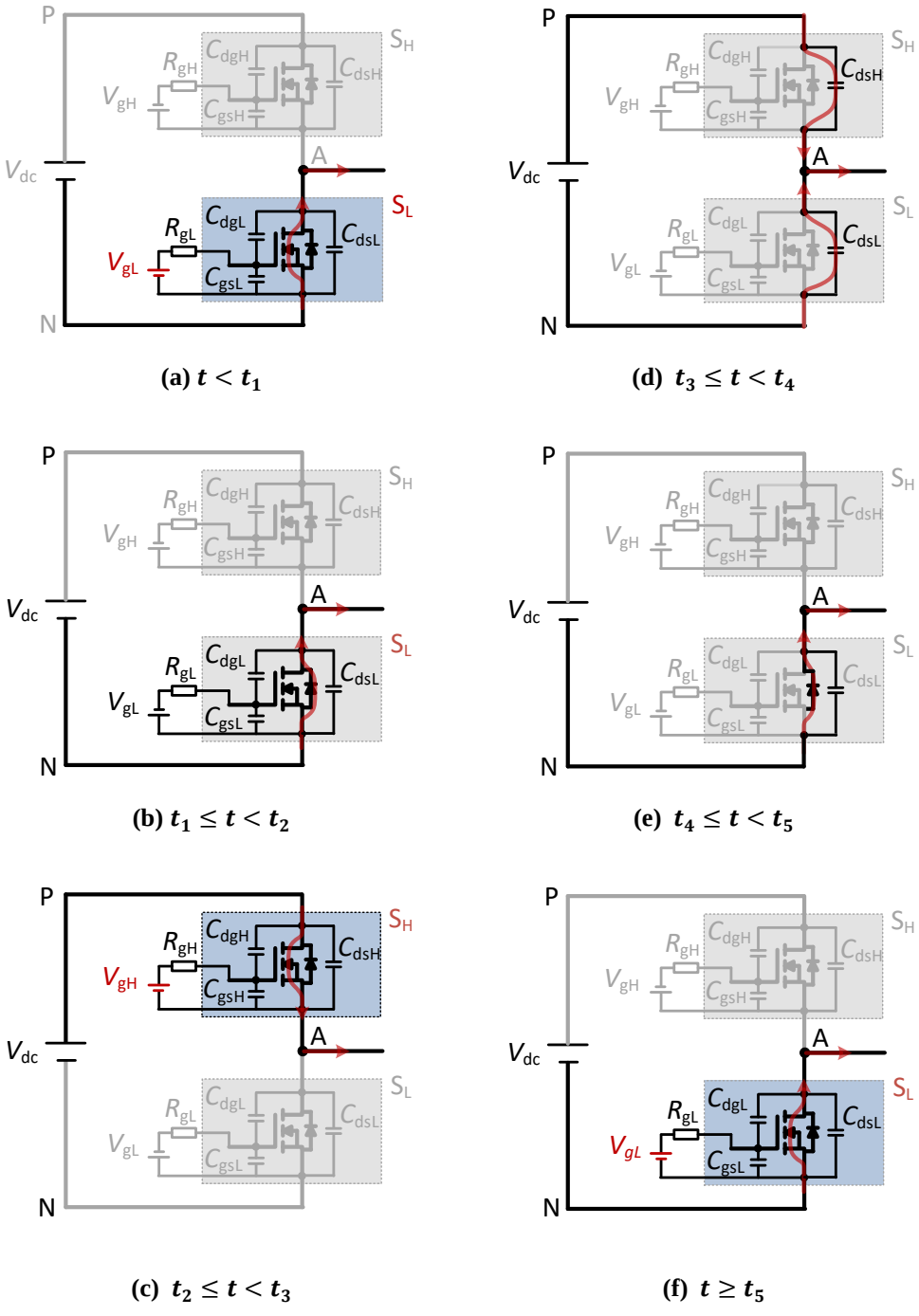


Figure 4.2 Switching transitions of SiC half-bridge inverter.

The switching commutation process can be divided into four intervals and the corresponding output voltage V_{AN} is shown in Figure 4.3 (a). Note that the output voltage V_{AN} is the voltage between the output node A and the negative dc-link N, as shown in Figure 4.2.

Interval 1 ($t_1 \leq t < t_2$) [Figure 4.2 (a) and (b)] Referring to Figure 4.2 (a), before turning OFF the lower switch S_L, the phase current flows through its channel where the switching device S_L works in "synchronous rectification mode", the output voltage V_{AN} is 0V. At the time t_1 the lower switching device S_L is turned OFF, the phase current is diverted from the device channel to its antiparallel freewheeling diode, as shown in Figure 4.2 (b). Since the current still flows through the lower switching device S_L, the actual output voltage V_{AN} remains unchanged at 0V, as shown in Figure 4.3 (a).

Interval 2 ($t_2 \leq t < t_3$) [Figure 4.2 (c)] After a dead time t_{dead}, i.e., $t = t_2$, the upper switch S_H is turned-ON with the turn-ON gate signal applying to it, allowing the phase current to transfer from the lower switch S_L to the upper switch S_H, as shown in Figure 4.2 (c). Meanwhile, the output voltage V_{AN} traverses from zero to the dc-link voltage V_{dc} simultaneous with the turn-ON gate signs of S_H. It should be noted that the switching time of the output voltage V_{AN} from zero to V_{dc} is governed by the adopted gate resistance and switching device's characteristics. Generally, the switching speed of SiC MOSFETs is extremely fast, which is within 10-100 ns. Therefore, the rising edge of V_{AN} can be denoted as a step edge, as shown in Figure 4.3 (a).

Interval 3 ($t_3 \leq t < t_4$) [Figure 4.2 (d)] Before $t = t_3$, the upper switching device S_H conducts the full load current. At the time t_3, S_H is turned OFF with the turned-OFF gate signal applying to it. However, the inverter output voltage V_{AN} does not immediately decrease to 0V due to the impact of the parasitic capacitance of the switching devices. Referring to Figure 4.2 (d), the phase current charges the output capacitance of S_H while discharges that of S_L. Therefore, the inverter output voltage V_{AN} tardily decreases to 0V, where the fall time t_{fall} depends on the parasitic capacitance of the switching devices and the instantaneous phase current I_{phase}, as:

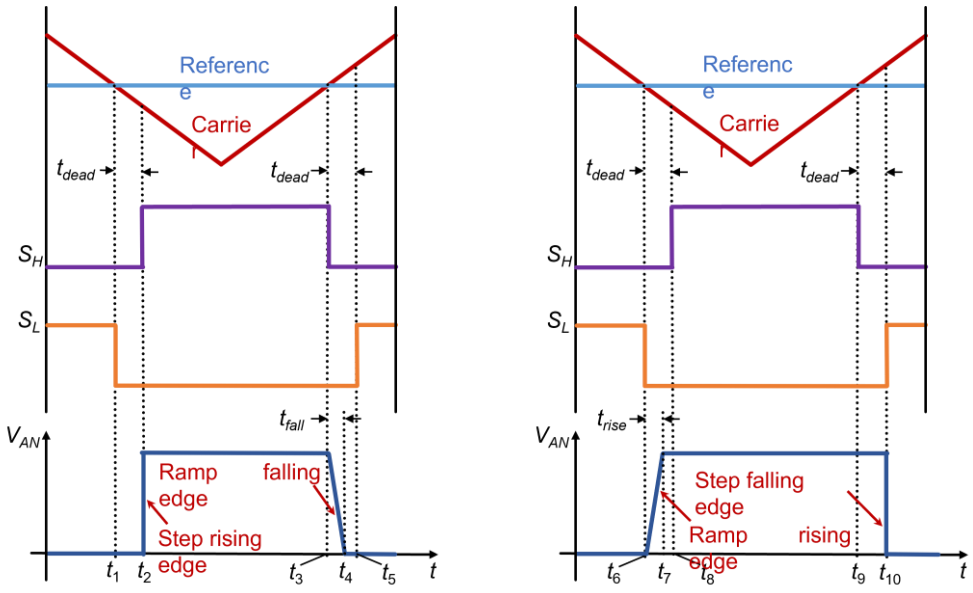
$$t_{fall} = \frac{2C_{coss}\, V_{dc}}{I_{phase}} \tag{4.1}$$

where, $C_{oss} = C_{ds} + C_{gd}$ is the output capacitance of the SiC MOSFETs. Since the output capacitance is assumed to be constant during the switching process, the output voltage of the inverter falls in a linear manner.

After the time t_{fall}, the inverter output voltage V_{AN} reaches to 0 V as the phase current fully discharges the output capacitance of S_L and charges the output capacitance of S_H. Referring to Figure 4.2 (e) the entire phase current flows through the antiparallel diode of the lower switch S_L. Therefore, the falling edge of the inverter output voltage V_{AN} can be denoted as a ramp edge, as shown in Figure 4.3 (a).

Interval 4 ($t \geq t_5$) [Figure 4.2 (f)] After the deadtime t_{dead}, i.e. $t = t_5$, S_L is turned on as the turn-ON gate signal is applied to it causing the load current to divert from the antiparallel diode to the switching device channel and V_{AN} remains at 0 V, as shown in Figure 4.3 (a).

In a similar commutation process, when the phase current is negative, the rising edge of the output voltage V_{AN} is affected by the load current and parasitic capacitance of the switching devices, while the falling edge is governed by the adopted gate resistance and switching devices' characteristics. Therefore, the rising edge of V_{AN} can be denoted as a ramp edge, while the falling edge can be denoted as a step edge, as shown in Figure 4.3 (b).



(a) load current is positive **(b) load current is negative**

Figure 4.3 The output waveform V_{AN} of the half bridge inverter.

4.2.2 Line Voltages of Three-phase SiC Inverter

Figure 4.4 shows a three-phase SiC-based inverter-fed motor drive system. Note that the earth wire is not shown in the figure. In this section, only the line voltage V_{AB} is analyzed because the switching mechanism of the other line voltages of the three-phase inverter is the same.

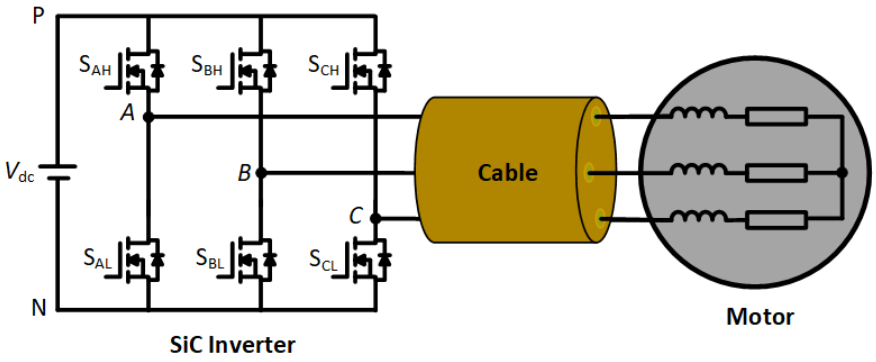


Figure 4.4 Three-phase SiC inverter-fed motor drive system.

Referring to Figure 4.4, the line voltage V_{AB} can be given as:

$$V_{AB} = V_{AN} - V_{BN} \tag{4.2}$$

where, V_{AN} and V_{BN} are the output voltage of phase *A* and phase *B* with respective to the negative dc-link (N), respectively. Since the line voltage V_{AB} is calculated as the difference between the output voltage of phase *A* and phase *B*, the switching transitions of V_{AB} are affected by the polarities of the phase currents i_A and i_B.

Figure 4.5 shows the current waveform of phase *A* and phase *B* (i_A and i_B) for one fundamental cycle. As shown, the phase currents can be divided into four regions according to the polarity of alternation. Figure 4.6 depicts the theoretical phase- and line-voltage waveforms at these four regions.

Region I ($i_A > 0, i_B < 0$) [Figure 4.6 (a)]: in this region, V_{AN} has a similar voltage waveform with Figure 4.3 (a) and V_{BN} has a similar waveform with Figure 4.3 (b). Therefore, the line voltage V_{AB} is synthesized as shown in Figure 4.6 (a), where V_{AB} varies between 0 and V_{dc}. Note that the rising edge of V_{AB} causes the voltage ascending from 0 to V_{dc}, while the falling edge of V_{AB} causes the voltage descending from V_{dc} to 0, as shown in Figure 4.6 (a). In this case, only the motor terminal overvoltage oscillations caused by

the rising edge of V_{AB} matters the resultant motor terminal overvoltage may exceed the design voltage level of the stator winding insulation. Referring to Figure 4.6 (a), the rising edge of V_{AB} is much faster than the falling edge, being affected by the adopted gate resistance and the switching devices' characteristics. Therefore, in this region, the motor terminal overvoltage is only affected by the adopted gate resistance and switching devices' characteristics.

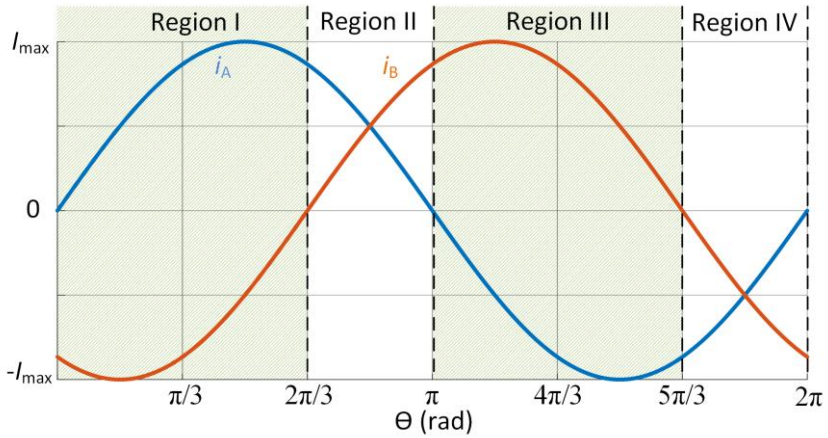


Figure 4.5 Classification of phase currents based on their polarities.

Region II ($i_A > 0, i_B > 0$) [Figure 4.6 (b) and (c)]: in this region, both V_{AN} and V_{BN} have similar waveforms with Figure 4.3 (a) as the phase currents are positive. If the duty cycle of phase *A* is larger than that of phase *B*, the line voltage $V_{AB} \geq 0$, as shown in Figure 4.6 (b). Oppositely, i.e., when the duty cycle of phase *A* is smaller than that of phase *B*, $V_{AB} \leq 0$, as shown in Figure 4.6 (c). Common to both figures, V_{AB} consists of a rectangle voltage waveform and a trapezoid voltage waveform. Therefore, both edges of V_{AB} are affected either by the gate resistance and the switching devices' characteristics or by the load current and parasitic capacitance of the switching devices. In this case, the motor terminal overvoltage oscillations caused by the rising and falling edges can be affected either by the adopted gate resistance and the switching devices' characteristics or the load current and parasitic capacitance of SiC MOSFETs.

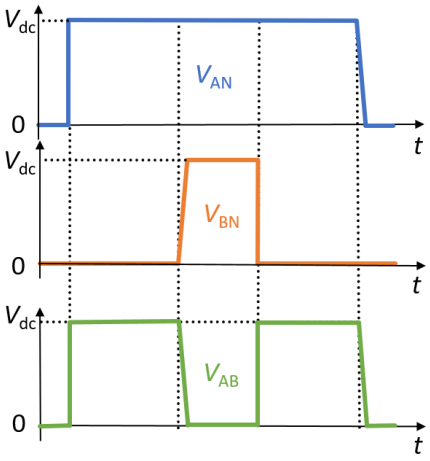
Region III ($i_A < 0, i_B > 0$) [Figure 4.6 (d)]: Referring to Figure 4.6 (d), the line voltage $V_{AB} \leq 0$, and the rising edges of V_{AB} are slower than the falling edges, being affected by the load current and the parasitic capacitance of the switching devices. As can be noticed, the rising edge of V_{AB} results in the voltage ascending from $-V_{dc}$ to 0V and the falling edge of V_{AB} results in the voltage descending from 0V to $-V_{dc}$. Therefore, only the motor terminal overvoltage oscillations caused by the falling edge matters due to the resultant

overvoltage imposes higher voltage stress across the motor stator windings. In this case, the motor terminal overvoltage is only affected by the adopted gate resistance and switching devices' characteristics in this region.

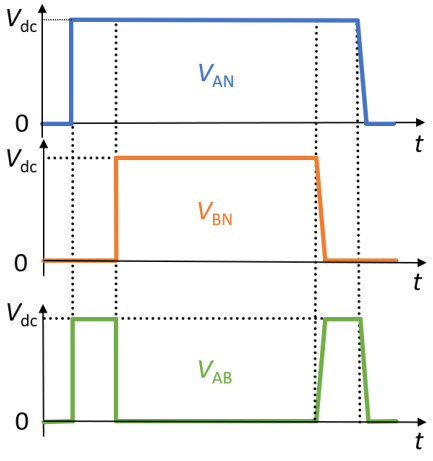
Region IV ($i_A < 0, i_B < 0$) [Figure 4.6 (e) and (f)]: both V_{AN} and V_{BN} have similar waveform with Fig. 6(b) since the phase currents are negative. Figure 4.6 (e) shows the line voltage V_{AB} when the duty cycle of phase A is larger than that of phase B, while Figure 4.6 (e) shows the line voltage waveform for the opposite case. Common to both figures, V_{AB} consists of a rectangle waveform and a trapezoid waveform. That is, the rising and falling edges of V_{AB} are affected either by the gate resistance and the switching devices' characterises or by the phase current and parasitic capacitance of the switching devices. In this case, the motor terminal overvoltage oscillations caused by the rising and falling edges can be either affected by the gate resistance and the switching devices' characteristics or the load current and parasitic capacitance of the switching devices.

In summary, the slope of the output voltages of three-phase SiC inverter have different rise and fall times depending on phase current polarities, phase-leg duty cycles and the devices' parasitic capacitance. For a given motor drive system, the motor terminal overvoltage is affected by the rise and fall times when the times are less than one third of the wave propagation time. Therefore, the motor terminal overvoltage is only pronounced at certain voltage transitions. When the current polarity of phase *A* and phase *B* is different, i.e., Region I and Region IV, the motor terminal overvoltage is only affected by the gate resistance and the switching devices' characteristics. While, when the current polarity is the same, i.e., Region II and Region III, the motor terminal overvoltage can be affected either by the gate driver and the switching devices' characteristics or the load current and parasitic capacitance of the switching devices.

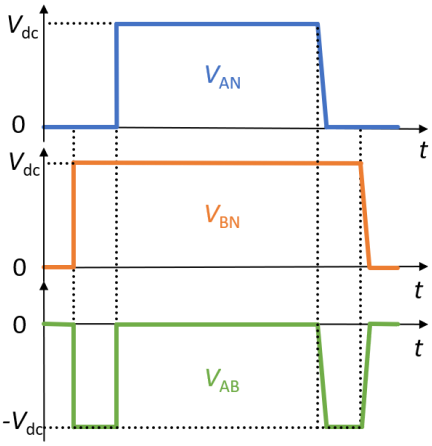
Therefore, the conventional DPT, which only focuses on the rising edge of the output voltage, cannot be accurately used to reveal the motor terminal overvoltage oscillations due to the RWP in three-phase inverter-fed motor drive system. The motor terminal overvoltage oscillations should be examined under different current load condition.



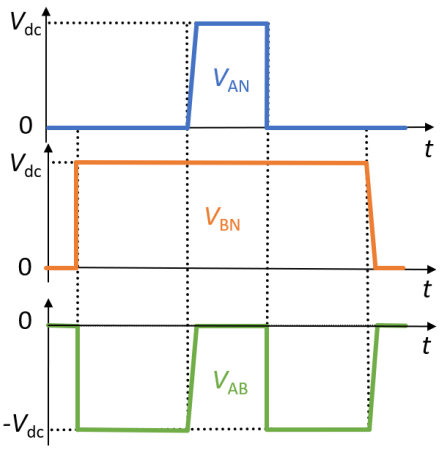
(a) region I



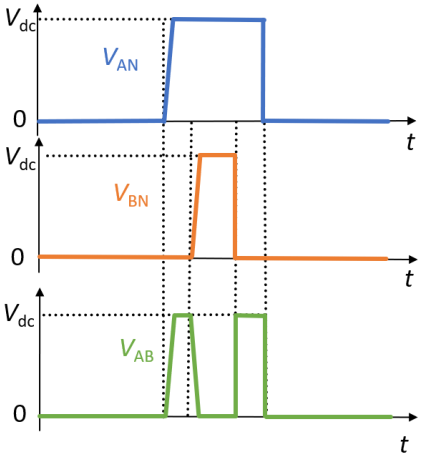
(b) region II and $V_{AN} > V_{BN}$



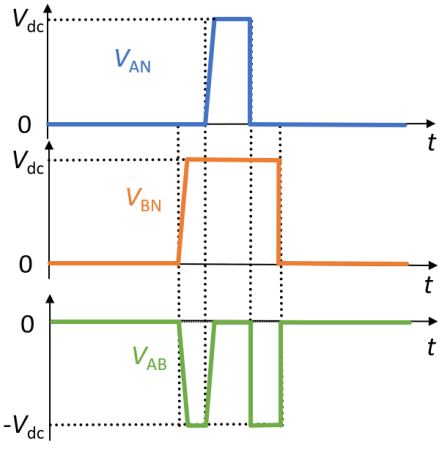
(c) region II and $V_{AN} < V_{BN}$



(d) region III



(e) region IV and $V_{AN} > V_{BN}$



(f) region IV and $V_{AN} < V_{BN}$

Figure 4.6 Switching transitions of the line voltage V_{AB} in different region.

4.3 Experimental Verification

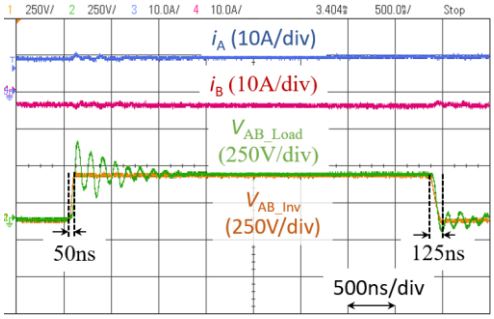
To verify the theoretical analysis, a three-phase inverter based on SiC MOSFETs (C2M0040120D) from Wolfspeed is built in the laboratory, as shown in Figure 4.7. The SiC MOSFETs are driven by gate drivers with 25 Ω gate resistance. Note that the gate driver is implemented with a DC/DC converter (MGJ2D051500SC), an optocoupler (ACPL-W484), and a driver (IXDN609SI). In this case, the switching time is about 50 ns. The inverter is supplied from 300 V dc-link and modulated under the conventional SPWM, where the switching and fundamental frequencies are 40 kHz and 50 Hz, respectively. The inverter is connected via 5 m long cable terminated to a three-phase *RL* load to emulate the RWP in the long cable-fed motor drive system, where $R_{phase} = 11\,\Omega$, and $L_{phase} = 1.2mH$.

Figure 4.7 The three-phase SiC inverter prototype.

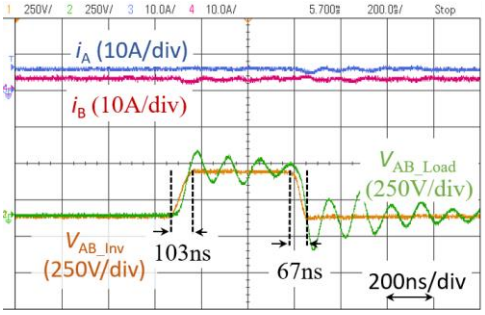
Figure 4.8 shows the experimental results of switching transitions of phase currents i_A and i_B, the inverter output line voltage V_{AB_Inv} and the load terminal line voltage V_{AB_Load} at different regions, where Figure 4.8 (a) shows the result for region I, Figure 4.8 (b) and (c) for region II, Figure 4.8 (d) for region III, and Figure 4.8 (e) for region IV, respectively. It can be noticed that the experimental results for the inverter output voltages show good agreement with the theoretical waveforms presented in Figure 4.6.

Referring to Figure 4.8, significant overvoltage oscillations exist across the load terminals due to the RWP caused by the characteristic impedance mismatch between the cable and the load. However, the load terminal voltage varies in different operation regions. This because the rise and fall times of the inverter output voltage are affected either by the gate

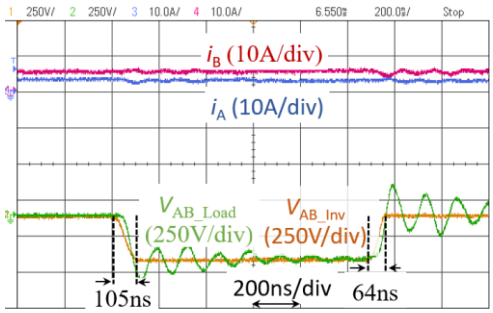
driver and the switching devices' characteristics or the load current and parasitic capacitance of the switching devices, as previously analysed.



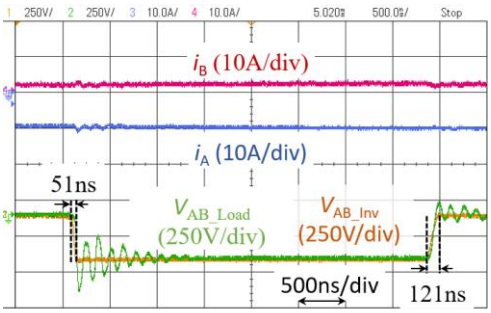
(a) region I



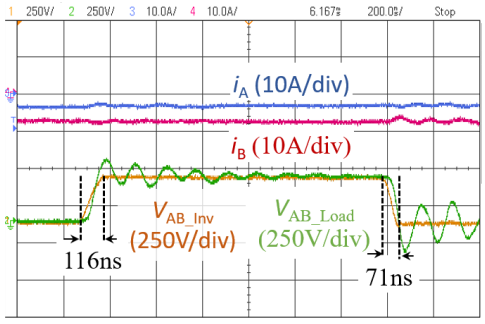
(b) region II and $V_{AN} > V_{BN}$



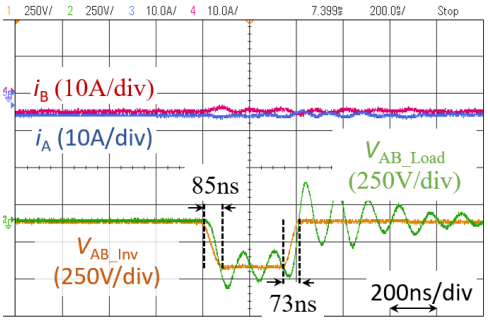
(c) region II and $V_{AN} < V_{BN}$



(d) region III



(e) region IV and $V_{AN} > V_{BN}$



(f) region IV and $V_{AN} < V_{BN}$

Figure 4.8 Experimental results of switching transitions of the line voltage V_{AB} of a three-phase SiC inverter supplying a three-phase load through power cables in different region.

As shown in region I (Figure 4.8 (a)), the line voltage of the inverter $V_{AB\_Inv} > 0$ and the fall time of V_{AB_Inv} is longer than the rise time, where the rise and fall times are about 50ns and 125ns, respectively. This is because the rise time is governed by the gate resistance and the switching devices' characteristics and the fall time is affected by the load current and

the parasitic capacitance of the switching devices. The fast rise time of V_{AB_Inv} leads to pronounced overvoltage oscillations across the load terminals, as shown in Figure 4.8 (a). However, the line voltage V_{AB_Inv} shows the opposite trend in region III, as shown in Figure 4.8 (d). Referring to Figure 4.8 (d), $V_{AB\_Inv} < 0$ and the fall time is about 50ns which is shorter than the rise time (121 ns). This is because in region III, the fall time is governed by the adopted gate resistance and the switching devices' characteristics, and the rise time is affected by the load current and the parasitic capacitance of the switching devices.

Figure 4.8 (b) shows the experimental results in region II when $V_{AN} > V_{BN}$. As can be noticed, the rise time and fall time of V_{AB_Inv} are 64 ns and 105 ns, respectively. Both the rise and fall times are longer than devices' switching time because the rise and fall times are affected by the load current and parasitic capacitance of the switching devices. Similar results can be observed in Figure 4.8 (c), (e) and (f). The discrepancy between the rise and fall times can be explained by (4.1) where the higher current leads to shorter transient time.

4.4 Conclusion

This chapter has studied the impacts of load current and parasitic elements of switching devices on motor terminal overvoltage oscillations caused by the high dv/dt and impedance mismatch. The switching commutation processes for a three-phase inverter are analysed supported with experimental verification, considering the impact of the parasitic capacitance. The conclusions of this chapter are the following:

- The conventional DPT is not sufficiently enough to investigate the RWP since it only shows the single-phase leg output voltage which cannot represent actual three-phase adjustable speed system. This chapter shows that to effectively investigate the impact of devices' parasitic capacitance and load current on the RWP, the output line voltage of the three-phase inverter should be considered under different current region.
- The motor terminal overvoltage shows non-uniform distribution due to the rise and fall times of the output voltage of SiC-based inverters varies in different switching cycles, where the rise and fall times of the inverter output voltage are affected by the load current direction and amplitude and parasitic capacitance of the switching devices.
- When the phase currents have the same polarity, the motor terminal overvoltage related to the slope of the output PWM pulse is only affected by the adopted gate

resistance and the switching devices' characteristics. Whereas, when phase currents have different polarities, the motor terminal overvoltage is affected either by the gate resistance and the switching devices' characteristic or the load current value and device parasitic capacitance.

Chapter 5
Waveform Shaping to Combat the Motor Terminal Overvoltage: Q3L PWM Scheme

This chapter aims to meet Research Objective 3 with the following subtasks listed below:

RO 3.1 Reveal the essence of the overvoltage mitigation mechanism of the Q3L PWM scheme in both time domain and frequency domain.

RO 3.2 Investigate the impact of the parasitic of switching devices on the mitigation of motor terminal overvoltage oscillations using the Q3L PWM T-type inverter.

RO 3.3 Develop the Q3L PWM scheme using the SiC module-parallel inverter to mitigate the motor terminal overvoltage as well as extend the device current capacity.

RO 3.4 Experimental verification of the Q3L PWM scheme using SiC T-type inverter and SiC module-parallel inverter.

The main content of this chapter has been published by the author in the following publication:

W. Zhou, M. Diab and X. Yuan, "Impact of Parasitic and Load Current on the Attenuation of Motor Terminal Overvoltage in SiC-Based Drives," *IEEE Transactions on Industry Applications*, vol. 58, no. 2, pp. 2229-2241, March-April 2022, doi: 10.1109/TIA.2022.3141703.

5.1 Introduction

Slowing down the dv/dt of the PWM voltage pulses can effectively mitigate the motor terminal overvoltage oscillations [125]. Through a body of literature, the dv/dt filter is the mainstream approach to attenuate the motor terminal overvoltage oscillations [126]. However, the essence of the overvoltage mitigation mechanism is not clear in the literature.

In fact, the motor terminal overvoltage oscillations can be entirely mitigated if there is no excitation source evoking the overvoltage oscillations in the motor drive system [33]. The essence of slowing down the dv/dt of the PWM voltage pules is addressing the motor terminal overvoltage at the excitation source, i.e., by actively shaping the excitation source, the consequence motor terminal overvoltage oscillations will not be excited anymore. Addressing the motor terminal overvoltage at source can be achieved by either passive dv/dt filter or active filter-less methods. Due to the disadvantages of passive filter such as additional power loss, large size and weight, this chapter investigates the filter-less active waveform shaping method, i.e., the Q3L PWM scheme, to mitigate the motor terminal overvoltage oscillations. The essence of the motor terminal overvoltage mitigation mechanism of the Q3L PWM scheme is analysed both in time domain and frequency domain. The detailed implementation of the Q3L PWM scheme using a T-type inverter and a module-parallel inverter are presented.

5.2 The Concept of the Q3L PWM Scheme

The Q3L PWM scheme is first proposed in [135] to mitigate the motor terminal overvoltage in a Si IGBT based long cable-fed motor drive system. The key idea of the Q3L PWM scheme is to break the rising and falling edges of the PWM voltage pules into two identical voltage steps separated by a dwell time t_{dwell} [134]. With a proper dwell time t_{dwell} setting, the reflected voltage oscillations of the first voltage step can be cancelled by that of the second. Therefore, the motor terminal overvoltage oscillations can be effectively mitigated. Since the reshaped rising and falling edges of the PWM voltage pulses have three voltage steps during switching transitions, i.e., low level (0), medium level ($\frac{V_{dc}}{2}$), and high level (V_{dc}), the PWM voltage waveform is referred as the Q3L PWM voltage waveform.

5.2.1 Analysis in Time Domain

Figure 5.1 elucidates the voltage reflection process and corresponding voltage waveform of the Q3L PWM scheme using a bounced diagram, where it assumes the wave propagation time t_p from the inverter side to the motor terminals is much longer than the rise time t_r of the inverter output voltage, and the reflection coefficients $\Gamma_s = -1$ and $\Gamma_m = 1$, i.e., voltage pulses experience full reflection at the inverter side and motor terminals. Referring to Figure 5.1, the inverter output voltage V_s consists of two identical voltage steps V_{s1} and V_{s2} with the rise time t_r and amplitude $\frac{V_{dc}}{2}$. The time shift between the two voltage steps

V_{s1} and V_{s2} is denoted as the dwell time t_{dwell}. The voltage reflection process of the Q3L PWM scheme can be divided into three intervals, as shown in Figure 5.1.

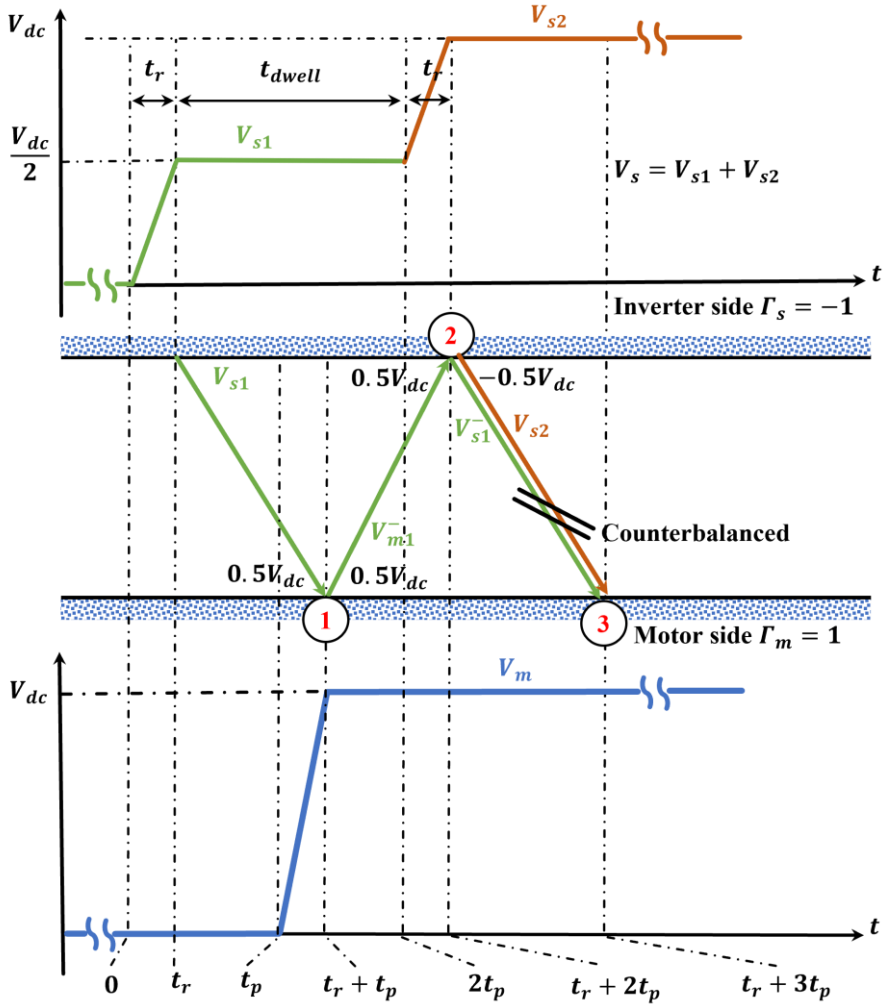


Figure 5.1 A bounced diagram of the Q3L PWM scheme.

Interval 1 ($0 < t \leq t_r + t_p$) Referring to Figure 5.1, at $t = 0$, the first segment of the inverter output voltage V_{s1} starts to propagate from the inverter side to the motor terminals through power cables where V_{s1} ramps up from zero to $\frac{V_{dc}}{2}$ within a rise time t_r. After a propagation time t_p, the leading edge of the voltage V_{s1} arrives at the motor terminals. At $t_r + t_p$, the full voltage V_{s1} arrives at the motor terminals and experiences a voltage reflection due to the characteristic impedance mismatch between the cable and motor, where the resultant voltage is V_{m1}^-. Since the amplitude of V_{s1} is $\frac{V_{dc}}{2}$, and the reflection coefficient at the motor terminals $\Gamma_m = 1$, the amplitude of the resultant V_{m1}^- is $\frac{V_{dc}}{2}$.

Therefore, after the first voltage reflection, the motor terminal voltage V_m ascends from zero to V_{dc}, as shown in Figure 5.1.

Interval 2 ($t_r + t_p < t \leq t_r + 2t_p$) After $t_r + t_p$, the reflected voltage V_{m1}^- propagates from the motor terminals toward the inverter side. The motor terminal voltage remains unchanged at V_{dc} during this interval. Referring to Figure 5.1, after another propagation time t_p, i.e., $t = t_r + 2t_p$, the full reflected voltage V_{m1}^- arrives at the inverter side and experiences a voltage reflection due to the characteristic impedance mismatch between the cable and inverter. Since $V_{m1}^- = \frac{V_{dc}}{2}$ and the reflection coefficient at the inverter side $\Gamma_s = -1$, the amplitude of the reflected voltage V_{s1}^- is $-\frac{V_{dc}}{2}$.

Interval 3 ($t > t_r + 2t_p$) At $t = t_r + 2t_p$, if another voltage V_{s2} with an amplitude $\frac{V_{dc}}{2}$ starts to propagate from the inverter side to the motor terminals, the voltage V_{s2} will be countered by the reflected voltage V_{s1}^-, as shown in Figure 5.1. Therefore, no voltage will propagate to the motor terminals after the time $t_r + 2t_p$, and the motor terminal voltage remains constant at V_{dc}. That is, the motor terminals will not experience any overvoltage oscillations, as shown in Figure 5.1.

According to the voltage reflection process discussed above, the optimum dwell time t_{dwell} to entirely mitigate the motor terminal overvoltage is:

$$t_{dwell} = 2t_p \tag{5.1}$$

In a similar overvoltage mitigation mechanism, if the falling edges of the inverter output voltages are shaped as a Q3L PWM waveform with the dwell time $t_{dwell} = 2t_P$, the motor terminals will not experience any overvoltage oscillations either.

For a given adjustable speed drive system, the motor terminal overvoltage due to the RWP is proportional to the inverter output voltage (the excitation source). Therefore, the motor terminal overvoltage mitigation mechanism can be further analysed using the superposition principle in the time domain, as illustrated in Figure 5.2.

Referring to Figure 5.2, the inverter output voltage V_s is composed of two identical voltages V_{s1} and V_{s2}, as:

$$V_s = V_{s1} + V_{s2} \tag{5.2}$$

where, the amplitudes of V_{s1} and V_{s2} are the $\frac{V_{dc}}{2}$.

The two voltage steps V_{s1} and V_{s2} are transmitted from the inverter side to the motor terminals experiencing voltage reflections as a result of the RWP in the motor drive system.

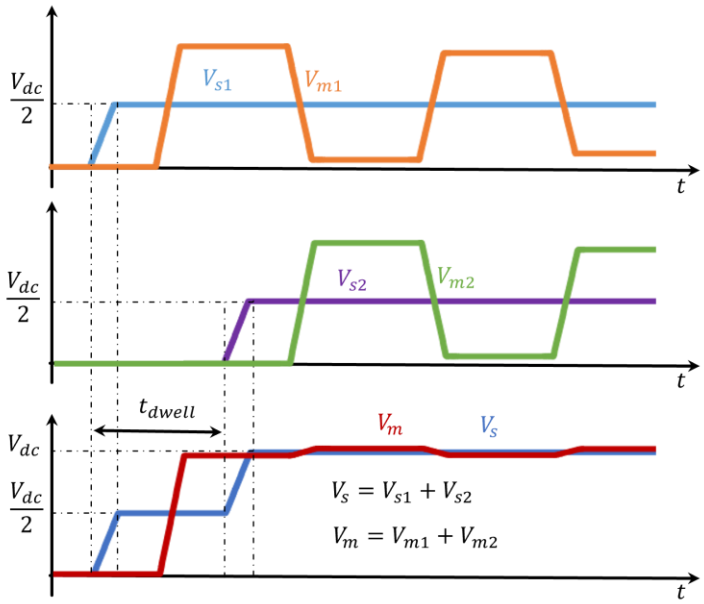


Figure 5.2 Overvoltage mitigation of the Q3L PWM using the superposition principle.

Accordingly, the resultant motor terminal voltage V_m can be given as:

$$V_m = V_{m1} + V_{m2} \tag{5.3}$$

where V_{m1} and V_{m2} are the consequent motor terminal voltages due to the inverter voltages V_{s1} and V_{s2}, respectively, as shown in Figure 5.2.

According to the modelling of the RWP analysed in Chapter 3, when the reflection coefficients at the inverter side and motor terminals are unity, the voltages V_{s1} and V_{s2} experience full voltage reflection once arriving at the motor terminals. Therefore, the amplitudes of the resultant voltages V_{m1} and V_{m2} are V_{dc} (i.e., double the voltage magnitude of V_{s1} and V_{s2}), and the oscillation frequency is $1/4t_p$. Referring to Figure 5.2, the resultant motor terminal overvoltage oscillations V_{m1} and V_{m2} can be counterbalanced if V_{s2} lags V_{s1} by $2t_p$. Thus, the motor terminals will not experience the overvoltage oscillations due to the RWP in the motor drive system.

5.2.2 Analysis in Frequency Domain

To reveal the essence of the motor terminal overvoltage mitigation mechanism of the Q3L PWM scheme, the frequency domain analysis is conducted in this section. Since the Q3L PWM voltage V_s is composed of two identical voltage steps V_{s1} and V_{s2} with a dwell time t_{dwell}, the inverter output voltage V_s can be represented by the voltage pulse-train shown in Figure 5.3.

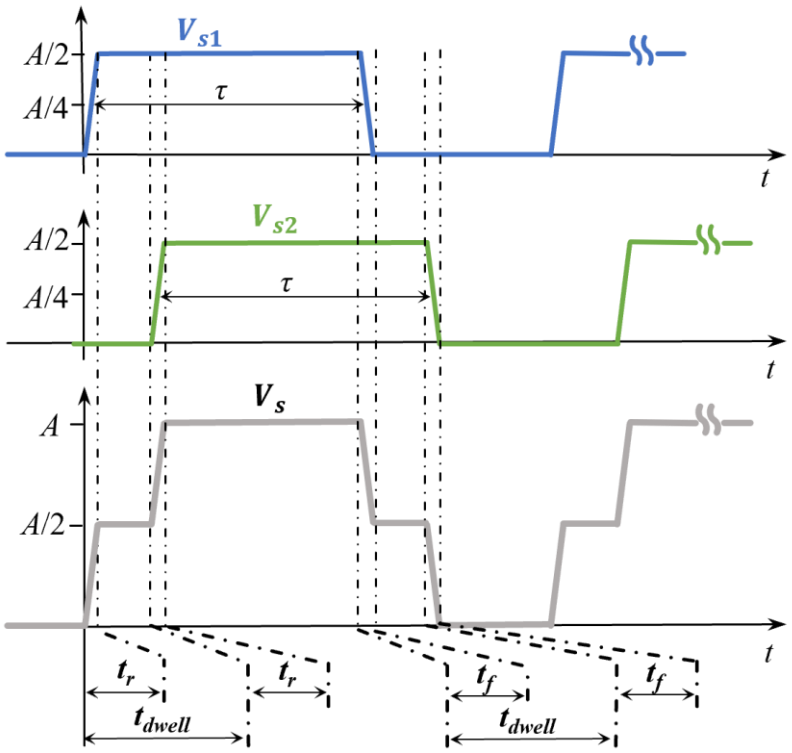


Figure 5.3 Q3L PWM voltage pulse train.

Referring to Figure 5.3, $A/2$ is the voltage pulse amplitude, τ is the average pulse width measured at half the pulse amplitude, T is the switching cycle, and t_r and t_f are the pulse rise and fall times of V_{s1} and V_{s2} respectively. For simplicity, the Q3L PWM voltage waveform shown in Figure 5.3 is assumed to be symmetrical (i.e., $t_r = t_f$) with a constant duty ratio ($D = \tau/T$).

According to the properties of the Fourier analysis, the pulse-train V_{s1} shown in Figure 5.3 can be expressed as:

$$V_{s1}(t) = \sum_{n=-\infty}^{n=\infty} c_{n1} e^{jn\omega t} \tag{5.4}$$

where ω is the angular frequency of the waveform and c_{n1} $(n1 = 1, 2, 3, \dots)$ is the Fourier series coefficient.

Note that c_{n1} can be given in complex exponential form, as:

$$c_{n1} = AD \operatorname{sinc}\left(\frac{n\omega\tau}{2}\right) \operatorname{sinc}\left(\frac{n\omega t_r}{2}\right) e^{-jn\omega\left(\frac{\tau+t_r}{2}\right)} \left(1 + e^{jn\omega t_{dwell}}\right) \tag{5.5}$$

where, $\operatorname{sinc}(x)$ denotes $\sin(x)/x$.

Owing to V_{s2} lags V_{s1} by t_{dwell}, according to the properties of the Fourier series, V_{s2} can be expressed as:

$$V_{s2}(t) = V_{s1}(t + t_{dwell}) = \sum_{n=-\infty}^{n=\infty} c_{n1} e^{jn\omega t_{dwell}} e^{jn\omega t} \tag{5.6}$$

Submitting (5.4) and (5.6) into (5.2), the Fourier series expansion of V_s can be given as:

$$V_s(t) = \sum_{n=-\infty}^{n=\infty} c_n e^{jn\omega t} \tag{5.7}$$

where, c_n $(n = 1, 2, 3, \dots)$ is the Fourier series coefficient of the inverter voltage V_s, given as:

$$c_n = AD \operatorname{sinc}\left(\frac{n\omega\tau}{2}\right) \operatorname{sinc}\left(\frac{n\omega t_r}{2}\right) e^{-jn\omega\left(\frac{\tau+t_r}{2}\right)} \left(1 + e^{jn\omega t_{dwell}}\right) \tag{5.8}$$

At the anti-resonance frequency f_{osc} of the cable-motor system, the Fourier series coefficient is:

$$c_n = AD \operatorname{sinc}(\pi f_{osc}\tau) \operatorname{sinc}(\pi f_{osc} t_r)\, e^{-jn\pi f_{osc}(\tau+t_r)} \left(1 + e^{j2\pi f_{osc} t_{dwell}}\right) \tag{5.9}$$

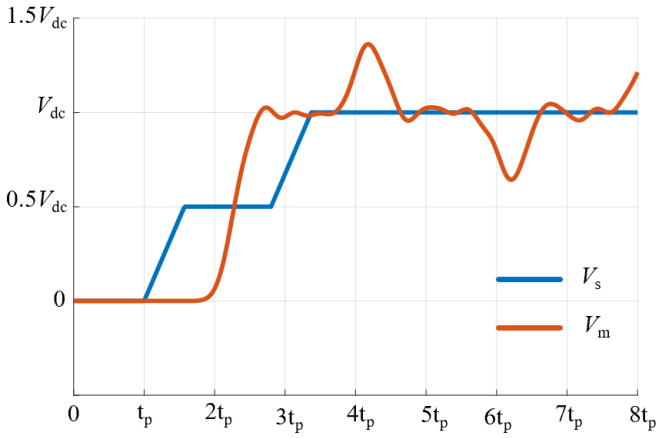
From (5.9), it can be derived that $c_n = 0$ when $t_{dwell} = \frac{1}{2f_{osc}} = 2t_p$, i.e., at this dwell time setting, there is no voltage component at the cable-motor's anti-resonance frequency. That is, the motor terminal overvoltage can be entirely mitigated due to no excitation source evoking the oscillations at the cable anti-resonance frequency.

The above frequency domain analysis reveals the essence of the Q3L PWM scheme is attenuating the motor overvoltage oscillations at the excitation source. That is reshaping the PWM voltages feeding to the motor drive system by actively eliminating the components at the cable-motor's anti-resonance frequency.

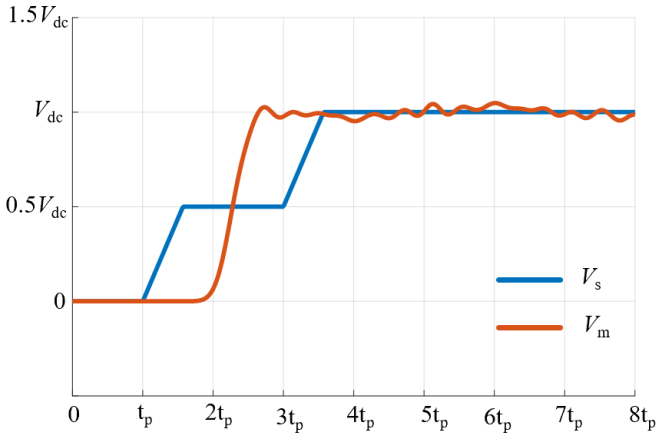
5.2.3 The Impact of Dwell Time

According to the above analysis, the effectiveness of the motor terminal overvoltage mitigation depends on the dwell time setting. However, there is not an analytical expression to quantify the impact of the dwell time on the motor terminal overvoltage. Therefore, the simulation study is conducted to qualitatively reveals the impact of dwell time on the motor terminal overvoltage oscillations. The detailed cable simulation model and its parameters can be found in Chapter 3. Note that the cable length is set as 10 m and the cable end is an open circuit to emulate the worst case for the RWP in the motor drive system. Figure 5.4 compares the simulation results for different dwell time setting, where Figure 5.4 (a), (b) and (c) show the voltages of the inverter and motor when $t_{dwell} = 1.8t_p$, $t_{dwell} = 2t_p$ and $t_{dwell} = 2.2t_p$, respectively.

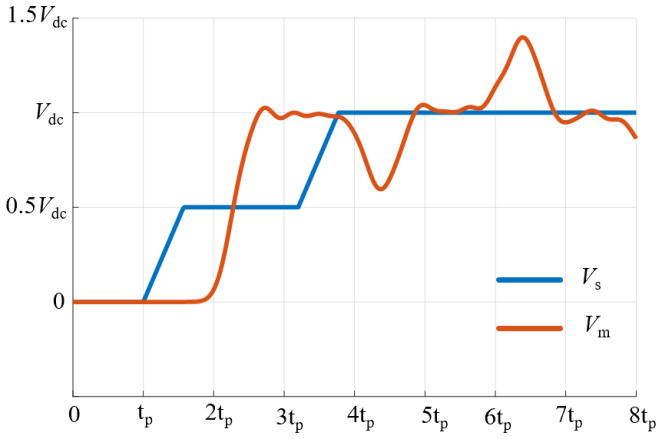
Referring to Figure **5.4**, the motor terminal overvoltage can be mitigated completely only when the dwell time is set as the optimum dwell time $2t_p$. It is worth noting that the voltages cross point of the inverter and motor indicates the optimum dwell time setting, where the motor terminal voltage crosses the inverter voltage at the dwell time midway for the optimum dwell time setting. Referring to Figure 5.4 (a), t_{dwell} is smaller than the optimum value, the voltages cross point is after the dwell time midway, where the maximum motor terminal voltage is about $1.4V_{dc}$. Referring to Figure **5.4**(c), when the dwell time is larger than the optimum dwell time, the voltage cross point of the inverter voltage and motor voltage is before the midway, where the maximum motor terminal voltage is about $1.4V_{dc}$.



(a) $t_{dwell} = 1.8\ t_p$



(b) $t_{dwell} = 2.0\ t_p$



(c) $t_{dwell} = 2.2\ t_p$

Figure 5.4 Simulation result of the inverter and motor voltages under the Q3L PWM scheme for different dwell time setting.

5.3 Implementation of the Q3L PWM Scheme using a T-type Inverter

The Q3L PWM scheme can be implemented using a three-level inverter. Instead of operating the inverter at the conventional three-level mode, the inverter can generate the Q3L PWM voltage waveform by actively controlling the switching states at the switching transients. This section uses a T-type inverter as an application example of the Q3L PWM scheme.

5.3.1 T-type Inverter

Figure 5.5 depicts the circuit diagram of a three-phase SiC-based T-type inverter, where a standard two-level inverter is supplemented with three auxiliary branches between the dc-link midpoint and the output terminals of each phase-leg [151]. The auxiliary branch usually consists of a pair of bidirectional switching devices in common source configuration, as shown in Figure 5.5. Note that the current flowing out from the inverter output nodes is denoted as positive.

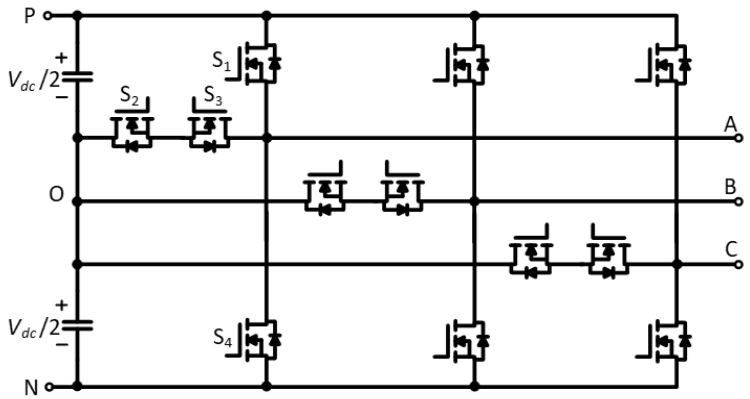


Figure 5.5 A three-phase SiC T-type inverter.

The output voltage of the T-type inverter V_{XN} referred against the negative dc-link voltage, where X=A, B or C, has three different voltage states, i.e., the low, intermediate, and high voltage levels (0, V_{dc} / 2 , and V_{dc}) depending on the switching state. Considering phase A as an example, the low voltage level can be produced by turning ON S_3 and S_4, the intermediate voltage level can be attained by turning ON S_2 and S_3, and the high voltage level can be achieved by turning ON S_1 and S_2. It is worth noting that the auxiliary branches of the T-type inverter only conduct the load current during the intermediate voltage level which is usually within several hundreds of nanoseconds (i.e., the dwell time). Therefore, the current rating of the switching devices in the auxiliary branch can be much lower than

that of the main switching devices. This is different from the case when the T-type inverter is operating in the standard three-level mode. Moreover, the auxiliary switching devices only block half of the dc-link voltage [136]. Thus, the switching devices of the auxiliary branches can be implemented with lower voltage and current rating switching devices when the T-type inverter is modulated under Q3L PWM scheme.

5.3.2 The Implementation of the Q3L PWM Scheme

Figure 5.6 illustrates how to generate the Q3L PWM voltage waveform for phase A, where $2t_p$ is the optimum dwell time for the motor terminal overvoltage mitigation, and t_{dead} is the deadtime between S_1 and S_3 or S_2 and S_4. Figure 5.7 shows the output voltage of the T-type inverter under the Q3L PWM scheme shown in Figure 5.6 for different current polarities, where Figure 5.7 (a) shows the case when the load current is positive and Figure 5.7 (b) shows the opposite case.

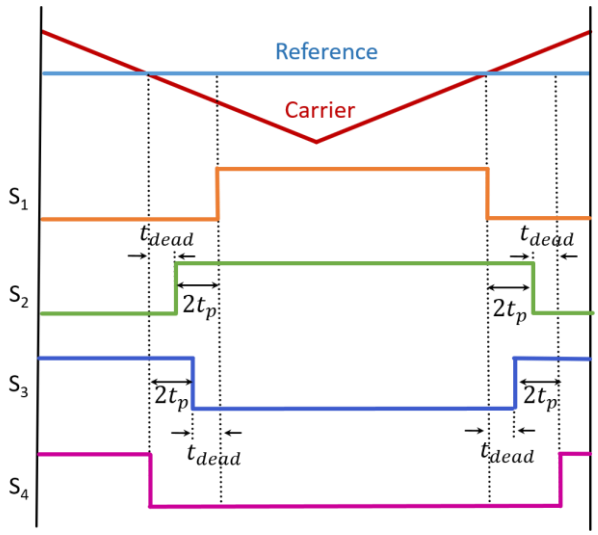
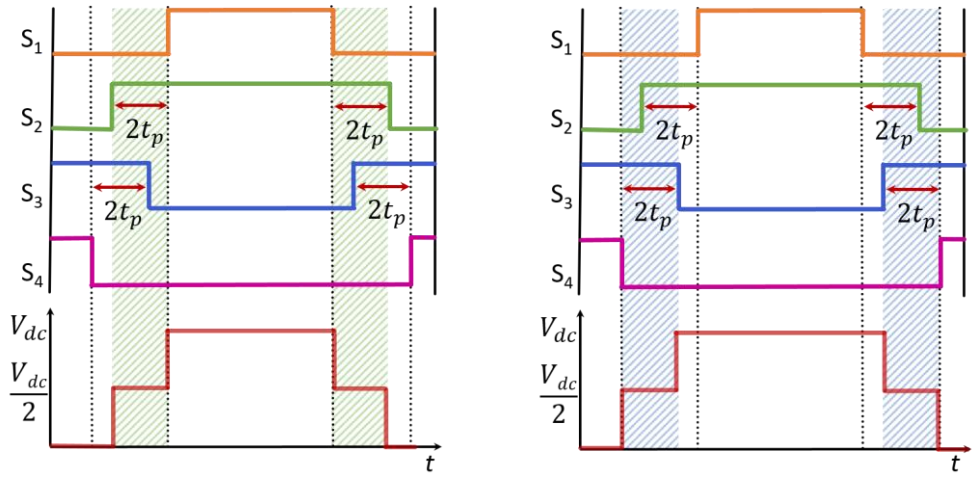


Figure 5.6 Gate signal generation of Q3L PWM in T-type inverters.

Referring to Figure 5.7 (a), when the load current is positive, the dwell time of the intermediate voltage level of V_{AN} is dominated by the ON-time of S_2. While for the opposite case, the intermediate voltage is dominated by S_3 as shown in Figure 5.7 (b). Since both the ON-time of S_2 and S_3 are equal, i.e., $2t_p$, the dwell time for the intermediate voltage remains the same as $2t_p$ for both current directions. Therefore, the Q3L PWM scheme shown in Figure 5.6 is independent of the load current polarities.



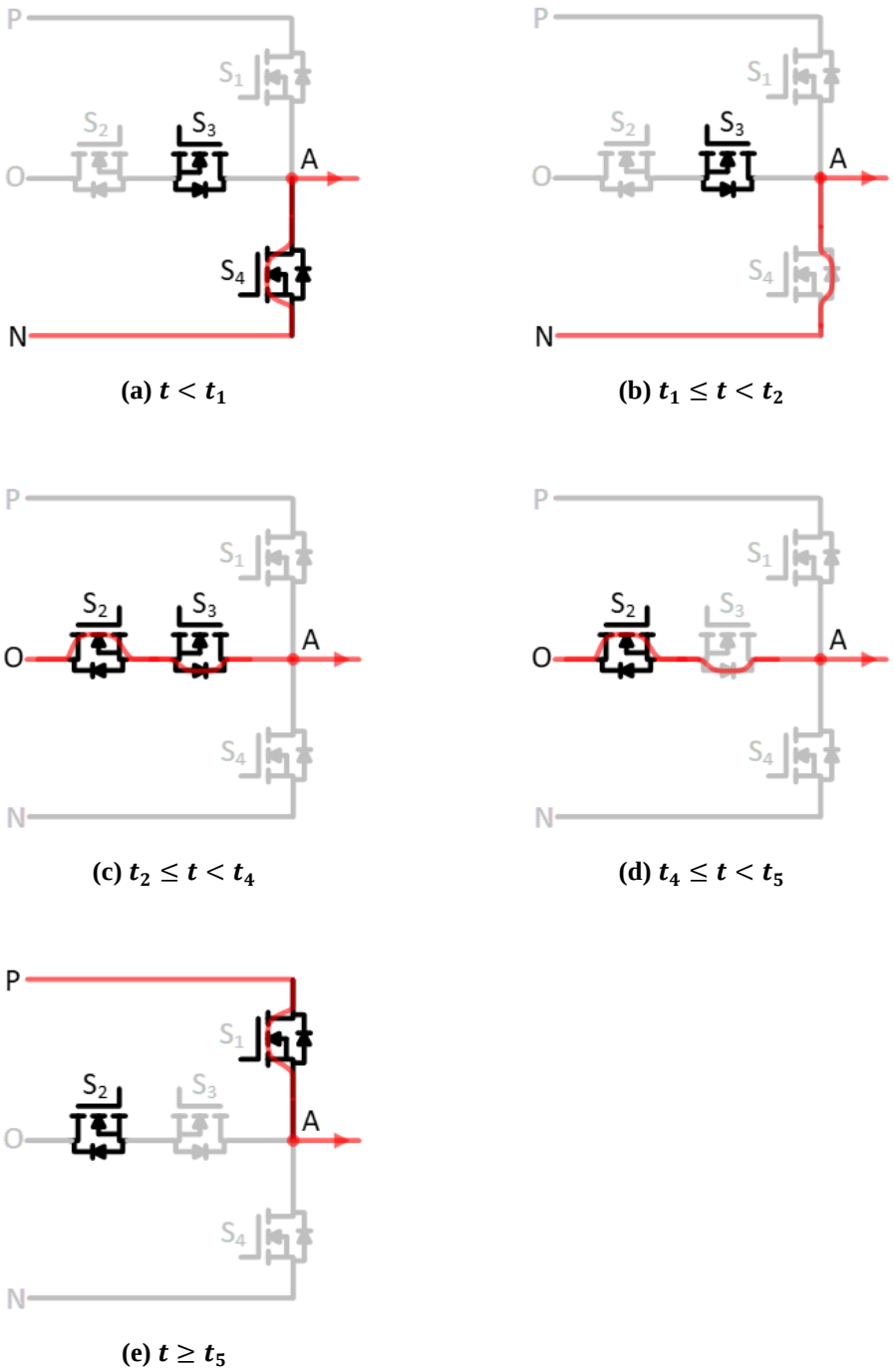
(a) phase current is positive **(b) phase current is negative**

Figure 5.7 Gate signals and output voltage of Q3L T-type inverter under different load current polarities.

5.3.3 The Impact of Parasitic on the Overvoltage Mitigation

According to Chapter 4, the switching transitions of the inverter output voltage are affected by the load current and parasitic capacitance of the switching devices, resulting in a non-uniform motor terminal overvoltage envelope. This may affect the effectiveness of Q3L PWM scheme, where the switching transitions of the T-type inverter are affected by the load current and parasitic, resulting in inaccurate dwell time setting. Therefore, it is necessary to investigate the switching commutation process of the T-type inverter under the Q3L PWM scheme considering the impact of SiC parasitic elements and load current. The analysis is first conducted for a single-phase T-type inverter and then extended for a three-phase case.

The commutation process can be divided into two switching transitions, i.e., the switching commutation of V_{AN} from zero to the intermediate voltage level $\frac{V_{dc}}{2}$ and then to the positive dc-link voltage V_{dc}, and V_{AN} from V_{dc} to the intermediate voltage level $\frac{V_{dc}}{2}$ and then to zero. In the following analysis, the load current is assumed to be positive and remain constant during the switching commutation processes. The switching commutation of V_{AN} from zero to the intermediate voltage level $\frac{V_{dc}}{2}$ and then to the positive dc-link voltage V_{dc} can be divided into four intervals as illustrated in Figure 5.8 and the corresponding output voltage waveform is shown in Figure 5.9.



(a) $t < t_1$ **(b)** $t_1 \leq t < t_2$

(c) $t_2 \leq t < t_4$ **(d)** $t_4 \leq t < t_5$

(e) $t \geq t_5$

Figure 5.8 The switching commutation processes for V_{AN} from 0 to V_{dc} when the load current is positive.

Interval 1 ($t_1 \leq t < t_2$) [Figure 5.8 (a) and Figure 5.8 (b)] referring to Figure 5.8 (a), before the switching interval, both S_3 and S_4 are ON, the current flows through the channel of S_4, where S_4 works in "synchronous rectification mode". The inverter output voltage V_{AN} is equal to zero, as shown in Figure 5.9. At a time instant t_1, S_4 is turned OFF as the

turn-OFF gate signal is applied to it, where the current starts to divert from the device channel to its antiparallel diode. Since the load current still flows thorough the lower main switch S_4, the output voltage V_{AN} remains unchanged at zero.

Interval 2 ($t_2 \leq t < t_4$) [Figure 5.8 (c)] After a dead time t_{dead}, i.e., $t = t_2$, the turn-ON gate signal is applied to S_2, allowing the load current to divert from S_4 to the auxiliary branch, as shown in Figure 5.8 (c). Meanwhile, the lower main switch S_4 blocks half of the dc-link voltage, where V_{AN} is $V_{dc}/2$ at $t = t_3$, as shown in Figure 5.9. It should be noted that the switching time for V_{AN} ascending from 0 to $V_{dc}/2$ is only governed by the adopted gate resistance and the switching device's characteristic. Since the switching speed is extremely fast, the rising edge of V_{AN} is denoted as a steep rising edge, as shown in Figure 5.9.

Interval 3 ($t_4 \leq t < t_5$) [Figure 5.8 d)] After a dwell time $2t_p$, i.e., $t = t_4$, S_3 is turned OFF as the turn-OFF gate signal is applied to it, where the current starts to divert from the device channel to its antiparallel diode. Since the auxiliary branches remains conducting, the output voltage V_{AN} is clamped at $V_{dc}/2$ during this interval.

Interval 4 ($t_5 \leq t < t_7$) [Figure 5.8 (e)] At a time instant t_5, the turn-ON gate signal is applied to S_1 allowing the load current to divert from the auxiliary branch to S_1 channel. Meanwhile, the lower main switch S_4 blocks the entire dc-link voltage, where V_{AN} remains V_{dc} after t_6, as shown in Figure 5.9. It should be noted that the switching time for V_{AN} traversing from $V_{dc}/2$ to V_{dc} is only governed by the adopted gate driver resistance. Thus, the rising edge of V_{AN} from $V_{dc}/2$ to V_{dc} can be denoted by a steep edge shown in Figure 5.9.

Referring to Figure 5.9, the rising edges of the voltage steps V_{s1} and V_{s2} have the same rise time t_r which is governed by the adopted gate resistance and switching device's characteristics. The effective dwell time remains $t_{dwell} = 2t_p$, which is the optimal dwell time for motor terminal overvoltage mitigation.

The switching commutation of V_{AN} from V_{dc} to zero is affected by the parasitic capacitance of the switching devices and load current which can be divided into two scenarios according to the load current value, i.e., the high current region and low current region.

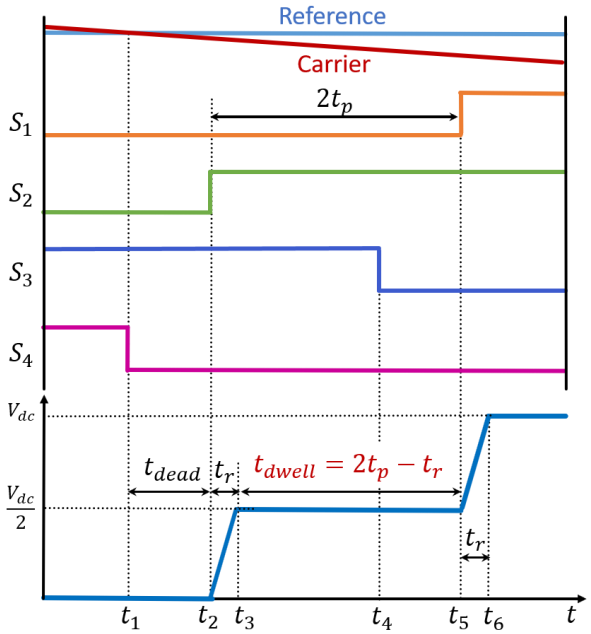


Figure 5.9 The output voltage during the commutation process for V_{AN} from zero to V_{dc} when the phase current is positive.

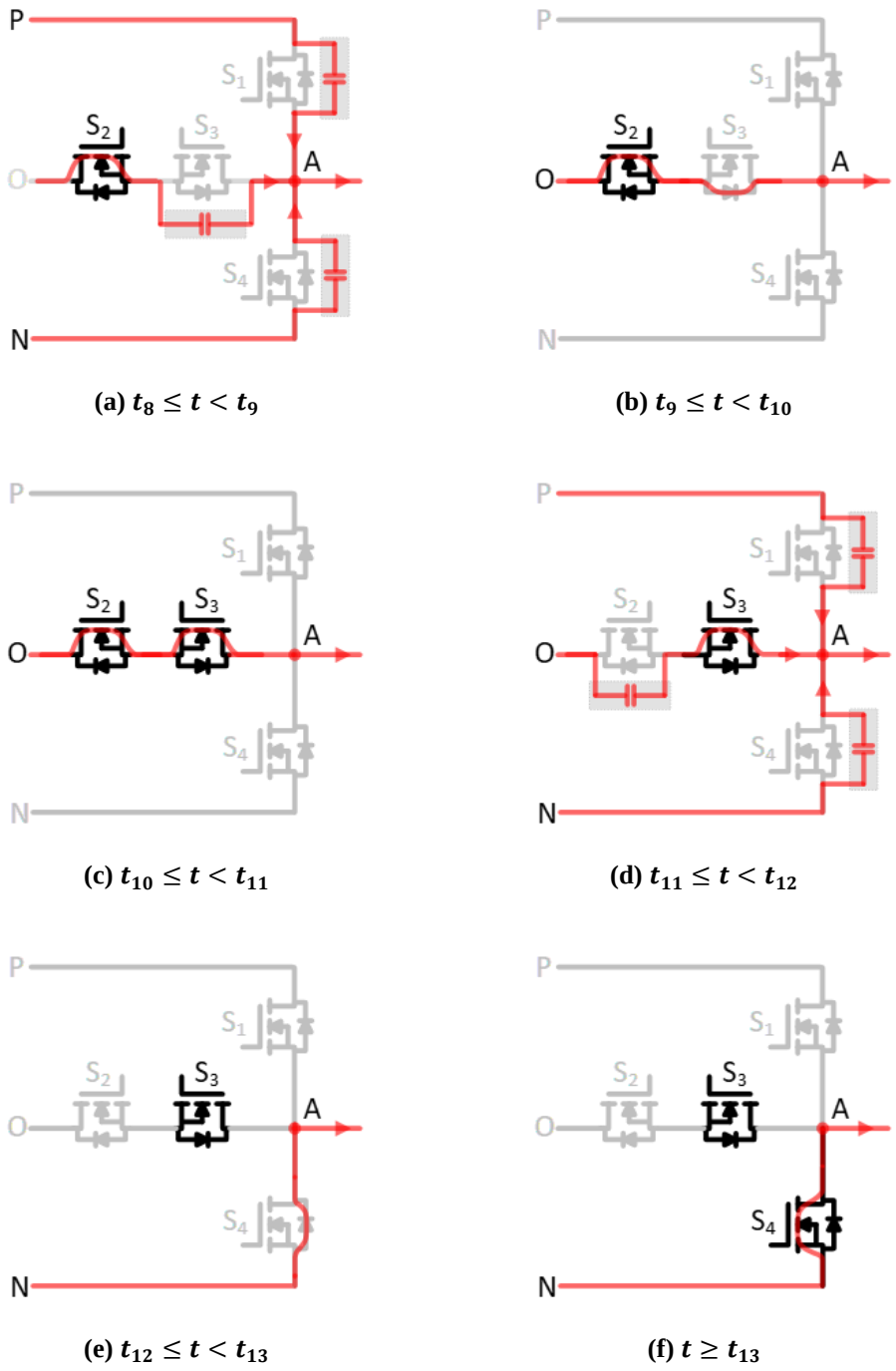
(a) High load current region

The switching commutation process can be divided into four intervals, as elucidated in Figure 5.10. The corresponding output voltage waveform is shown in Figure 5.11 (a).

Interval 1 ($t_8 \leq t < t_{10}$) [Figure 5.10 (a) and (b)] At a time instant t_8, S_1 is instantly turned OFF as the turn-OFF gate signal is applied to it. Referring to Figure 5.10 (a), the voltage V_{AN} does not promptly decrease due to the impact of parasitic capacitance, where the load current discharges the output capacitance of S_3 and S_4 while charges that of S_1. Therefore, the voltage V_{AN} tardily decreases in a linear manner within a fall time t_{fall}, as shown in Figure 5.11 (a). Referring to Figure 5.10 (b), at t_9 the voltage V_{AN} reaches $V_{dc}/2$, the voltage across S_3 is zero and the current starts to flow through its antiparallel diode. Then V_{AN} is clamped to $V_{dc}/2$. The fall time t_f is given by:

$$t_f = \frac{3C_{oss}V_{dc}}{2I_{load}} \tag{5.10}$$

Note that the output parasitic capacitance of the switching devices is assumed to be the same for all the switching devices in the T-type inverter. According to (5.10) for a given inverter the fall time depends on the instantaneous load current I_{load}.



(a) $t_8 \leq t < t_9$ **(b)** $t_9 \leq t < t_{10}$

(c) $t_{10} \leq t < t_{11}$ **(d)** $t_{11} \leq t < t_{12}$

(e) $t_{12} \leq t < t_{13}$ **(f)** $t \geq t_{13}$

Figure 5.10 The commutation processes for V_{AN} from V_{dc} to zero when the load current is positive.

Interval 2 ($t_{10} \leq t < t_{11}$) [Figure 5.10 (c)] After a dead time t_{dead}, i.e., $t = t_{10}$, the turn-ON gate signal is applied to S_3 allowing the current to divert from its body diode to the channel. Due to the auxiliary branches remains conducting the load current, the output voltage V_{AN} remains unchanged at $V_{dc}/2$, as shown in Figure 5.11 (a).

Interval 3 ($t_{11} \leq t < t_{13}$) [Figure 5.10 (d) and (e)] After a dwell time $2t_p$, i.e., $t = t_{11}$, S_2 begins to be turned OFF as the turn-OFF gate signal is applied to it. However, as seen in Figure 5.10 (d) the voltage V_{AN} does not promptly decrease where the load current discharges the output capacitance of S_4 while charges that of S_1 and S_2. Thus, the voltage V_{AN} tardily decreases in a linear manner within a fall time t_{fall}, as given by (5.10). Referring to Figure 5.10 (e) and Figure 5.11, at t_{12}, V_{AN} reaches 0 and the current starts to flow through the antiparallel diode of S_4.

Interval 9 ($t \geq t_{13}$) [Figure 5.10 (e)] At t_{13}, the turn-ON gate signal is applied to S_4 allowing the load current to divert from the body diode to the S_4 device channel, where S_4 works in "synchronous rectification mode", the output voltage V_{AN} is equal to zero, as shown in Figure 5.11.

From above commutation process, the output voltage V_{AN} is clamped to $V_{dc}/2$ before turning on S_3, and becomes equal to zero after turning on S_4, the duration of the intermediate level $t_{dwell} = 2t_p$, which is the optimal dwell time for the Q3L PWM. Theoretically, the motor terminal overvoltage can be entirely mitigated at the high current region.

(b) Low* load *current region

According to (5.10), when the inverter operates at low current region, the fall time t_f would be significantly longer, the corresponding output voltage V_{AN} is shown in Figure 5.11 (b). The whole process can be divided into four intervals and the interval label is denoted by 1' to 4' distinguishing them from the high load current case.

Interval 1' ($t_8 \leq t < t_{10}$) [Figure 5.10 (a)] This interval is similar to interval 1. According to (5.10), the fall time would be much longer when the load current is close to zero. Therefore, the output voltage V_{AN} is larger than $V_{dc}/2$ at t_{10}, where the energy stored in the output capacitance of S_3 has not been fully transferred to the auxiliary branch before t_{10} as shown in Figure 5.10 (a).

Interval 2' ($t_{10} \leq t < t_{11}$) [Figure 5.10 (c)] As can be noticed, at a time instant t_{10} the channel of the S_3 turns on before the drain-source voltage of S_3 reduces to zero, the drain-source residual voltage across the equivalent parasitic device capacitance discharge through its channel and then the voltage is clamped to $V_{dc}/2$ at t'_{10}. Then the auxiliary branch remains conducting the load current, the output voltage V_{AN} remains unchanged at

$V_{dc}/2$. It should be noted that the fall time $t_{f2} = t_{11} - t_{10}$ is controlled by the gate resistance and the switching devices' characteristics.

Interval 3' ($t_{11} \leq t < t_{13}$) [Figure 5.10 (d)] This interval is similar to interval 3. According to (5.10), the fall time would be much longer when the load current is close to zero. Therefore, the output voltage V_{AN} is larger than 0 at t_{13}, where the energy stored in the output capacitance of S_4 has not been fully transferred to the lower switch S_4 before t_{13} as shown in Figure 5.10 (d).

Interval 4' ($t \geq t_{13}$) [Figure 5.10 (e)] As shown, when the turn-ON gate signal is applied to S_4 at t_{13}, the output voltage V_{AN} is still larger than 0, resulting in the residual drain-source voltage across the equivalent parasitic device capacitance being discharged thorough the channel of S_4 and then the voltage is clamped to 0.

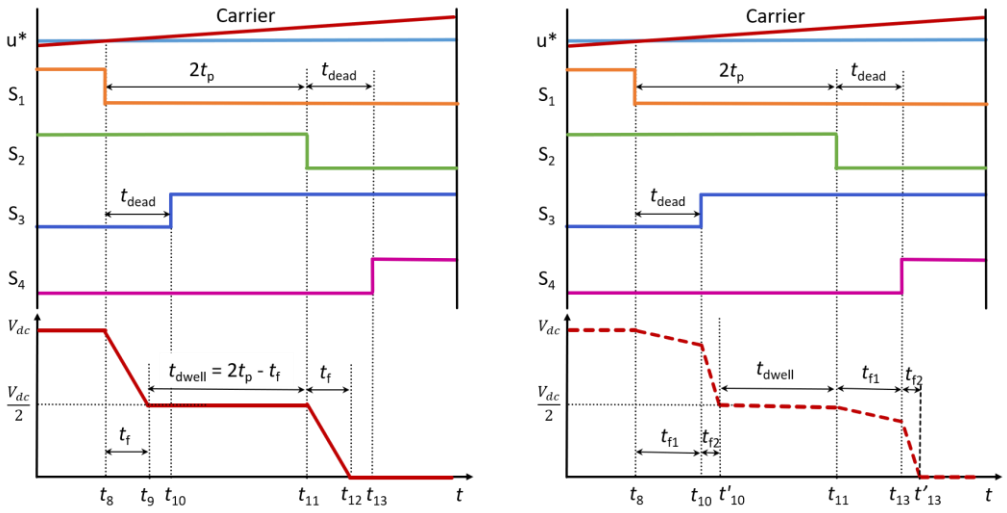
Accordingly, when the load current is positive, the output voltage waveform of the T-type inverter under the Q3L PWM scheme is shown in Figure 5.12 (a), where the rising edge (blue line) is only governed by the adopted gate resistance and switching devices' characteristics, while the falling edge (red line) is affected by the parasitic of switching devices and the load current. Oppositely, i.e., when the load current is negative, the rising edge (red line) is affected by the parasitic of switching devices and load current while falling edge is governed by the adopted gate resistance, as shown in Figure 5.12 (b). It should be noted that the red solid lines indicate the inverter operation at high-current region while the red dotted lines indicate the low-current region. Therefore, when the load current is close to zero, the Q3L PWM cannot entirely mitigate the motor terminal overvoltage oscillations due to the impact of the parasitic capacitance of the switching devices and load current.

Comparing Figure 5.12 to Figure 4.3, the rising and falling edges of the output voltage V_{AN} of T-type inverter show the similar characteristics of the two-level inverters. Therefore, the line voltage V_{AB} of the three-phase T-type inverter under the Q3L PWM scheme is similar to the two-level counterpart. Figure 5.13 shows the inverter's voltage waveforms at different operation regions according to the load current polarities. The characteristics of the line voltage V_{AB} of the T-type inverter under the Q3L PWM can be summarized as follows:

In region I (Figure 5.13 (a)) and region III (Figure 5.13 (d)), the Q3L PWM can completely mitigate the motor terminal overvoltage oscillations because the effective dwell time is the

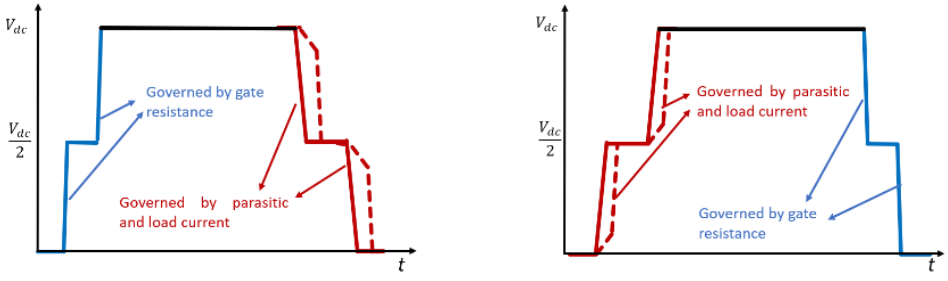
optimal one as the switching transitions of the output voltage are governed by the gate resistance and switching devices' characteristics.

In regions II and IV, the motor terminal overvoltage mitigation ability of the Q3L PWM scheme would be affected by the parasitic elements of the switching devices and the load current. Specifically, in region II when $V_{AB} < 0$ (Figure 5.13 (b)) and i_A is close to zero, or when $V_{AB} > 0$ (Figure 5.13 (c)) and i_B is close to zero, the Q3L PWM scheme cannot entirely mitigate the motor terminal overvoltage oscillations. Whereas, in region IV when $V_{AB} > 0$ (Figure 5.13 (e)) and i_A is close to zero, or when the line $V_{AB} < 0$ (Figure 5.13 (f)) and i_B is close to zero, the Q3L PWM cannot entirely mitigate the motor terminal overvoltage oscillations either.



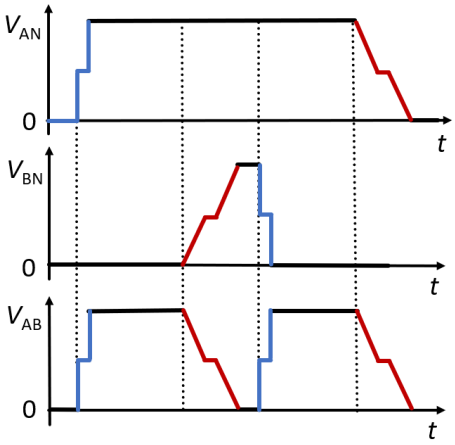
(a) high load current region **(b) low load current region**

Figure 5.11 The output voltage V_{AN} during the commutation process from V_{dc} to zero.

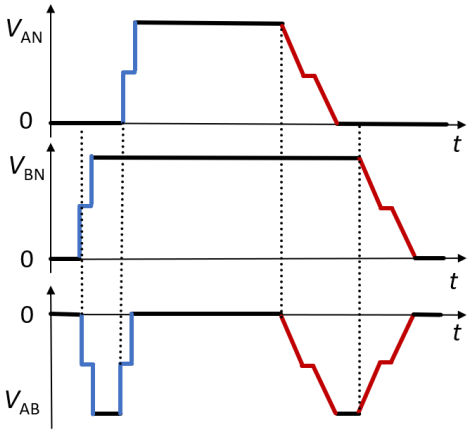


(a) **(b)**

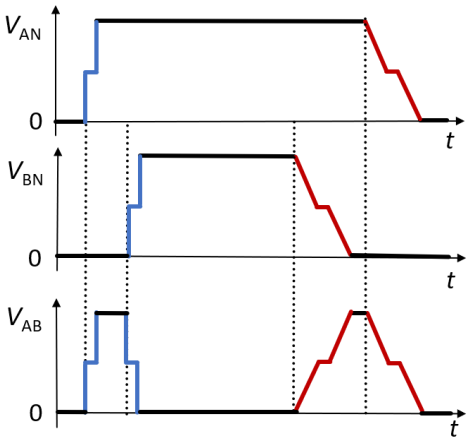
Figure 5.12 The output voltage of the T-type inverter under Q3L PWM when the load current is (a) positive and (b) negative.



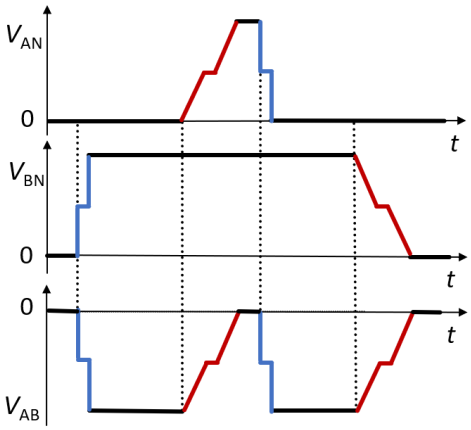
(a) region I



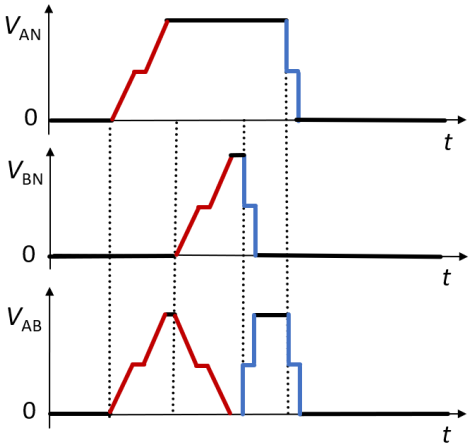
(b) region II when $V_{AN} > V_{BN}$



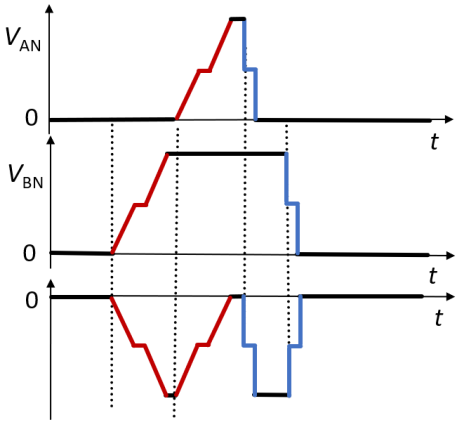
(c) region II when $V_{AN} < V_{BN}$



(d) region III



(e) region IV when $V_{AN} > V_{BN}$



(f) region IV when $V_{AN} < V_{BN}$

Figure 5.13 Switching transitions of the line voltage V_{AB} of T-Type inverter under the Q3L PWM in different current regions.

5.3.4 Experimental Results

To verify the theoretical analysis, a three-phase T-type inverter based on SiC MOSFETs (C2M0040120D) from Wolfspeed is built in the laboratory. Figure 5.14 shows the experimental setup, where a three-phase SiC T-type inverter supplies a three-phase four-core 7.5 kW induction motor through 12.5m long power, four-core 13 AWG unshielded PVC cables. The dc-link voltage is 400V. Note that the SiC MOSFETs are driven by gate drivers with 25 Ω gate resistance.

The inverter is first operated as a standard two-level inverter under the conventional SPWM and then under the Q3L PWM scheme. Note that the two-level inverter can be easily achieved by disabling the auxiliary branches of the T-type inverter without any hardware modification. The dwell time for the T-type inverter is set as $2t_p$, where t_p is measured by the experiment. The detailed experimental parameters are given in Table 5.1. The voltages and currents are measured using high bandwidth oscilloscope MSO-X 3054A from Keysight Technologies. The differential voltage probes from Pico Technology (TA042, 100MHz, 1kV) and the current probe from Agilent Technologies (N2783A, 100MHz, 30A) are utilized for the voltage and current measurement.

Figure 5.15 shows the line voltages at the inverter side and the motor terminals when the motor is supplied by the two-level inverter, where Figure 5.15 (a) shows the voltages for one switching cycle and Figure 5.15 (b) and (c) show zoomed-in views for the rising and falling edges, respectively. Referring to Figure 5.15, there is a significantly overvoltage oscillations at the motor terminals due to the RWP in the motor drive system, where the motor terminal voltage oscillates in a damped manner and the maximum overvoltage is about 2 pu for both the rising and falling transitions.

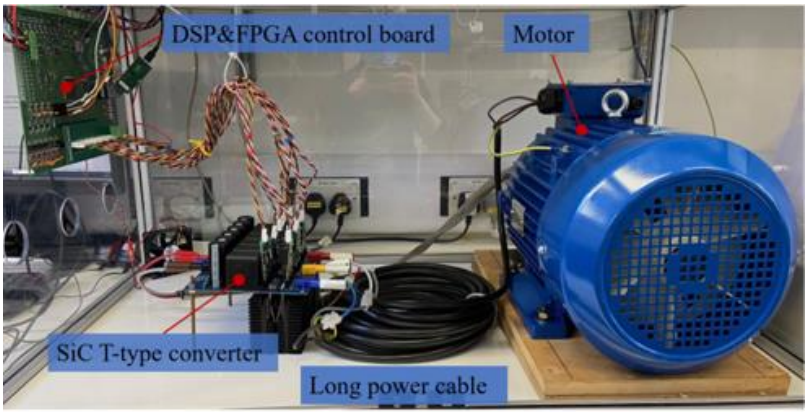
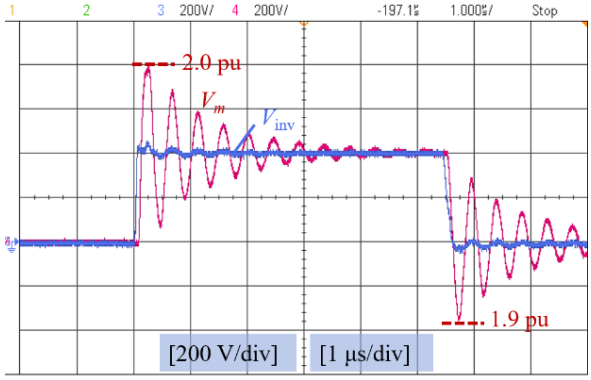
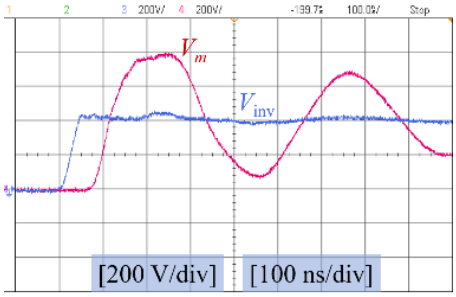


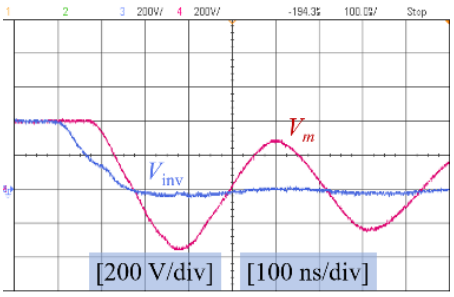
Figure 5.14 The experimental setup.



(a) switching cycle view transition



(b) a zoomed view at the rising



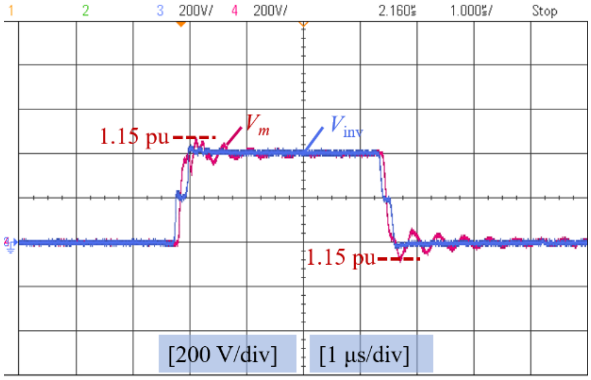
(c) a zoomed view at the falling transition

Figure 5.15 Inverter and motor line voltages under two-level SPWM.

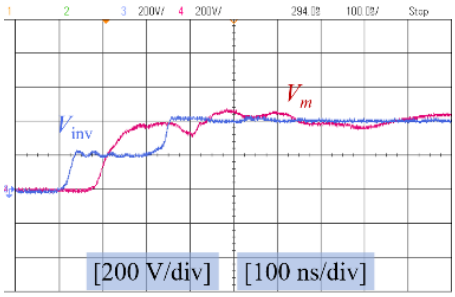
Table 5.1 Main experimental parameters.

Symbol	Value	Symbol	Value
Dwell time (t_{dwell})	220ns	Switching frequency	20 kHz
Dead time (t_{dead})	300ns	Fundamental frequency	50 Hz

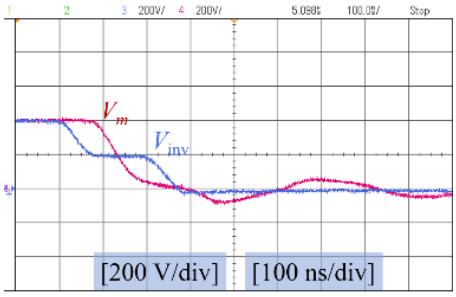
With the adoption of the Q3L PWM scheme, Figure 5.16 (a) shows the line voltages at the inverter side and motor terminals for one switching cycle. As shown, the Q3L PWM can effectively attenuate the motor terminal overvoltage, where the maximum motor terminal voltage is limited within 1.15 p.u for both rising and falling transitions. Figure 5.16 (b) and (c) further show the zoomed-in views of the motor terminal voltage in response to Q3L voltage waveform at the rising and falling edges, respectively. It is worth noting that while the motor is supplied by the Q3L voltage waveform, the voltage at the motor terminals shows a two-level waveform, as shown in Figure 5.16.



(a) switching cycles view transition



(b) a zoomed view at the rising

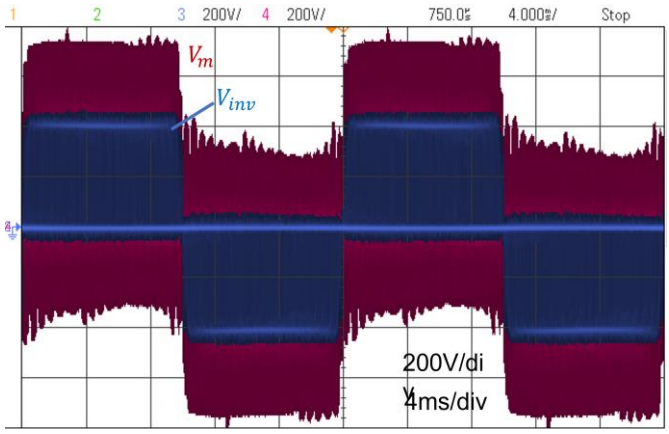


(c) a zoomed view at the falling transition

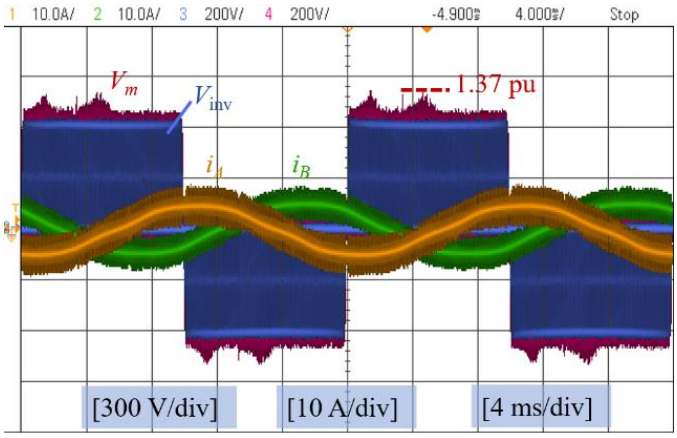
Figure 5.16 Inverter and motor line voltages under the Q3L PWM.

Figure 5.17 shows the experimental result for two fundamentals, where Figure 5.17 (a) shows the inverter output line voltage V_{inv} (from phase A to phase B), and the corresponding motor line voltage V_m, when the motor is supplied by the hard-switching inverter and Figure 5.17 (b) shows inverter output current of phase A and B (i_A and i_B), the inverter output line voltage V_{inv} (from phase A to phase B), and the corresponding motor line voltage V_m, when the motor is supplied by the three-phase SiC-based T-type inverter under the Q3L PWM scheme, for two fundamental cycles.

Referring to **Figure 5.17** (a), the motor terminal voltage is about 2.0 pu in the fundamental cycles when the motor is supplied by the hard-switching inverter. With the adoption of the Q3L PWM scheme, the motor terminal voltage is limited to 1.15 pu for most of the fundamental cycles, as shown in **Figure 5.17** (b). However, there is a voltage hump when the load current is close to zero, where the maximum motor terminal overvoltage is about 1.37 pu. This is because the dwell time is not the optimal value as a result of the parasitic capacitance of the switching devices and load current, as previously analysed.



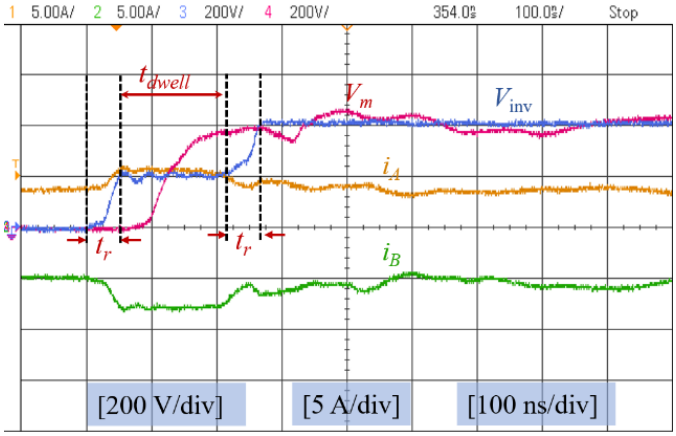
(a)



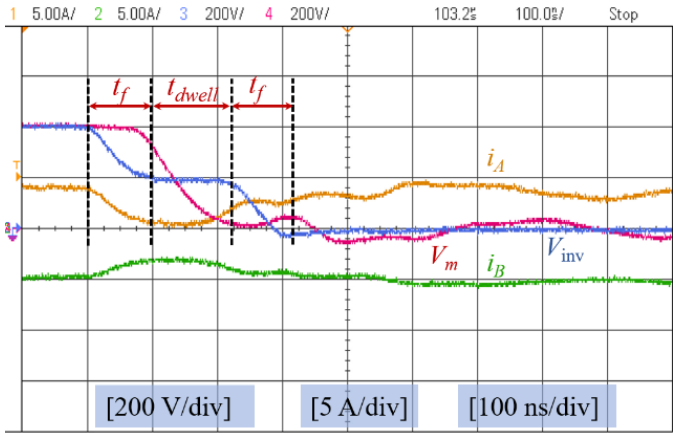
(b)

Figure 5.17 Switching The line voltages at the inverter side V_{inv} and motor terminals V_m in (a) the hard-switching inverter-fed system (b) the Q3L T-type inverter-fed system.

Figure 5.18-Figure 5.21 show zoomed views at the switching transitions verifying the theoretical analysis of the voltage waveforms during different operation regions, where Figure 5.18 shows the experimental results for region I, where the load currents for phase A and B are about 4A and -5A, respectively. Figure 5.19 shows the experimental results for region III, where the load currents for phase A and B are about -3A and 5A, respectively. Figure 5.20 shows the results for region II, where the load currents for phase A and B are about 1A and 4A, respectively. Figure 5.21 shows the results for region IV, where the load currents for phase A and B are about -1A and -4.5A, respectively. As noticed, the experimental measured waveforms show good agreement with the theoretical counterpart presented in Figure 5.13.



(a) rising transition

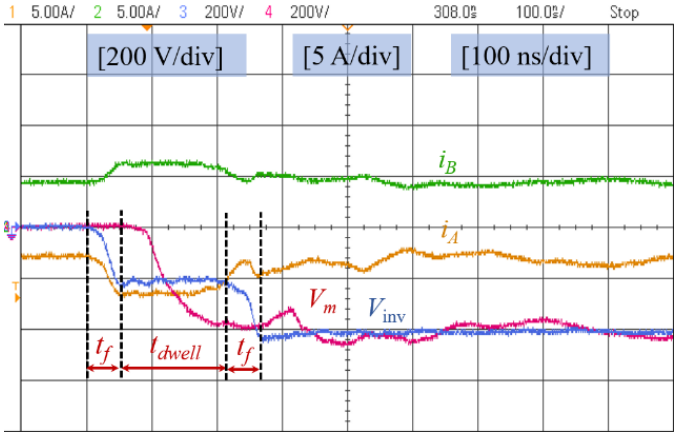


(b) falling transition

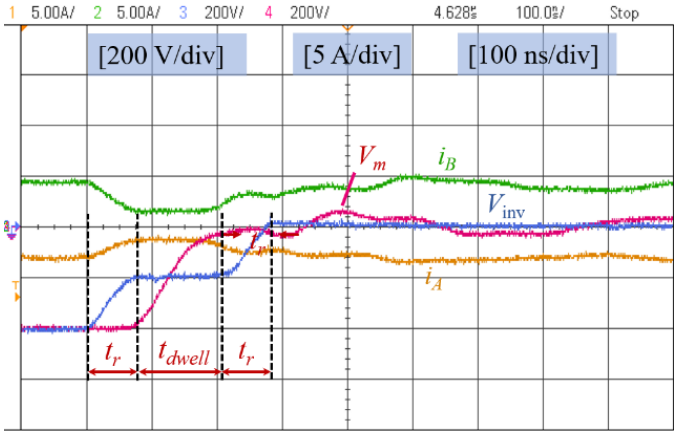
Figure 5.18 Phase currents i_A and i_B, and the line voltages at the inverter side V_{inv} and motor terminals V_m under the Q3L PWM during the switching transitions in region I.

Referring to Figure 5.18, in the region I, the inverter line voltage V_{inv} has different rise and fall times, where the rise time t_r is about 50 ns while the fall time t_{fall} is about 100 ns. This is because the rising time is only governed by the gate driver and switching devices' characteristics while the falling time is affected by the parasitic capacitance of SiC MOSFETs and load current.

However, in region III (**Figure 5.19**), the inverter line voltage V_{inv} shows the opposite trend. As can be noticed, the inverter line voltage $V_{inv} < 0$ and the rise time (60 ns) is longer than the fall time (50 ns). Common to Figure 5.18 and **Figure 5.19**, the maximum motor terminal overvoltage is maintained within 1.15 pu because the dwell time is the optimal value where the rising and falling edges of the line voltage are governed by the gate resistance.



(a) rising transition

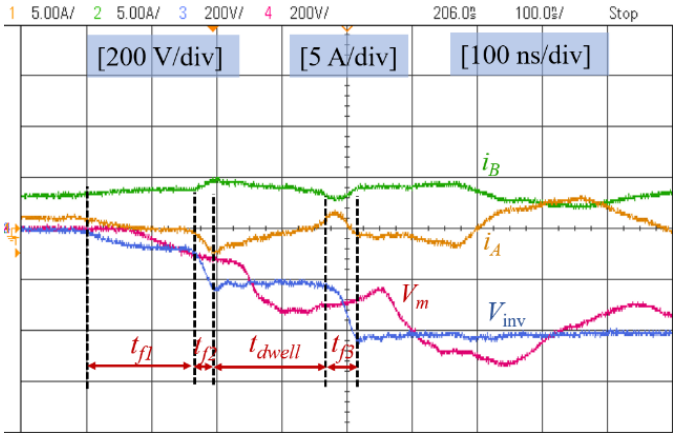


(b) falling transition

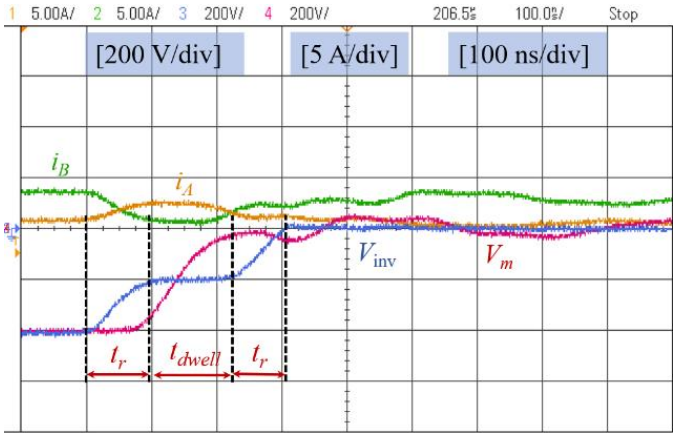
Figure 5.19 Phase currents i_A and i_B, and the line voltages at the inverter side V_{inv} and motor terminals V_m under the Q3L PWM during the switching transitions in region III.

Figure 5.20 shows the experimental results in region II when the inverter line voltage $V_{inv} < 0$, where the rising edge and falling edge are shown in Figure 5.20 (a) and (b), respectively. As can be noticed, both rise and fall times of V_{inv} are longer than the switching time. Referring to Figure 5.20 (a), the rising edges have three different rise times resulting in a non-optimal dwell time setting, causing an increased motor terminal overvoltage, where the maximum overvoltage is 1.37 pu. This is because both rise and fall times are affected by the parasitic capacitance of switching devices and load current, as previously analysed. Note that compared with the theoretical analysis in Figure 5.13 (b), t_{f4} does not show up in Figure 5.20 (a). This occurs because the theoretical analysis assumes the inverter output current remains constant, while in fact the high dv/dt of the output voltage charges and discharges the parasitic capacitance of the cable resulting in a variable current during the switching transients. Referring to Figure 5.20 (a), i_A changes

from positive to negative, i.e., the inverter operation region switches from region II ($i_A > 0$, $i_B > 0$) to region III ($i_A < 0$, $i_B > 0$). Therefore, t_{f4} does not show up in the experimental result, i.e., the falling edges (t_{f1}, t_{f2}) show a similar pattern with that in region II, and the falling edge (t_{f3}) shows a similar pattern with that in region III. Similar experimental results can be observed in region IV, as depicted in Figure 5.21.

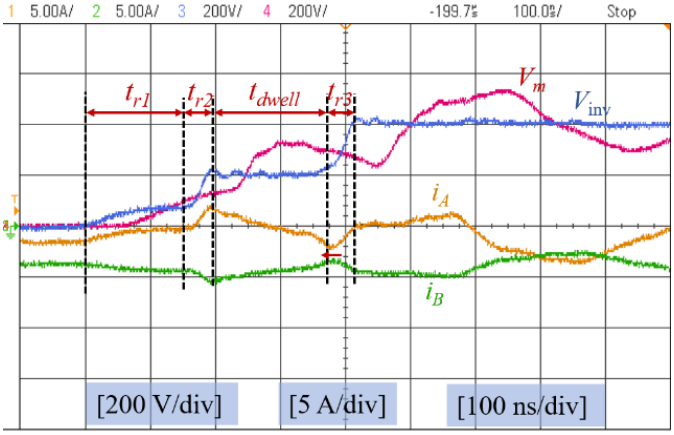


(a) rising transition

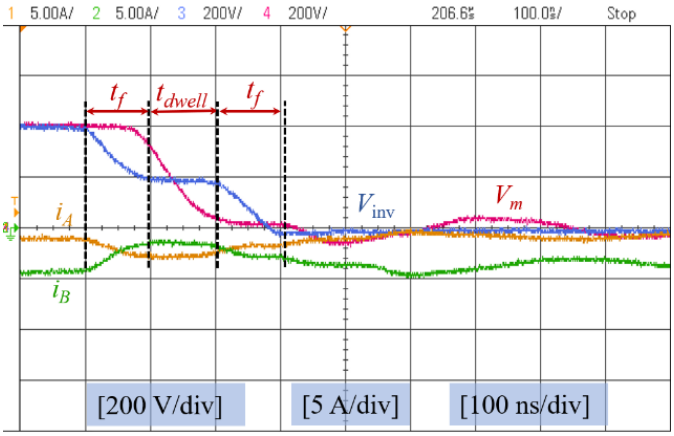


(b) falling transition when $V_{inv} < 0$.

Figure 5.20 Phase currents i_A and i_B, and the line voltages at the inverter side V_{inv} and motor terminals V_m under the Q3L PWM during the switching transitions in region II.



(a) rising transition



(b) falling transition when $V_{inv} > 0$

Figure 5.21 Phase currents i_A and i_B, and the line voltages at the inverter side V_{inv} and motor terminals V_m under the Q3L PWM during the switching transitions in region IV.

5.4 Implementation of the Q3L PWM using a Module-parallel Inverter

The above section shows the motor terminal overvoltage can be effectively mitigated when the T-type inverter is modulated under the Q3L PWM. The power rating of the inverter is limited by the adopted switching devices' current rating. However, inverters with high power rating are expected in the future application. For example, the 100-500kW power inverter for electric vehicles and the megawatts power inverter for the electric airplanes are highly demanded.

To achieve such high-power rating, the dc-link voltage and the switching devices' current rating need to be increased. However, the dc-link voltage is fixed for most of application, for example, a nominal 800V dc-link voltage is being considered for next generation EVs

[2]. Therefore, improving the current rating of switching devices is an inevitable approach. Since the current rating of commercial SiC chip is within 100 A, parallel connection of SiC MOSFETs would be an approach to improve the exiting switching devices' current capacity [82], [152]. Furthermore, parallel connection of switching devices is a cost-effective approach even in low power application since the high-current devices are generally more expensive than equivalently rated parallel-connected low-current counterparts. For example, at the time of writing, the C3M0016120D (1200V/115A, $70.4) is 37% more expensive than two C3M0032120D (1200V/62A, $ 25.7) from Wolfspeed [153].

However, paralleling SiC devices is a challenging approach due to the imbalance current among parallel SiC MOSFETs [152]. Owing to the unavoidable switching times mismatch and/or characteristic difference among the parallel devices, both the steady-state and transient currents will not be equally shared among the devices, resulting in overcurrent and overtemperature. This adversely affects the inverter reliability and limits the current rating of the devices. Therefore, several approaches have been proposed to overcome the imbalance current among the switching devices. For example, [154] use active gate drivers to handle the imbalance current. However, it requires high-band current sensors and feedback control, where it increases the implement complexity. Moreover, paralleling multi-chips also poses challenges on the gate driver design, where a very-high current output capability is required to drive the parallel chips to achieve simultaneous turn-ON and turn-OFF while providing a very fast switching speed.

Instead of using the chip-parallel method to extend the power rating of the power inverter, a module-parallel power inverter is proposed in this chapter. In addition to extend the power rating of the power inverter, the module-parallel power inverter can generate the Q3L PWM voltage waveform to mitigate the motor terminal overvoltage oscillations.

5.4.1 The Module-parallel Power Inverter

Figure 5.22 shows the circuit schematic of a three-phase SiC module-parallel power inverter where each phase consists of two bridge-legs connected using two identical inductors. This inverter can be further extended to multiple bridge-legs parallel inverter depending on the switching devices' current rating and the required power level of the inverter. For simplify, the two bridge-leg parallel inverter shown in Figure 5.22 is studied in this PhD work. Note that the inductors shown in Figure 5.22 can be either the coupled

or uncoupled inductor. The coupled inductor is employed herein because it can significantly reduce the core loss and size, comparing with the uncoupled one.

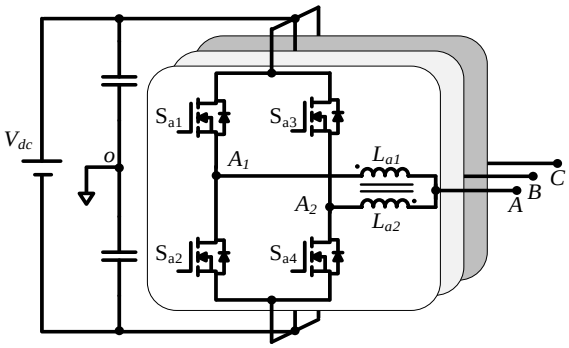


Figure 5.22 Three-phase SiC bridge-leg parallel inverter.

5.4.2 The Implementation of the Q3L PWM Scheme

Referring to Figure 5.22, the inverter output voltage V_{AN} for phase A is pertinent to the output voltages (V_{AN1} and V_{AN2}) of bridge-legs $A1$ and $A2$, as:

$$V_{AN} = \frac{V_{AN1} + V_{AN2}}{2} \tag{5.11}$$

Accordingly, the Q3L voltage waveform can be realized by inserting a time shift t_{dwell} between the output voltage of the bridge-legs ($A1$ and $A2$). Figure 5.23 illustrates the gate signal generation for the switching devices in phase A, where a modulation signal is compared with two identical triangular carrier signals but shifted by t_{dwell}.

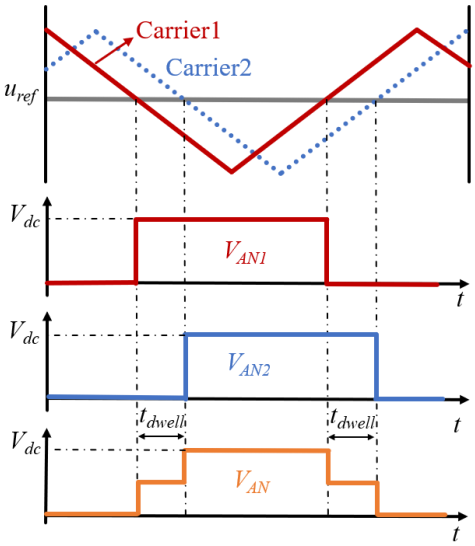


Figure 5.23 Q3L wave generation using module-parallel inverter.

Figure 5.24 illustrates the detailed switching transitions considering the devices' parasitic elements, when the output current is positive, where Figure 5.24 (a)-(e) illustrate the commutation process of the output voltage from 0V to V_{dc}, while the opposite case is shown in Figure 5.24 (f)-(j). The corresponding waveforms for the commutation processes are shown in Figure 5.25. The phase current i_A is assumed to be equally distributed among the bridge-legs (A1 and A2) when the commutation starts.

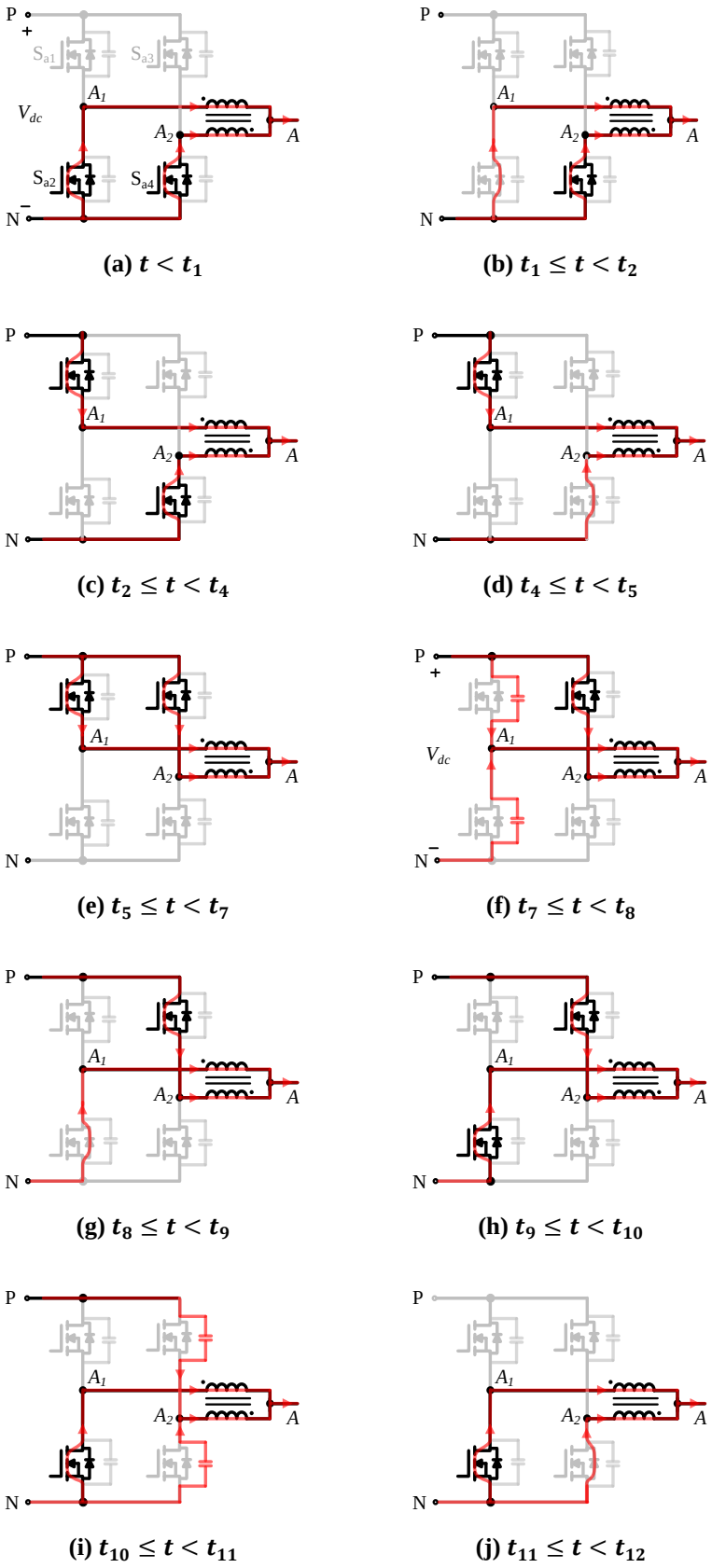
It is worth noting that for a single bridge-leg, the commutation process for the output voltage traversing from 0V to V_{dc} is governed by the gate resistance of the adopted gate driver, while the opposite commutation process is affected by the load current and parasitic elements as analysed in Chapter IV. Referring to Figure 5.24 (a)-(c), the output voltage V_{AN1} ascends from zero to V_{dc} when the turn-ON gate signal is applied to the top switch. Therefore, the output voltage V_{AN1} is denoted by the steep rising edge, as shown in Figure 5.25. According to (5.11), the inverter output voltage V_{AN} becomes $V_{dc}/2$ with the voltage slew rate halved. Meanwhile, the inductor current i_{LA1} starts to increase and while i_{LA2} decreases, with the same current slew rate, as:

$$\frac{di_{LA1}}{dt} = -\frac{di_{LA2}}{dt} = \frac{V_{dc}}{2L} \tag{5.12}$$

The same commutation processes are applicable to the bridge-leg A2 as shown in Figure 5.24 (d) and (e). The output voltage V_{A2} starts to increase from zero to V_{dc} when the turn-ON signal is applied to S_{AH2}, as shown in Figure 5.24 (d) and (e). According to (11), the inverter output voltage V_{AN} traverses from $V_{dc}/2$ to V_{dc}, as shown in Figure 5.25. After the switching transitions, the inductor current remains fixed due to the voltage across the inductors is zero. Referring to Figure 5.25, the duration of the intermediate voltage level of the inverter output voltage V_{AN} depends on the time shift between the gate signal for S_{AH1} and S_{AH2}.

Considering the opposite case, the output voltage traverses from V_{dc} to zero. Figure 5.24 (f)-(h) show the commutation process for bridge-leg A1 from the top switch to the bottom switch. Since the commutation is affected by the load current and parasitic elements of the devices, the voltage V_{AN1} tardily decreases in a linear manner within a fall time t_{fall}, as show in Figure 5.25. t_{fall} is given by:

$$t_{fall} = \frac{2C_{coss}V_{dc}}{i_{load}} \tag{5.13}$$



(a) $t < t_1$ **(b)** $t_1 \le t < t_2$

(c) $t_2 \le t < t_4$ **(d)** $t_4 \le t < t_5$

(e) $t_5 \le t < t_7$ **(f)** $t_7 \le t < t_8$

(g) $t_8 \le t < t_9$ **(h)** $t_9 \le t < t_{10}$

(i) $t_{10} \le t < t_{11}$ **(j)** $t_{11} \le t < t_{12}$

Figure 5.24 Switching commutation process of the module-parallel power inverter.

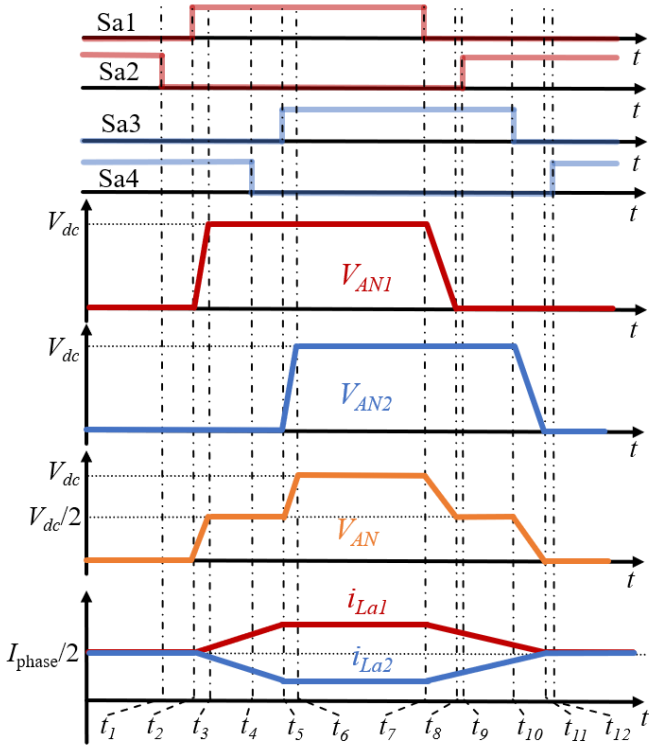


Figure 5.25 The gate signals, the output voltages (VAN1 and VAN2) and currents (iLa1 and iLa2) for bridge-legs (A1 and A2), the inverter output voltage during switching transitions.

The output voltage V_{AN1} remains $V_{dc}/2$ after the current fully traverse to the bottom switch of the bridge leg A1. Meanwhile, the inductor current i_{LA1} decreases and i_{LA2} increases respectively with the same current slew rate as (5.12).

After a dwell time t_{dwell}, the same commutation processes are applied to bridge-leg A2, resulting in the output voltage traverses from $V_{dc}/2$ to zero, as seen in Figure 5.24 (h)-(i). After the switching commutation, the inverter voltage is zero voltage and the currents flow through the coupled inductor resumes the same again, as shown in Figure 5.25.

In summary, the main idea of the module-parallel converter under the Q3L PWM is applying the gate signal for one bridge-leg prior to the other bridge-leg by t_{dwell}. The inverter can generate the Q3L voltage waveform for both the rising and falling edges.

Referring to Figure 5.25, the current flows through the bridge-leg A1 is higher than that of bridge-leg A2 during the switching transient, resulting in higher power loss and temperature rise in bridge-leg A1 than A2. Besides, due to inevitable characteristic difference among the switching devices, the current flows through the two bridge-legs would be unequal under the steady state, resulting in different steady state loss and

temperature rise among the bridge-legs. The above issues would result in core saturation and thermal unbalance among the switching devices reducing the power rating. Therefore, the current sharing among the bridge-legs should be actively controlled.

Figure 5.26 shows a flow chart for the active current balancing approach for phase A, where the inductor currents are measured and accordingly decide which bridge-leg is triggered first before the switching transition. For example, if the $i_{LA1} > i_{LA2}$, the bridge-leg A2 will be switched first.

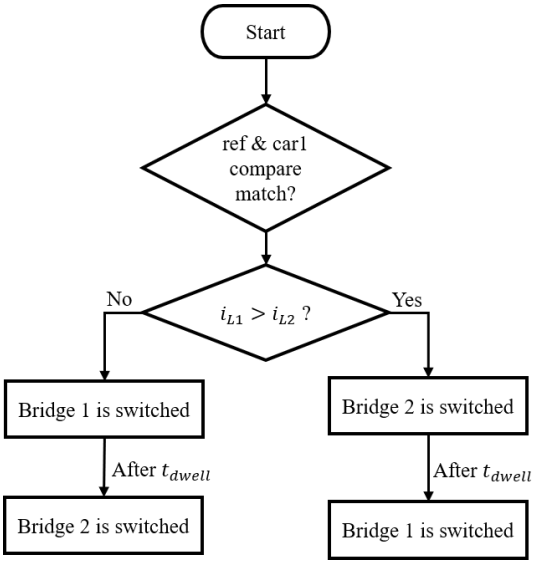


Figure 5.26 Flow chart for active current control.

5.4.3 Experimental Results

In order to verify above analysis, a single-phase bridge-leg parallel inverter based on Wolfspeed E3M0065090D SiC MOSFETs is built in the laboratory. To reduce the core loss and keep the same inductance among the bridge-leg, a coupled inductor with bifilar winding structure is used and the inductance 9.5 μH. Note that the effectiveness of the Q3L PWM on motor terminal overvoltage mitigation mechanism has been experimentally verified with the T-type converter in Section 5.3.4. Therefore, in this section only feasibility of the Q3L PWM using the module-parallel inverter is experimentally verified.

Figure 5.27 shows the voltages at nodes A1, A2 and A, where V_{AN1} and V_{AN2} are the output voltage of bridge-legs A1 and A2, V_{AN} is the output voltage of module-parallel inverter, respectively. As can be noticed, while the output voltage of each bridge-leg shows a two-

level voltage waveform, the module-parallel inverter generates a Q3L voltage waveform. In addition, the slew rate of V_{AN} is half of V_{AN1} and V_{AN2}, as shown in Figure 5.27.

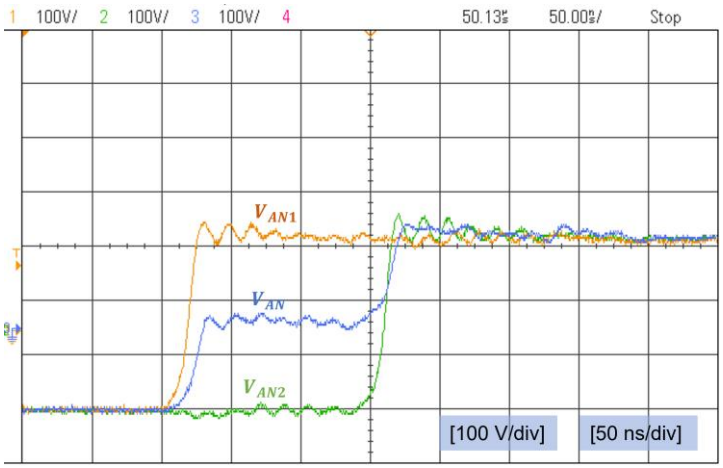


Figure 5.27 Output voltages of the bridge-legs A1 and A2, and the module-parallel inverter.

5.5 Conclusion

This chapter has investigated the active waveform shaping, i.e., Q3L PWM scheme, to mitigate the motor terminal overvoltage oscillations due to the RWP in SiC-based long cable-fed motor drive system. A general idea of overvoltage oscillations mitigation mechanism in the motor drive system has been discussed in both time domain and frequency domain. The detailed implementation of the Q3L PWM scheme using a T-type inverter has been presented. In addition, this chapter has proposed a module-parallel inverter based Q3L PWM to mitigate the motor terminal overvoltage oscillations and extend the devices' current rating. The conclusions of this chapter are the following:

- The motor terminal overvoltage oscillations can be significantly attenuated when the rise and fall times of the PWM voltage pulses are shaped as Q3L PWM with the dwell time $t_{dwell} = 2t_p$.
- The essence of the overvoltage mitigation mechanism of the Q3L PWM scheme is eliminating the excitation source for the overvoltage oscillations by actively shaping the voltages feeding to the drive system, i.e., the component of the excitation source at the anti-resonance frequency of the cable-motor system is zero. Since there is no excitation source to cause the overvoltage oscillations, the motor terminal overvoltage oscillations can be significantly mitigated.

- The parasitic elements of the switching devices and load current may adversely affect the ability of the Q3L T-type converter to mitigate the motor terminal overvoltage oscillations in certain cases, due to the variation in the switching rise and fall times.
- The proposed Q3L module-parallel inverter can generate the Q3L PWM voltage for the motor terminal overvoltage oscillations mitigation as well as elevating the current capacity of switching devices.

Chapter 6

Waveform Shaping to Combat the Motor Terminal Overvoltage: Soft-Switching Voltage Slew Rate (dv/dt) Profiling

This chapter aims to meet Research Objective 4 with the following subtasks listed below:

RO 4.1 Derive the optimum rise and fall times for entirely mitigation of the motor terminal overvoltage.

RO 4.2 Reveal the essence of the overvoltage mitigation mechanism of the proposed voltage slew rate profiling in both time domain and frequency domain.

RO 4.3 Experimental demonstration of the voltage slew rate profiling concept with a SiC-based soft-switching inverter, i.e., the auxiliary resonant commutated pole inverter (ARCPI).

The main content of this chapter has been published by the author in the following publication:

W. Zhou, M. Diab, X. Yuan, and C. Wei, "Mitigation of Motor Overvoltage in SiC-Based Drives using Soft-Switching Voltage Slew-Rate (dv/dt) Profiling'' *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9612-9628, Aug. 2022, doi: 10.1109/TPEL.2022.3157395.

6.1 Introduction

As a rule of thumb, increasing the rise and fall times of inverter output voltages using dv/dt limiter is an effective method to suppress the motor terminal overvoltage oscillations due to the RWP in SiC-based adjustable speed drive system [125]. The mainstream dv/dt limiter is using the passive dv/dt filters such as the RLC dv/dt filter

at the inverter side to reduce the dv/dt of the PWM voltage pulses feeding to the motor drive system [126]. Despite their effectiveness, the passive dv/dt filters have disadvantages such as increasing the size, power loss, and cost of the motor drive system, countering the benefits of using SiC switching devices in motor drive system [32], [134]. Furthermore, how to design the optimum rise and fall times for different cable length? What is the essence of the overvoltage mitigation mechanism by limiting the dv/dt? What is the limitation of these methods? After searching through a body of literature, it was found that the answers to these questions are not reported in literature.

To fill these gaps, this chapter investigates these questions and proposes a soft-switching voltage slew rate (dv/dt) profiling approach to mitigate the motor terminal overvoltage oscillations in long cable-fed adjustable speed drives. The auxiliary resonant commutated pole inverter (ARCPI) is used as an example of the soft-switching inverter to experimentally verify the effectiveness of the proposed approach.

6.2 The Concept of the Voltage Slew Rate Profiling

6.2.1 Analysis in Time Domain

Figure **6.1** illustrates the voltage reflection process and corresponding voltage waveforms of the voltage slew rate profiling approach using a bounced diagram, where it assumes the rise time of the inverter output voltage $t_r = 4t_p$, the amplitude is V_{dc}, and the reflection coefficients $\Gamma_s = -1$ and $\Gamma_m = 1$, i.e., the voltage pulses experience full reflection at the inverter side and motor terminals.

Referring to Figure 6.1, the rising edge of the inverter output voltage V_s can be divided into four identical voltage segments (V_{s1}, V_{s2}, V_{s3} and V_{s4}), where the amplitude is $0.25V_{dc}$ and the rise time is t_p for each segment. The voltage reflection process can be divided into four intervals, as shown in Figure 6.1.

Interval 1 ($\boldsymbol{0 < t \leq 2t_p}$) At $t = 0$, the first segment of the inverter voltage V_{s1} starts to propagate from the inverter side to the motor terminals through power cables where the inverter voltage V_{s1} ramps up from zero to $0.25V_{dc}$ within a rise time t_p. At $t = t_p$, the leading edge of V_{s1} arrives at the motor terminals and experiences a voltage reflection due to the characteristic impedance mismatch between the power cable and motor. Meanwhile, the second segment of the inverter voltage V_{s2} starts to propagate from the inverter side to the motor terminals though power cables. At $t = 2t_p$, the full voltage V_{s1} arrives at the

motor terminals and experiences a voltage reflection. Since the reflected coefficient at the motor terminals $\Gamma_m = 1$, the amplitude of the reflected voltage V_{m1}^- is $0.25V_{dc}$. Therefore, after the first voltage reflection interval, the motor terminal voltage rises from $0\,V$ to $0.5V_{dc}$, as shown in Figure 6.1.

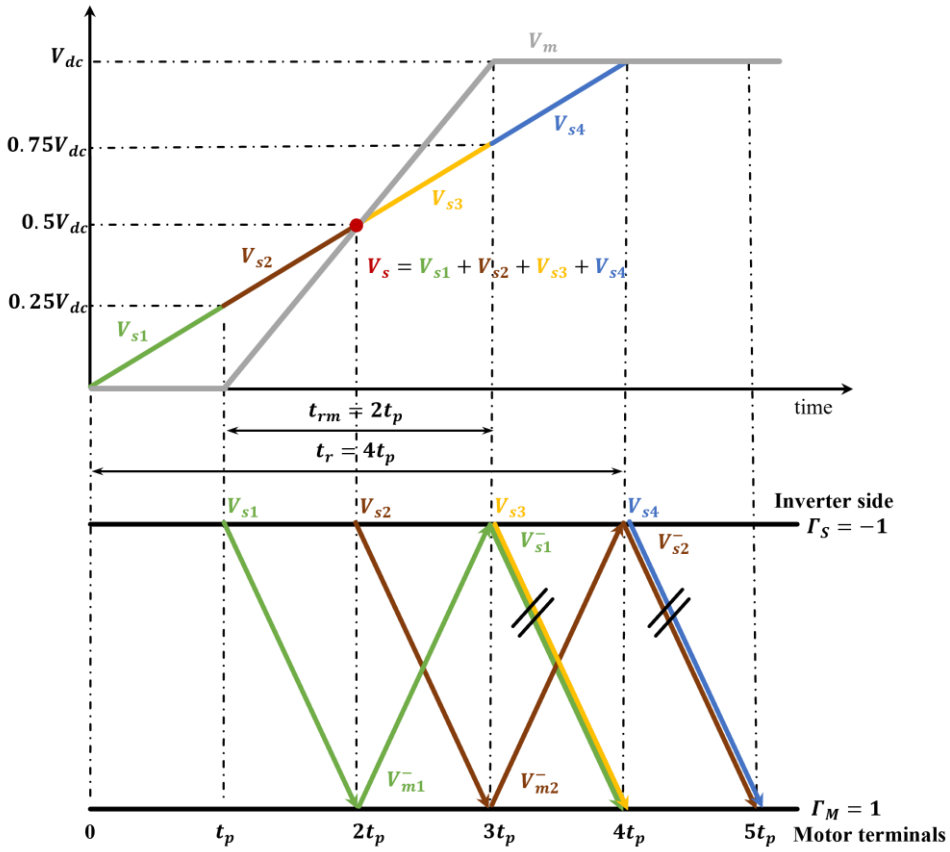


Figure 6.1 A bounced diagram of the voltage slew rate profiling approach.

Interval 2 ($2t_p < t \leq 3t_p$) After the first voltage reflection, the reflected voltage V_{m1}^- propagates from the motor terminals toward the inverter side. Referring to Figure 6.1, at $t = 2t_p$, the leading edge of V_{s2} arrives at the motor terminals and experiences a voltage reflection due to the characteristic impedance mismatch between the cable and motor. At a time $3t_p$, the full voltage V_{s2} arrives at the motor terminals and experiences a full voltage reflection, where the amplitude of the resultant reflected voltage V_{m2}^- is $0.25V_{dc}$. Therefore, after the second voltage reflection the motor terminal voltage increases from $0.5V_{dc}$ to V_{dc}, as shown in Figure 6.1.

It is worth noting that, at $t = 3t_p$, the full reflected voltage V_{m1}^- arrives at the inverter side and experiences a voltage reflection due to the characteristic impedance mismatch between

the power cable and inverter. Since $V_{m1}^{-} = 0.25V_{dc}$ and the reflection coefficient at the inverter side $\Gamma_s = -1$, the reflected voltage V_{s1}^{-} is $-0.25V_{dc}$. Referring to Figure 6.1, at $t = 3t_p$, the third voltage segment V_{s3} with an amplitude $0.25V_{dc}$ starts to propagate from the inverter side to the motor side, the voltage V_{s3} will be countered by the reflected voltage V_{s1}^{-}.

Interval 3 ($3t_p < t \leq 4t_p$) At $t = 4t_p$, the full reflected voltage V_{m2}^{-} arrives at the inverter side and experiences a voltage reflection due to the characteristic impedance mismatch between the power cable and inverter. Since $V_{m2}^{-} = 0.25V_{dc}$ and the reflection coefficient at the inverter side $\Gamma_s = -1$, the reflected voltage V_{s2}^{-} is $-0.25V_{dc}$. Referring to Figure 6.1, at $t = 4t_p$, the fourth voltage segment V_{s4} with an amplitude $0.25V_{dc}$ starts to propagate from the inverter side to the motor terminals, the voltage V_{s4} will be countered by the reflected voltage V_{s2}^{-}.

Interval 4 ($t > 4t_p$) Referring to Figure 6.1, there is no voltage propagating to the motor terminals after $4t_p$. Therefore, the motor terminal voltage remains constant at V_{dc}.

According to the voltage reflection process discussed above, the reflected voltage V_{s1}^{-} caused by V_{s1} is counterbalanced by the third segment of the inverter voltage V_{s3} at the inverter side, and the reflected voltage V_{s2}^{-} caused by V_{s2} is counterbalanced by the fourth segment of the inverter voltage V_{s4} at the inverter side. After the reflected process, the motor terminal voltage remains constant at V_{dc}. Therefore, the motor terminals will not experience overvoltage oscillations when the rise time is set as $4t_p$.

Referring to Figure 6.1, the rise time t_{rm} of the motor terminal voltage is half of the inverter output voltage, i.e., $t_{rm} = 0.5t_r = 2t_p$, and the motor terminal voltage V_m crosses the inverter voltage V_s at the switching rise time midway. It should be noted that this is an indicator to judge whether the rise time is the optimum rise time to entirely mitigate the motor terminal overvoltage oscillations associated with the voltage reflection. When the rise time t_r is lower than the optimum rise time $4t_p$, the motor terminal voltage V_m crosses V_s before the midway of V_s. While for the opposite case, i.e., the rise time t_r is longer than the optimum rise time, the motor terminal voltage V_m crosses V_s after the midway of V_s. Common to both cases, the motor terminal overvoltage oscillations due to the RWP are partially mitigated.

Although Figure 6.1 only illustrates the voltage slew rate profiling concept at the rising switching transition by actively shaping the rise time $t_r = 4t_p$, the same results can be obtained at the falling switching transition when the fall time $t_f = t_r = 4t_p$.

For a given adjustable speed drive system, the motor terminal overvoltage is proportional to the inverter voltage, i.e., the excitation source. Therefore, the motor terminal overvoltage mitigation mechanism of the voltage slew rate profiling can be further analysed using the superposition principle in time domain, as illustrated in Figure 6.2, where the inverter output voltage V_s consists of two identical voltage steps V_{s1} and V_{s2} with the rise time t_r and amplitude $0.5V_{dc}$.

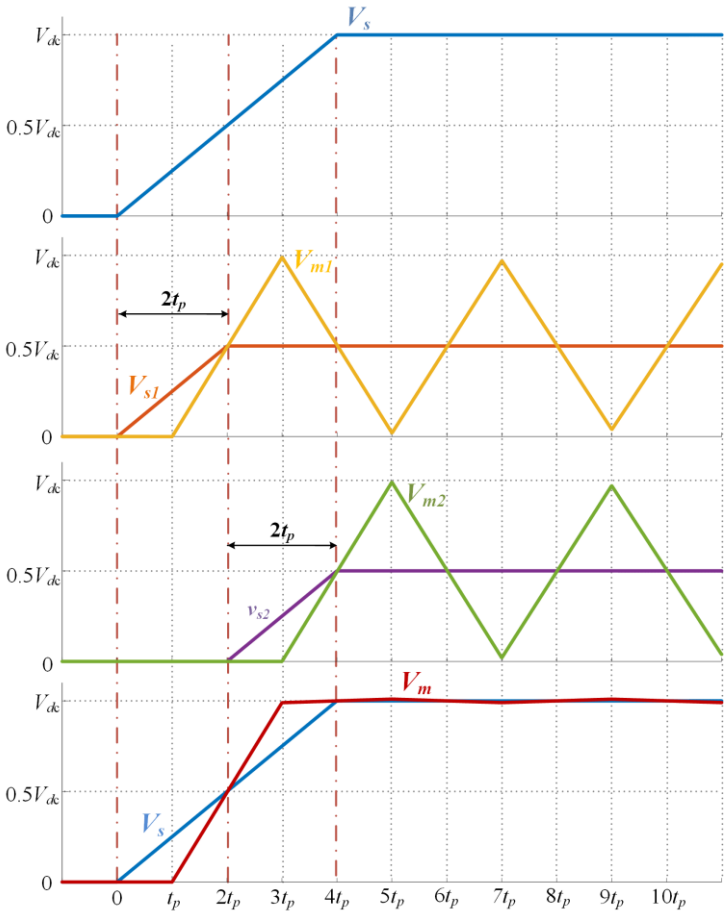


Figure 6.2 Overvoltage mitigation mechanism of the voltage slew-rate profiling approach in time domain using the superposition principle.

Referring to Figure 6.2, the two voltage steps V_{s1} and V_{s2} propagate from the inverter side to the motor terminals experiencing voltage reflections due to the characteristic impedance

mismatch between the cable and motor in the motor drive system. The inverter output voltage V_s can be given by the two voltages V_{s1} and V_{s2}, as:

$$V_s = V_{s1} + V_{s2} \tag{6.1}$$

where, the amplitudes of V_{s1} and V_{s2} are $0.5V_{dc}$.

Accordingly, the resultant motor terminal voltage V_m can be given as:

$$V_m = V_{m1} + V_{m2} \tag{6.2}$$

where, V_{m1} and V_{m2} are the consequent motor terminal voltages of V_{s1} and V_{s2} due to the RWP in the motor drive system, respectively. With unity reflection coefficient at the motor terminals, the voltage pulses V_{s1} and V_{s2} experience full voltage reflection once arriving at the motor terminals. Therefore, the voltage magnitude of V_{m1} and V_{m2} is V_{dc}, i.e., double the voltage magnitude of V_{s1} and V_{s2}, while the voltage oscillation frequency is $1/4t_p$.

If the rise times of V_{s1} and V_{s2} are $2t_p$, i.e., V_{s2} lags V_{s1} by $2t_p$, the motor terminal overvoltage oscillations caused by V_{s1} and V_{s2} can be counterbalanced altogether, as demonstrated in Figure 6.2. Thus, the amplitude of the motor terminal voltage V_m is the same with the inverter voltage V_s. Therefore, the motor terminals will not experience the overvoltage oscillations due to the RWP in the motor drive system.

6.2.2 Analysis in Frequency Domain

To reveal the essence of motor terminal overvoltage mitigation mechanism of the proposed voltage slew rate profiling approach, a frequency domain analysis is conducted in this section.

The inverter output voltage of one phase-leg with fixed duty cycle can typically be represented by a periodic trapezoidal waveform, as shown in Figure 6.3, which is the fundamental element to construct the inverter output PWM voltage waveform. Note that A is the amplitude of the trapezoidal waveform, τ is the average pulse width measured at half the pulse amplitude, T is the switching period, and t_r and t_f are the rise and fall times, respectively. For simplicity, the trapezoid shown in Figure 6.3 is assumed to be symmetrical (i.e., $t_r = t_f$) with a constant duty ratio ($D = \tau/T$).

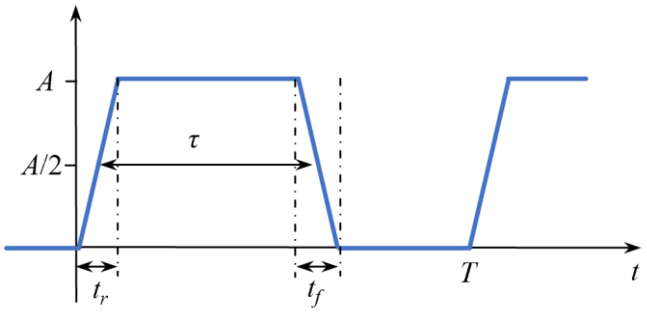


Figure 6.3 Trapezoidal pulse-train.

According to the properties of the Fourier series, the trapezoidal waveform illustrated in Figure 6.3 can be expressed as:

$$V(t) = \sum_{n=-\infty}^{n=\infty} c_n e^{jn\omega t} \tag{6.3}$$

where, ω is the switching frequency of the PWM waveform and c_n $(n = 1, 2, 3, \ldots)$ is the Fourier series coefficient. Note that c_n can be given in complex exponential form, as [23]:

$$c_n = AD\,\mathrm{sinc}\left(\frac{n\omega\tau}{2}\right)\mathrm{sinc}\left(\frac{n\omega t_r}{2}\right)e^{-jn\omega\left(\frac{\tau+t_r}{2}\right)} \tag{6.4}$$

where, $\mathrm{sinc}(x)$ denotes $\sin(x)/x$.

At the anti-resonance frequency f_{osc} of the cable-motor system, the Fourier series coefficient is:

$$c_n = AD\,\mathrm{sinc}(\pi f_{osc}\tau)\,\mathrm{sinc}(\pi f_{osc} t_r)\,e^{-j\pi f_{osc}(\tau+t_r)} \tag{6.5}$$

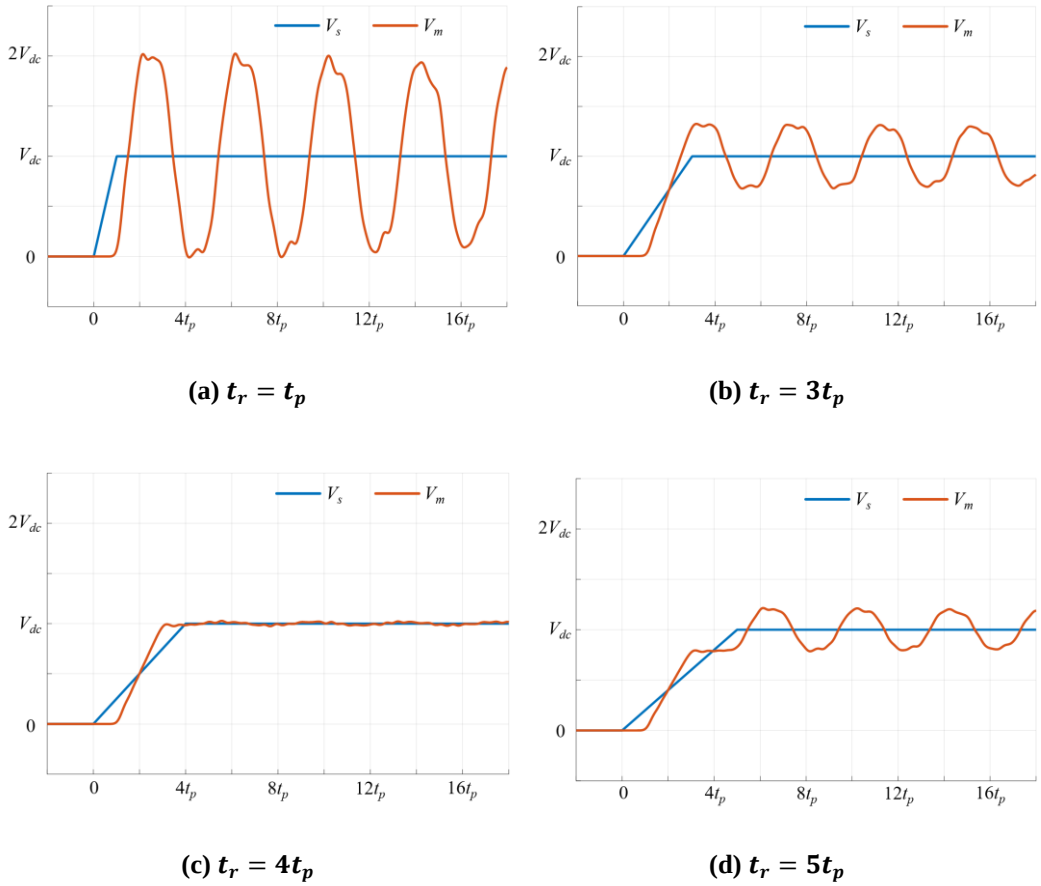
From (6.5), it can be derived that when $t_r = 1/f_{osc}$, the coefficient $c_n = 0$, i.e., at this rise and fall times setting there is no voltage component at the cable anti-resonance frequency. Therefore, the motor terminal overvoltage oscillations can be entirely mitigated because there is no excitation source to produce the resonance at the cable anti-resonance frequency.

Since the anti-resonance frequency $f_{osc} = 1/4t_p$, the optimal rise and fall times t_{r_opt} for the motor terminal overvoltage mitigation can be given as:

$$t_{r\_opt} = 4t_p \tag{6.6}$$

6.3 Simulation Study

To evaluate the proposed voltage slew rate profiling approach for motor terminal overvoltage mitigation, a cable-motor model based on MATLAB/Simulink is built to predict the motor terminal overvoltage in the long cable-fed motor drive system at different inverter switching rise and fall times, i.e., $t_r = t_p$, $t_r = 3t_p$, $t_r = 4t_p$, and $t_r = 5t_p$, respectively. The detailed cable simulation model and its parameters can be found in Chapter III. The inverter output voltage is emulated by the PWM voltage pulse-train with adjustable rise and fall times. It is worth noting that in order to emulate the worst case of the drive system, the motor side is regarded as an open circuit, where the reflected coefficient at the motor terminals $\Gamma_m = 1$, the voltages are fully reflected. The simulation results are shown in Figure 6.4.



(a) $t_r = t_p$ **(b) $t_r = 3t_p$**

(c) $t_r = 4t_p$ **(d) $t_r = 5t_p$**

Figure 6.4 Inverter and motor voltage waveforms at different rise time setting. In order to emulate the worst case of the drive system, the motor side is regarded as an open circuit. The cable length l_c=10m, the wave propagation time t_p = 51ns.

In Figure 6.4 (a), the rise time of the inverter output voltage is set as t_p to show the voltage reflection phenomenon at the motor terminals due to the impedance mismatch between the cable and motor. As shown, the motor terminals experience significant overvoltage oscillations due to the RWP when the rise time equals the wave propagation time (i.e., $t_r = t_p$), where the peak motor voltage is 2 pu, the oscillation frequency is $1/4t_p$.

With the rise time increasing, the motor terminal overvoltage oscillations can be partially or completely mitigated as evidenced in Figure 6.4 (b)-(d). Referring to Figure 6.4 (b), when the rise time is increased to triple the wave propagation time, i.e., $t_r = 3t_p$, the motor terminal overvoltage oscillations can be partially attenuated, where the peak motor terminal voltage is 1.4 pu, the oscillation frequency remains unchanged at $1/4t_p$. In Figure 6.4 (c), the rise time is set as the optimum rise time, i.e., $t_r = 4t_p$, the motor terminal overvoltage can be completely mitigated with negligible oscillations. However, if the rise time is further increased, the motor terminal overvoltage is partially attenuated to 1.25pu as shown in Figure 6.4 (d), where the rise time $t_r = 5t_p$.

It is worth noting that the voltages cross point of the inverter and motor implies the optimum setting of the rise time. Figure 6.4 (b) shows the case that the switching rise time are set slower than the optimum rise time (i.e., $t_r = 3t_p$), the motor terminal voltage V_m crosses the inverter voltage V_s before the midpoint. Oppositely, the motor terminal voltage V_m crosses the inverter voltage V_s after the midpoint, as shown in Figure 6.4 (d). With the optimal setting of the rise time (i.e., $t_r = 4t_p$), the motor terminal voltage V_m crosses the inverter voltage V_s at the midpoint, as shown in Figure 6.4 (c).

Figure 6.5 shows the simulation results of the maximum motor terminal voltage variation at different rise and fall times, where the rise and fall times are set as integer multiples of the wave propagation time. Referring to Figure 6.5, overall, the motor terminal overvoltage decreases with the rise time. It is worth noting that there is almost no motor terminal overvoltage when $t_r = 4nt_p$ $(n = 1, 2, 3, \dots)$. This is because at these specific rise times, there is no excitation source to produce the resonant at the cable anti-resonance frequency, as previously analysed.

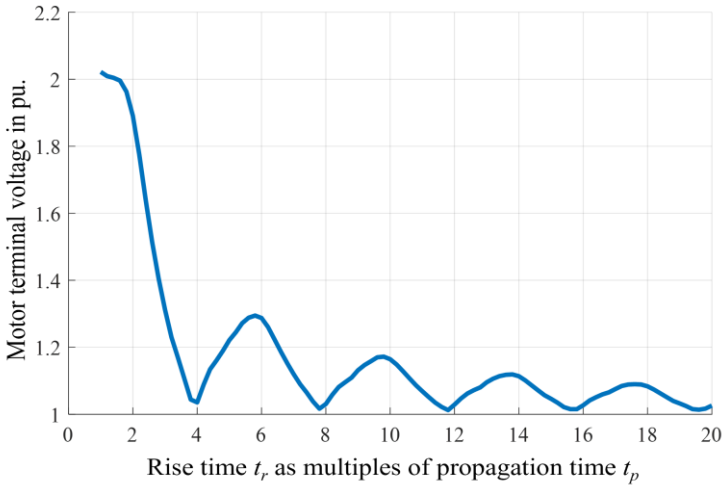


Figure 6.5 Variation of the maximum motor terminal voltage with the rise time.

6.4 Implementation of the Voltage Slew Rate Profiling with the Auxiliary Resonant Commutated Pole Inverter

The proposed voltage slew rate profiling can be implemented using soft-switching inverters because their output voltage can be actively profiled due to the resonance of the resonant circuit in these inverters. In general, the output voltage of the soft-switching inverter is part of a sinusoidal waveform due to the resonance in the inverter.

While several soft-switching inverter topologies have been proposed in literature, they can be classified into two categories, i.e., the resonant dc-link inverters (RDCIs) and commutated pole inverters (CPIs) [155], [156]. Compared with RDCIs, CPIs are easier to control and have higher efficiency where they are more common in literature [68], [69], [156]. One example of the CPIs is the ARCPI that was proposed in the 1990s [157]. The ARCPI has become a popular soft-switching inverter topology due to its advantages such as simple structure, easy to control, and high degree of PWM compatibility [156]. A multitude of papers have reported the modelling, control and protection of the ARCPI [158]–[165].

However, their main focuses are on improving the system efficiency and reliability, the profiled dv/dt is merely treated as a by-product. In contrast, this PhD work selects the ARCPI as a candidate soft-switching inverter topology using its controllable dv/dt characteristic by actively profiling the rise and fall times as $4t_p$ to implement the voltage slew rate profiling approach for motor terminal overvoltage oscillations mitigation.

Therefore, this PhD work explores new function of the ARCPI without sacrificing its soft-switching advantages.

Figure 6.6 illustrates the circuit diagram of a single-phase SiC-based ARCPI, where it is composed of a main branch and an auxiliary branch [68]. As shown, the main branch consists of a standard half bridge phase-leg (S_1 and S_4) and two resonant capacitors (C_{r1} and C_{r4}), where $C_{r1} = C_{r4} = C_r$. The auxiliary resonant branch is composed of a pair of auxiliary switches (S_2 and S_3) that are in common source configuration, and a resonant inductor (L_r). The main branch is interconnected with the auxiliary branch between the dc-bus middle point O and the output node *A* [26]. Note that two clamping diodes (D_{c1} and D_{c2}) are not the main part of the ARCPI which are only used to protect the auxiliary switches against overvoltage caused by the resonance between the inductor L_r and the parasitic capacitance of the auxiliary switches [68]. The three-phase ARCPI version can be realized by employing three phase-legs with the three auxiliary resonant circuits sharing the same dc-bus middle point O [156].

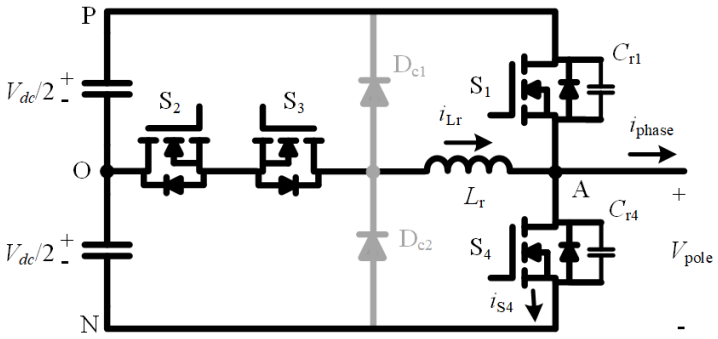


Figure 6.6 A single-phase SiC-based ARCPI circuit diagram.

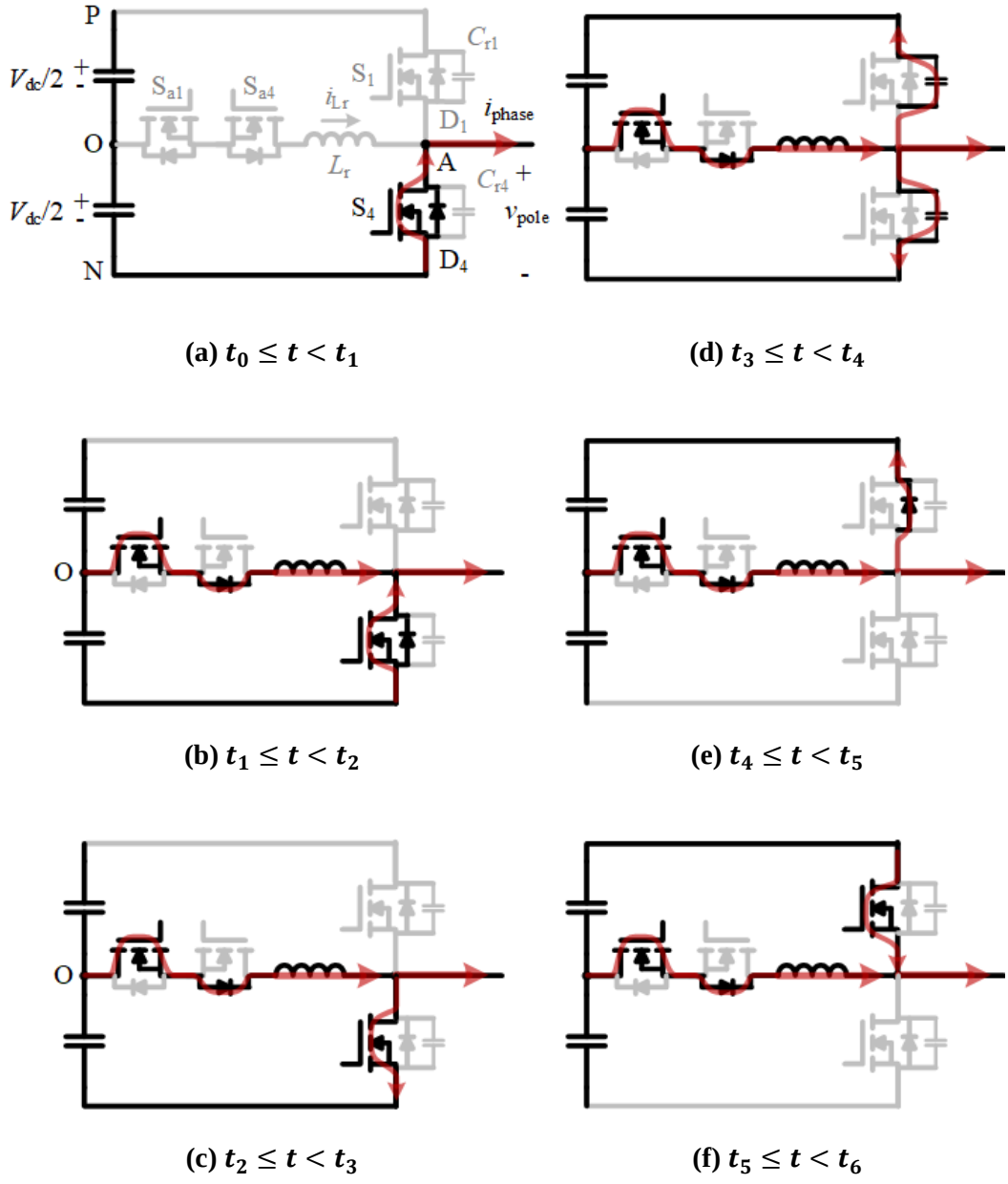
6.4.1 Principle of Operations

The ARCPI operation process has been extensively described in literature [26], [68], [156]. Here, only the basic operation process will be recalled.

Figure 6.7 illustrates the turn-ON transitions when the inverter output current $i_{phase} > 0$, i.e., the switching commutation process from the bottom main switch S_4 to the top main switch S_1. The waveforms of the gate driver signal, the resonant inductor current i_{Lr}, and the inverter output voltage V_{pole} during the turn-ON transitions are shown in Figure 6.8. Note that the auxiliary switch S_2 is involved in the commutation process from S_4 to S_1, while the auxiliary switch S_3 is involved in the opposite commutation process regardless of

the load current polarity. Since the switching commutation process is very short (typical within 1μs), the inverter output current i_{phase} is assumed to be constant I_{phase} in the following analysis.

Referring to Figure 6.7 and Figure 6.8, the turn-ON commutation process can be divided into four intervals, i.e., the ramp up interval, resonant interval, soft-switching interval, and ramp down interval, which will be analysed in detail in the following part.



(a) $t_0 \le t < t_1$ **(d) $t_3 \le t < t_4$**

(b) $t_1 \le t < t_2$ **(e) $t_4 \le t < t_5$**

(c) $t_2 \le t < t_3$ **(f) $t_5 \le t < t_6$**

Figure 6.7 The turn-ON switching commutation process of the ARCPI when the load current is positive.

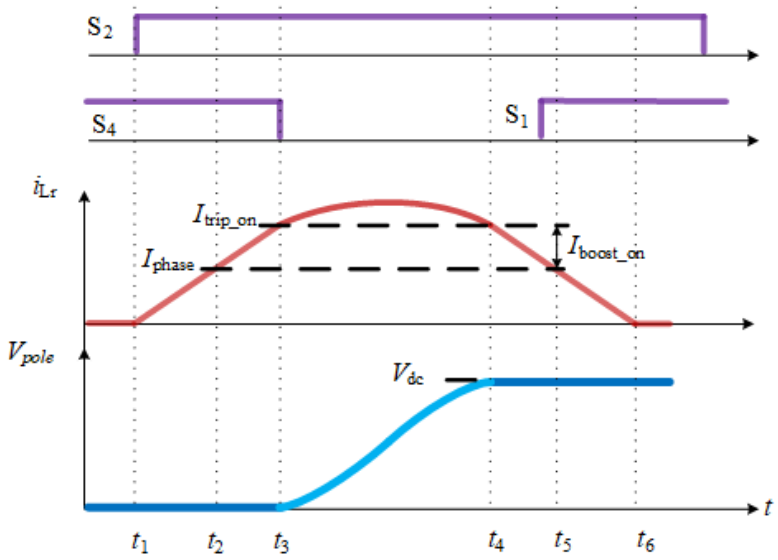


Figure 6.8 The gate signals, the resonant inductor current i_{Lr}, and the output voltage V_{pole} during the turn-ON commutation process when the load current is positive.

Ramp up interval ($t_1 \leq t < t_3$) [Figure 6.7 (b) and (c)] Referring to Figure 6.7 (a), before the turn-ON commutation process, the load current flows through the bottom main switch S_4, the inverter output voltage is 0V. At time t_1, the auxiliary switch S_2 is turned-ON as shown in Figure 6.7 (b) and Figure 6.8. Since the auxiliary switch S_2 is in series with the resonant inductor L_r, S_2 is turned-ON under zero current switching (ZCS). The resonant inductor current i_{Lr} starts to increase linearly with the voltage $V_{dc}/2$ being imposed to the resonant inductor L_r, as shown in Figure 6.8. The amplitude of the inductor current can be calculated as a function of the resonant inductance L_r, the dc-link voltage V_{dc} and the ramp up time t_{ramp}, as:

$$i_{Lr} = \frac{V_{dc}}{2L_r} t_{ramp} \tag{6.7}$$

Meanwhile, the bottom main switch current i_{S4} decreases at the same rate as (6.7). At time $t = t_2$, the inductor current i_{Lr} exceeds the phase current and then continues to ramp up. Note that S_4 conducts the difference of $i_{Lr} - i_{phase}$, as shown in Figure 6.7 (c).

When $t = t_3$, the inductor current reaches to the prescribed trip current I_{trip_on}. The difference between the trip current and the inverter output current is denoted as the boost current I_{boost_on}, which is given as:

$$I_{boost\_on} = I_{trip\_on} - I_{phase} \tag{6.8}$$

The boost current is used to counter the power loss in the auxiliary branch and provide enough energy for the imminent resonance process which is necessary to guarantee the success of the resonance process [156]. The boost current affects the rise and fall times of the output voltages for a given ARCPI [166].

According to (6.7), for a prescribed I_{trip_on}, the ramp up time t_{ramp_on} can be calculated as:

$$t_{ramp\_on} = \frac{2L_r I_{trip\_on}}{V_{dc}} \tag{6.9}$$

Resonant interval ($t_3 \leq t < t_4$) [Figure 6.7 (d)] At time t_3, S_4 is turned OFF and the resonant inductor L_r resonates with the two resonant capacitors C_{r1} and C_{r4} simultaneously. Referring to Figure 6.8, during this interval the resonant capacitors C_{r1} and C_{r4} are charged and discharged in a sinusoidal manner, respectively. Therefore, the inverter output voltage V_{pole} starts ascending from 0V to the dc-link voltage V_{dc} in a resonant manner and then it is clamped by the antiparallel diode of the main switch S_1 after the time t_4.

In fact, the resonant interval t_{res_on} is the rise time of the output voltage V_{pole}, which can be calculated as [156]:

$$t_{res\_on} = \frac{2}{\omega_r} tan^{-1}\left(\frac{V_{dc}}{2Z_r(I_{trip\_on} - I_{phase})}\right) \tag{6.10}$$

where ω_r and Z_r are the resonant angular frequency and resonant impedance of the ARCPI, and are given as:

$$\omega_r = \sqrt{\frac{1}{2L_r C_r}} \tag{6.11}$$

$$Z_r = \sqrt{\frac{L_r}{2C_r}} \tag{6.12}$$

Therefore, the rise time of the inverter output voltage is determined by the boost current and resonant impedance of the ARCPI. Since it makes no sense to change the hardware (i.e., L_r and C_r) of the ARCPI once designed, the rise time can be adjusted by controlling

the value of the boost current according to (6.10). A higher boost current would result in a shorter rise time. This is because the sinusoids oscillate to more extreme peaks with more energy providing to the resonant circuit, the resonance delivers extreme and shorter output voltage edges. According to (6.10), when $\frac{V_{dc}}{I_{trip\_on}-I_{phase}}$ keeps fixed, the rising time of the output voltage V_{pole} can remain constant regardless of the dc-link voltage.

Soft-switching interval ($t_4 \leq t < t_5$) [Figure 6.7 (e)] After t_4, the voltage across the main switch S_1 is clamped to zero by its antiparallel diode, as shown in Figure 6.7 (e). The resonant inductor current decreases in a linear manner since $-V_{dc}/2$ is applied to L_r. S_1 can be turned on under zero voltage switching (ZVS) before the inductor current reaches I_{phase} again. Therefore, the voltage and current of S_1 are completely decoupled with zero switching loss theoretically, as shown in Figure 6.8.

Ramp down interval ($t > t_5$) [Figure 6.7 (f)] After t_5, the inductor current i_{Lr} continues to decrease in a linear manner. Once the inductor current reaches zero, the auxiliary switch S_3 can be turned OFF to complete the switching commutation process.

Similar switching commutation processes apply to the turn-OFF switching transitions. Figure 6.9 shows the waveforms for the turn-OFF commutation process. Note that the boost current I_{boost_off} during the turn-OFF transition is different from that of the turn-ON transition, where I_{boost_off} is given as [26], [68], [156]:

$$I_{boost\_off} = I_{trip\_off} + I_{phase} \tag{6.13}$$

where, I_{trip_off} is the tripped current for the turn-OFF process.

The resonant interval of the turn-OFF switching process can be calculated as:

$$t_{res\_off} = \frac{2}{\omega_r} tan^{-1}\left(\frac{V_{dc}}{2Z_r(I_{trip\_off} + I_{phase})}\right) \tag{6.14}$$

According to (6.14), when $\frac{V_{dc}}{I_{trip\_off}+I_{phase}}$ keeps fixed, the falling time of the output voltage V_{pole} can remain constant regardless of the dc-link voltage.

Overall, all the main switches of the ARCPI achieve ZVS and all the auxiliary switches achieve ZCS as analysed in above commutation process. Therefore, there is no switching

losses in the ARCPI, theoretically. The voltage and current of the main switches are decoupled and the output voltage waveform is smoothed and shaped in a sinusoidal manner.

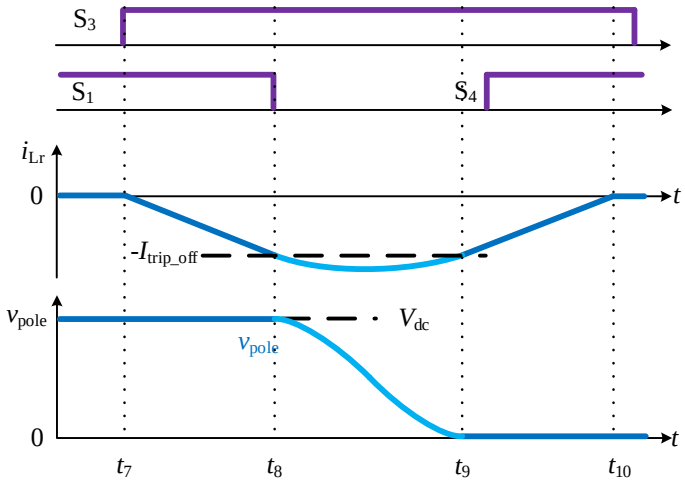


Figure 6.9 The gate signals, the resonant inductor current i_{Lr}, and the output voltage V_{pole} during the turn-OFF process when the load current is positive.

6.4.2 The Control of the ARCPI

According to the switching commutation process discussed above, the rise and fall times of the inverter output voltage can be actively profiled by controlling how much boost current is put into the resonant circuit [156]. There are two classical control methods, i.e., the fixed-timing control and variable-timing control [166]. The fixed-timing control keeps the ramp-up/down interval fixed, while the variable-timing control varies ramp-up/down interval according to the load current throughout the fundamental cycle [26].

Figure 6.10 shows the trip current I_{trip_on} during the turn-ON transitions for the fixed-timing control and the variable-timing control when $i_{phase} > 0$. As can be noticed, compared with the fixed-timing control, the variable-timing control has a lower trip current because it adjusts the trip current according to the load current in the fundamental cycle. This means it would increase the control complexity. On the other hand, the variable-timing control has a constant rise time for the inverter output voltage in the fundamental cycle as benefits, as shown in Figure 6.11.

Since the proposed voltage slew rate profiling approach needs to set the rise time of the inverter output voltage as the optimum time $4t_p$ to mitigate the motor terminal overvoltage

oscillations, only the variable timing control is suitable to carry out the voltage slew rate profiling approach.

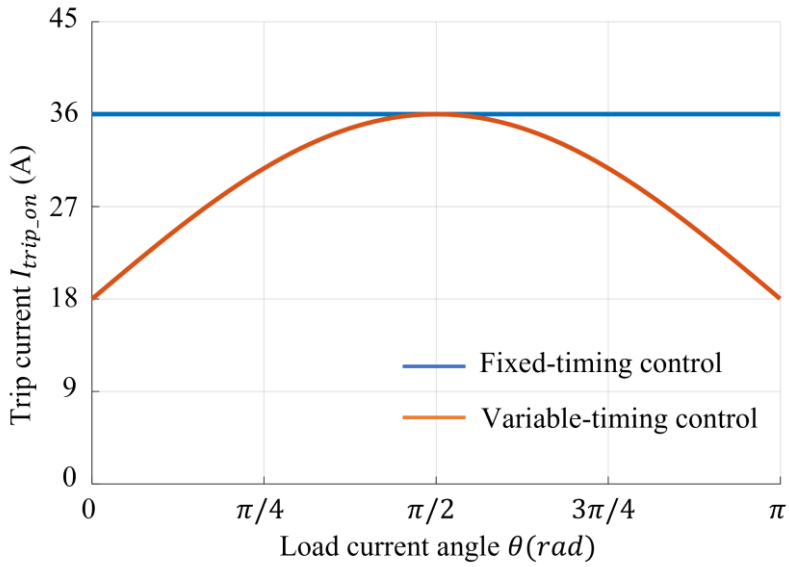


Figure 6.10 The trip current for the variable-timing control and fixed-timing control in the fundament cycle, where L_r = 2.7μH, C_r = 8.2nF, V_{dc} = 500V.

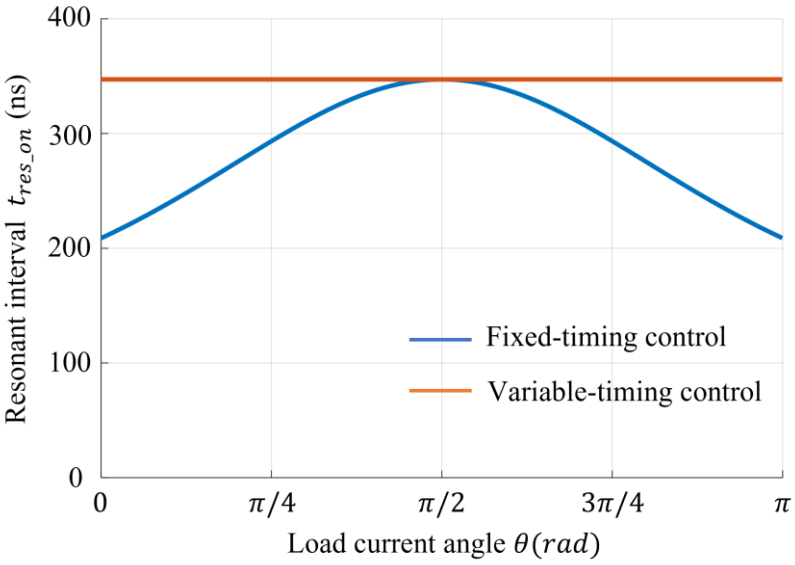


Figure 6.11 The resonant interval for the variable-timing control and fixed-timing control in the fundament cycle, where L_r = 2.7μH, C_r = 8.2nF, V_{dc} = 500V.

6.4.3 Parameters Design

To verify the voltage slew rate profiling approach for the motor terminal overvoltage mitigation, a three-phase ARCPI prototype is designed and built in the laboratory. A case

study for a three-phase SiC ARCPI supplying a motor through 12m long, 12 AWG cable is considered in this PhD work. Due to the limitation of the laboratory, a 500V, 5kW ARCPI prototype is designed. The maximum modulation index is assumed to be 0.83 and the power factor is assumed to be 0.88 (inductive), where such a circuit condition leads to a maximum load current $I_{peak} = 18$ A. Note that there is no physical limitation for the maximum modulation index, i.e., the modulation index is just related to the load current level. For the 12m long, 12 AWG cable length, the wave propagation time t_p is about 73 ns. The wave propagation time can be determined using the methods presented in the Appendix.

Figure 6.12 illustrates the design flow diagram. As shown, the flow diagram consists of five processes, where it begins with the key parameters defining such the dc-link voltage, the required output power rating, and cable parameters.

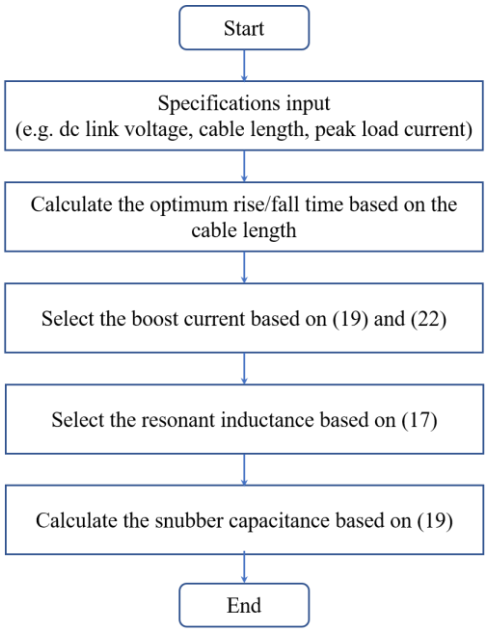


Figure 6.12 A The flow chart for the ARCPI design.

1) Selection of the rise/fall times

To mitigate the motor terminal overvoltage at both rising and falling edges, the rise time and fall times are designed to be the optimum rise and fall times $4t_p$, i.e., $t_r = 292$ ns.

2) Selection of the trip current

According to the switching commutation process, the auxiliary switches experience the highest current stress in the ARCPI. The maximum current in the auxiliary branch I_{aux_pk} is calculate, as [156]:

$$I_{aux\_pk} = I_{peak} + \sqrt{\left(\frac{V_{dc}}{2Z_r}\right)^2 + \left(I_{trip\_on} - I_{peak}\right)^2} \tag{6.15}$$

The amplitude I_{aux_pk} indicates the devices' current stress and power loss in the auxiliary branches during the switching commutation process. According to (6.15), a larger trip current and small resonant impedance leads to higher current stress for the auxiliary switches and causes higher conduction loss in the auxiliary branches. Thus, a smaller trip current and larger resonant impedance Z_r are recommended for the design to reduce the switching devices' current stress and the power loss in the auxiliary branches.

According to (6.10) and (6.14), to achieve the same rise and fall times for the output voltage, the following condition should be satisfied:

$$I_{trip\_on} - I_{phase} = I_{trip\_off} + I_{phase} \tag{6.16}$$

Since $I_{trip\_on} \geq 0$ and $I_{trip\_off} \geq 0$, the minimum boost current can be achieved when $I_{trip\_off} = 0$ at the maximum load condition I_{peak}. Therefore, the minimum boost current can be given as:

$$I_{boost\_on} = I_{boost\_off} = I_{peak} \tag{6.17}$$

3) Selection of the resonant circuit parameters

Figure 6.13 shows the relationship between the resonant capacitance C_r and resonant inductance L_r when the rise time $t_r = 292ns$. As can be noticed, C_r decreases with L_r, i.e., the resonant impedance Z_r increases with the resonant inductance L_r. Since a larger Z_r can reduce the maximum current in the auxiliary branch I_{aux_pk}, a larger inductance is recommended for the design. However, a larger inductance results in longer ramp up time which may limit the maximum switching frequency and reduce the dc-link utilization ratio. Considering the trade-off between the maximum current in the auxiliary branch and the total duration for the switching process, the maximum ramp up time t_{ramp_on} is set as 400ns.

According to (6.7), the resonant inductance can be designed as:

$$L_{\mathrm{r}} = \frac{V_{\mathrm{dc}} t_{\mathrm{ramp\_on}}}{4 I_{\mathrm{phase\_max}}} \tag{6.18}$$

Therefore, when $t_{\mathrm{ramp\_on}} = 400\mathrm{ns}$, the resonant inductance is $L_{\mathrm{r}} = 2.7$ µH.

Substituting the optimum rise time $t_{opt} = 292\ ns$ and $I_{boost\_on} = 18$ A, $L_{\mathrm{r}} = 2.7$ µH into (6.10), results in $C_r = 9.2$ nF. Due to the availability of the capacitor, the capacitance of 8.2 nF is selected. Note that, the resonant circuit parameters are designed under the ideal conditions. The resonant interval is affected by the parasitic resistance in the resonant circuit and the turn-ON and turn-OFF delay of the switches [156] . Therefore, the boost current should be tuned to get the designed rise and fall times during the experiment. Therefore, the parameters of the ARCPI are shown in Table 6.1

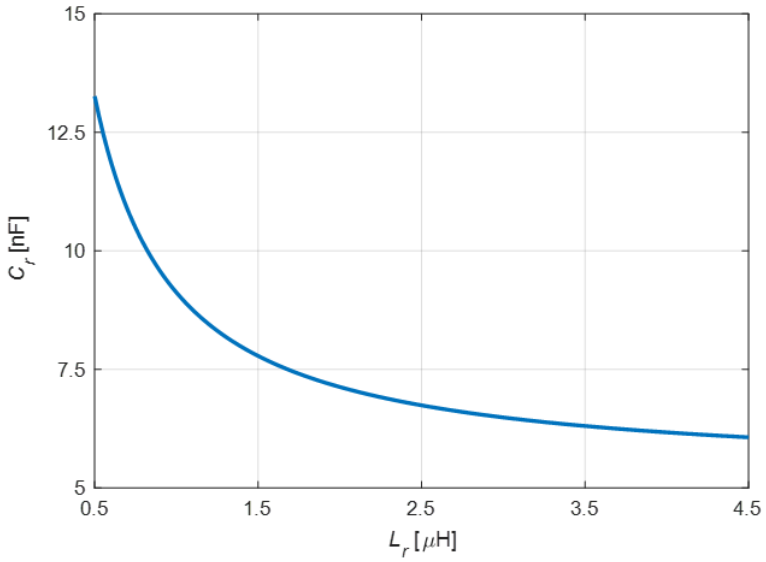


Figure 6.13 The relationship between the resonant capacitance C_r and resonant inductance L_r for the designed rise time.

Table 6.1 The ARCPI parameters.

Symbol	Value
Resonant inductance (L_r)	2.7 µH
Resonant capacitance (C_r)	8.2 nF

6.5 Experimental Verification

6.5.1 Experimental Set-up

In order to prove the effectiveness of the proposed soft-switching voltage slew rate profiling, a three-phase SiC-based ARCPI is used to supply a motor through a long cable, as shown in Figure 6.14. It worth noting that the magnetic flux is confined in the semi-closed slot region and no flux links the rotor at the high frequency region [167], [168]. Therefore, there is no significant difference for the characteristic impedance between the stator and the standard motor at the high frequency region [168]. Henceforth, only the stator winding is employed to perform the experimental study. The main parameters of the motor are given in Table 6.2.

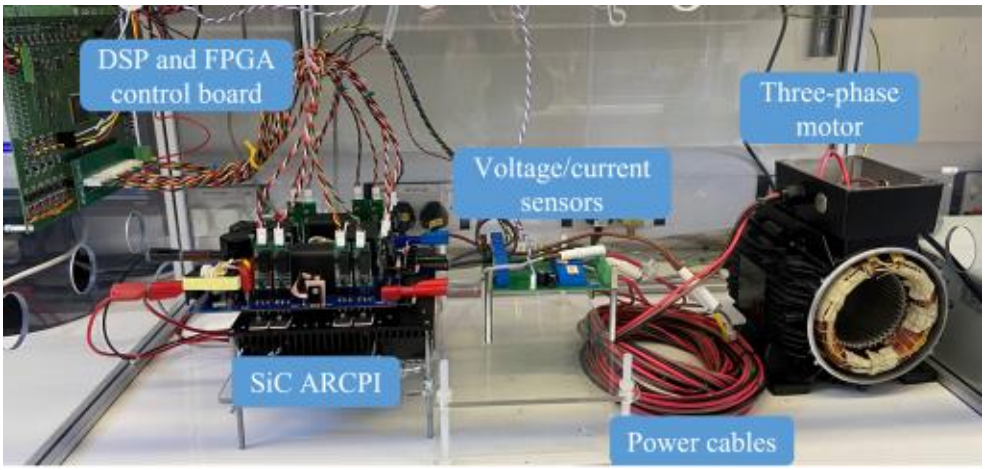


Figure 6.14 Experimental setup.

The resonant parameters of the ARCPI are shown in Table 6.1, which is designed according to the process present in Section 6.4.3. The SiC MOSFETs (C2M0040120D from Wolfspeed) are driven using gate drivers with -5/+15V driving voltage, 25 Ω gate resistance. The gate drivers are implemented with an isolated DC/DC converter (MGJ2D051500SC, input: 5V output: -5/+15V), an optocoupler (ACPL-W484), and a driver (IXDN609SI). Note that the gate driver is an existing driver in the laboratory that the author used for the experimental work. The driving voltage can also be -5/+20V to achieve better performance for the MOSFETs (C2M0040120D). The main parameters of the cable are given in Table 6.3.

The experimental results obtained under the ARCPI are compared with the hard-switching inverter, and the hard-switching inverter + RLC dv/dt filter. The hard-switching inverter

can be easily realized by disabling the auxiliary branches of the ARCPI. Figure 6.15 shows the circuit schematic of the hard-switching inverter + RLC dv/dt filter, where the filter is installed at the inverter output node. The filter parameters (L_f, C_f, and R_f) are shown in Table 6.4, which are designed using the method presented in [133].

Table 6.2 The motor parameters.

	Symbol	Value	Symbol	Value
Motor	Motor type	Induction motor	Pole number	4
	Phase number	3	Power rating	2.2kW

Table 6.3 The cable parameters.

	Symbol	Value
Cable	length (l_c)	12 m
	Cable gauge	12 AWG
	Cable per meter inductance (L_c)	0.26 μH
	Cable per meter capacitance (C_c)	104.7 pF

Table 6.4 The *dv/dt* filter parameters.

	Symbol	Value
dv/dt filter	Filter inductance (L_f)	2.7 μH
	Filter capacitance (C_f)	22 nF
	Filter damping resistance (R_f)	25 Ω

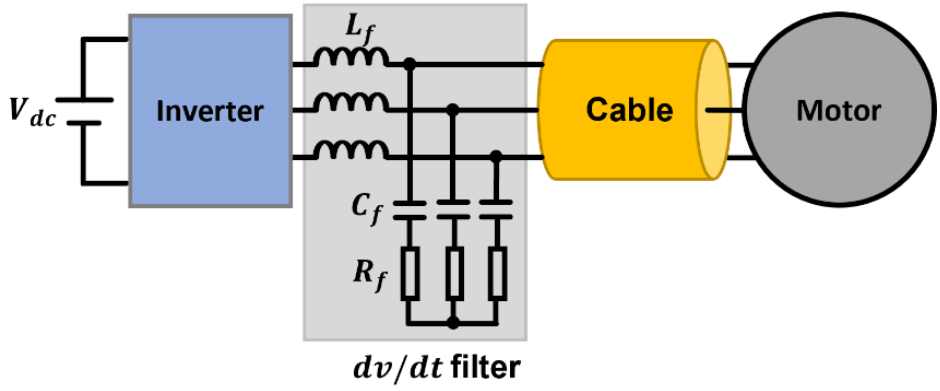


Figure 6.15 The RLC filter for SiC-based adjustable speed drives.

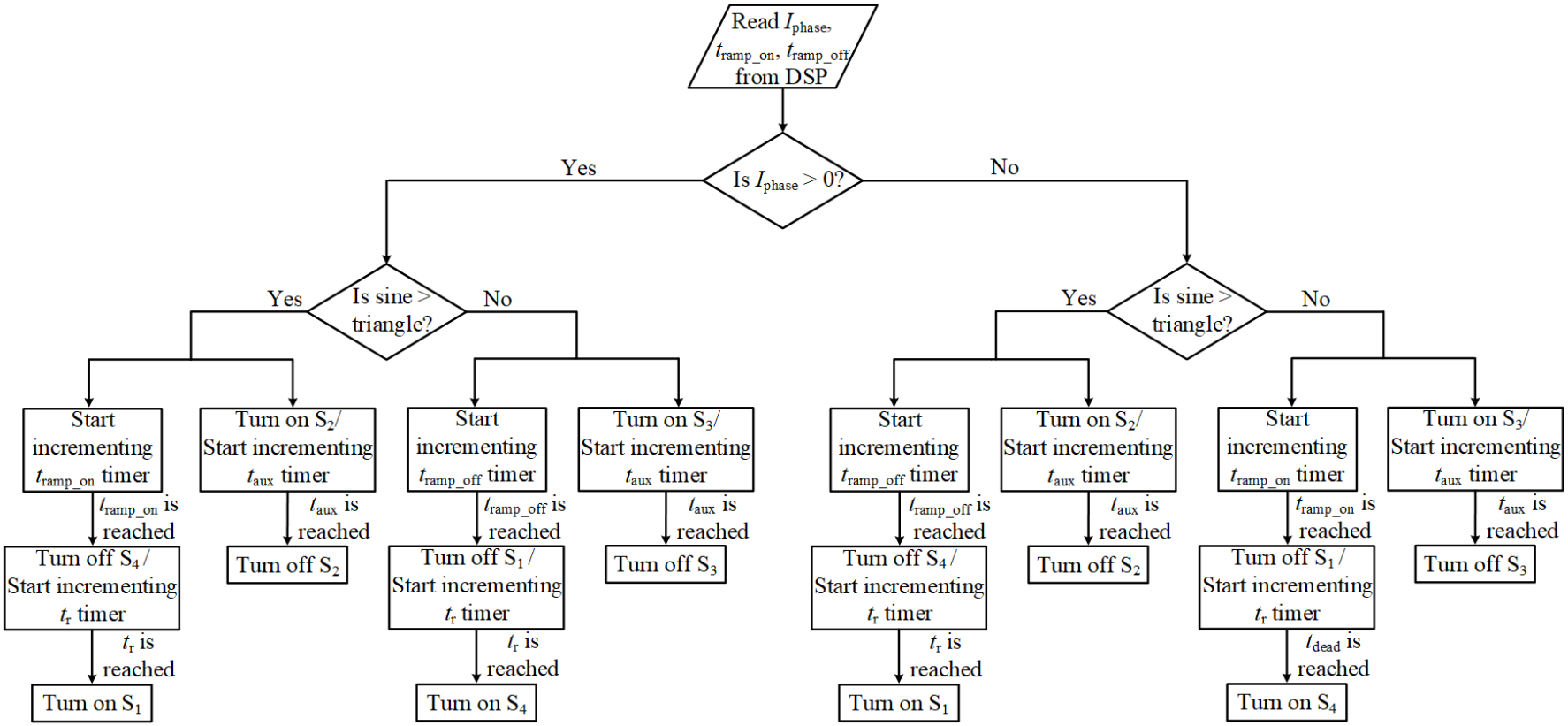


Figure 6.16 The flow chart of the variable-timing control method for the ARCPI.

The inverter is controlled by a control board which consists of a DSP (TI TMS320F28335), an FPGA (XILINX XC3S400), and two ADCs (AD7667), as shown in Figure 6.14. The ARCPI is modulated using the variable-timing control method, as shown in Figure 6.16. It should be noted that the ramp up/down times and the auxiliary time are calculated in the DSP, where the ramp times is calculated using (6.9) based on the instantaneous measured load current. The auxiliary time is the total commutation time. Both the ARCPI and hard-switching inverter are modulated with 50 Hz and 20 kHz as the fundament and switching frequencies, respectively. To protect the stator and limit the maximum load current, the dc-link voltage is set as 300 V.

6.5.2 Experimental Results

Figure 6.17 compares the experimental results in the fundamental cycles when the motor is supplied by the hard-switching inverter, the hard-switching inverter + dv/dt filter and the ARCPI, respectively. Note that I_a and I_b are the phase currents measured at the inverter output nodes *A* and *B*, V_s and V_m are the line voltages measured at the inverter side and motor terminals, respectively.

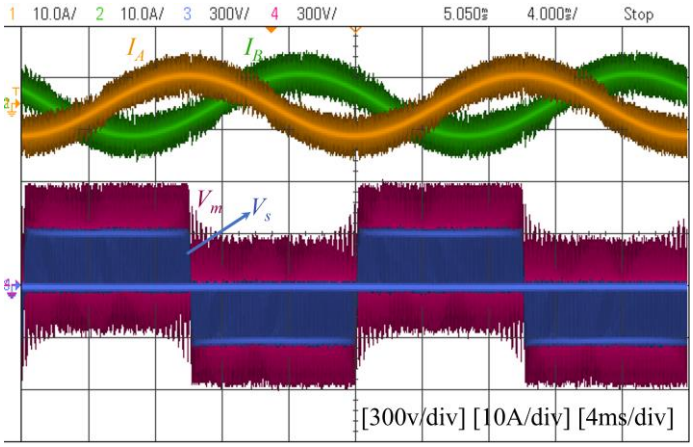
Referring to Figure 6.17 (a), there is a significant overvoltage at the motor terminals due to the RWP when the motor is supplied by the hard-switching inverter, where the maximum overvoltage is about 2.0 pu. In addition, there are high-frequency harmonics of the inverter output current. This is because the high dv/dt of the PWM voltage pulses charges and discharges the power cable parasitic capacitance during the switching transient, resulting in high spike currents.

With the adoption of the dv/dt filter, the motor terminal overvoltage can be limited within 1.35 pu, as shown in Figure 6.17 (b). Although the dv/dt filter can effectively attenuate the motor terminal overvoltage, it results in the highest output current at the inverter side among the three inverters. The reason is that besides the load current, a large spike current flows through the dv/dt filter during the switching transients. This can be proved in Figure 6.18, where it shows the inverter output current I_A measured at the inverter output node, the corresponding load current I_{load} measured at the filter output node, the inverter output voltage V_s and the filter output voltage V_f for one switching cycle. It should be noted that to clearly show the additional current caused by the dv/dt filter, the experimental result shown in Figure **6.18** is captured when the load current is closed to zero.

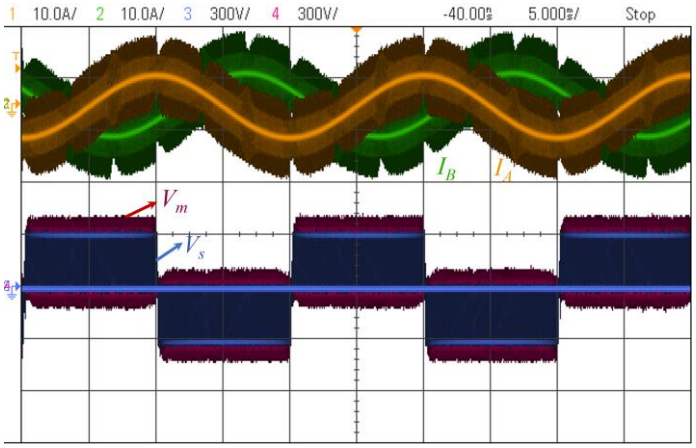
Referring to Figure 6.18, the inverter output current is much higher than the load current for both the turn-ON and turn-OFF transients. Since the dv/dt filter leads to higher inverter output current, the inverter power loss will be accordingly increased. Furthermore, the filter results in additional power loss, deteriorating the system's power efficiency. It is worth noting that the inverter output current of the hard-switching inverter + dv/dt filter can be reduced using a larger inductance. However, it would reduce the effective voltage applied to the motor because the voltage drops across the dv/dt filter are proportional to the filter inductance, i.e., a larger inductance leads to higher voltage drops. Considering the trade-off between the current flowing through the dv/dt filter and the resultant voltage drops across the filter, the inductance is selected as 2.7 μH.

In contrast, the motor terminal overvoltage can be entirely attenuated when the ARCPI is adopted, as shown in Figure 6.17 (c), where the rise and fall times are set as the optimum time $4t_p$ in the fundamental cycle. Compared with output currents of the hard-switching inverter in Figure 6.17 (a) and the output currents of the hard-switching inverter + dv/dt filter in Figure 6.17 (b), the output current of the ARCPI is the cleanest. This is because the ARCPI is a soft-switching inverter with slowed and smoothed output voltages, as analysed in the above section. It should be noted that both the dv/dt filter and the ARCPI can effectively mitigate the motor terminal overvoltage because the rise and fall times of the voltage feeding to the motor are prolonged. This will be analysed in detailed in the following section.

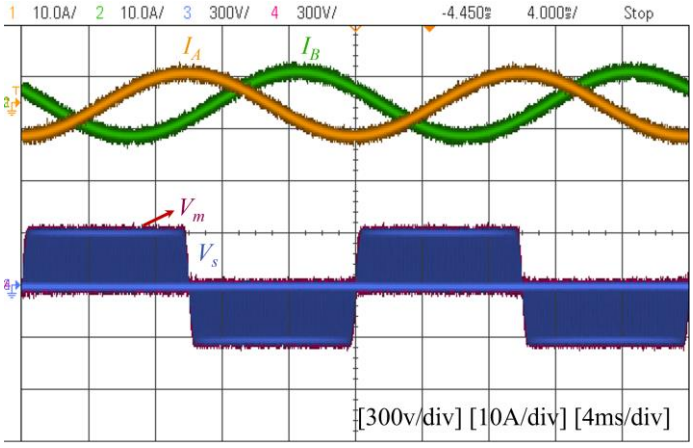
Figure 6.19-Figure 6.21 shows the experimental results for one switching cycle when the motor is supplied by the hard-switching inverter, the hard-switching inverter + dv/dt filter and the ARCPI, respectively. Referring to Figure 6.19 (a), the motor terminal voltage oscillates in a damped manner when the motor is supplied by the hard-switching inverter, where the maximum motor terminal voltage is about 1.95 pu for both the rising and falling edges. The motor terminal overvoltage is due to the RWP caused by the high dv/dt and the impedance mismatch in the motor drive system, as previously analysed. The extended view of this switching cycle showing how the motor terminal voltage oscillations during the rising and falling transitions are given in Figure 6.19 (b) and (c), respectively. Note that the time delay between the inverter output voltage V_s and the motor terminal voltage V_m is the wave propagation time from the inverter side to the motor terminals.



(a)



(b)



(c)

Figure 6.17 Experimental results of the phase currents and line voltage at the inverter sides and motor terminals for two fundamental cycles when the motor is supplied by (a) the hard-switching inverter and (b) the hard-switching inverter + *dv/dt* filter and (c) the ARCPI.

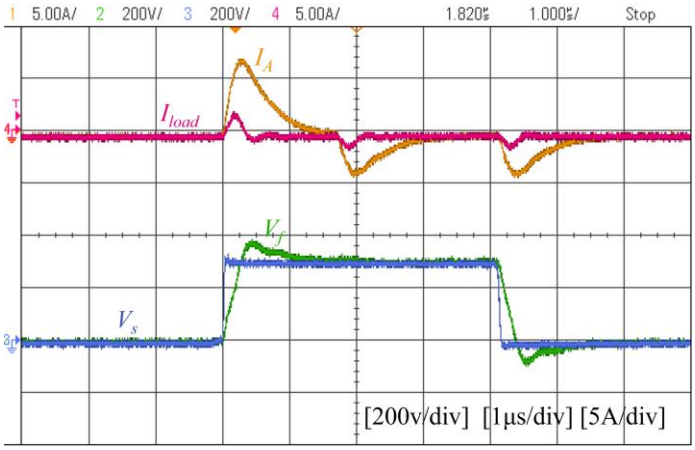
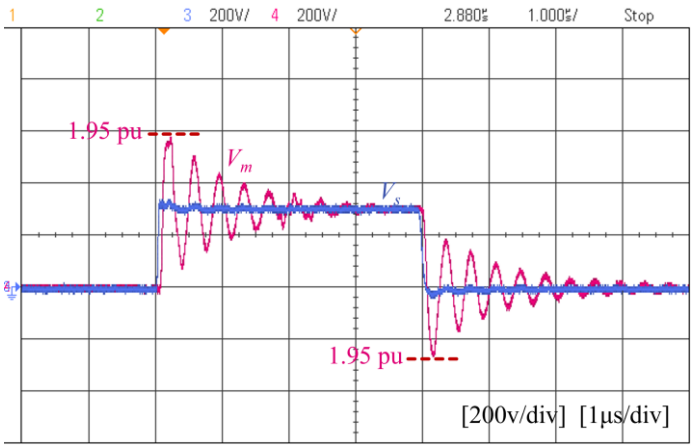
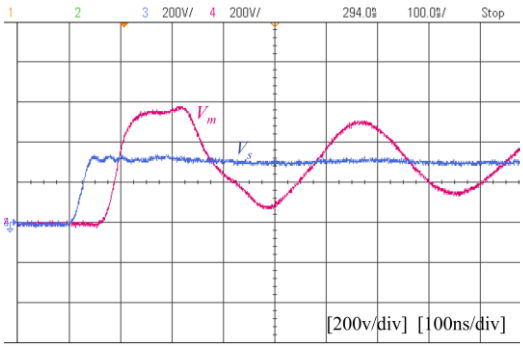


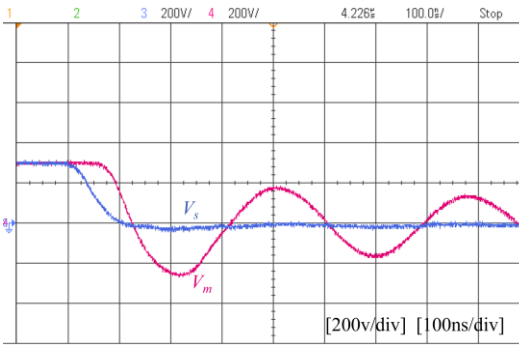
Figure 6.18 The load current I_{load}, the inverter output current I_A, the inverter output voltage V_s and the filter output voltage V_f during the switching transient for the hard-switching inverter + *dv/dt* filter.



(a) one switching cycle view



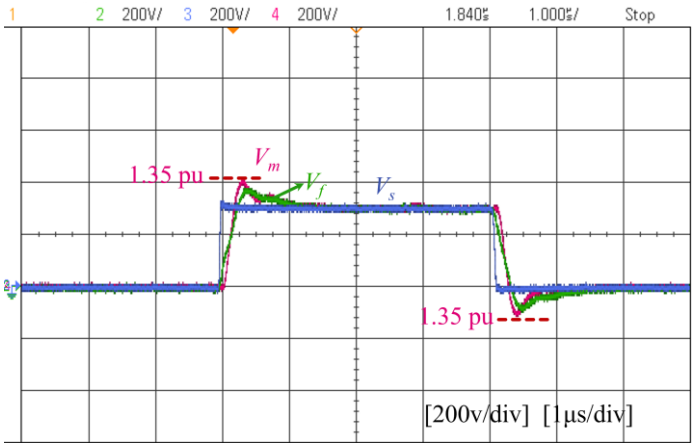
(b) extended view at rising transitions



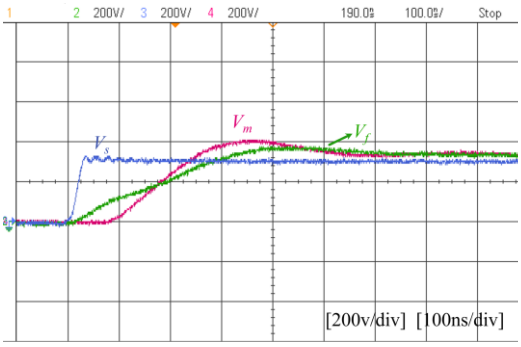
(c) extended view at the falling transitions.

Figure 6.19 Inverter and motor voltages when the motor is supplied by the hard-switching inverter.

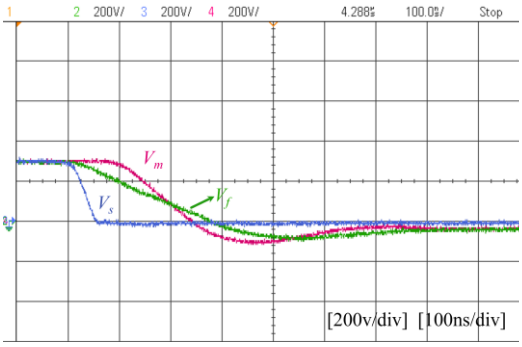
Figure 6.20 shows the experimental results for one switching cycle when the motor is supplied by the hard-switching inverter + dv/dt filter, where the voltages are measured at the inverter output node, the filter output node, and the motor terminals. Referring to Figure 6.20 (a), with the adoption of the dv/dt filter, the inverter output voltage V_s is slowed as V_f for both rising and falling edges, where the rise and fall times are about 400ns. However, the filter output voltage is a bit higher than that of the inverter, which is about 1.32 pu. The motor terminal overvoltage is limited to 1.35 pu due to the prolonged rising and falling edges of V_f. This is highlighted in Figure 6.19 (b) and (c) showing the extended view during the rising and falling edges, respectively.



(a) one switching cycle view



(b) rising transitions

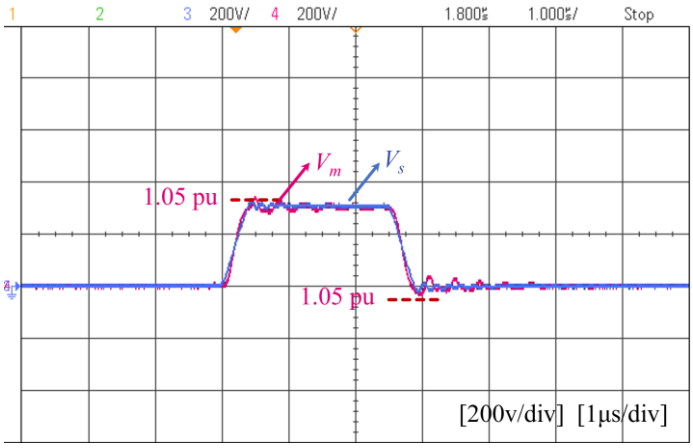


(c) falling transitions

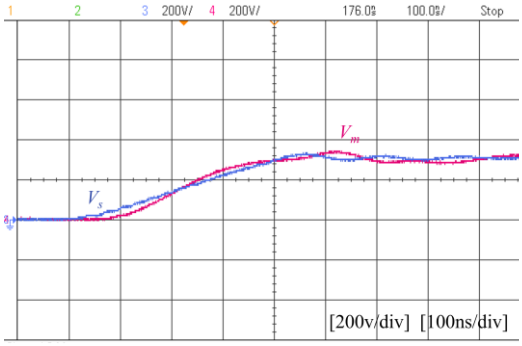
Figure 6.20 Inverter output voltage V_s, the filter output voltage V_f and motor voltage V_m when the motor is supplied by the hard-switching inverter + *dv/dt* fitler.

With the adoption of the ARCPI, Figure 6.21 shows the ARCPI and motor terminal voltages for one switching cycle. Since the ARCPI is operated under the variable timing control, the rising and falling time of the output voltage of the inverter remains fixed as $4t_p$

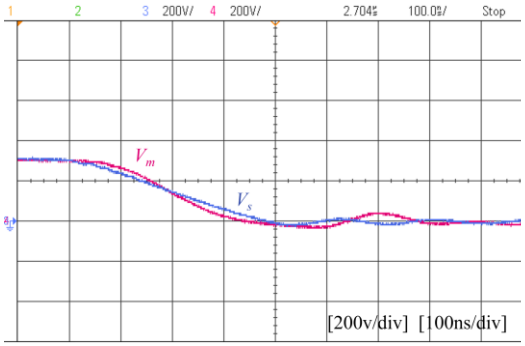
regardless of the load current. Referring to Figure 6.21 (a), the motor terminal overvoltage oscillations are completely attenuated due to the prolonged rise/fall times of the output voltage. The enlarged view during the rising and falling edges for this switching cycle is shown in Figure 6.21 (b) and (c), respectively. It worth noting that the inverter voltage V_s equals V_m at the midway.



(a) one switching cycle view



(b) extended view at rising transitions



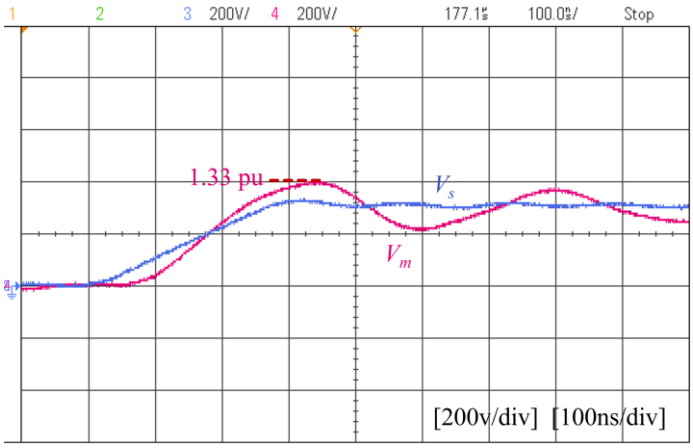
(c) extended view at the falling transitions.

Figure 6.21 Inverter and motor voltages when the motor is supplied by the ARCPI.

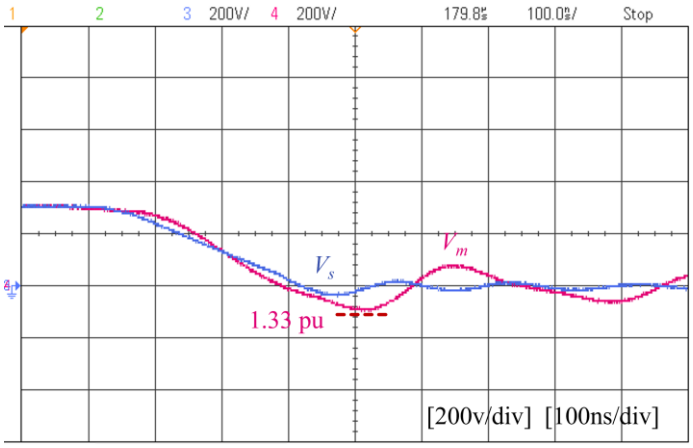
Comparing Figure 6.20 with Figure 6.21, while the rise and fall times for both inverters are set as the optimum value, i.e., $4t_p$, the motor terminal overvoltage is partially mitigated when the motor is supplied by the hard-switching inverter + dv/dt filter. This is because the output voltage of the hard-switching inverter + dv/dt filter is slightly higher than that of the ARCPI, as shown in Figure 6.20.

Figure 6.22 shows the inverter and motor terminal voltages when the rise and fall times of the inverter output voltages are longer than the optimum time, where Figure 6.22 (a) and

(b) show the rising and falling edges of the output voltage of the ARCPI, respectively. As shown, the motor terminal overvoltage is partial mitigated for both rising and falling edges, where the maximum motor terminal voltage is about 1.33 pu. It is worth noting that the inverter voltage output voltage V_s equals the motor terminal voltage V_m after the midway.



(a) view at the rising edge



(b) view at the falling transitions

Figure 6.22 Inverter and motor voltages when the rise and fall times are faster than the optimum value.

Besides the motor overvoltage mitigation, the soft-switching voltage slew rate profiling approach inherits the advantages of the ARCPI including EMI performance improvement and switching loss reduction, as evidenced in Figure 6.23-Figure 6.26.

Figure **6.23** shows the rising edge of the output voltage V_{pole} of the ARCPI under different dc-link voltage, where the dc-link voltage is set as 100V, 200V and 300V, respectively. As

shown, while the dc-link varies, the rising time of the output voltage V_{pole} of the ARCPI keeps fixed.

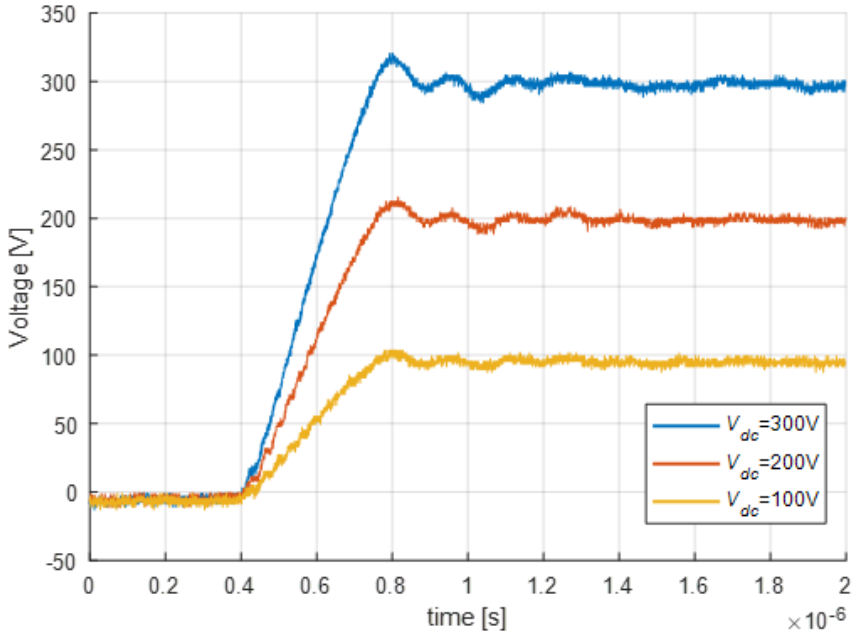


Figure 6.23 The rising edge of the output voltage of the ARCPI at different dc-link voltage.

Figure 6.24 compares the frequency spectrum of the motor terminal voltage when the motor is supplied by the hard-switching inverter and the ARCPI. As can be noticed, while at the low frequency region, both inverter shows similar frequency spectrum, the ARCPI exhibits less frequency harmonics content above 1MHz than the hard-switching inverter. This is because the output voltages of the ARCPI have smoother and longer edges, as shown in Figure 6.21, than that of the hard-switching inverter, as shown in Figure 6.19. Specifically, compared with the hard-switching inverter, the ARCPI can achieve about 20 dB frequency harmonic attenuation at 1MHz. In addition, the high frequency voltage oscillations due to the RWP in the motor drive system, further deteriorates the EMI performance of the hard-switching inverter. For example, the protuberances of the frequency spectrum at 2.7 MHz are caused by the high frequency overvoltage oscillations, as shown in Figure 6.19, while the ARCPI can successfully attenuate it, as shown in Figure 6.24.

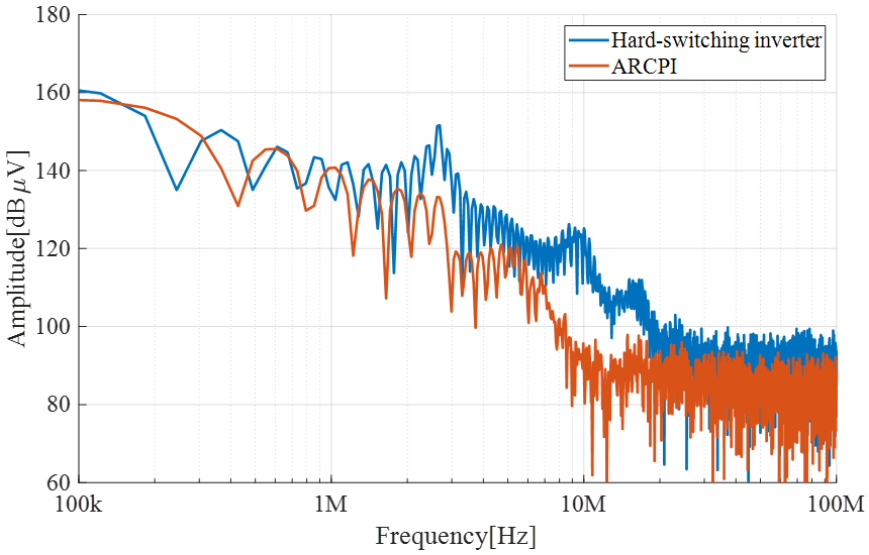
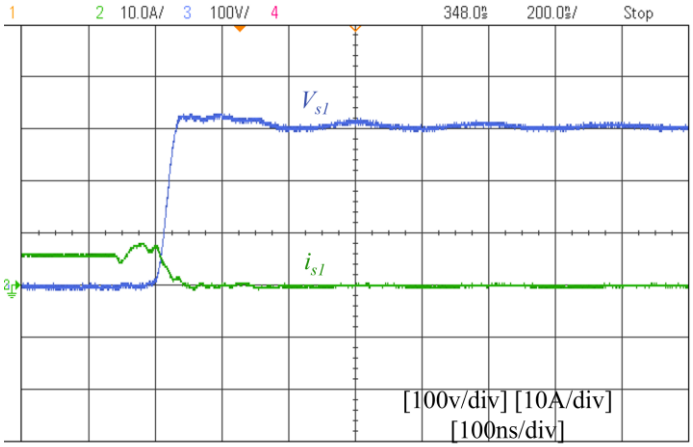


Figure 6.24 Frequency spectrum of the motor voltage using the hard-switching inverter and the ARCPI.

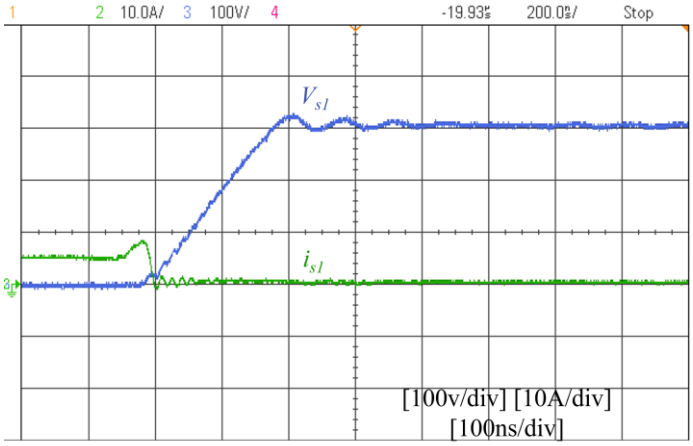
Figure 6.25 shows the switching device's voltage and current during the switching transient, where Figure 6.25 (a) and (b) show the experimental result for the hard-switching inverter and the ARCPI, respectively.

Referring to Figure 6.25 (a), the switching device's voltage and current of the hard-switching inverter are coupled, yielding substantial switching losses during the switching transients. However, the device's voltage and current of the ARCPI are decoupled during the switching transients which can reduce the switching loss, as shown in Figure 6.25 (b). Therefore, the ARCPI would have a higher system efficiency than the hard-switching inverter theoretically.

Figure 6.26 compares the efficiency of the ARCPI and the hard-switching inverter + dv/dt filter. Note that the efficiency calculation has been performed while connecting an RL load to the inverter through long cables, where the load resistance $R_{phase} = 11\Omega$ and the load inductance $L_{phase} = 5mH$. The motor is replaced with the RL load because the motor stator consumes very small active power which cannot reflect the efficiency at different power level.



(a)



(b)

Figure 6.25 The device current and voltage during the turn-off switching transients of (a) the hard-switching converter and (b) the ARCPI.

Owing to the output current and voltage have a very high dv/dt and high frequency oscillations, the conventional method using a power analyser to measure the power efficiency is inaccurate. Therefore, high bandwidth voltage and current probes are used to measure the accurate current and voltage waveforms and to calculate the power efficiency. Since the efficiency are measured under same conditions, the experimental error caused by the measurement equipment should be the same for the ARCPI and the hard-switching inverter + RLC dv/dt filter. Note that other measurement such as the calorimeter can be used to improve the improve the measurement accuracy.

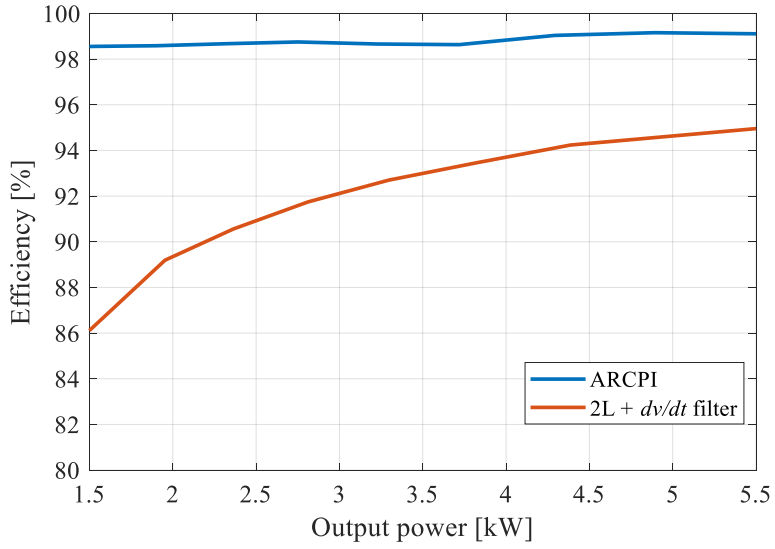


Figure 6.26 The efficiency at different load conditions.

The differential voltage probes (TA042, 100MHz, 1kV) from Pico Technology and the current probe (N2783A, 100MHz, 30A) from Agilent Technologies are utilised for the voltage and current measurement. The results are recoded using the bandwidth and high sampling rate oscilloscope HD08000 (1GHz, 2.5-GSa/s) from Teledyne LeCroy. To ensure the measurement accuracy, all the probes are calibrated, i.e., all the channels are de-skewed and the offset is compensated before the measurement. The efficiency η is calculated by measuring the three-phase load voltages (v_a, v_b, and v_c) and currents (i_a, i_b, and i_c), and the dc link voltage V_{dc} and current I_{dc} for one fundamental cycle (T). The efficiency can then be expressed as:

$$\eta = \frac{\int_0^T v_a i_a + \int_0^T v_b i_b + \int_0^T v_c i_c}{V_{dc} I_{dc} T} \tag{6.19}$$

Referring to Figure 6.26, the ARCPI has higher efficiency than the hard-switching inverter + dv/dt filter, where the maximum efficiency of the ARCPI is about 99%, while the maximum efficiency of the hard-switching inverter + dv/dt is about 95%. The ARCPI exhibits higher efficiency at different power range because the ARCPI can mitigate the switching loss of the main switching devices, as evidenced in Figure 6.25. For the hard-switching inverter + dv/dt filter, the filter causes higher current for the inverter, as shown in Figure 6.18, which increases the power loss for the hard-switching inverter. Moreover, the filter itself contributes with additional power loss to the system.

6.6 Conclusion

This chapter has proposed a soft-switching voltage slew rate profiling approach to mitigate the motor terminal overvoltage oscillations due to the RWP in SiC-based long cable-fed motor drive system. A general idea of overvoltage oscillations mitigation mechanism in the motor drive system has been discussed in both time domain and frequency domain. The effectiveness of the proposed soft-switching voltage slew rate profiling approach has been experimentally verified with the SiC ARCPI long cabled-fed motor drive system. The conclusions of this chapter are the following:

- Besides the characteristic impedance mismatch between the cable and motor, the rise and fall times of the PWM voltage pulses feeding to the motor drive system affect the motor terminal overvoltage oscillations. Generally, for a given cable length the maximum motor terminal overvoltage decreases with larger rise and fall times.
- The motor terminal overvoltage oscillations can be entirely attenuated when the rise and fall times of the PWM voltage pulses are set as integer multiples of the cable-motor's anti-resonance period, i.e., $4nt_p$. Note that $4t_p$ is denoted as the optimum rise and fall times for the motor terminal overvoltage mitigation.
- The philosophy used to tackle the overvoltage issue is eliminating the excitation source for the overvoltage oscillations by shaping the voltages feeding to the drive system, i.e., the component of the excitation source at the anti-resonance frequency of the cable-motor system is zero. Since there is no excitation source to cause the overvoltage oscillations, the motor terminal overvoltage oscillations can be entirely mitigated.
- In addition to the motor overvoltage mitigation, the proposed soft-switching voltage profiling approach inherits the characteristics of the soft-switching inverter such as lower EMI and higher power efficiency, compared with the conventional hard-switching inverter counterpart.

Chapter 7
Conclusion and Potential Future Work

7.1 Thesis Summary

This PhD thesis has systematically investigated the RWP in inverter-fed motors with fast-switching WBG converters and proposed the active waveform shaping techniques to mitigate the motor terminal overvoltage without compromising the benefits of WBG devices. This thesis consists of both theoretical analysis and detailed experimental verification. The four research objectives set out in Chapter 1 have been met.

Chapter 2 reviewed existing research literature relating to the PhD work. The limitations of existing literature and research opportunities have been identified.

Chapter 3 and Chapter 4 thoroughly investigated the RWP in WBG based cable-fed motor drive system. Chapter 3 has investigated the RWP in both time domain and frequency domain. The relationship between the time domain and frequency domain of the RWP has been revealed, which is the foundation for developing active waveform shaping techniques including the Q3L PWM and the voltage slew rate (dv/dt) profiling to mitigate motor terminal overvoltage oscillations. Chapter 4 has investigated the motor terminal overvoltage oscillations in a three-phase motor drive system, considering the impacts of parasitic capacitance of the switching devices and load current during the switching transitions. Also, the analysis has been experimentally verified in this chapter.

Chapter 5 developed the Q3L PWM scheme for motor terminal overvoltage mitigation. The essence of the overvoltage mitigation mechanism of the Q3L PWM scheme has been investigated in both time domain and frequency domain for the first time. The impact of parasitic capacitance of switching device in SiC T-type inverter on the motor terminal overvoltage mitigation has been analysed and experimentally verified. Furthermore, the Q3L PWM has been extended to the module-parallel inverter which can mitigate the motor terminal overvoltage as well as extend the switching devices current capacity. In addition,

the SiC T-type inverter and module-parallel inverter has been built to experimentally implement the Q3L PWM scheme.

Chapter 6 has proposed the soft-switching voltage slew rate (dv/dt) profiling to mitigate the motor terminal overvoltage. The essence of overvoltage mitigation mechanism of the voltage slew rate profiling have been investigated in both time domain and frequency domain for the first time. The ARCPI has been built to experimentally verify the effectiveness of the proposed approach.

7.2 Conclusions

The key conclusions associated with the research objectives are summarised as:

Research Objective 1: Gain deep understanding of the RWP and crystallize the underlying cause of motor terminal overvoltage oscillations in cable-fed motors using fast-switching SiC inverters, providing the foundation for developing overvoltage mitigation techniques through active waveform shaping.

- The motor overvoltage oscillations are due to the RWP in the long cable-fed motor drive system, caused by the high steep voltage (high dv/dt) PWM pulses and the impedance mismatch in the motor drive system. Three typical motor overvoltages can be observed, i.e., the CM overvoltage between each phase and ground at the motor terminals, the DM overvoltage between phases at the motor terminals, and the CM overvoltage between the netrual point and ground at the motor neutral point.
- The overvoltage oscillation frequency can be obtained by the wave propagation time t_p in the cable or the anti-resonance frequency of the motor drive system. In fact, the motor overvoltage oscillations are due to the resonance in the motor drive system caused by an excitation source.
- The motor overvoltage oscillations are more common and severe in SiC-based cable-fed motor drive system due to the fast-switching speed. With switching frequency and modulation index increasing, the motor terminal overvoltage would exceed two times the inverter voltage.

Research Objective 2: Investigate the impact of parasitic of switching devices on motor terminal overvoltage in cable-fed motors using SiC inverters.

- The conventional method using the DPT to investigate the RWP is not precise enough to reveal the actual case. It may overestimate or underestimate the motor terminal overvoltage oscillations. The motor terminal overvoltage shows non-uniform distribution due to the rise and fall times of the output voltage of SiC-based inverters varies in different current region.
- The switching cycles, where the rise and fall times of the inverter output voltage are affected by the load current and parasitic capacitance of the switching devices. When the phase currents have the same polarity, the motor terminal overvoltage is only affected by the adopted gate resistance and the switching devices' characteristics. Whereas, when phase currents have different polarities, the motor terminal overvoltage is affected either by the gate resistance and the switching devices' characteristic or the load current value and device parasitic capacitance.

Research Objective 3: Address the motor terminal overvoltage oscillations due to the RWP in motor drive system at source by using the active waveform shaping technique, i.e., quasi-three-level (Q3L) PWM scheme.

- The motor terminal overvoltage oscillations can be significantly attenuated when the rise and fall times of the PWM voltage pulses are shaped as Q3L PWM with the dwell time $t_{dwell} = 2t_p$.
- The essence of the overvoltage mitigation mechanism of the Q3L PWM scheme is eliminating the excitation source for the overvoltage oscillations by actively shaping the voltages feeding to the drive system, i.e., the component of the excitation source at the anti-resonance frequency of the cable-motor system is zero. Since there is no excitation source to cause the overvoltage oscillations, the motor terminal overvoltage oscillations can be significantly mitigated.
- The parasitic elements of the switching devices and load current may adversely affect the ability of the Q3L T-type converter to mitigate the motor terminal overvoltage oscillations in certain cases, due to the variation in the switching rise and fall times.
- The proposed Q3L module-parallel inverter can generate the Q3L PWM voltage for the motor terminal overvoltage oscillations mitigation as well as elevate the current capacity of switching devices.

Research Objective 4: Address the motor terminal overvoltage oscillations at source using the active waveform shaping technique, i.e., soft-switching voltage slew rate (dv/dt) profiling without compromising the benefits of SiC devices.

- Besides the characteristic impedance mismatch between the cable and motor, the rise and fall times of the PWM voltage pulses feeding to the motor drive system affect the motor terminal overvoltage oscillations. Generally, for a given cable length the maximum motor terminal overvoltage decreases with the rise and fall times of the PWM voltage pulses.
- The motor terminal overvoltage oscillations can be entirely attenuated when the rise and fall times of the PWM voltage pulses are set as integer multiples of the cable-motor's anti-resonance period, i.e., $4nt_p$. Note that $4t_p$ is denoted as the optimum rise and fall times for the motor terminal overvoltage mitigation.
- The philosophy used to tackle the overvoltage issue is eliminating the excitation source for the overvoltage oscillations by shaping the voltages feeding to the drive system, i.e., the component of the excitation source at the anti-resonance frequency of the cable-motor system is zero. Since there is no excitation source to cause the overvoltage oscillations, the motor terminal overvoltage oscillations can be entirely mitigated.
- In addition to the motor overvoltage mitigation, the proposed soft-switching voltage profiling approach inherits the characterises of the soft-switching inverter such as lower EMI and higher power efficiency, compared with the conventional hard-switching inverter counterpart.

7.3 Future Work

While this PhD work has successfully mitigated the motor terminal overvoltage due to the RWP in SiC based cable-fed motor drive system, there are several other interesting topics and potential future work need to be carried out to fully use WBG devices in adjustable speed drive systems.

7.3.1 Evaluation of Waveform Shaping Techniques on Motor Stator Winding Voltage Distribution

It is well established in literature that in inverter-fed motor drive systems, the fast-switched PWM voltage pulses result in non-uniform voltage distribution within motor stator windings. This overstress is further exacerbated when long power cables are used to connect the inverter to the motor. This PhD work has successfully attenuated the motor

terminal overvoltage using active waveform shaping techniques. The voltage stress on the stator winding can be alleviated. However, how these overvoltage mitigation techniques affect the voltage distribution within the motor stator windings is still unknow. The systematically evaluation of the uneven voltage distribution within stator windings using different active waveform shaping techniques should be conducted.

7.3.2 Mitigation of Motor Neutral Point Overvoltage Oscillations

In addition to the motor terminal (CM and DM) overvoltage oscillations, the motor neutral point also experiences overvoltage oscillations. The motor neutral point overvoltage oscillations arise from the propagation of the voltage pulses through the motor winding itself which emulates the same effect of long cables. Since the motor neutral point is normally floating, the inverter CM voltage pulses travelling through the motor winding encounter an infinite impedance (open circuit) between the neutral point and ground. The mismatch between the motor CM impedance and the neutral-to-ground infinite impedance causes the inverter CM voltage pulses to experience voltage reflection at the motor stator neutral point. This results in overvoltage that externally manifests at the motor neutral-to-ground voltage with peak voltage stress at the coils close to the neutral point. This overvoltage phenomenon is characterized by an oscillatory response at the motor winding antiresonance frequency which depends on the motor geometry and stator winding connection. The neutral point overvoltage oscillations also significantly affect the lifetime of the motor drive system. However, this issue has been scarcely addressed in literature with no adequate investigation of appropriate mitigation strategies. To improve the reliability and lifetime of the motor drive system, the motor neutral point oscillation should be mitigated.

7.3.3 Evaluation of Partial Discharge Activity

The overvoltage stress on the motor stator winding reduces the lifetime of the motor because when the voltage stress across the motor stator windings exceeds the PD Inception Voltage (PDIV), it would increase the possibility to incept PDs. Therefore, the overvoltage stress across motor winding turns accelerates the winding insulation aging through inception of PDs that progressively yield to the degradation and local heating of organic coatings of random-wound motor coils. However, to the best of the auther’s knowledge, how the proposed active waveform shaping techniques affect the PD activity of the motor is still unknown. Therefore, further work can be conducted to systematically evaluate the PD activities with/without motor overvoltage mitigation techniques.

References

[1] J. W. Kolar *et al.*, 'Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"', in *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2020, p. 27.7.1-27.7.4. doi: 10.1109/IEDM13553.2020.9372022.

[2] I. Husain *et al.*, 'Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles', *Proc. IEEE*, pp. 1–21, 2021, doi: 10.1109/JPROC.2020.3046112.

[3] C. Liu, K. T. Chau, C. H. T. Lee, and Z. Song, 'A Critical Review of Advanced Electric Machines and Control Strategies for Electric Vehicles', *Proc. IEEE*, pp. 1–25, 2020, doi: 10.1109/JPROC.2020.3041417.

[4] J. He, T. Zhao, X. Jing, and N. A. O. Demerdash, 'Application of wide bandgap devices in renewable energy systems — Benefits and challenges', in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, Milwaukee, WI, USA, Oct. 2014, pp. 749–754. doi: 10.1109/ICRERA.2014.7016485.

[5] C. Chen, M. Su, Z. Xu, and X. Lu, 'SiC-based automotive traction drives, opportunities and challenges', in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, Oct. 2017, pp. 25–30. doi: 10.1109/WiPDA.2017.8170497.

[6] A. Rujas, V. M. Lopez, A. Garcia-Bediaga, A. Berasategi, and T. Nieva, 'Influence of SiC technology in a railway traction DC-DC converter design evolution', in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, Oct. 2017, pp. 931–938. doi: 10.1109/ECCE.2017.8095885.

[7] W. Perdikakis, M. J. Scott, K. J. Yost, C. Kitzmiller, B. Hall, and K. A. Sheets, 'Comparison of Si and SiC EMI and Efficiency in a Two-Level Aerospace Motor Drive Application', *IEEE Trans. Transp. Electrification*, vol. 6, no. 4, pp. 1401–1411, Dec. 2020, doi: 10.1109/TTE.2020.3010499.

[8] J. F. Hansen and F. Wendt, 'History and State of the Art in Commercial Electric Ship Propulsion, Integrated Power Systems, and Future Trends', *Proc. IEEE*, vol. 103, no. 12, pp. 2229–2242, Dec. 2015, doi: 10.1109/JPROC.2015.2458990.

[9] A. K. Morya *et al.*, 'Wide Bandgap Devices in AC Electric Drives Opportunities and Challenges', *IEEE Trans. Transp. Electrification*, vol. 5, no. 1, pp. 3–20, Mar. 2019, doi: 10.1109/TTE.2019.2892807.

[10] P. A. Owusu and S. Asumadu-Sarkodie, 'A review of renewable energy sources, sustainability issues and climate change mitigation', *Cogent Eng.*, vol. 3, no. 1, p. 1167990, Dec. 2016, doi: 10.1080/23311916.2016.1167990.

[11] T. Ackermann, 'Wind energy technology and current status: a review', *Renew. Sustain. Energy Rev.*, vol. 4, no. 4, pp. 315–374, Dec. 2000, doi: 10.1016/S1364-0321(00)00004-6.

[12] N. Kannan and D. Vakeesan, 'Solar energy for future world: - A review', *Renew. Sustain. Energy Rev.*, vol. 62, pp. 1092–1105, Sep. 2016, doi: 10.1016/j.rser.2016.05.022.

[13] A. Roberts, B. Thomas, P. Sewell, Z. Khan, S. Balmain, and J. Gillman, 'Current tidal power technologies and their suitability for applications in coastal and marine areas', *J. Ocean Eng. Mar. Energy*, vol. 2, no. 2, pp. 227–245, May 2016, doi: 10.1007/s40722-016-0044-8.

[14] X. Yuan, I. Laird, and S. Walder, 'Opportunities, Challenges, and Potential Solutions in the Application of Fast-Switching SiC Power Devices and Converters', *IEEE Trans.*

Power Electron., vol. 36, no. 4, pp. 3925–3945, Apr. 2021, doi: 10.1109/TPEL.2020.3024862.

[15] H. P. Nguyen *et al.*, 'The electric propulsion system as a green solution for management strategy of CO_2 emission in ocean shipping: A comprehensive review', *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 11, Nov. 2021, doi: 10.1002/2050-7038.12580.

[16] O. Farrok, K. Ahmed, A. D. Tahlil, M. M. Farah, M. R. Kiran, and Md. R. Islam, 'Electrical Power Generation from the Oceanic Wave for Sustainable Advancement in Renewable Energy Technologies', *Sustainability*, vol. 12, no. 6, p. 2178, Mar. 2020, doi: 10.3390/su12062178.

[17] M. Bagheri, N. Shirzadi, E. Bazdar, and C. A. Kennedy, 'Optimal planning of hybrid renewable energy infrastructure for urban sustainability: Green Vancouver', *Renew. Sustain. Energy Rev.*, vol. 95, pp. 254–264, Nov. 2018, doi: 10.1016/j.rser.2018.07.037.

[18] B. K. Bose, 'Evaluation of modern power semiconductor devices and future trends of converters', *IEEE Trans. Ind. Appl.*, vol. 28, no. 2, pp. 403–413, Apr. 1992, doi: 10.1109/28.126749.

[19] E. Hoene, G. Deboy, C. R. Sullivan, and G. Hurley, 'Outlook on Developments in Power Devices and Integration: Recent Investigations and Future Requirements', *IEEE Power Electron. Mag.*, vol. 5, no. 1, pp. 28–36, Mar. 2018, doi: 10.1109/MPEL.2017.2782398.

[20] B. Wu and M. Narimani, 'High-Power Converters and AC Drives', p. 25.

[21] A. Bolotnikov *et al.*, '3.3kV SiC MOSFETs designed for low on-resistance and fast switching', in *2012 24th International Symposium on Power Semiconductor Devices and ICs*, Bruges, Belgium, Jun. 2012, pp. 389–392. doi: 10.1109/ISPSD.2012.6229103.

[22] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, 'Understanding switching losses in SiC MOSFET: Toward lossless switching', in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, USA, Nov. 2015, pp. 257–262. doi: 10.1109/WiPDA.2015.7369295.

[23] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, 'Analysis of Shaped Pulse Transitions in Power Electronic Switching Waveforms for Reduced EMI Generation', *IEEE Trans. Ind. Appl.*, vol. 47, no. 5, pp. 2154–2165, Sep. 2011, doi: 10.1109/TIA.2011.2161971.

[24] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, 'SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors', *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872–2882, Jul. 2011, doi: 10.1109/TIE.2010.2072896.

[25] Z. J. Shen and I. Omura, 'Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles', *Proc. IEEE*, vol. 95, no. 4, pp. 778–789, Apr. 2007, doi: 10.1109/JPROC.2006.890118.

[26] W. Zhou and X. Yuan, 'Experimental Evaluation of SiC Mosfets in Comparison to Si IGBTs in a Soft-Switching Converter', *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5108–5118, Sep. 2020, doi: 10.1109/TIA.2020.2999440.

[27] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, 'Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules', *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019, doi: 10.1109/TPEL.2018.2834345.

[28] C. Zhang, S. Srdic, S. Lukic, Y. Kang, E. Choi, and E. Tafti, 'A SiC-Based 100 kW High-Power-Density (34 kW/L) Electric Vehicle Traction Inverter', in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 3880–3885. doi: 10.1109/ECCE.2018.8558373.

[29] E. Abramushkina, A. Zhaksylyk, T. Geury, M. El Baghdadi, and O. Hegazy, 'A Thorough Review of Cooling Concepts and Thermal Management Techniques for Automotive WBG Inverters: Topology, Technology and Integration Level', *Energies*, vol. 14, no. 16, 2021, doi: 10.3390/en14164981.

[30] Y. Xu *et al.*, 'Impact of High Switching Speed and High Switching Frequency of Wide-Bandgap Motor Drives on Electric Machines', *IEEE Access*, vol. 9, pp. 82866–82880, 2021, doi: 10.1109/ACCESS.2021.3086680.

[31] M. J. Scott *et al.*, 'Reflected wave phenomenon in motor drive systems using wide bandgap devices', in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, Knoxville, TN, Oct. 2014, pp. 164–168. doi: 10.1109/WiPDA.2014.6964647.

[32] M. S. Diab, W. Zhou, and X. Yuan, 'Evaluation of Topologies and Active Control Methods for Overvoltage Mitigation in SiC-Based Motor Drives', in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, BC, Canada, Oct. 2021, pp. 4867–4873. doi: 10.1109/ECCE47101.2021.9595730.

[33] W. Zhou, M. Diab, X. Yuan, and C. Wei, 'Mitigation of Motor Overvoltage in SiC-Based Drives using Soft-Switching Voltage Slew-Rate (dv/dt) Profiling', *IEEE Trans. Power Electron.*, pp. 1–1, 2022, doi: 10.1109/TPEL.2022.3157395.

[34] G. Suresh, H. A. Toliyat, D. A. Rendusara, and P. N. Enjeti, 'Predicting the transient effects of PWM voltage waveform on the stator windings of random wound induction motors', *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 23–30, Jan. 1999, doi: 10.1109/63.737589.

[35] C. Petrarca, A. Maffucci, V. Tucci, and M. Vitelli, 'Analysis of the Voltage Distribution in a Motor Stator Winding Subjected to Steep-Fronted Surge Voltages by Means of a Multiconductor Lossy Transmission Line Model', *IEEE Trans. Energy Convers.*, vol. 19, no. 1, pp. 7–17, Mar. 2004, doi: 10.1109/TEC.2003.821834.

[36] A. Narang, B. K. Gupta, E. P. Dick, and D. K. Sharma, 'Measurement and Analysis of Surge Distribution in Motor Stator Windings', *IEEE Power Eng. Rev.*, vol. 9, no. 3, pp. 38–39, 1989, doi: 10.1109/MPER.1989.4310548.

[37] B. Taghia, B. Cougo, H. Piquet, D. Malec, A. Belinger, and J.-P. Carayon, 'Overvoltage at motor terminals in SiC-based PWM drives', *Math. Comput. Simul.*, vol. 158, pp. 264–280, Apr. 2019, doi: 10.1016/j.matcom.2018.09.009.

[38] M. Diab, W. Zhou, C. Emersic, X. Yuan, and I. Cotton, 'Impact of PWM Voltage Waveforms on Magnet Wire Insulation Partial Discharge in SiC-Based Motor Drives', *IEEE Access*, vol. 9, pp. 156599–156612, 2021, doi: 10.1109/ACCESS.2021.3129266.

[39] L. Lusuardi, A. Rumi, A. Cavallini, D. Barater, and S. Nuzzo, 'Partial Discharge Phenomena in Electrical Machines for the More Electrical Aircraft. Part II: Impact of Reduced Pressures and Wide Bandgap Devices', *IEEE Access*, vol. 9, pp. 27485–27495, 2021, doi: 10.1109/ACCESS.2021.3058089.

[40] V. Madonna, P. Giangrande, W. Zhao, H. Zhang, C. Gerada, and M. Galea, 'Electrical Machines for the More Electric Aircraft: Partial Discharges Investigation', *IEEE Trans. Ind. Appl.*, pp. 1–1, 2020, doi: 10.1109/TIA.2020.3046434.

[41] A. Rumi, L. Lusuardi, A. Cavallini, M. Pastura, D. Barater, and S. Nuzzo, 'Partial Discharges in Electrical Machines for the More Electrical Aircraft. Part III: Preventing Partial Discharges', *IEEE Access*, vol. 9, pp. 30113–30123, 2021, doi: 10.1109/ACCESS.2021.3058090.

[42] T. G. Arora, M. M. Renge, and M. V. Aware, 'Effects of switching frequency and motor speed on common mode voltage, common mode current and shaft voltage in PWM inverter-fed induction motors', in *2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, Siem Reap, Jun. 2017, pp. 583–588. doi: 10.1109/ICIEA.2017.8282911.

[43] I. Mitiche, G. Morison, A. Nesbitt, M. Hughes-Narborough, B. Stewart, and P. Boreham, 'Imaging Time Series for the Classification of EMI Discharge Sources', *Sensors*, vol. 18, no. 9, p. 3098, Sep. 2018, doi: 10.3390/s18093098.

[44] F. A. Kharanaq, A. Emadi, and B. Bilgin, 'Modeling of Conducted Emissions for EMI Analysis of Power Converters: State-of-the-Art Review', *IEEE Access*, vol. 8, pp. 189313–189325, 2020, doi: 10.1109/ACCESS.2020.3031693.

[45] F. (Fred) Wang and Z. Zhang, 'Overview of Silicon Carbide Technology: Device, Converter, System, and Application', *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, Dec. 2016, doi: 10.24295/CPSSTPEA.2016.00003.

[46] J. W. Milligan, S. Sheppard, W. Pribble, Y.-F. Wu, G. Muller, and J. W. Palmour, 'SiC and GaN Wide Bandgap Device Technology Overview', in *2007 IEEE Radar Conference*, Waltham, MA, USA, Apr. 2007, pp. 960–964. doi: 10.1109/RADAR.2007.374395.

[47] G. Iannaccone, C. Sbrana, I. Morelli, and S. Strangio, 'Power Electronics Based on Wide-Bandgap Semiconductors: Opportunities and Challenges', *IEEE Access*, vol. 9, pp. 139446–139456, 2021, doi: 10.1109/ACCESS.2021.3118897.

[48] W. Zhou, M. S. Diab, and X. Yuan, 'Impact of Parasitics and Load Current on the Switching Transient Time and Motor Terminal Overvoltage in SiC-Based Drives', in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 225–232. doi: 10.1109/ECCE44975.2020.9235417.

[49] D. Divan, P. Kandula, and M. J. Mauger, 'The Case for Soft Switching in Four-Quadrant Power Converters', p. 17, 2021.

[50] H. Wang and F. Blaabjerg, 'Power Electronics Reliability: State of the Art and Outlook', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 6, pp. 6476–6493, Dec. 2021, doi: 10.1109/JESTPE.2020.3037161.

[51] 'Power electronics-the enabling technology for renewable energy integration', *CSEE J. Power Energy Syst.*, 2021, doi: 10.17775/CSEEJPES.2021.02850.

[52] T. Horigome, K. Kurokawa, K. Kishi, and K. Ozu, 'A 100-kV thyristor converter for high-voltage dc transmission', *IEEE Trans. Electron Devices*, vol. 17, no. 9, pp. 809–815, Sep. 1970, doi: 10.1109/T-ED.1970.17079.

[53] H. W. van der Broeck, H.-C. Skudelny, and G. V. Stanke, 'Analysis and realization of a pulsewidth modulator based on voltage space vectors', *IEEE Trans. Ind. Appl.*, vol. 24, no. 1, pp. 142–150, Jan. 1988, doi: 10.1109/28.87265.

[54] D. M. Brod and D. W. Novotny, 'Current Control of VSI-PWM Inverters', *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 3, pp. 562–570, May 1985, doi: 10.1109/TIA.1985.349711.

[55] B. J. Baliga, M. S. Adler, R. P. Love, P. V. Gray, and N. D. Zommer, 'The insulated gate transistor: A new three-terminal MOS-controlled bipolar power device', *IEEE Trans. Electron Devices*, vol. 31, no. 6, pp. 821–828, Jun. 1984, doi: 10.1109/T-ED.1984.21614.

[56] T. L. Grant and T. H. Barton, 'Control Strategies for PWM Drives', *IEEE Trans. Ind. Appl.*, vol. IA-16, no. 2, pp. 211–216, Mar. 1980, doi: 10.1109/TIA.1980.4503773.

[57] A. Lidow, T. Herman, and H. W. Collins, 'Power MOSFET technology', in *1979 International Electron Devices Meeting*, 1979, pp. 79–83. doi: 10.1109/IEDM.1979.189545.

[58] L. Gyugyi and F. Cibulka, 'The High-Frequency Base Converter-A New Approach to Static High-Power Conversion', *IEEE Trans. Ind. Appl.*, vol. IA-15, no. 4, pp. 420–429, Jul. 1979, doi: 10.1109/TIA.1979.4503682.

[59] H. S. Patel and R. G. Hoft, 'Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I--Harmonic Elimination', *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973, doi: 10.1109/TIA.1973.349908.

[60] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, 'Modeling of Wide Bandgap Power Semiconductor Devices—Part I', *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015, doi: 10.1109/TED.2014.2368274.

[61] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, 'A Survey of Wide Bandgap Power Semiconductor Devices', *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[62] J. D. van Wyk and F. C. Lee, 'On a Future for Power Electronics', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 1, no. 2, pp. 59–72, Jun. 2013, doi: 10.1109/JESTPE.2013.2271499.

[63] S. Chowdhury, B. L. Swenson, M. H. Wong, and U. K. Mishra, 'Current status and scope of gallium nitride-based vertical transistors for high-power electronics application', *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074014, Jul. 2013, doi: 10.1088/0268-1242/28/7/074014.

[64] J. Millan, 'A review of WBG power semiconductor devices', in *CAS 2012 (International Semiconductor Conference)*, Sinaia, Romania, Oct. 2012, pp. 57–66. doi: 10.1109/SMICND.2012.6400696.

[65] P. Friedrichs, 'Silicon carbide power semiconductors-new opportunities for high efficiency', in *2008 3rd IEEE Conference on Industrial Electronics and Applications*, Singapore, Jun. 2008, pp. 1770–1774. doi: 10.1109/ICIEA.2008.4582824.

[66] K. Shenai, 'High-Density Power Conversion and Wide-Bandgap Semiconductor Power Electronics Switching Devices', *Proc. IEEE*, vol. 107, no. 12, pp. 2308–2326, Dec. 2019, doi: 10.1109/JPROC.2019.2948554.

[67] I. C. Kizilyalli, Y. A. Xu, E. Carlson, J. Manser, and D. W. Cunningham, 'Current and future directions in power electronic devices and circuits based on wide band-gap semiconductors', in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, Oct. 2017, pp. 417–417. doi: 10.1109/WiPDA.2017.8170583.

[68] W. Zhou, X. Yuan, and I. Laird, 'Elimination of Overshoot and Oscillation in the Auxiliary Branch of a SiC Auxiliary Resonant Commutated Pole Inverter (ARCPI)', in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, Busan, Korea (South), May 2019, pp. 383–389.

[69] W. Zhou, X. Yuan, and I. Laird, 'Performance Comparison of the Auxiliary Resonant Commutated Pole Inverter ARCPI using SiC MOSFETs or Si IGBTs', in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, Sep. 2019, pp. 1981–1987. doi: 10.1109/ECCE.2019.8912876.

[70] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, 'Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices', *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017, doi: 10.1109/TPEL.2017.2655496.

[71] S. Ji, Z. Zhang, and F. Wang, 'Overview of high voltage sic power semiconductor devices: development and application', *CES Trans. Electr. Mach. Syst.*, vol. 1, no. 3, pp. 254–264, Sep. 2017, doi: 10.23919/TEMS.2017.8086104.

[72] A. Marzoughi, R. Burgos, and D. Boroyevich, 'Investigating Impact of Emerging Medium-Voltage SiC MOSFETs on Medium-Voltage High-Power Industrial Motor Drives', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019, doi: 10.1109/JESTPE.2018.2844376.

[73] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, 'Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments', *IEEE Trans. Device Mater. Reliab.*, vol. 10, no. 4, pp. 418–426, Dec. 2010, doi: 10.1109/TDMR.2010.2077295.

[74] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, 'A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature,

High-Frequency Applications', *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307–2320, May 2014, doi: 10.1109/TPEL.2013.2283245.

[75] J. B. Casady and R. W. Johnson, 'STATUS OF SILICON CARBIDE (SIC) AS A WlDE-BANDGAP SEMICONDUCTOR FOR HIGH-TEMPERATURE APPLICATIONS: A REVIEW', p. 14.

[76] M. Bhatnagar and B. J. Baliga, 'Comparison of 6H-SiC, 3C-SiC, and Si for power devices', *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, Mar. 1993, doi: 10.1109/16.199372.

[77] Y. Gao, A. Q. Huang, S. Krishnaswami, J. Richmond, and A. K. Agarwal, 'Comparison of Static and Switching Characteristics of 1200 V 4H-SiC BJT and 1200 V Si-IGBT', *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 887–893, 2008, doi: 10.1109/TIA.2008.921408.

[78] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, 'An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations', *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014, doi: 10.1109/TPEL.2013.2278919.

[79] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, 'Analytical Methodology for Loss Calculation of SiC MOSFETs', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019, doi: 10.1109/JESTPE.2018.2863731.

[80] H. Li, Y. Jiang, C. Feng, and Z. Yang, 'A Voltage-injected Active Gate Driver for Improving the Dynamic Performance of SiC MOSFET', in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, Sep. 2019, pp. 6943–6948. doi: 10.1109/ECCE.2019.8912602.

[81] I. Laird, X. Yuan, J. Scoltock, and A. J. Forsyth, 'A Design Optimization Tool for Maximizing the Power Density of 3-Phase DC–AC Converters Using Silicon Carbide (SiC) Devices', *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2913–2932, Apr. 2018, doi: 10.1109/TPEL.2017.2705805.

[82] Y. Li *et al.*, 'A 500kW Forced-air-cooled Silicon Carbide (SiC) 3-Phase DC/AC Converter with a Power Density of 1.246MW/m3 and Efficiency >98.5%', *IEEE Trans. Ind. Appl.*, pp. 1–1, 2021, doi: 10.1109/TIA.2021.3087546.

[83] K. Takao, S. Harada, T. Shinohe, and H. Ohashi, 'Performance evaluation of all SiC power converters for realizing high power density of 50 W/cm^3', in *The 2010 International Power Electronics Conference - ECCE ASIA -*, Sapporo, Japan, Jun. 2010, pp. 2128–2134. doi: 10.1109/IPEC.2010.5543727.

[84] L. Zhang *et al.*, 'Evaluation of Different Si/SiC Hybrid Three-Level Active NPC Inverters for High Power Density', *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8224–8236, Aug. 2020, doi: 10.1109/TPEL.2019.2962907.

[85] T. Zhao, J. Wang, A. Q. Huang, and A. Agarwal, 'Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems', in *2007 IEEE Industry Applications Annual Meeting*, New Orleans, LA, USA, Sep. 2007, pp. 331–335. doi: 10.1109/07IAS.2007.51.

[86] D. Han, Y. Li, and B. Sarlioglu, 'Analysis of SiC based power electronic inverters for high speed machines', in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 304–310. doi: 10.1109/APEC.2015.7104367.

[87] Puqi Ning *et al.*, 'SiC Wirebond Multichip Phase-Leg Module Packaging Design and Testing for Harsh Environment', *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 16–23, Jan. 2010, doi: 10.1109/TPEL.2009.2027324.

[88] J. Homberger, A. B. Lostetter, K. J. Olejniczak, T. McNutt, S. M. Lal, and A. Mantooth, 'Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments', in *2004 IEEE Aerospace Conference Proceedings (IEEE Cat. No.04TH8720)*, Big Sky, MT, USA, 2004, vol. 4, pp. 2538–2555. doi: 10.1109/AERO.2004.1368048.

[89] R. A. Mastromauro, M. C. Poliseno, S. Pugliese, F. Cupertino, and S. Stasi, 'SiC MOSFET Dual Active Bridge converter for harsh environment applications in a more-electric-aircraft', in *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, Aachen, Germany, Mar. 2015, pp. 1–6. doi: 10.1109/ESARS.2015.7101427.

[90] L. A. Navarro *et al.*, 'Thermomechanical Assessment of Die-Attach Materials for Wide Bandgap Semiconductor Devices and Harsh Environment Applications', *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2261–2271, May 2014, doi: 10.1109/TPEL.2013.2279607.

[91] 'Mitsubishi Electric to Launch Railcar Traction Inverter with All-SiC Power Module'. https://www.mitsubishielectric.com/news/2013/1225.html

[92] 'Toyota and Denso develop SiC power semiconductor for power control units; targeting 10% improvement in hybrid fuel efficiency'. https://www.greencarcongress.com/2014/05/20140520-sic.html

[93] T. M. Jahns and B. Sarlioglu, 'The Incredible Shrinking Motor Drive: Accelerating the Transition to Integrated Motor Drives', *IEEE Power Electron. Mag.*, vol. 7, no. 3, pp. 18–27, Sep. 2020, doi: 10.1109/MPEL.2020.3011275.

[94] W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, 'A Review of Integrated Motor Drive and Wide-Bandgap Power Electronics for High-Performance Electro-Hydrostatic Actuators', *IEEE Trans. Transp. Electrification*, vol. 4, no. 3, pp. 684–693, Sep. 2018, doi: 10.1109/TTE.2018.2853994.

[95] H. Lee, V. Smet, and R. Tummala, 'A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020, doi: 10.1109/JESTPE.2019.2951801.

[96] 'The 2nd Generation John Deere SiC Inverter – Smaller, but BIG in Capability'. https://www.deere.com/en/electronics/news-room/news-articles/2nd-generation-sic-inverter/

[97] M. Ghassemi, 'Accelerated insulation aging due to fast repetitive voltages A review identifying challenges and future research needs', *IEEE Trans. Dielectr. Electr. Insul.*, vol. 26, no. 5, pp. 1558–1568, Oct. 2019, doi: 10.1109/TDEI.2019.008176.

[98] P. Wang, A. Cavallini, and G. C. Montanari, 'Characteristics of PD under square wave voltages and their influence on motor insulation endurance', *IEEE Trans. Dielectr. Electr. Insul.*, vol. 22, no. 6, pp. 3079–3086, Dec. 2015, doi: 10.1109/TDEI.2015.005158.

[99] M. Pastura, S. Nuzzo, M. Kohler, and D. Barater, 'DvDt Filtering Techniques for Electric Drives Review and Challenges', in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, Lisbon, Portugal, Oct. 2019, pp. 7088–7093. doi: 10.1109/IECON.2019.8926663.

[100] D. D'Amato, J. Loncarski, V. G. Monopoli, F. Cupertino, L. P. Di Noia, and A. Del Pizzo, 'Impact of PWM Voltage Waveforms in High-Speed Drives: A Survey on High-Frequency Motor Models and Partial Discharge Phenomenon', *Energies*, vol. 15, no. 4, p. 1406, Feb. 2022, doi: 10.3390/en15041406.

[101] P. Yi, P. K. S. Murthy, and L. Wei, 'Performance evaluation of SiC MOSFETs with long power cable and induction motor', in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7. doi: 10.1109/ECCE.2016.7855344.

[102] J. L. Guardado and K. J. Cornick, 'The effect of coil parameters on the distribution of steep-fronted surges in machine windings', *IEEE Trans. Energy Convers.*, vol. 7, no. 3, pp. 552–559, Sep. 1992, doi: 10.1109/60.148578.

[103] Y. Xie, J. Zhang, F. Leonardi, A. R. Munoz, M. W. Degner, and F. Liang, 'Modeling and Verification of Electrical Stress in Inverter-Driven Electric Machine

Windings', *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 5818–5829, Nov. 2019, doi: 10.1109/TIA.2019.2937068.

[104] S. Sundeep, J. B. Wang, A. Griffo, and F. Alvarez-Gonzalez, 'Anti-resonance Phenomenon and Peak Voltage Stress within PWM Inverter Fed Stator Winding', *IEEE Trans. Ind. Electron.*, pp. 1–1, 2021, doi: 10.1109/TIE.2020.3048286.

[105] S. Sundeep, J. Wang, and A. Griffo, 'Holistic Modeling of High Frequency Behavior of Inverter-fed Machine Winding, Considering Mutual Couplings in Time Domain', *IEEE Trans. Ind. Appl.*, pp. 1–1, 2021, doi: 10.1109/TIA.2021.3105954.

[106] T. Billard, T. Lebey, and F. Fresnet, 'Partial discharge in electric motor fed by a PWM inverter: off-line and on-line detection', *IEEE Trans. Dielectr. Electr. Insul.*, vol. 21, no. 3, pp. 1235–1242, Jun. 2014, doi: 10.1109/TDEI.2014.6832270.

[107] B. Mirafzal, G. L. Skibinski, and R. M. Tallam, 'A Failure Mode for PWM Inverter-Fed AC Motors Due to the Antiresonance Phenomenon', *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1697–1705, 2009, doi: 10.1109/TIA.2009.2027524.

[108] J. He, H. Chen, R. Katebi, N. Weise, and N. A. O. Demerdash, 'Mitigation of uneven surge voltage stress on stator windings of induction motors fed by SiC-MOSFET-based adjustable speed drives', in *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, USA, May 2017, pp. 1–7. doi: 10.1109/IEMDC.2017.8002402.

[109] V. C. de Paula and H. de Paula, 'Employing DC transmission in long distance AC motor drives: Analysis of the copper economy and power losses reduction in mining facilities', in *2015 IEEE Industry Applications Society Annual Meeting*, Addison, TX, USA, Oct. 2015, pp. 1–7. doi: 10.1109/IAS.2015.7356899.

[110] X. Guo, Q. Xun, Z. Li, and S. Du, 'Silicon Carbide Converters and MEMS Devices for High-temperature Power Electronics: A Critical Review', *Micromachines*, vol. 10, no. 6, p. 406, Jun. 2019, doi: 10.3390/mi10060406.

[111] M. Bendjedia, A. Khlaief, and M. Boussak, 'Sensorless speed control of outrunner PMSM drive connected to long cable for flying remote operative vehicle', in *2012 XXth International Conference on Electrical Machines*, Marseille, France, Sep. 2012, pp. 2252–2258. doi: 10.1109/ICElMach.2012.6350195.

[112] P. Xie, G. Vakil, and C. Gerada, 'Electric drive systems with long feeder cables', *IET Electr. Power Appl.*, vol. 14, no. 1, pp. 16–30, Jan. 2020, doi: 10.1049/iet-epa.2018.5507.

[113] J. A. Antonino-Daviu, A. Quijano-Lopez, M. Rubbiolo, and V. Climente-Alarcon, 'Advanced Analysis of Motor Currents for the Diagnosis of the Rotor Condition in Electric Motors Operating in Mining Facilities', *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3934–3942, Jul. 2018, doi: 10.1109/TIA.2018.2818671.

[114] J. C. G. Wheeler, 'Effects of converter pulses on the electrical insulation in low and medium voltage motors', *IEEE Electr. Insul. Mag.*, vol. 21, no. 2, pp. 22–29, Mar. 2005, doi: 10.1109/MEI.2005.1412216.

[115] G. Skibinski, 'Design methodology of a cable terminator to reduce reflected voltage on AC motors', in *IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, San Diego, CA, USA, 1996, vol. 1, pp. 153–161. doi: 10.1109/IAS.1996.557009.

[116] B. Narayanasamy, A. S. Sathyanarayanan, F. Luo, and C. Chen, 'Reflected Wave Phenomenon in SiC Motor Drives: Consequences, Boundaries, and Mitigation', *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10629–10642, Oct. 2020, doi: 10.1109/TPEL.2020.2975217.

[117] H. Xiong, J. Zhang, and A. Von Jouanne, 'Control of Variable Frequency Drive PWM to Mitigate Motor Overvoltage Due to Double Pulsing in Reflected Wave Phenomenon', in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, Sep. 2018, pp. 6563–6570. doi: 10.1109/ECCE.2018.8558140.

[118] S. Walder and X. Yuan, 'Effect of load parasitics on the losses and ringing in high switching speed SiC MOSFET based power converters', in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 6161–6168. doi: 10.1109/ECCE.2015.7310523.

[119] L. Wang, C. Ngai-Man Ho, F. Canales, and J. Jatskevich, 'High-Frequency Modeling of the Long-Cable-Fed Induction Motor Drive System Using TLM Approach for Predicting Overvoltage Transients', *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2653–2664, Oct. 2010, doi: 10.1109/TPEL.2010.2047027.

[120] R. M. Tallam and D. Leggate, 'Control of a PWM Voltage-Source Inverter in the Pulse-Dropping Region to Reduce Reflected-Wave Motor Overvoltage', *IEEE Trans. Ind. Appl.*, vol. 49, no. 2, pp. 873–879, Mar. 2013, doi: 10.1109/TIA.2012.2228613.

[121] G. Skibinski, R. Tallam, R. Reese, B. Buchholz, and R. Lukaszewski, 'Common Mode and Differential Mode Analysis of Three Phase Cables for PWM AC Drives', in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, Tampa, FL, Oct. 2006, vol. 2, pp. 880–888. doi: 10.1109/IAS.2006.256629.

[122] M. Denk and M. M. Bakran, 'Partial Discharge Measurement in a Motor Winding Fed by a SiC Inverter - How Critical is High dV/dt Really?', in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Jun. 2018, pp. 1–6.

[123] I. Mitiche, G. Morison, A. Nesbitt, P. Boreham, and B. G. Stewart, 'Classification of partial discharge EMI conditions using permutation entropy-based features', in *2017 25th European Signal Processing Conference (EUSIPCO)*, Kos, Greece, Aug. 2017, pp. 1375–1379. doi: 10.23919/EUSIPCO.2017.8081434.

[124] A. von Jouanne, D. Rendusara, P. Enjeti, and W. Gray, 'Filtering techniques to minimize the effect of long motor leads on PWM inverter fed AC motor drive systems', in *IAS '95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, Orlando, FL, USA, 1995, vol. 1, pp. 37–44. doi: 10.1109/IAS.1995.530281.

[125] W. Zhou, M. S. Diab, and X. Yuan, 'Mitigation of Motor Overvoltage in SiC-Device-Based Drives using a Soft-Switching Inverter', in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 662–669. doi: 10.1109/ECCE44975.2020.9236099.

[126] J. He, G. Y. Sizov, P. Zhang, and N. A. O. Demerdash, 'A review of mitigation methods for overvoltage in long-cable-fed PWM AC drives', in *2011 IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, USA, Sep. 2011, pp. 2160–2166. doi: 10.1109/ECCE.2011.6064054.

[127] S. Lee and K. Nam, 'Overvoltage Suppression Filter Design Methods Based on Voltage Reflection Theory', *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 264–271, Mar. 2004, doi: 10.1109/TPEL.2003.820538.

[128] A. F. Moreira, P. M. Santos, T. A. Lipo, and G. Venkataramanan, 'Filter Networks for Long Cable Drives and Their Influence on Motor Voltage Distribution and Common-Mode Currents', *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 515–522, Apr. 2005, doi: 10.1109/TIE.2005.844237.

[129] A. F. Moreira, T. A. Lipo, G. Venkataramanan, and S. Bernet, 'High-frequency modeling for cable and induction motor overvoltage studies in long cable drives', *IEEE Trans. Ind. Appl.*, vol. 38, no. 5, pp. 1297–1306, Sep. 2002, doi: 10.1109/TIA.2002.802920.

[130] Han-Jong Kim, Geun-Ho Lee, Cheol-Ho Jang, and Jea-Pil Lee, 'Cost-effective design of an inverter output reactor in ASD applications', *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1128–1135, Dec. 2001, doi: 10.1109/41.969391.

[131] R. M. Tallam, G. L. Skibinski, T. A. Shudarek, and R. A. Lukaszewski, 'Integrated differential-mode and common-mode filter to mitigate the effects of long motor leads

on AC drives', in *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, Sep. 2010, pp. 838–845. doi: 10.1109/ECCE.2010.5617910.

[132] R. Ruffo, P. Guglielmi, and E. Armando, 'Inverter Side *RL* Filter Precise Design for Motor Overvoltage Mitigation in SiC-Based Drives', *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 863–873, Feb. 2020, doi: 10.1109/TIE.2019.2898623.

[133] J. He *et al.*, 'Multi-Domain Design Optimization of dvdt Filter for SiC-Based Three-Phase Inverters in High-Frequency Motor-Drive Applications', *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5214–5222, Sep. 2019, doi: 10.1109/TIA.2019.2922306.

[134] M. S. Diab and X. Yuan, 'A Quasi-Three-Level PWM Scheme to Combat Motor Overvoltage in SiC-Based Single-Phase Drives', *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12639–12645, Dec. 2020, doi: 10.1109/TPEL.2020.2994289.

[135] Sangcheol Lee and Kwanghee Nam, 'An overvoltage suppression scheme for AC motor drives using a half DC-link voltage level at each PWM transition', *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 549–557, Jun. 2002, doi: 10.1109/TIE.2002.1005379.

[136] W. Zhou, M. Diab, and X. Yuan, 'Impact of Parasitic and Load Current on the Attenuation of Motor Terminal Overvoltage in SiC-Based Drives', *IEEE Trans. Ind. Appl.*, vol. 58, no. 2, pp. 2229–2241, Mar. 2022, doi: 10.1109/TIA.2022.3141703.

[137] M. S. Diab and X. Yuan, 'A Quasi-Three-Level Modulation Scheme to Combat Motor Overvoltage in SiC-Based Drives with Open-End Stator Winding Configurations', in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, Singapore, Oct. 2020, pp. 844–851. doi: 10.1109/IECON43393.2020.9254629.

[138] M. S. Diab and X. Yuan, 'A Modular Quasi-Multilevel Converter using 10kV SiC MOSFETs for Medium-Voltage Cable-Fed Variable-Speed Motor Drives', in *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, Singapore, Singapore, May 2021, pp. 781–786. doi: 10.1109/ECCE-Asia49820.2021.9479096.

[139] Y. Zhang and H. Li, 'A WBG Based Active Reflected Wave Canceller for SiC Motor Drives', in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, Oct. 2019, pp. 75–79. doi: 10.1109/WiPDA46397.2019.8998888.

[140] Y. Zhang, H. Li, and F. Z. Peng, 'A Low-Loss Compact Reflected Wave Canceller for SiC Motor Drives', *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2461–2465, Mar. 2021, doi: 10.1109/TPEL.2020.3014579.

[141] F. Bertoldi, M. Pathmanathan, R. S. Kanchan, K. Spiliotis, and J. Driesen, 'Quasi-Two-Level Converter for overvoltage mitigation in medium voltage drives', in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, May 2018, pp. 488–494. doi: 10.23919/IPEC.2018.8507745.

[142] D. Sun, Z. Zheng, B. Lin, W. Zhou, and M. Chen, 'A Hybrid PWM-Based Field Weakening Strategy for a Hybrid-Inverter-Driven Open-Winding PMSM System', *IEEE Trans. Energy Convers.*, vol. 32, no. 3, pp. 857–865, Sep. 2017, doi: 10.1109/TEC.2017.2676020.

[143] W. Zhou, D. Sun, M. Chen, and B. Lin, 'Simplified PWM for fault tolerant control of open winding PMSM fed by hybrid inverter', in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 2912–2918. doi: 10.1109/ECCE.2015.7310068.

[144] W. Zhou, D. Sun, and B. Lin, 'A modified flux weakening direct torque control for open winding PMSM system fed by hybrid inverter', in *2014 17th International Conference on Electrical Machines and Systems (ICEMS)*, Hangzhou, China, Oct. 2014, pp. 2917–2922. doi: 10.1109/ICEMS.2014.7013995.

[145] F. Bertoldi, M. Pathmanathan, and R. S. Kanchan, 'Quasi - two-level converter operation strategy for overvoltage mitigation in long cable applications', in *2019 IEEE International Electric Machines & Drives Conference (IEMDC)*, San Diego, CA, USA, May 2019, pp. 1621–1627. doi: 10.1109/IEMDC.2019.8785123.

[146] X. Li *et al.*, 'Impact of the Leakage Inductance on the Reflected Wave Phenomenon in MMC based Motor Drives', in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, Mar. 2020, pp. 734–740. doi: 10.1109/APEC39645.2020.9124004.

[147] J. A. de Castro, H. de Paula, and B. J. C. Filho, 'A new configuration for motor drive systems based on long cable connection between rectifier and inverter — Part I: Analysis of the losses reduction and copper economy', in *2009 Brazilian Power Electronics Conference*, Bonito-Mato Grosso do Sul, Sep. 2009, pp. 848–855. doi: 10.1109/COBEP.2009.5347718.

[148] H. Chen and H. Zhao, 'Review on pulse-width modulation strategies for common-mode voltage reduction in three-phase voltage-source inverters', *IET Power Electron.*, vol. 9, no. 14, pp. 2611–2620, Nov. 2016, doi: 10.1049/iet-pel.2015.1019.

[149] A. M. Hava and E. Un, 'Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters', *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 241–252, Jan. 2009, doi: 10.1109/TPEL.2008.2005719.

[150] K. Wang, X. Yang, H. Li, L. Wang, and P. Jain, 'A High-Bandwidth Integrated Current Measurement for Detecting Switching Current of Fast GaN Devices', *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6199–6210, Jul. 2018, doi: 10.1109/TPEL.2017.2749249.

[151] M. Schweizer and J. W. Kolar, 'Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications', *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013, doi: 10.1109/TPEL.2012.2203151.

[152] Z. Zeng, X. Zhang, and Z. Zhang, 'Imbalance Current Analysis and Its Suppression Methodology for Parallel SiC MOSFETs with Aid of a Differential Mode Choke', *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1508–1519, Feb. 2020, doi: 10.1109/TIE.2019.2901655.

[153] 'Wolfspeed product'. https://www.wolfspeed.com/

[154] Y. Wen, Y. Yang, and Y. Gao, 'Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules', *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021, doi: 10.1109/TPEL.2020.3006071.

[155] R. Teichmann and S. Bernet, 'Investigation and comparison of auxiliary resonant commutated pole converter topologies', in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, Fukuoka, Japan, 1998, vol. 1, pp. 15–23. doi: 10.1109/PESC.1998.701873.

[156] A. Charalambous, X. Yuan, and N. McNeill, 'High-Frequency EMI Attenuation at Source With the Auxiliary Commutated Pole Inverter', *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5660–5676, Jul. 2018, doi: 10.1109/TPEL.2017.2743041.

[157] R. W. De Doncker and J. P. Lyons, 'The auxiliary resonant commutated pole converter', in *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting*, Seattle, WA, USA, 1990, pp. 1228–1235. doi: 10.1109/IAS.1990.152341.

[158] A. Cheriti, K. Al-Haddad, and D. Mukhedkar, 'Calculation of power loss in soft commutated PWM inverters', in *Conference Record of the 1991 IEEE Industry Applications Society Annual Meeting*, Dearborn, MI, USA, 1991, pp. 782–788. doi: 10.1109/IAS.1991.178328.

[159] J. Dawidziuk, S. Jalbrzykowski, and Z. Prajs, 'An analysis and experimental studies of auxiliary resonant commutated pole inverters', in *ISIE '93 - Budapest: IEEE International Symposium on Industrial Electronics Conference Proceedings*, Budapest, Hungary, 1993, pp. 780–785. doi: 10.1109/ISIE.1993.268706.

[160] M. Ohsugi, T. Shimizu, G. Kimura, A. Toba, and S. Sano, 'The analyses of ZVS turn-off loss and the new snubber circuit for the ARCP inverter', in *Proceedings of*

IECON'94 - 20th Annual Conference of IEEE Industrial Electronics, Bologna, Italy, 1994, vol. 1, pp. 316–321. doi: 10.1109/IECON.1994.397795.

[161] Jih-Sheng Lai, 'Practical design methodology of auxiliary resonant snubber inverters', in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, Baveno, Italy, 1996, vol. 1, pp. 432–437. doi: 10.1109/PESC.1996.548616.

[162] H.-J. Pfisterer and H. Spath, 'Switching behaviour of an auxiliary resonant commutated pole (ARCP) converter', in *7th IEEE International Power Electronics Congress. Technical Proceedings. CIEP 2000 (Cat. No.00TH8529)*, Acapulco, Mexico, 2000, pp. 359–364. doi: 10.1109/CIEP.2000.891440.

[163] W. Dong *et al.*, 'Comparative experimental evaluation of soft-switching inverter techniques for electric vehicle drive applications', in *Conference Record of the 2001 IEEE Industry Applications Conference. 36th IAS Annual Meeting (Cat. No.01CH37248)*, Chicago, IL, USA, 2001, vol. 3, pp. 1469–1476. doi: 10.1109/IAS.2001.955729.

[164] J. Voss, J. Warmuz, D. Mathai, and R. W. De Doncker, 'Adapted Auxiliary-Resonant Commutated Pole in the Dual-Active Bridge', *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 4, pp. 2553–2560, Dec. 2019, doi: 10.1109/JESTPE.2019.2894164.

[165] M. Yamamoto, 'Full SiC soft switching inverter Stability performance for false turn on phenomenon', in *2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS)*, Kitakyushu, Apr. 2013, pp. 159–164. doi: 10.1109/PEDS.2013.6527007.

[166] Ke Ma, Dehong Xu, Tao Zhang, and S. Igarashi, 'The evaluation of control strategies for Auxiliary Resonant Commutated Pole inverter', in *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, Sep. 2009, pp. 810–816. doi: 10.1109/ECCE.2009.5315974.

[167] S. Sundeep, J. Wang, and A. Griffo, 'Prediction of Transient Voltage Distribution in Inverter-fed Stator Winding, Considering Mutual Couplings in Time Domain', in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 517–524. doi: 10.1109/ECCE44975.2020.9235981.

[168] B. Mirafzal, G. L. Skibinski, and R. M. Tallam, 'Determination of Parameters in the Universal Induction Motor Model', *IEEE Trans. Ind. Appl.*, vol. 45, no. 1, pp. 142–151, 2009, doi: 10.1109/TIA.2008.2009481.

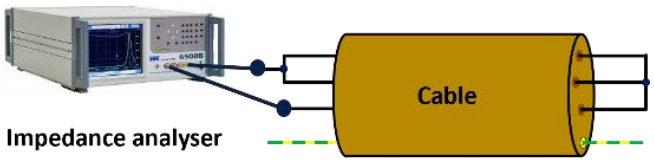
Appendix 1

Cable Parameter Measurement Method

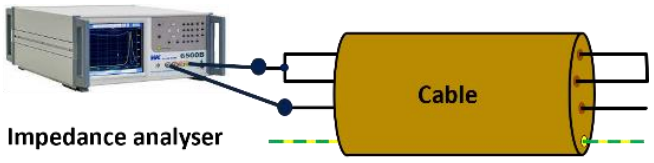
A1.1 Cable per Meter Capacitance (C_c) and Inductance (L_c)

In general, the cable's L_c and C_c are not listed in the datasheet. These parameters can be extracted from the short-circuit and open-circuit impedance measurements. Figure A1.1 illustrates the measurement schematics, where Figure A1.1(a) and (b) show the measurement schematic for short-circuit and open-circuit, respectively.

Figure A1.2 shows the impedance for 1m sample cable, where Figure A1.2 (a)and (b) show the impedance for short-circuit and open-circuit, respectively. L_c can be determined from the 20dB/decade slope of short-circuit impedance as shown in Figure A1.2 (a). Whereas, C_c can be determined from the -20dB/decade slope of open-circuit impedance as shown in Figure A1.2 (b).

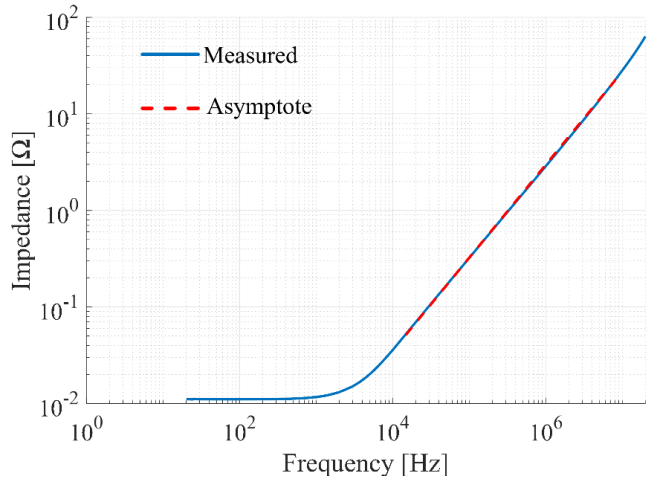


(a)

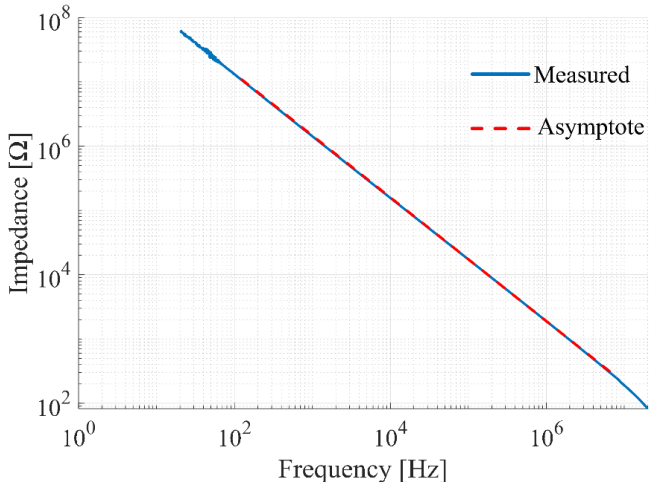


(b)

Figure A1.1 Measurement schematic for cable (a) short-circuit impedance and (b) open-circuit impedance.



(a)



(a)

Figure A1.2 Measurement schematic for cable (a) short-circuit impedance and (b) open-circuit impedance.

A1.2 Wave Propagation Time Calculation

In addition to calculating wave propagation time according to the cable's L_c and C_c, the wave propagation time can be obtained using the experimental methods.

A1.2.1 Method I

Using an oscilloscope to measure the propagation delay between the incident voltage (inverter voltage V_s) and the resultant voltage (motor terminal voltage V_m). Since the time shift is the wave propagation time (t_p), the ideal rise time can be calculated as $4t_p$. Note that this method can be used in the lab before the deployment of the drives since the inverter and the motor are usually placed in separated location in real applications, where it is

difficult to measure the inverter voltage and the motor voltage at the same time. In general, the long cable is looped together to calculate the wave propagation time due to the limited space in the lab. In fact, there is no significant difference between the looped cable and straight cable.

Figure A1.3 compares the experimental results for the long cable-fed motor drive system when the cable is looped and not looped, where $V_{m-ring\ coiled\ cable}$ and $V_{m-straight\ cable}$ are the motor voltage using the ring coiled (looped) cable and straight cable, respectively. As shown, the wave propagation time t_p does not vary too much for the two cases.

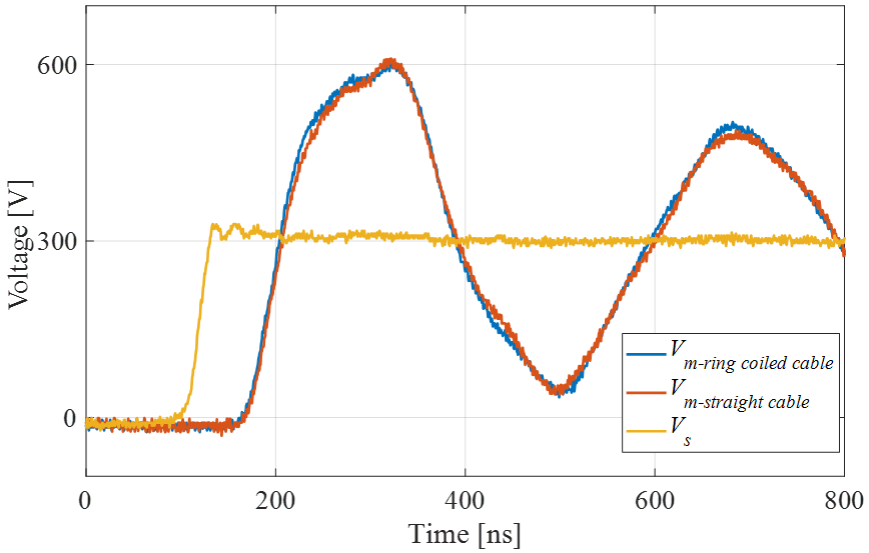


Figure A1.3 The voltages of the inverter and motor when the cable is straight and looped.

A1.2.2 Method II

Measuring the cable's first anti-resonance frequency, which corresponds to $1/4t_p$, as shown in Figure A1.4, then the optimal time can be calculated. Note that the cable's first anti-resonance frequency can be obtained by measuring its common mode (CM) impedance using an impedance analyzer. Figure A1.5 shows how to measure the CM impedance, where Figure A1.5 (a) and (b) show the single-phase and three-phase cases, respectively. Referring to Figure A1.5 (a), for the single-phase case, the live and neutral terminals are shorted-circuited into a common terminal from both ends while the cable CM impedance is obtained by measuring the impedance between the common terminal and the cable earth wire in open-circuit configuration. Referring to Figure A1.5 (b), for three-phase case, the equivalent CM circuit is formed as a two-port network with the paralleled three-phase and ground wire. Therefore, the CM impedance can be obtained by measuring the impedance of the two-port network in open-circuit configuration, as shown in Figure A1.5 (b).

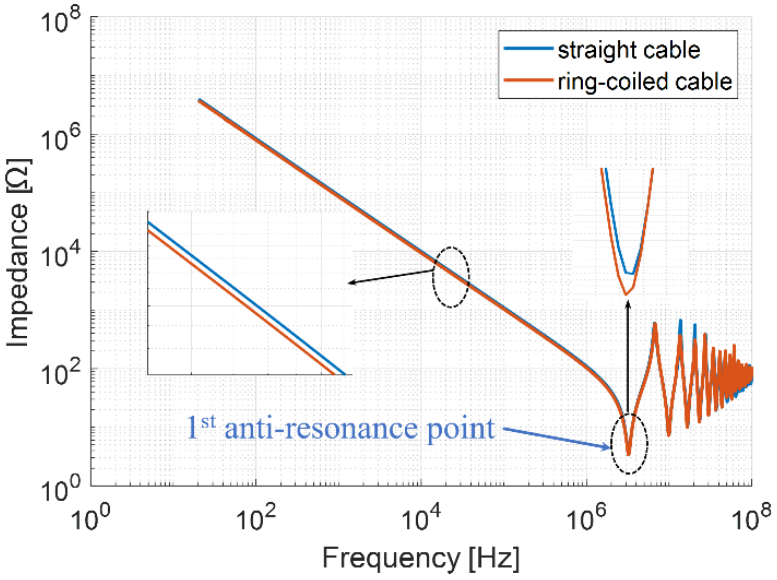
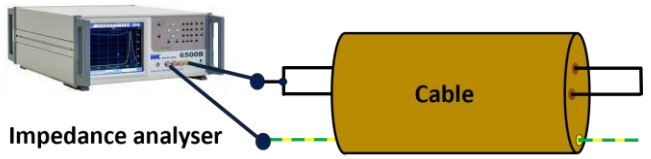
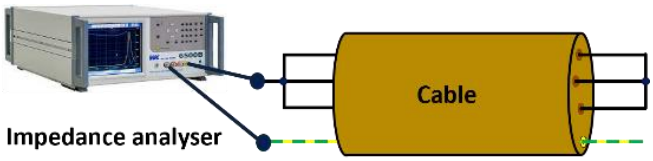


Figure A1.4 The CM impedance of ring-coiled cable and straight cable.



(a)



(b)

Figure A1.5 Cable CM impedance measurement schematic for (a) single phase case and (b) three-phase case..