EERA DeepWind Offshore Wind R&D Conference IOP Publishing
Journal of Physics: Conference Series **2362** (2022) 012002 doi:10.1088/1742-6596/2362/1/012002

Development of a Geographically Distributed Real-Time Test Facility

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Abstract. Europe's electric power network is entering a period of extreme flux as we move to an era where it is dominated by non-linear, asynchronous generation such as wind power plants. The rapid rise of new technologies in this space has led to increasingly complex interactions within the power network that are difficult to cover through traditional test regimes. Existing facilities are not fully equipped to address these new system orientated challenges and while investing in new sites and facilities is one way forward, this is likely to be prohibitively expensive and runs the risk of only being applicable to niche applications. This work presents the first stage in an alternative approach which seeks to address these challenges through the pooling of existing resources. In this concept, geographically distributed test facilities are combined virtually to create new capabilities and perform complex system level validations. This can be done through a Geographically Distributed – Power Hardware in the Loop (GD-PHIL) setup. To achieve this, each site requires a PHIL setup allowing the Device Under Test (DUT) to interact in real time with a simulation. This work will present the outcome of the first step towards the development of such a network, developing and demonstrating the stable communications interfaces necessary to link geographically distributed real time simulators from two different manufacturers.

1. Introduction

Representative and repeatable testing has always been the cornerstone of scientific and engineering advancement. Yet until recently, much of the testing of modern wind turbines was conducted in the field and relied on particular, often non-repeatable, weather conditions. This has hampered product development and delayed rollout increasing costs. Recently though, through test bench facilities such as those available at ORE Catapult and PNDC and University of Strathclyde, manufacturers have been able to accelerate product testing and gain valuable knowledge about their devices.

Geographically Distributed – Hardware in the Loop (GD-HIL) enables the capabilities of different test centres to be combined without the need for large scale investment. The Hardware in the Loop (HIL) systems at both ORE Catapult and PNDC are linked to the wider test facilities, as such it is envisioned that full scale wind/tidal turbines undergoing powertrain testing at either the 15MW or 3MW test facilities with eGrid at ORE Catapult can link to the electrical 11kV network facilities at PNDC. As such highly representative system level testing can be conducted without relying on electrical models wholly built in the simulation environment.

In the area of power systems, Geographically Distributed Simulations (GDS) were first reported in 2006 [1] as a concept. It was followed in 2009 by the first GDS between the Florida State University and the University of Alberta, a 3500km link for the study of thermo-electrical simulations of shipboards [2]. Incorporating hardware equipment in GDS appeared in 2014 [3], being at its infancy stage it was an asynchronous, soft-real-time link. Developments in the area of internet communications led to a revisit of the method in 2015 by the University of South Carolina and Rheinisch-Westfälische Technische Hochschule (RWTH) Aachen University with a transatlantic link of 7,300km [4]. This was soon followed by an interconnection link between Stiftelsen for Industriell og Teknisk Forskning (SINTEF) and RWTH [5]. Another transatlantic link was also developed between Commonwealth Scientific and Industrial Research Organisation (CSIRO) and National Renewable Energy Laboratory (NREL), at a distance of 13,500km it is the longest reported interconnection till today [6] and the first to attempt implementing hardware on both sides. The success of those projects enforced confidence and led to a more widespread adoption of the methodology with a transatlantic interconnection of eight institutes under the “Global Real-time SuperLab” project [7].

2. Testbeds

This section offers a brief description of the assets of the institutes that are involved in this project. The University of Strathclyde, Dynamic Power Systems Laboratory (DPSL), Power Networks Demonstration Centre (PNDC) and Offshore Renewable Energy Catapult, Blyth.

2.1. DPSL

The Dynamic Power Systems Laboratory (DPSL) is an electrical test facility within University of Strathclyde. It has a total capacity of 115kVA at 400V (three phase). The network can be divided into three individual islanded micro-grids that are independently controlled or combined in different combinations as a single whole electrical system. This high degree of flexibility enables the investigation of numerous scenarios. Furthermore, a digital real-time simulator from Real Time Digital Simulation (RTDS) Technologies, allows for Controller Hardware in the Loop (CHIL) and Power Hardware in the Loop (PHIL) setups. To this end a 90kVA back-to-back (B2B) converter is used. The three micro-grids have Phasor Measurement Units (PMUs) installed through the wide area monitoring, protection and control platform. For conducting scalable, CHIL implementations, up to 64 distributed controllers can be implemented.

2.2. PNDC

The Power Networks Demonstration Centre (PNDC) is an industry facing facility with an 11kV and 400V dedicated electrical network environment for system and integration testing. The network is representative of UK networks and provides a configurable testing environment for different electrical equipment and emerging technologies. Primary and secondary equipment can be connected to the test bays within the electrical test network and enables the connection of multiple energy storage and converter technologies. An optional motor generator grid infeed allows for testing of islanded networks and the application of voltage and frequency disturbances in the network under test. The real-time simulation capabilities and expertise of PNDC promote the testing and validation of new generation, network, demand-side management and storage systems mechanics. Finally, a 540kVA Power Amplifier Interface permits HIL architectures in both local and distributed configurations. The platform is domain agnostic thus further supporting studies of utility, transport and naval applications.

2.3. OREC

OREC’s powertrain testing facilities in Blyth are capable of full wind turbine system and individual component performance testing for typical and extreme conditions both at MW and kW scale, e.g. tests can be conducted on full drivetrain systems including bearings, gearbox, generator and converter. An offshore anemometry hub is able to provide high quality wind and ambient environmental data for validation and comparison of sensor technologies. Finally, the addition of a grid emulator (eGrid) will expand the testing capabilities of the facility and further support the development of innovative decision tools. OREC's offshore wind turbine in Levenmouth provides an opportunity for trial and demonstration of novel technologies in real-life conditions. Innovative control algorithms can be implemented and optimized, in combination with actual aero-elastic and aerodynamic mechanics.

3. Simulation set-up

In this section a description of the key elements of the simulation set-up is given as well as an evaluation of the time delay between the two sites and the respective compensation. For this initial phase of the project as was mentioned in the introduction, real-time simulators were used and coupled together over an internet connection. In ***Figure 1*** the high-level connection approach can be observed.

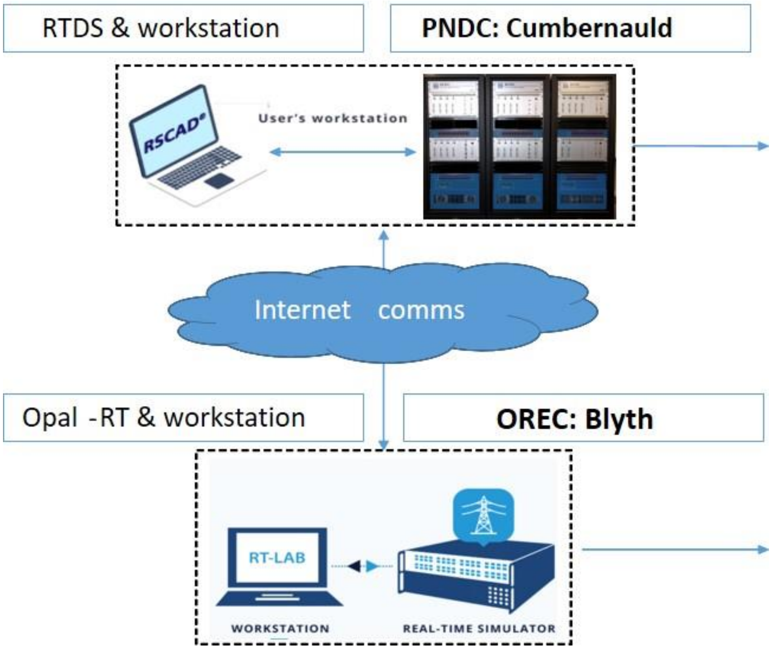

Figure 1. High level GD-HIL connection of PNDC and OREC

3.1. PNDC Assets

PNDC will use its own Real Time Simulator RTS, the Real Time Digital Simulator (RTDS), from the supplier RTDS Technologies Inc. The RTDS uses its dedicated modelling software suite RSCAD and its native power system and control libraries. Additionally, capability exists for translating PSCAD and Matlab control models to the RTDS native code. RTDS makes use of custom hardware arranged in cubicles. Each cubicle can carry several cards in individual racks. Every rack, depending on the application, can be independently composed by a combination of types of processor and communication cards.

3.2. OREC Assets

OPAL-RT is utilized within the OREC facility. It is a rapid prototyping and real-time HIL simulation system, optimized to execute Matlab/Simulink code. Scalable from 6 to 64 processors, and using 10Gb/s communications link, OPAL-RT can simulate models with time steps as low as 10μs. When combined with Field Programmable Gate Arrays (FPGA) co-processors and OPAL-RT's RT-XSG blockset, simulation time steps can be reduced to the nanoseconds range.

3.3. Interface and signals

Various interface algorithms have been analyzed in the literature concerning power hardware in the loop. For this project the Voltage-type Ideal Transformer Method (VT-ITM) was selected for the straightforward implementation and stability [8]. A voltage is created in subsystem 1 and communicated to subsystem 2 though a controlled voltage source. The currents in subsystem 2 are then fed back through a controlled current source to subsystem 1. In ***Figure 2*** a single line diagram of the ITM setup interface is shown.

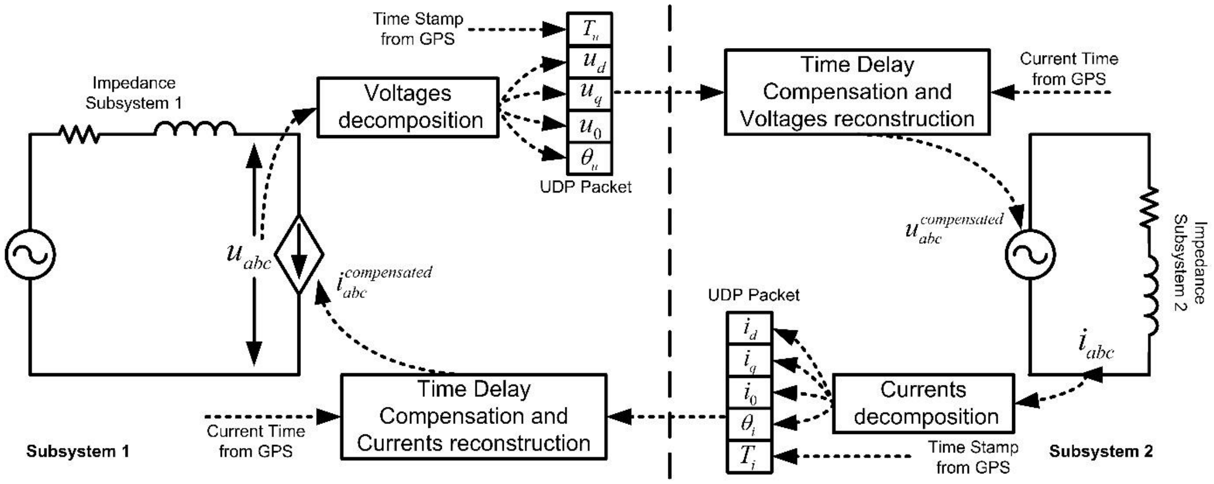

Figure 2. Single line diagram for ITM, GD-RTS interface [9]

The instantaneous values of voltages and currents need to be transformed as time domain signals are not appropriate for direct transmission over packed-based communications protocols [10]. Furthermore, for synchronized simulation and time compensation the phase of the communicated waveforms is also required [11]. Taking these into account, the synchronous reference frame transformation to dq0 components was selected.

3.4. Communication and synchronisation

The signals are packaged and transferred between subsystems. Because of geographical separation, the connection has been realized through an internet connection. Considering the available infrastructure, the User Datagram Protocol (UDP) has been deemed appropriate for connecting the two simulators as it has been efficiently used for real time applications before.

As mentioned in section 3.2. the signals to be communicated from subsystem 1, that resides in the RTDS of PNDC, are the voltage, decomposed to dq0 (u_d, u_q, u_0) components and the phase (θ_i). The decomposition of voltage is as in equation (1).

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(wt) & \cos\left(wt - \frac{2\pi}{3}\right) & \cos\left(wt + \frac{2\pi}{3}\right) \\ -\sin(wt) & -\sin\left(wt - \frac{2\pi}{3}\right) & -\sin\left(wt + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{1}$$

Respectively from subsystem 2 that resides in the OPAL-RT of OREC the signals are the current, decomposed to dq0 components (i_d, i_q, i_0) and its phase. The current decomposition is calculated as in equation (2)

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(wt) & \cos\left(wt - \frac{2\pi}{3}\right) & \cos\left(wt + \frac{2\pi}{3}\right) \\ -\sin(wt) & -\sin\left(wt - \frac{2\pi}{3}\right) & -\sin\left(wt + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2}$$

Both subsystems need to exchange an additional signal, the timestamp (T_u, T_i). This is because communication over geographical distance introduces time-delay that negatively affects the stability and accuracy of the simulation. To compensate for the time delay, it must be accurately measured [12]. In this project, time delay is calculated via the timestamps that are produced from a Global Positioning System (GPS) clock and embedded in the communicated UDP packages.

3.5. Time-delay compensation

To calculate the time delay, the timestamp of the UDP packet is subtracted from the current GPS clock time. The effect of the time-delay from subsystem 1 to subsystem 2 is referred to as feed-forward time delay τ_{dff} and is evident in the reconstructed voltage that is advanced by a phase φ_{ff} when compared to the reference voltage in subsystem 1. The feed-forward phase compensation is calculated as in equation (3).

$$\varphi_{ff} = \tau_{dff} \times 2\pi \times f_m \tag{3}$$

Respectively from subsystem 2 to subsystem 1 the time delay is referred to as feedback time delay τ_{dfb} and is apparent in the reconstructed currents that are also advanced by a phase φ_{fb} when compared to the reference current in subsystem 2. The feedback phase compensation is calculated as in equation (4)

$$\varphi_{fb} = \tau_{dfb} \times 2\pi \times f_m \tag{4}$$

To compensate, the waveforms should be shifted by the measured phase difference [12]. The compensated phase needs to be adaptive to measured frequency f_m to avoid steady state errors after transients. The reconstruction of the signals with the added time delay compensation can be calculated as seen in equation (5) and equation (6) below for voltage and current respectively.

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} \cos(\omega t + \varphi_{ff}) & -\sin(\omega t + \varphi_{ff}) & 1 \\ \cos\left(\omega t - \frac{2\pi}{3} + \varphi_{ff}\right) & -\sin\left(\omega t - \frac{2\pi}{3} + \varphi_{ff}\right) & 1 \\ \cos\left(\omega t + \frac{2\pi}{3} + \varphi_{ff}\right) & -\sin\left(\omega t + \frac{2\pi}{3} + \varphi_{ff}\right) & 1 \end{bmatrix} \begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \cos(w\omega t + \varphi_{fb}) & -\sin(\omega t + \varphi_{fb}) & 1 \\ \cos\left(\omega t - \frac{2\pi}{3} + \varphi_{fb}\right) & -\sin\left(\omega t - \frac{2\pi}{3} + \varphi_{fb}\right) & 1 \\ \cos\left(\omega t + \frac{2\pi}{3} + \varphi_{fb}\right) & -\sin\left(\omega t + \frac{2\pi}{3} + \varphi_{fb}\right) & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{6}$$

Figure 3, ***Figure 4*** and ***Figure 5***, show the reconstructed signals of voltage and current and the time delay that was observed when coupling PNDC and OREC's subsystems. The peak voltage created in RTDS is 325V and the load in OPAL-RT is set to an arbitrary 1kW. This creates a current of 2A in OPAL-RT that passes back to RTDS, closing the loop. The time delay calculated is 18.6ms. In reality, time delay does not hold a constant value but is related to the internet traffic at the time of the simulation.

A range of 16ms-21ms was observed through the duration of the project (***Figure 5*** shows variation in time delay over a 0.1 second timescale). This value is then used for the time delay compensation as was explained previously in this section.

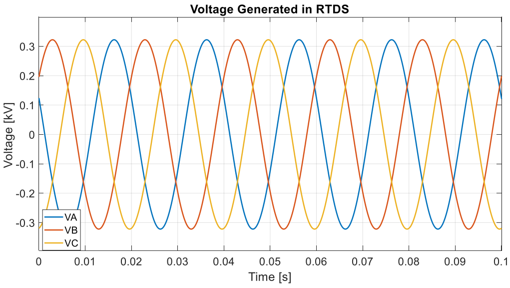

Figure 3. Voltage created from subsystem 1 in RTDS

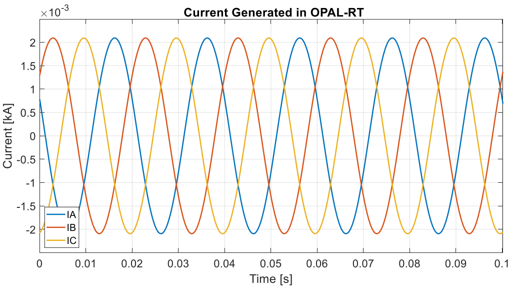

Figure 4. Current created in subsystem 2 in OPAL-RT

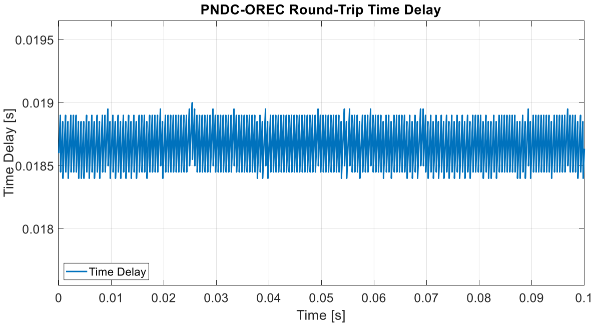

Figure 5. Measured round-trip time delay between PNDC and OREC

4. Demonstration scenario and models

To demonstrate the accuracy and stability of the coupling interface in an electrical grid application the following models and scenario were developed.

4.1. Scenario

The demonstration scenario concerns a frequency event. A sudden decrease in demand, represented by the disconnection of a load, leading to the frequency and voltage rise that can be observed on both subsystems. In this case there is no frequency control loops implemented and the network eventually finds a new steady state at higher values of voltage and frequency. The scenario was chosen for the straightforward implementation making use of appropriate, previously validated models. In ***Figure 6*** below, the single line diagram of the distributed simulation can be observed.

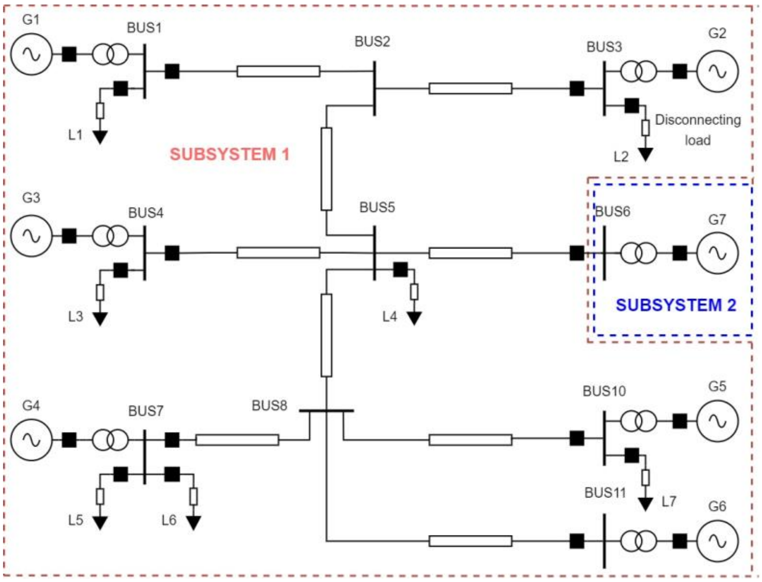

Figure 6. Single line diagram of the entire network divided in two subsystems

4.2. Subsystem 1 in PNDC

For subsystem 1 in PNDC a previously developed model is utilised. This model was developed in RSCAD, includes 6 buses, and represents a reduced, distribution model of Great Britain, with 66GVA capacity modelled at 400kV. This model has already been validated [13]. The parameters of the validated model can be found in [14]. Other important elements of subsystem 1 includes: the ITM interface, time delay calculation and compensation loop, composition/decomposition of transmitted signals in dq0.

4.3. Subsystem 2 in OREC

The model running in OPAL-RT, is built in Matlab. It includes a generator at 575V, 10 MW and a 400kV/575V transformer. The generator modelled in Matlab represents a wind farm connected to the GB electrical network in subsystem 1. As in subsystem 1, the simulation also includes the ITM interface and the composition and decomposition of signals. It should be noted at this point that at the moment this paper is written the GPS card of OPAL-RT was newly acquired and not fully integrated yet with the system. As such there was not time delay compensation in subsystem 2.

5. Results

The results presented below show a comparison between a local RTDS simulation that also includes the PQ source and a co-simulation between RTDS and OPAL-RT where the PQ source was distributed to subsystem 2 as a dynamic load. The disconnected load is set to demand 12.5GW of active power and 6GVar of reactive power. The event leads to a Voltage rise from 386kV rms to 388kV rms and a frequency rise from 49.95Hz to 51.3Hz. As expected, this leads to a dip in the current from 23A rms to 22A rms.

It can be observed from ***Figure** 7* and ***Figure** 8* that the rms voltage and frequency signals on both subsystems is identical with the maximum error calculated at ~0.001%.

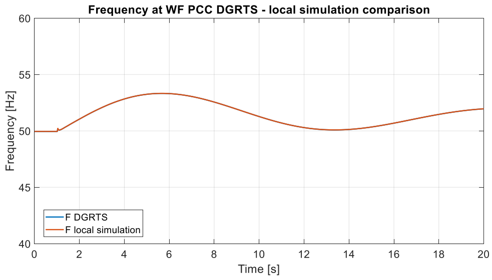

Figure 7. Comparison of frequency signals

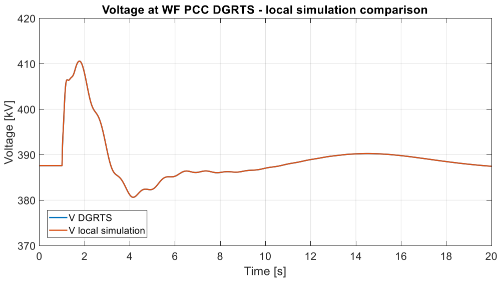

Figure 8. Comparison of rms voltage signals

For current and active power, the profiles of the signals are very closely matching as seen in ***Figure 9*** and ***Figure 10*** thus, proving the accuracy of the co-simulation approach.

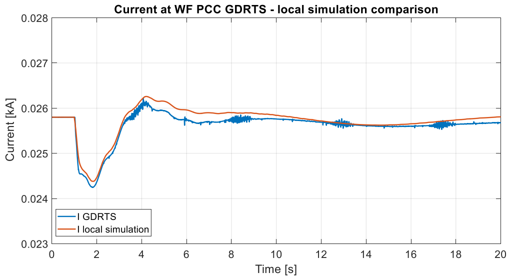

Figure 9. Comparison of rms current signals

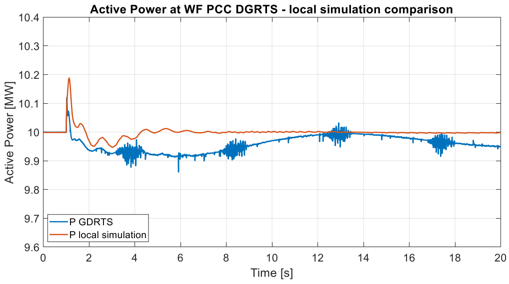

Figure 10. Comparison of active power signals

An additional high frequency disturbance can be observed in the signals of current and power above, every 4.6s. This disturbance is due to the way the time delay is compensated. As was mentioned in sections 3.4. and 3.5. time delay compensation needs to occur on both subsystems for the feed-forward and the feedback loop. In this project, the time delay compensation was applied only on subsystem 2 for the whole round-trip, causing this disturbance on the signals generated in subsystem 1. This approach was chosen as an alternative method after an investigation of the available hardware pointed to an issue with the instigation of the GPS clock and its signal routing.

The effect of the time delay compensation in subsystem 1 can be observed in the next results. At the time that this exercise took place, the round-trip delay of the PNDC-OREC connection was calculated at 16ms. This delay is compensated after receiving the current signals from OPAL-RT and before injecting them into the simulation model. A comparison of the compensated and uncompensated current waveforms is presented in ***Figure 11*** below.

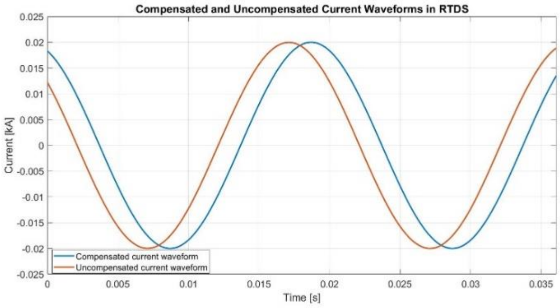

Figure 11. Time-delay compensated and uncompensated current waveform

6. Conclusion And Next Steps

In this paper the real time link between two sites was presented. Measurements and outputs of the one subsystem were replayed at the other subsystem at each simulation time step. In this way the assets at PNDC were combined with those at OREC to create a more representative test environment for a future DUT. Specialized communications blocks were developed within the OPAL-RT and RTDS

environments located in the Power Networks Demonstration Centre (PNDC in Cumbernauld), Dynamic Power Systems Lab (DPSL in Glasgow City Centre), and OREC's drivetrain and eGrid test facilities (Blyth). To validate these blocks, a representative Great Britain Network model is simulated within the PNDC RTDS test environment and a Matlab generator model, representing a wind farm is simulated in the OREC OPAL-RT test environment. The response of this interfaced simulation environment model to a frequency disturbance event and its response in terms of simulation stability and fidelity was presented.
The next immediate steps are the full integration of the GPS clock in OPAL-RT in order to extinguish the frequency disturbance observed in the current waveform. The implementation of a 1GW windfarm in OPAL-RT and of a low frequency event scenario based on the 9th of August 2019 UK Blackout event, ***Figure 12***. This scenario was chosen through stakeholder engagement with industry and is significant for a wide number of stakeholders including the Transmission System Operator, the Distribution Network Operator, Suppliers, and Co/Prosumers.

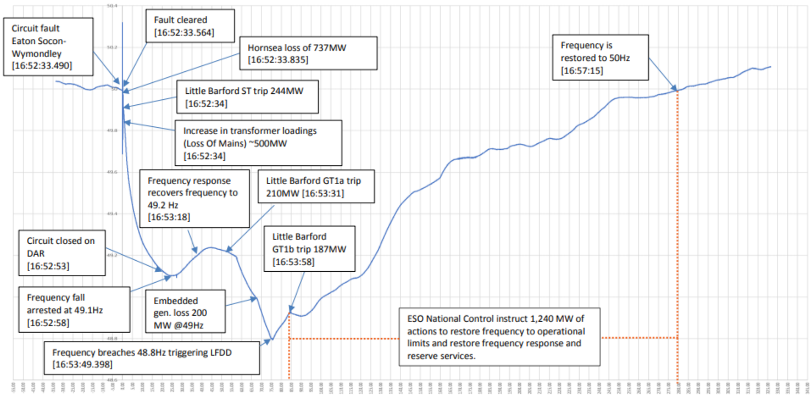

Figure 12. Frequency trace of the 9th of August UK black out event [15]

Finally, the application of PHIL will be utilized as seen in the high-level configuration in ***Figure 13***. This enables the interface of physical, electrical and mechanical assets into the multi-site test system providing a GD-HIL platform for the refinement and optimization of integration control solutions encompassing wind turbines, electrical infrastructure, energy storage, and associated controls. This would maximize the impact of the research carried out and has the potential to become the baseline platform for cooperation regarding future experimental demonstration projects.

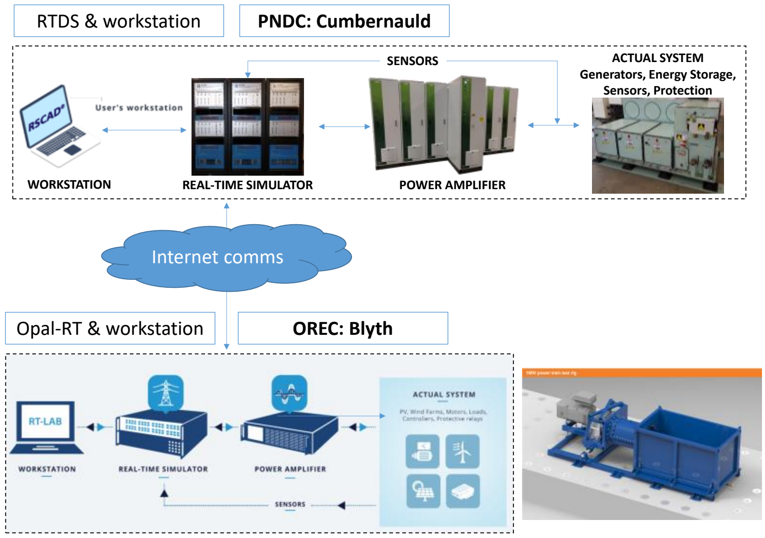

Figure 13. High level GD-HIL configuration for the next phase of the project

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