令　和　二　年　度　　修　士　論　文

CMOS Reference Voltage Generation Circuit and Bipolar Base Current Compensation Techniques

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CMOS Reference Voltage Generation Circuit and Bipolar Base Current Compensation Techniques

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Abstract

There are two parts in this paper. The first part describes a CMOS reference voltage generation circuit. By utilizing the temperature characteristic of the diode-connected NMOS, which the gate-source voltage has a positive temperature coefficient under the condition of large current flowing through the drain source, whereas it has a negative temperature coefficient under the condition of small current flowing through the drain source，a reference voltage insensitive to temperature can be generated. This reference voltage changes only 0.0045v from temperature -20℃ to 120℃. The second part proposes two kinds of the base current compensation techniques used for bipolar analog circuits. One is for current mirror circuit where we combine the base current compensation technique with the cascode and level-shift configuration. Not only the deviation between the input current and the output current is reduced but also the circuit has a lower output voltage that can maintain the output current stable. The other one is used in the bipolar differential amplifier circuit with wilson active load, so that the differential amplifier has high input impedance and high gain.

First Part: CMOS Reference Voltage Generation Circuit

1 Introduction

1.1 Background

The reference voltage source is an indispensable basic module in analog circuits such as A/D, D/A converters, phase-locked loops, linear regulators, and temperature sensors. It provides a known stable reference voltage for the system. This stable voltage is used to compare with the collected signal as a standard value, which can accurately quantify any signal. The reference voltage determines the performance of these circuits.

At present, the most commonly used reference voltage source is the bandgap reference voltage circuit. In bandgap reference voltage circuit, the base-emitter voltage of single bipolar transistor (V_{BE}) has a negative temperature characteristic as shown in Fig. 1.1.1. while under the different current density biases, the difference of base-emitter voltages (ΔV_{BE}) between two bipolar transistors has a positive temperature coefficient characteristic as shown in Fig. 1.1.2. Then, these two voltages (V_{BE} and ΔV_{BE}) are linearly added with a certain weight to obtain a reference voltage with a low temperature coefficient. The Fig. 1.1.3 shows the basic bandgap reference voltage generation circuit [3].

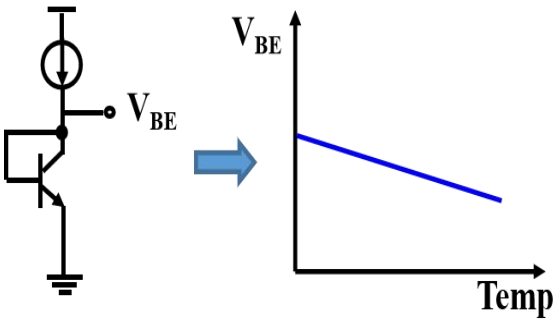


Fig. 1.1.1 CTAT: Decrease of base-emitter voltage for temperature increase.

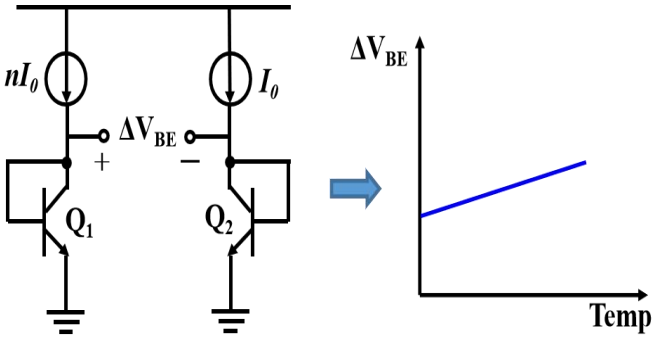


Fig. 1.1.2 PTAT: Increase of base-emitter voltage for temperature increase.

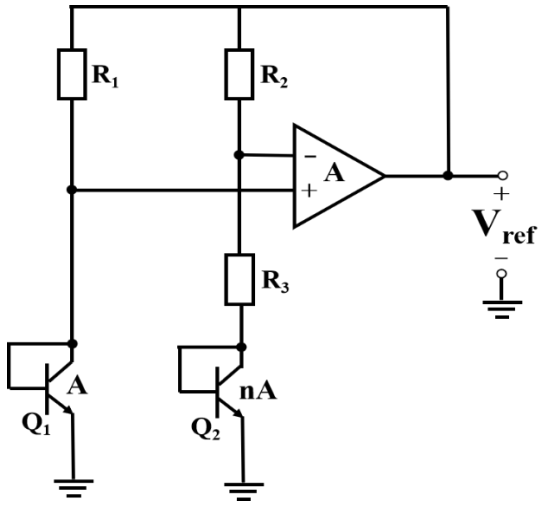


Fig. 1.1.3 Basic bandgap reference voltage generation circuit

While, as the feature size of integrated circuits is getting smaller in recent years, in some cases, the reference voltage circuit needs to be simplified which consists of only standard MOSFETs (without parasitic BJTs). At the same time, it can also operate even in harsh environments such as a wide temperature range. So in this part, we use only NMOSs to generate PTAT voltage and CTAT voltage and generate a reference voltage with a simple NMOS circuit [1].

1.2 Abstract

Chapter 2 introduces the temperature characteristics of NMOSs. Chapter 3 presents the specific reference voltage generation circuit. Chapter 4 shows the LTspice simulation results, and Chapter 5 gives a summary about the reference voltage generation circuit and proposes the future works.

2. Temperature Characteristics of MOSFETs

2.1 Drain-gate connected NMOSFET

Firstly, we show the temperature characteristics of MOSFET.

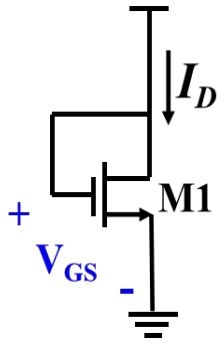


Fig. 1.2.1 the drain-gate connected NMOSFET

Fig. 1.2.1 shows the schematic of the drain-gate connected NMOSFET. The NMOS is always in the saturation region and the drain current I_D is given by the following [2]：

$$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_{th})^2 \cdots\cdots\cdots (2.1)$$

Based on Eq. 2.1, we can get the V_{GS} equation as follows：

$$V_{GS} = \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} + V_{th} \cdots\cdots\cdots\cdots (2.2)$$

(W/L：channel width/length, C_{ox}：gate oxide film capacitance per unit area, V_{th}：threshold voltage, μ：mobility of NMOS). In Eq.2.2, there are two quantities affected by temperature. One is the mobility of NMOS (μ), which is given as follows：

$$\mu = \mu_0(T/T_0)^{-1.5} \cdots\cdots\cdots\cdots (2.3)$$

μ_0 is the mobility at T_0 ($=273.1K$), whereas μ is the one at T. we can see μ has a negative temperature coefficient. The other one is the threshold voltage V_{th}, which can be expressed as follows：

$$V_{th} = \frac{\sqrt{2eN_A\varepsilon_{Si}(2\phi_B)}}{C_{ox}} + 2\phi_B + V_{FB} \cdots\cdots (2.4)$$

$$\frac{dV_{th}}{dT} = \frac{d\phi_B}{dT}\left(\frac{1}{C_{ox}}\sqrt{\frac{eN_A\varepsilon_{Si}}{\phi_B}} + 2\right) \cdots\cdots\cdots (2.5)$$

ϕ_B is the built-in potential, and n_i is the intrinsic carrier density of the NMOSFET.

$$\phi_B = \frac{K_BT}{e}\ln\left(\frac{N_A}{n_i}\right) \cdots\cdots\cdots\cdots (2.6)$$

$$n_i = Nexp\left(-\frac{\varepsilon_g}{2k_BT}\right) \cdots\cdots\cdots (2.7)$$

Substitute (2.7) for (2.6). Then (2.8) is obtained.

$$\frac{dV_{th}}{dT} = -1 \sim -3 \ [\text{mV/°C}] \cdots\cdots\cdots (2.8)$$

V_{th} also has a negative temperature coefficient. So in Eq.2.2, when the temperature

becomes high, the value of $\sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}}$ becomes lager while the V_{th} becomes smaller. It seems to be difficult to judge how V_{GS} changes with temperature.

However, we can intuitively see that V_{GS} has opposite temperature characteristic under flowing through different drain currents in the I_D-V_{GS} characteristic curve as shown in Fig. 1.2.2. The gate voltage has a temperature insensitive characteristic point as shown at the current point I_p. In case that the drain current is larger than I_p, the gate voltage increases as the temperature becomes high, whereas in case the drain current is smaller than I_p, the gate voltage decreases. Even if the current is so small that the drain-gate connected NMOS is located in the subthreshold region, the V_{GS} still has a negative temperature characteristic.

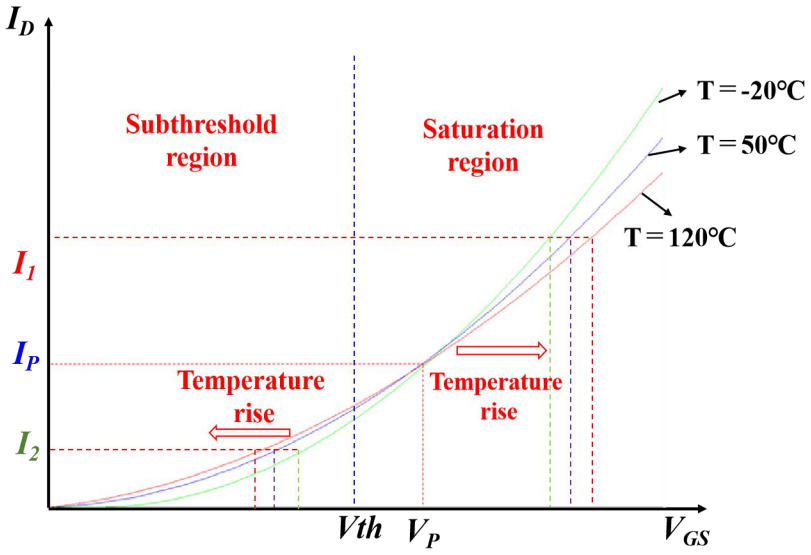


Fig. 1.2.2 I_D-V_{GS} characteristics of Fig 2.1

2.2 PTAT and CTAT

Based on the characteristics, we can generate a simple reference voltages sensitive to temperature as shown in Fig. 1.2.3 and Fig. 1.2.4. In Fig. 1.2.3, as the temperature rises, the gate-source voltage of the diode connected MOSFET increases for the current through NMOS is larger than Ip, whereas in Fig. 1.2.4, the gate-source voltage of the diode connected NMOS decreases for the current through NMOS is smaller than I_p.

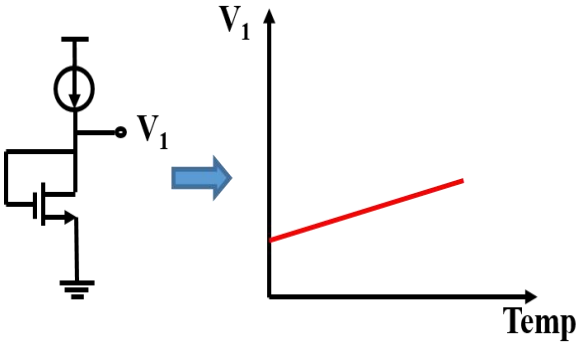


Fig. 1.2.3 PTAT: Increase of gate-source voltage(I_1>I_p) for temperature increase.

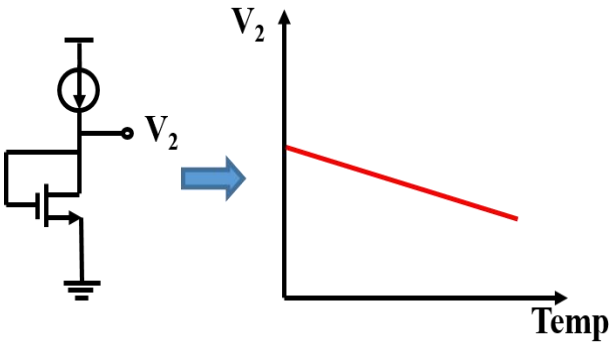
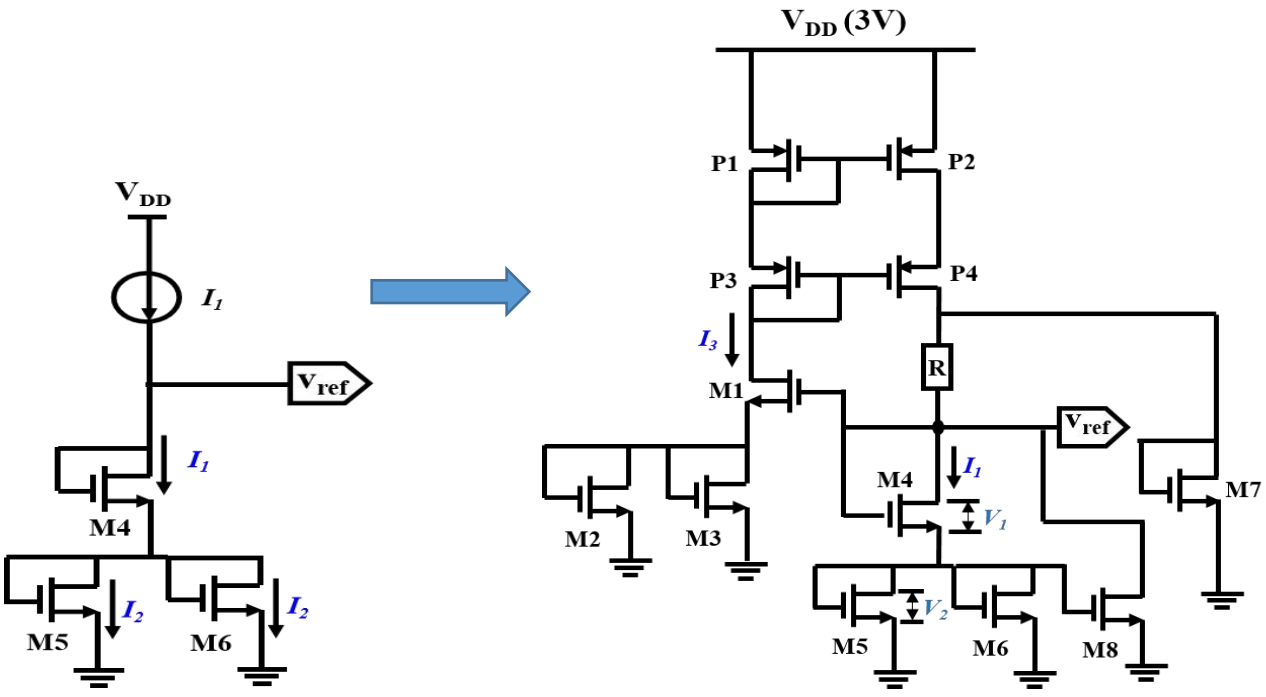


Fig. 1.2.4 CTAT: Decrease of gate-source voltage(I_2 < I_p) for temperature increase.

3. Proposed Reference Voltage Generation Circuit

Fig 1.3.1(a) shows our proposed reference voltage generation circuit, where M4 is connected to M5 and M6 in series (where a start-up circuit is not included for simplicity). Since the channel width of M5 is equal to that of M6, I_1 is twice larger than I_2. Large current (I_1) flows through M4 while small current (I_2) flows through M5, M6. Then two different gate-source voltages are added so that their temperature characteristics are canceled and the total output voltage V_{ref} can be insensitive to temperature.



(a) (b)

Fig. 1.3.1 Proposed reference voltage generation circuit.

For the circuit in Fig. 1.3.1 (a), the current source should also be fairly insensitive to the temperature so that it can generate a constant current through NMOS. Therefore, we utilize P1, P2, P3, P4, M1, M2, M3 to compose a constant current source as shown in Fig. 1.3.1 (b). This circuit looks like a current mirror. The current in the left part (I_3) has the same temperature characteristic with the current in the right part (I_1) as shown in Fig. 1.3.2 and Fig. 1.3.3. In the left part in Fig. 1.3.1 (b), M2 and M3 are used to adjust the value of the input current. M4, M5, M6 are designed to compensate for the temperature sensitivity of V_{ref}. Although the current I_1 is not constant completely over temperature variation, the gate-source voltages of M4 and M6 also follow the temperature characteristics in Fig. 1.2.3 and Fig. 1.2.4, as shown in Fig. 1.3.4 and Fig. 1.3.5.

Besides, M7 and M8 are used to suppress the variation of V_{ref} from the supply voltage V_{DD} changes. As V_{DD} increases, I_3 tends to increase; this is mirrored to P2, P4, but also the drain current increases of M7, M8 can suppress the increase of I_1. Drain current variations of M7,M8 are compensated each other for temperature change.

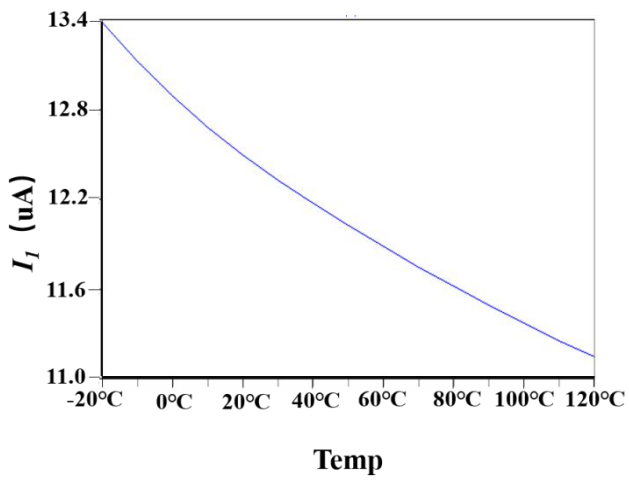


Fig. 1.3.2 Current I_1 in Fig 1.3.1 (b).

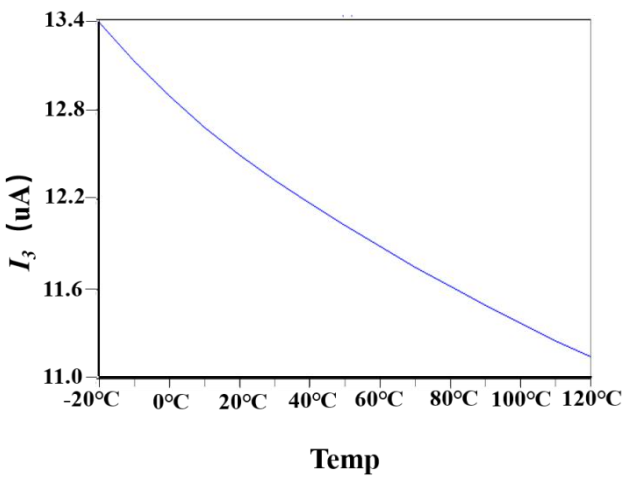


Fig. 1.3.3 Current I_3 in Fig 1.3.1 (b).

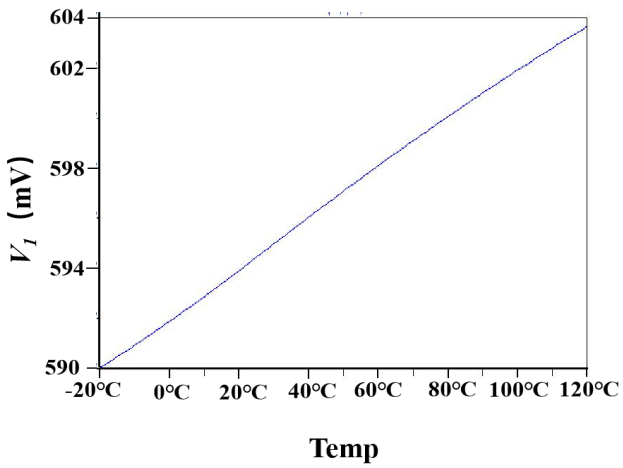


Fig. 1.3.4 Gate-source voltage of M4 in Fig 1.3.1(b).

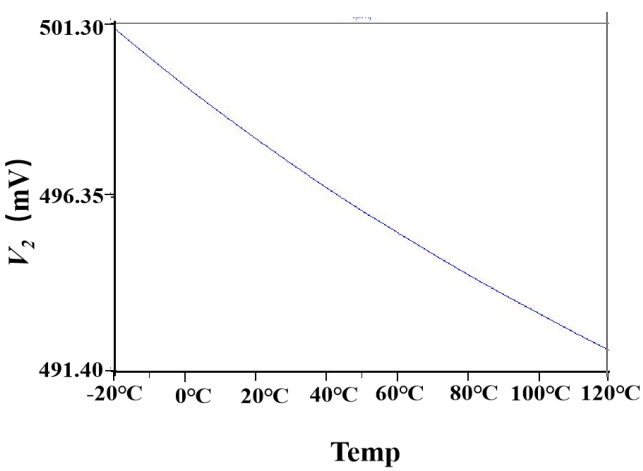


Fig. 1.3.5 Gate-source voltage of M5 in Fig 1.3.1(b).

4. Parameter and Simulation Result

Fig. 1.4.1 shows SPICE simulation results with conditions in Table 1. The reference voltage deviation is within ±0.5% at maximum as shown in Table 2, from temperature -20℃ to 120℃, as a reference of temperature 20℃, for the supply voltage of 3V. We see that the circuit in Fig. 1.3.1 (b) generates a reference voltage that is well insensitive to temperature with a simple configuration.

TABLE 1. SIMULATION CONDITIONS FOR THE CIRCUIT IN FIG 1.3.1 (B)

Parameter	Value(μm)	Parameter	Value(μm)
P1、P3	W=10, L=2	M5、M6	W=5, L=2
P2、P4	W=25, L=2	M7	W=20, L=2
M1、M4	W=7, L=2	M8	W=18, L=2
M2、M3	W=5, L=2	R	3kΩ

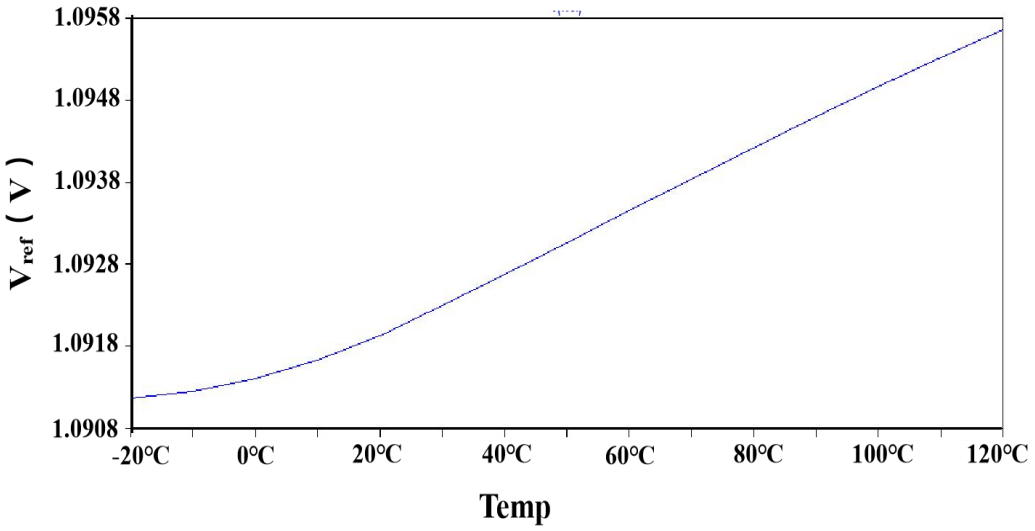


Fig. 1.4.1 SPICE simulation of the circuit in Fig. 1.3.1 (b).

TABLE 2. GENERATED REFERENCE VOLTAGE FOR VARIOUS TEMPERATURE WITH SUPPLY VOLTAGE OF 3V

Temperature(°C)	Value(V)	Difference from 20°C (%)
-20	1.09118	-0.0678
0	1.09141	-0.0678
20	1.09192	0.0
50	1.09308	0.1062
80	1.09422	0.2106
120	1.09567	0.3434

5. Summary

In this part, we have focused on the temperature characteristics of MOS voltage in different cases of the drain currents. We have proposed the simple reference voltage generation circuit insensitive to the temperature using several MOSFETs. We show their circuit configurations and their effectiveness with SPICE simulation. As a next step, we will focus on this circuit in more details, as well as supply voltage variation effects to the circuit.

6. References

[1] I. Lee, D. Blaauw, "A 31 pW-to-113nW Hybrid BJT and CMOS Voltage

Reference with 3.6% ±3δ-inaccuracy from 0℃ to 170℃ for Low-Power High-Temperature IoT Systems”, VLSI Circuit Symposium, Kyoto (June 2019).

[2] T. Ida, N. Tsukiji, Y. Shibasaki A. Kuwana, H. Kobayashi, “MOS Reference Current Source Insensitive to Temperature Variation”, International Conference on Mechanical, Electrical and Medical Intelligent System (ICMEMIS), Kiryu, Japan (Nov. 2018).

[3] B. Razavi, "The Bandgap Reference", IEEE Solid-State Circuits Magazine (Summer 2016).

[4] L. Sha, A. Kuwana, M. Horiguchi, H. Kobayashi, "Simple Reference Voltage Generation Circuit Insensitive to Temperature", International SoC Design Conference (ISOCC), Yeosu, Korea (Oct. 2020)

[5] Baker R. J, "CMOS Circuit Design, Layout, and Simulation”, Revised Second Edition[M]. IEEE Press, 2007.

Second Part：Bipolar Base Current Compensation Techniques

1. Introduction

1.1 Background

Basic modules such as current mirror, reference voltage source, and differential amplifier constitute various complex and high-performance analog circuits. As the development and popularization of portable electronics and micro-electronic products, the semiconductor process size is becoming smaller, higher requirements have been proposed in allusion to these basic modules for the low supply voltage, low power consumption and high performance and accuracy.

This part investigates two kinds of the base current compensation techniques used for bipolar analog circuits. The first one is for current mirror circuit where we combine the base current compensation technique with the cascode and level-shift configuration. The second one is for the input stage of the differential amplifier circuit with high input impedance and cascode configuration utilizing active load. The SPICE simulation results demonstrate the effectiveness of the proposed circuit techniques.

In addition, most of circuits in this part are based on bipolar transistor. Because until now, bipolar analog circuits are still used in industry, such as for monolithic operational amplifiers and comparators as shown in Fig. 2.1.1 and Fig. 2.1.2, thanks to their low 1/f noise characteristics and low input offset voltage. Also even in pure CMOS LSIs, parasitic bipolar transistors are used for bandgap reference circuits; the authors believe that studying the bipolar circuit techniques are useful for realizing competitive ICs [1-6].

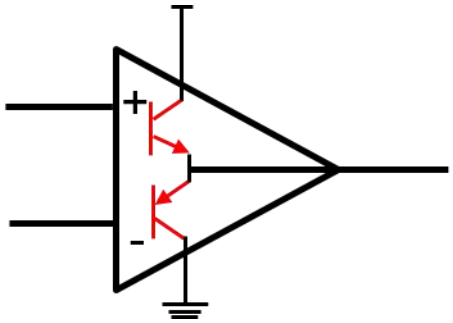


Fig 2.1.1 Bipolar transistor amplifier.

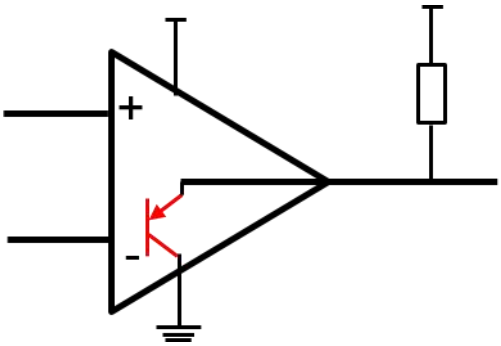


Fig 2.1.2 Bipolar transistor comparator.

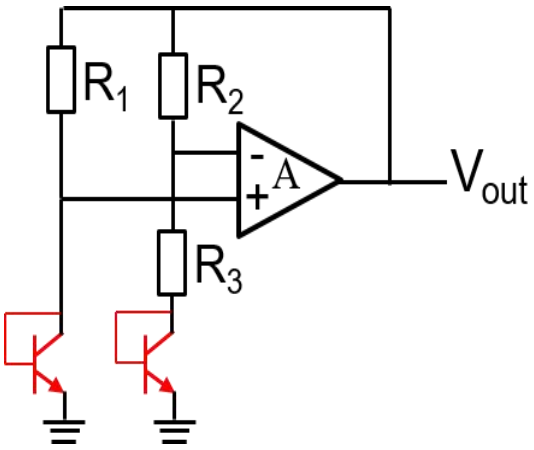


Fig 2.1.3 Bandgap reference circuit with parasitic bipolar transistors

1.2 Abstact

Chapter 2 introduces one of the base current compensation techniques used in basic current mirror circuit and cascode current mirror circuit; Chapter 3 introduces another one used in bipolar differential amplifiers; Chapter 4 presents the base current compensation technique applied in a curvature compensation circuit of the bandgap reference voltage circuit； Chapter 5 gives a summary of this part.

2. Bipolar Current Mirrors with Base Current Compensation

2.1 Basic Bipolar Transistor Current Mirror Circuit

Current mirrors are basic blocks of analog circuit design. They can copy the current multiplied by a coefficient by choosing an appropriate channel width ratio. As shown in Fig. 2.2.1, there can be several output branches when the current steering DAC is designed, and they have the same base current $\frac{Io}{\beta}$. The deviation between the input and output currents is $\frac{(N+1)\,Io}{\beta}$, due to the base currents. Here, β is the current gain of the bipolar transistor, and throughout this paper, N=16 is used for simulation. We consider to compensate for the base current so that the input and output currents are almost the same.

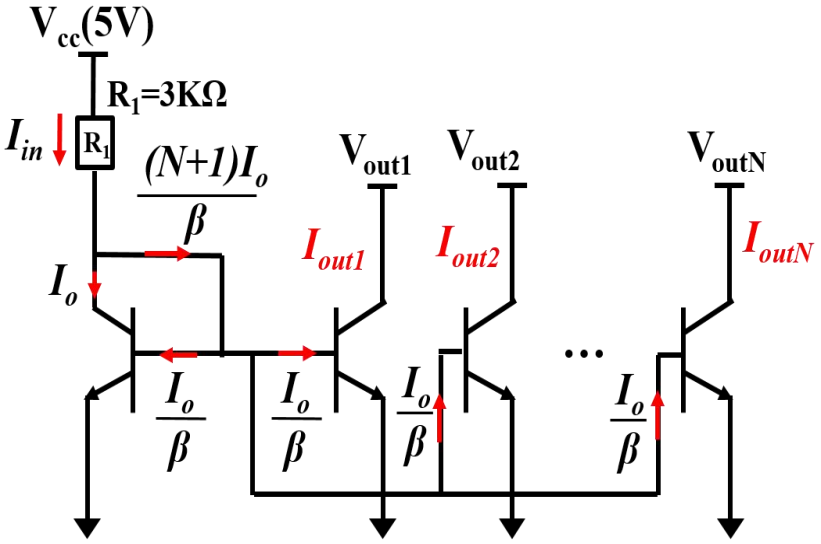


Fig 2.2.1 Basic bipolar transistor current mirror

2.2 Bipolar Transistor Current Mirrors Circuit with Base Current Compensation

To improve the input and output current deviation due to the finite base current, the current mirror circuit with the base current compensation is often used, as shown in Fig. 2.2.2. The deviation between the input and output currents in this circuit is only the base current of Q1. Since the base current of every output branch is $\frac{Io}{\beta}$, the emitter current of Q1 is $(N+1)*\frac{Io}{\beta}$. Thus, the base current of Q1 is $\frac{(N+1)\ Io}{\beta(1+\beta)}$. Compared with the deviation in the basic current mirror in Fig. 2.2.1, the deviation in this circuit is reduced by $\frac{1}{1+\beta}$.

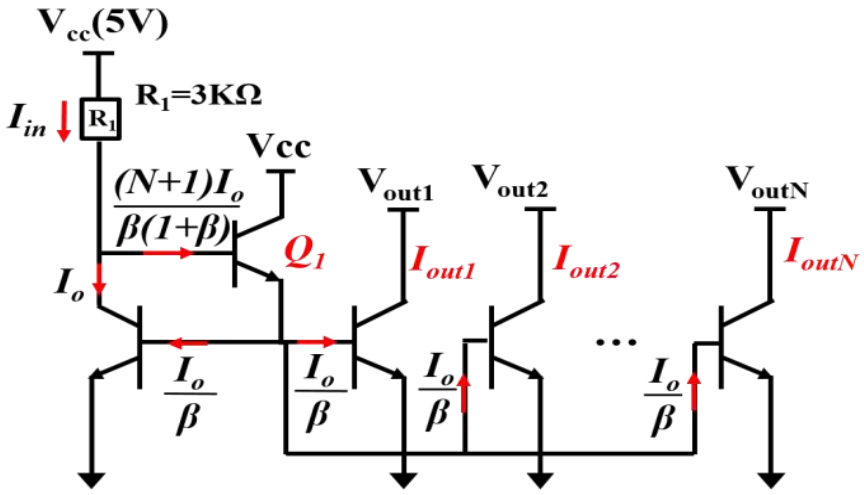
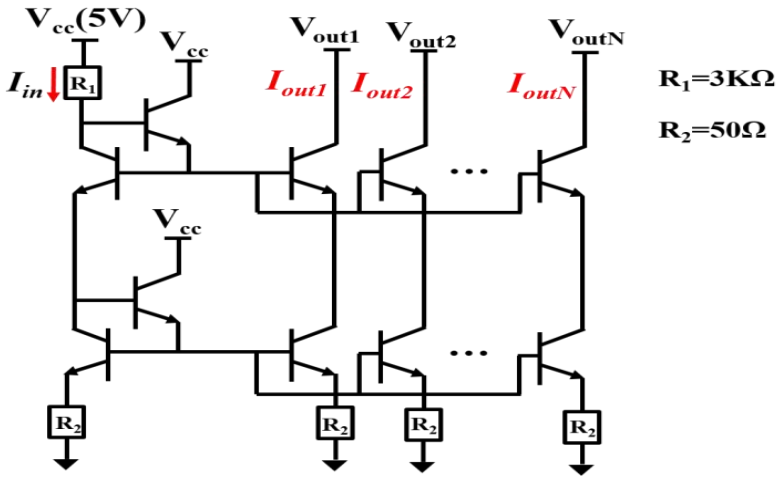


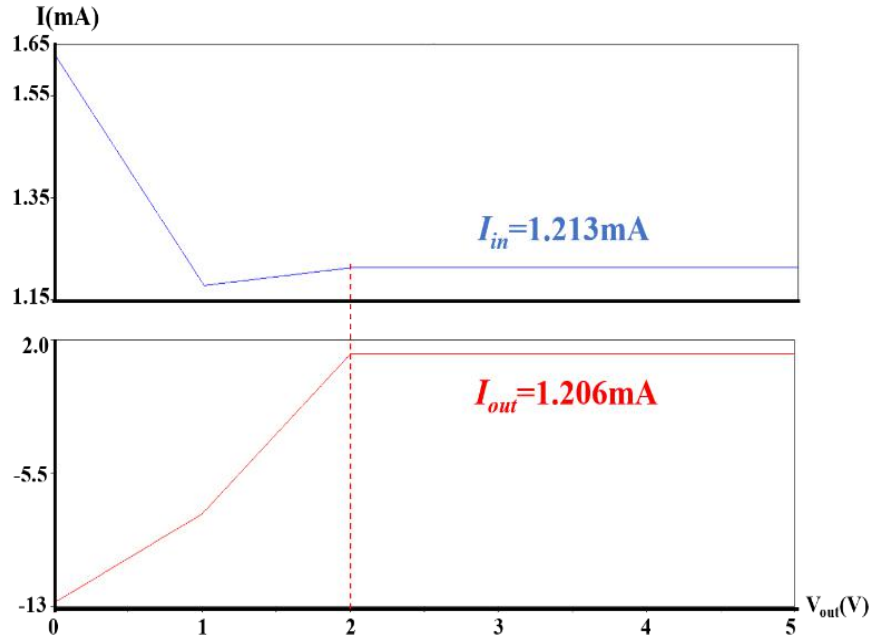
Fig. 2.2.2 Current mirror with the base current compensation circuit.

2.3 Bipolar Transistor Current Mirror Circuits with Cascode and Base Current Compensation Configuration

Because of the Early effect in bipolar transistor, there can be some deviation between the input and output currents in the basic bipolar transistor current mirror circuit in Fig. 2.2.1. We consider here the base current compensation configuration in the cascode current mirror circuit as shown in Fig. 3 (a). Fig. 3 (b) shows its simulation result of the input current (I_{in}) and the output current (I_{out}). We can see that I_{out} is fairly close to I_{in} in the saturation state. However, the output current in this circuit cannot maintain a constant value when the output voltage is lower than 2V; the output voltage provided by the external load has to be smaller than 2V.



(a) Circuit schematic.



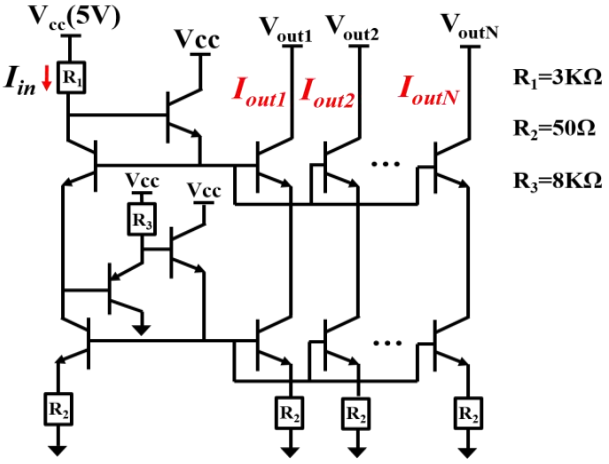
(b) Simulation result.

Fig. 2.2.3 Current mirror circuit with

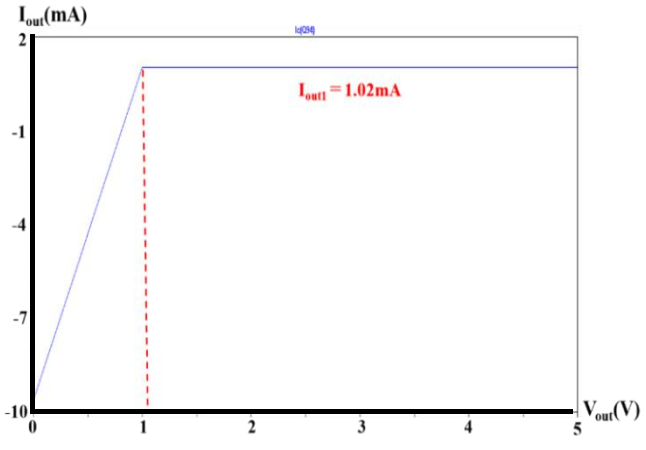
the cascode and base current compensation configuration.

2.4 Bipolar Mirror Circuits with Cascode, Level-Shift and Base Current Compensation Configuration

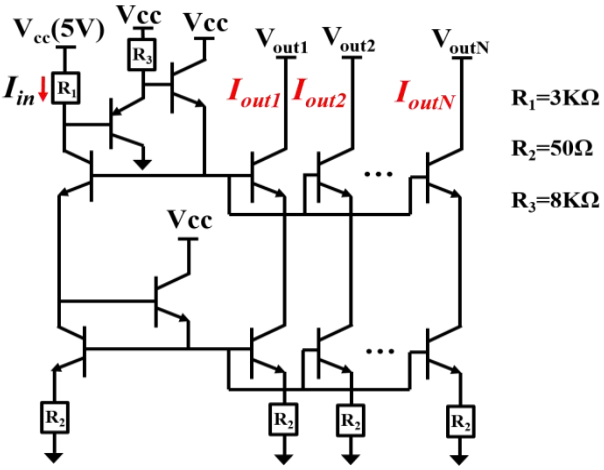
For the problem previously mentioned, we add a PNP transistor and a resistor (PNP emitter follower circuit) into the current compensation configuration to form a level-shift configuration as well as further base current compensation, similar to the Darlington configuration (Figs. 2.2.4 (a), (c), (e)). There the level-shift by the base-emitter voltage of the NPN transistor is cancelled by that of the PNP.



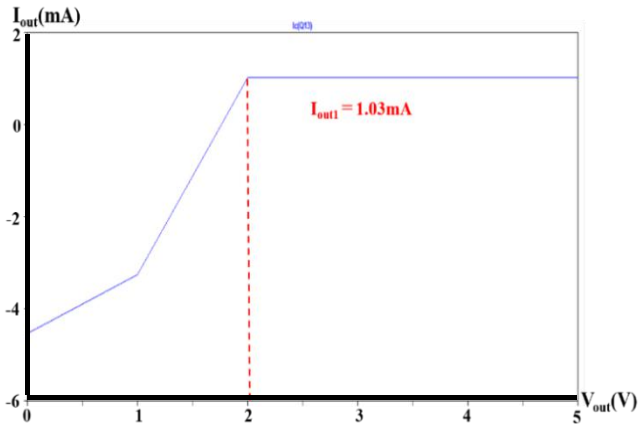
(a) Circuit schematic.



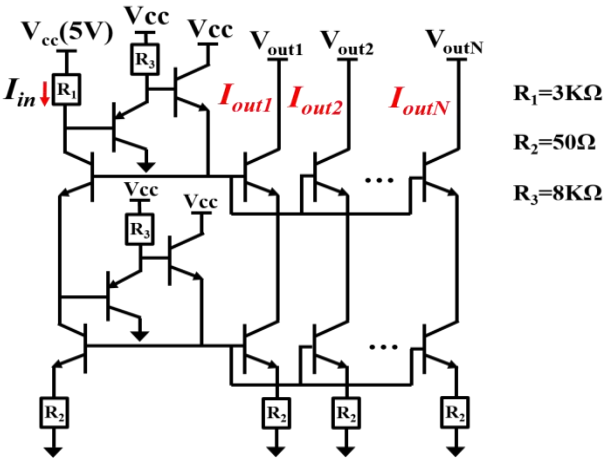
(b) Simulation result.



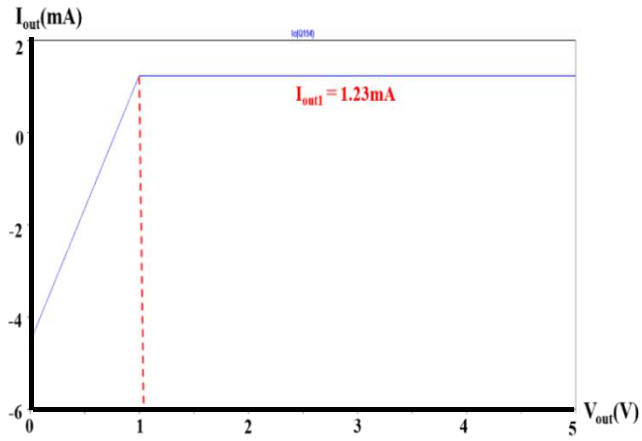
(c) Circuit schematic.



(d) Simulation result.



(e) Circuit schematic.



(f) Simulation result.

Fig. 2.2.4 Current mirror circuit with the cascode, level-shift and base current compensation configuration.

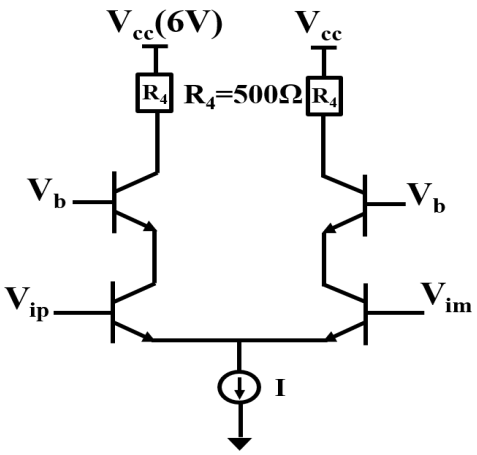
Their output current I_{out} simulation results are shown in Figs. 2.2.4 (b), (d), (f). Compared with the circuit in Fig. 2.2.4 (c), the circuits in Figs. 2.2.4 (a), (e) can operate with a lower output voltage (as low as 1V) that can maintain the output current constant. The circuit in Fig. 2.2.4 (e) has the further smaller deviation between the input and output currents compared with the circuit in Fig. 2.2.4 (a).

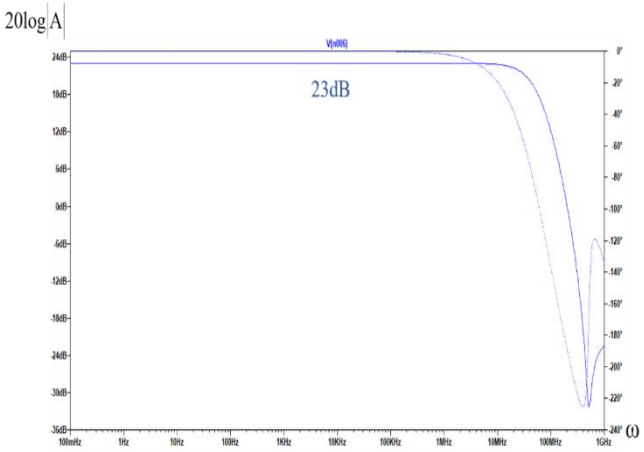
3. Bipolar Differential Amplifier with Base Current Compensation

The base current compensation technique can be also used in the differential amplifier for high input impedance.

3.1 Basic Bipolar Differential Amplifier with Resistor Load

Fig 2.3.1 shows a basic bipolar differential amplifier whose voltage gain is 23dB.



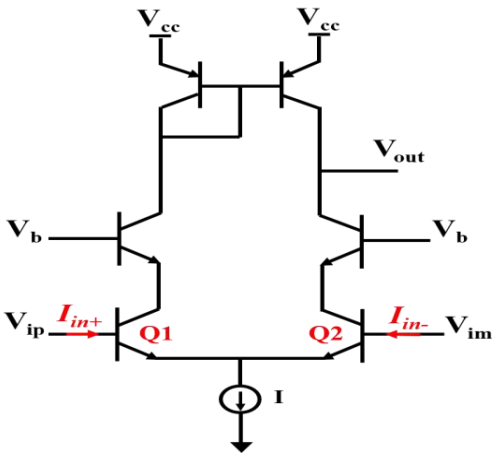


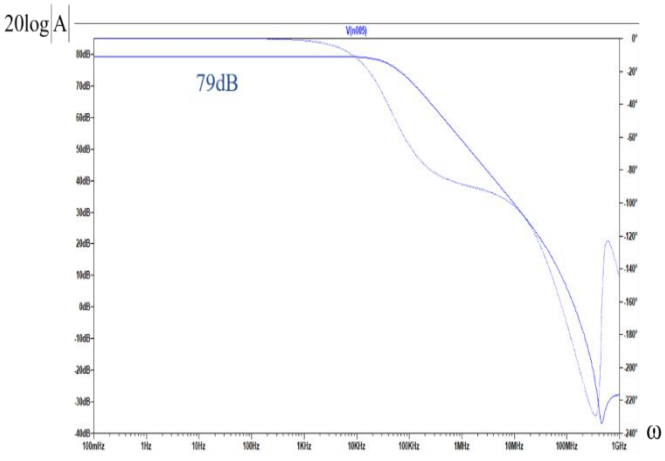
(a) Schematic. (b) Simulation result.

Fig. 2.3.1. Differential amplifier with resistor load.

3.2 Basic Bipolar Differential Amplifier with Active Load

In the circuit of Fig. 2.3.2(a), we replace the resistor load with a simple active load, and the gain of the amplifier has been increased (Fig. 2.3.2 (b)).



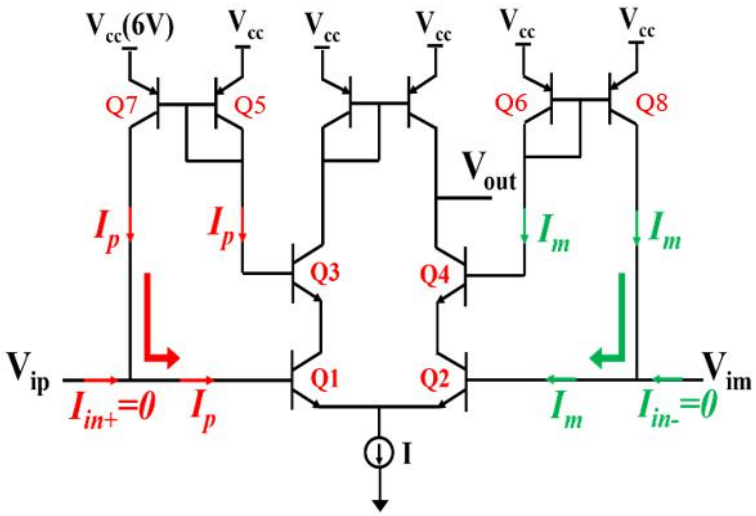


(a) Circuit schematic. (b) Simulation result.

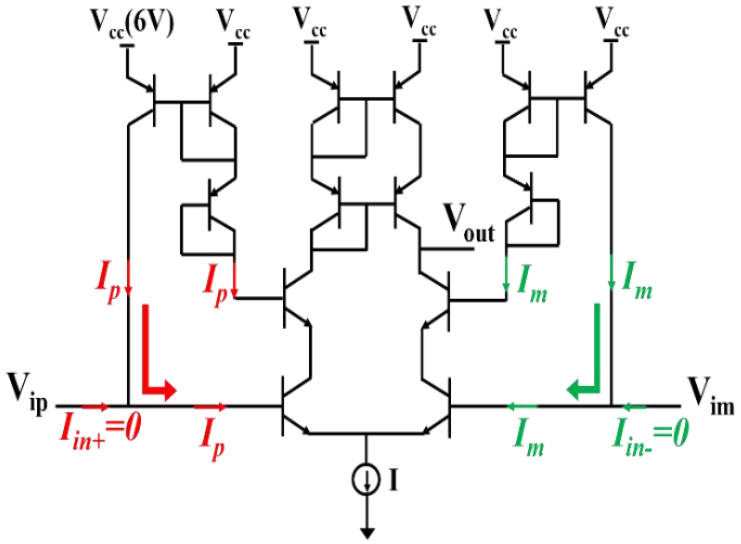
Fig. 2.3.2 Differential amplifier with simple active load.

3.3 Bipolar Differential Amplifier with Base Current Compensation and Active Load

In order to obtain the high input impedance, we use the base current compensation technique to make the input current I_{in+} and I_{in-} as small as possible. In Fig. 2.3.3(a), we connect two current mirrors (Q5, Q7) and (Q6, Q8) to the bases of Q1 and Q2 respectively. Since the current in the left part of the current mirror (Q5, Q7) is equal to the current in the right part and the base current of Q1 is equal to the base current of Q3, the input current I_{in} is very small. More specifically, compared with I_{in+} in Fig. 2.3.2(a), I_{in+} in Fig. 2.3.3(a) reduces to 1/24. The current mirror (Q6, Q8) and I_{in-} are in the same situation as the current mirror (Q5, Q7) and I_{in+}. Consequently, this amplifier has high input impedance. To improve the gain of the differential amplifier, we replace the simple active load with the cascode active load as shown in Fig 2.3.3(b).



(a) Simple active load.

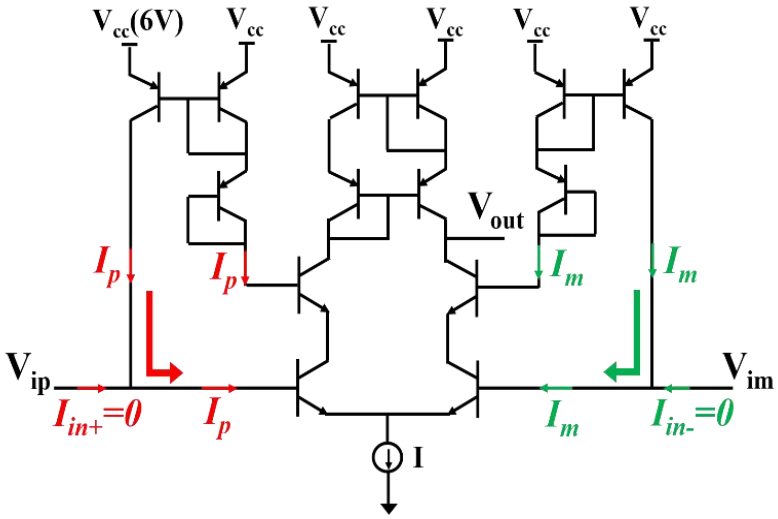


(b) Cascode active load.

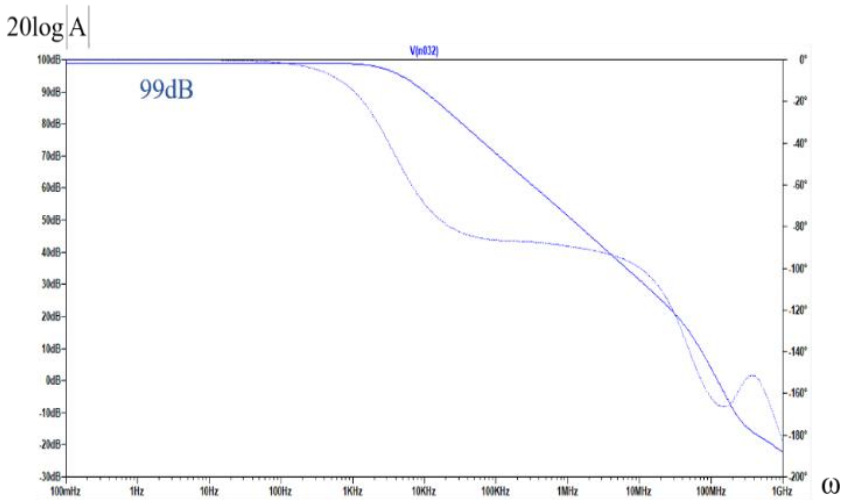
Fig. 2.3.3 Differential amplifier with base current compensation and simple active load.

3.4 Bipolar Differential Amplifier with Base Current Compensation and Wilson Active Load

In this subsection, we investigate the usage of the Wilson active load, which balances the base current effects of the active load right and left parts. We see from Fig. 2.3.4 (a), (b) that the differential amplifier with the Wilson active load has a high voltage gain, though the second pole effects have to be considered. At the same time, the input currents (I_{in+}, I_{in-}) is almost equal to 0.



(a) Circuit schematic.



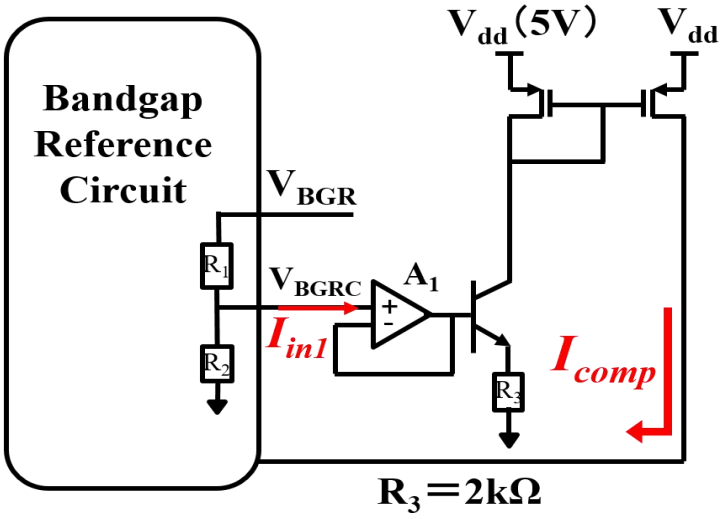
(b) Simulation result.

Fig. 2.3.4 Differential amplifier with the base current compensation and the Wilson active load.

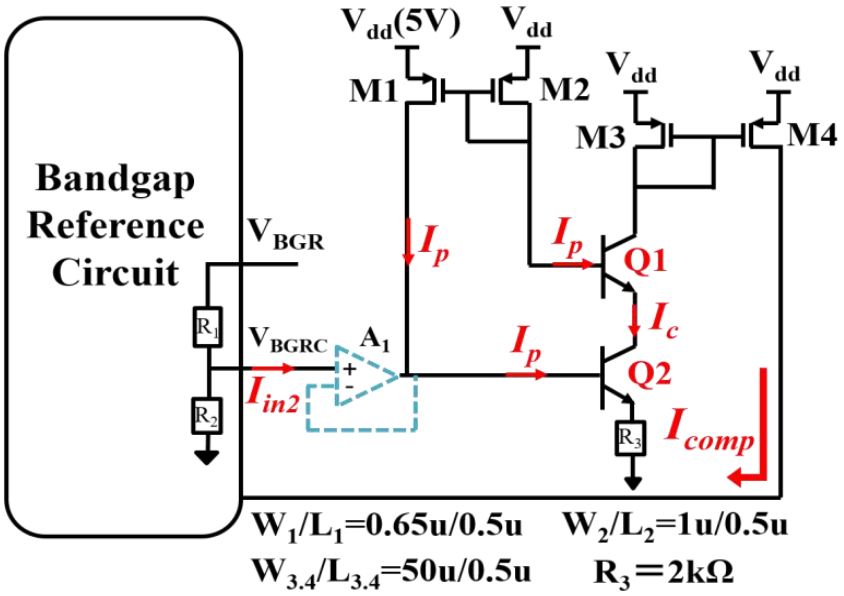
4. Curvature Compensation Circuit in Bandgap Reference Circuit with Base Current Compensation

Fig. 2.4.1 (a) shows a bandgap reference circuit with curvature compensation circuit [5]. The curvature compensation circuit is in the right part and it effectively improves the total temperature characteristics of the output voltage. However, the current flowing from the bandgap reference circuit to curvature compensation circuit will induce the inaccuracy of V_{BGR}, so that a voltage follower circuit is used; however, it consumes some extra power.

Utilizing the base current compensation technique in this curvature compensation circuit can solve this problem as shown in Fig. 2.4.1 (b), by regulating the sizes of M1, M2, M3, M4 to make the base current of Q1 equal to the base current of Q2. Because of the current mirror, the base current of Q1 is also equal to the Ids of M1. Therefore, compared with Iin1 in Fig. 2.4.1 (a), I_{in2} in (b) can reduce to 2nA. Then the curvature compensation circuit has a high input impedance; in this case, the voltage follower A1 is not required. The V_{BGR} has a reliable and simple curvature compensation circuit.



(a) Curvature compensation circuit with base current.



(b) Curvature compensation circuit with base current compensation.

Fig. 2.4.1 Curvature compensation current in bandgap reference circuit with base current compensation.

5. Summary

In this paper, we have introduced two base current compensation techniques used in bipolar transistor current mirror circuit and in bipolar differential amplifier circuit

respectively.

In current mirror circuit, we combine the base current compensation technique with PNP level-shift configuration in the cascode current mirror circuit; not only the deviation between the input current and the output current is reduced but also the circuit has a lower output voltage that can maintain the output current stable. This is suitable for low supply voltage operation with high output impedance current mirror.

Furthermore, we have investigated a bipolar differential amplifier circuit with base current compensation and Wilson active load, which has high input impedance and high gain. This is suitable as low power sensor interface circuit in the IoT system. Notice that this circuit needs to consider the values of β and Early voltage of the PNP transistors as well as the matching accuracy of pair PNP transistors, for mass production. In many bipolar processes, PNP transistor characteristics are not taken care of sufficiently, compared to NPN ones.

Lastly, we have demonstrated a curvature compensation circuit with the base current compensation that can provide a dependable and simple curvature compensation to the bandgap reference circuit.

Acknowledgements

The authors would like to thanks Mr. Hiroki Sonoda and Mr. Koichi Yamazaki of Renesas Electronics Corp. for his valuable comments about bipolar ICs in industry today.

6. References

[1] Paul R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons Inc. (2009).

[2] A. B. Grebene, “Bipolar and MOS Analog Integrated Circuit Design”, Wiley-Interscience (1984).

[3] L. Meifang, L. Shibin, “Improved EF-Augmented Current Mirror”, Electronic Measurement Technology (2007).

[4] W. D. Llewellyn, “NPN Transistor Current Mirror Circuit”, US Patents, Patent Number 4,546,307 (Oct.8, 1985). https://www.freepatentsonline.com/4546307.pdf

[5] S. Sano, Y. Takahashi, M. Horiguchi, M. Ota, “A sub-1V 3.9 μW Bandgap Reference with a 3σ Inaccuracy of ± 0.34% from −50◦C to +150◦C using

Piecewise-Linear-Current Curvature Compensation", Proc. VLSI Circuits Symposium, Kyoto (Jun. 2012).

[6] D. Johns, K. Martin, "Analog integrated circuit design[J]". analog integrated circuit design, 1997, 9(1-2):343 - 349.

Conclusion

In this paper, we have proposed the simple reference voltage generation circuit insensitive to the temperature using several MOSFETs. When the environment temperature changes from -20℃ to 120℃, the reference voltage only varies 0.0045v. In the future, we will focus on this circuit in more details, as well as supply voltage variation effects to the circuit.

Moreover, we have proposed two kinds of the base current compensation techniques used for bipolar current mirror circuits and bipolar differential amplifiers. The performance of these bipolar circuits have been effectively improved because of the base current compensation techniques.

List of Published Papers

[1] **Lei Sha**, Anna Kuwana, Masashi Horiguchi, Haruo Kobayashi, "Simple Reference Voltage Generation Circuit Insensitive to Temperature", 17th International SOC Design Conference, Yeosu, Korea (Oct. 21-24, 2020)

[2] **Lei Sha**, Minh Tri Tran, Anna Kuwana, Haruo Kobayashi, "Revisit to Bipolar Analog Circuits: Two Base Current Compensation Techniques", 4th International Conference on Technology and Social Science, Kiryu, Japan, (Dec. 2-4, 2020)

[3] **Lei Sha**, Anna Kuwana, Haruo Kobayashi (Gunma Univ.). "Reference Voltage Generation Circuit Insensitive to Temperature", 5th Taiwan and Japan Conference on Circuits and Systems (TJCAS 2019 at Nikko) , Nikko, Tochigi, Japan, August 19-21, 2019

[4] Jianglin Wei, Nene Kushita, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, Hirotaka Arai, **Lei Sha**, Anna Kuwana, Takayuki Nakatani, Kazumi Hatayama, Haruo Kobayashi "Short-Time INL Testing Methodology for High-Resolution ΔΣ ADC",Journal of Mechanical and Electrical Intelligent System (JMEIS, J. Mech. Elect. Intel. Syst.). vol. 3, no. 2, pp.87-101 (May 2020).

[5] Takashi Hosono, **Lei Sha**, Souma Yamamoto, Mayu Hirano, Takashi Ida, Anna Kuwana, Haruo Kobayashi, Yoichi Moroshima, Hiromichi Harakawa, Takeshi Oikawa, "Improved Nagata Current Source Insensitive to Temperature and Power Supply Voltage", 17th International SOC Design Conference, Yeosu, Korea (Oct. 21-24, 2020)

[6] Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa (Rohm Semiconductor), Jiang-Lin Wei, Nene Kushita, Hirotaka Arai, **Lei Sha**, Anna Kuwana, Takayuki Nakatani, Kazumi Hatayama, Haruo Kobayashi (Gunma University) "An Effective INL Test Methodology For Low Sampling Rate and High Resolution Analog-to-Digital Converter", Poster Session, IEEE International Test Conference, Washington, D. C. (Nov. 2019).

[7] Takashi Hosono, **Lei Sha**, Souma Yamamoto, Mayu Hirano, Takashi Ida, Anna Kuwana, Haruo Kobayashi, Yoichi Moroshima, Hiromichi Harakawa, Takeshi Oikawa, "Simple Reference Current Source Insensitive to Power Supply Voltage and Temperature", 6th Taiwan and Japan Conference on Circuits and Systems (TJCAS 2020), On-line (Nov. 14, 2020)

[8] Jianglin Wei, Nene Kushita, Takahiro Arai, **Lei Sha**, Anna Kuwana, Haruo Kobayashi, Takayuki Nakatani, Kazumi Hatayama, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, "High-Resolution Low-Sampling-Rate ΔΣ ADC Linearity Testing Algorithm", 3rd International Conference on Technology and Social Science (ICTSS2019) , Kiryu, Japan (8-10 May, 2019)

[9] (invited paper) Haruo Kobayashi, Kosuke Machida, Yuto Sasaki, Yusuke Osawa Pengfei Zhang, **Lei Sha**, Yuki Ozawa, Anna Kuwana, "Fine Time Resolution TDC Architectures-Integral and Delta-Sigma Types", 13th IEEE International Conference on ASIC (ASICON 2019), Chongqing, China (Oct. 29 – Nov. 1, 2019)

Award

[1] Best Student Paper Award: International Conference on Mechanical, Electrical and Medical Intelligent System 2019, Kiryu, Japan (Nov. 29 - Dec. 1, 2019).

[2] Best Student Presentation Paper Award: International Conference on Technology and Social Science 2020, Kiryu, Japan (Dec. 2 - Dec 4, 2020)