令　和　三　年　度　　修　士　論　文

ホップフィールドネットワークに基づく
非同期逐次比較近似 AD 変換器の研究

Research of Asynchronous SAR ADC
Based on Hopfield Network

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contents

1. Abstract

1.1 Research Background

In recent years, as the applications of electronic equipment are becoming more and more popular, the semiconductor industry has also ushered in explosive development. Among them, analog to digital converters (ADCs) is a very important part. What is ADC or DAC? It is the mutual conversion of analog signals and digital signals. Especially in today's digital society, almost all data is digitized to facilitate subsequent processing, transmission and storage. Therefore, it can be imagined that in a world without ADC, society will not develop normally.

As a research topic, we study a method to reduce the error rate to realize AD conversion in Hopfield network. Why do we revisit Hopfield network? According to the original literature, it is very fast SAR ADC, non-binary SAR ADC as well as binary, and simple design. It can be seen that this ADC design can have better performance than the traditional SAR ADC in some applications. For these reasons, this is a meaningful study.

1.2 Research Objective

The Hopfield network has been investigated as an ADC architecture for several tens of years [1], but it has not been widely used in practice. Here we revisit the Hopfield network and consider several interesting configurations. We expect that resistive networks such as the Hopfield network and the active resistive network [2] besides resistive DACs [3, 4] revive in analog signal processing fields.

It is known that the Hopfield network ADC often falls into the so-called local minimum, which means high error rate and which makes it impractical for commercial application. However, the Hopfield network ADC is attractive because it is very fast, its operation is asynchronous and its design is simple. We consider that its modification may lead to a high performance reliable asynchronous SAR ADC, which is now a very hot topic in ADC research fields, and hence we revisit the Hopfield network ADC here. We have improved the Hopfield network ADC by discarding the feedback paths from the lower bits to the upper bits to avoid the local minima problem. We also show that a non-binary weighted SAR ADC can be realized by proper design of resistor values; as an example, we show a Fibonacci number weighted SAR ADC. Further we point out that the improved Hopfield network ADC has a DAC array inside the network. These are verified with SPICE simulations.

1.3 Configuration of Thesis

The construction of this thesis is as follows.

Chapter 1, as an abstract, describes the outline of this thesis. In Chapter 2, we introduce the basic principle and common types of ADC, and give the parameter method to evaluate the performance. In Chapter 3, the traditional Hopfield network is analyzed and evaluated. In Chapter 4, we introduce the structure of the improved SAR ADC, and explain the advantages of non-binary asynchronous SAR ADC through simulation results. Finally, Chapter 5 summarizes the matters described in this thesis as a conclusion.

2. Introduction to ADC

2.1 Interpretation of ADC

Since the computer can only process digital signals, it is necessary to convert analog signals into digital signals. Common analog signals include temperature, sound, light and so on. These analog signals are converted into electrical signals by sensors, amplified by amplifiers, and then processed by digital to analog converters into discrete digital quantities that can be read by computers.

In general, ADC generally goes through four processes: sampling, holding, quantization and coding.

Fig. 1 Analog-to-digital converter

2.2 Sampling and Holding

Analog signals are like countless digital signals, but in fact we can only collect a limited number of points in order to convert them into digital signals we need. In short, sampling is to convert analog quantity that changes continuously with time into discrete analog quantity.

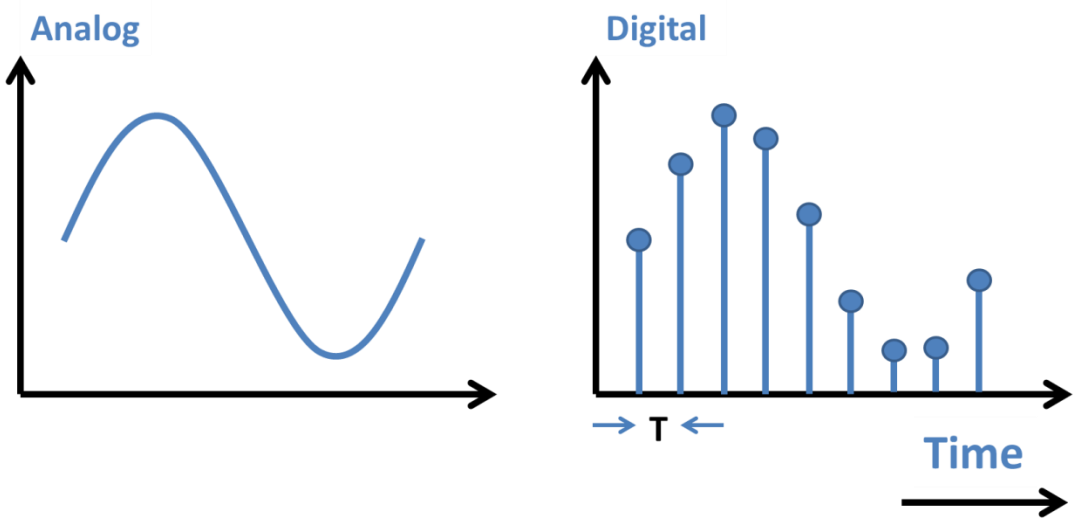


Fig. 2 Sampling frequency

The structure diagram of sampling circuit is shown in Fig. 3. The sampling signal S(t) controls the transmission gate. During one pulse, the transmission gate is turned on, the output signal Vout(t) is the input signal Vin(t), while during the end of the pulse, the transmission gate is closed, and the value of the output signal Vout(t) is Vin(tn), where t0 shows the n-th sampling timing.

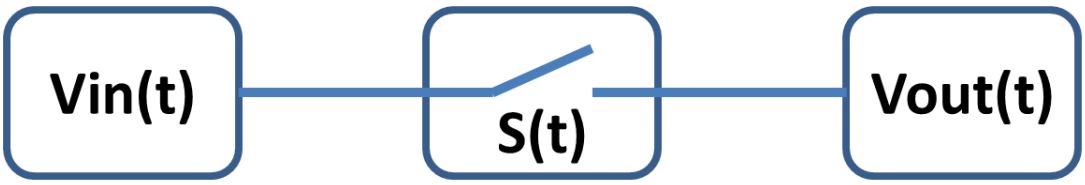


Fig. 3. Sampling circuit structure

The signal waveform in the sampling circuit is shown in Fig. 4.

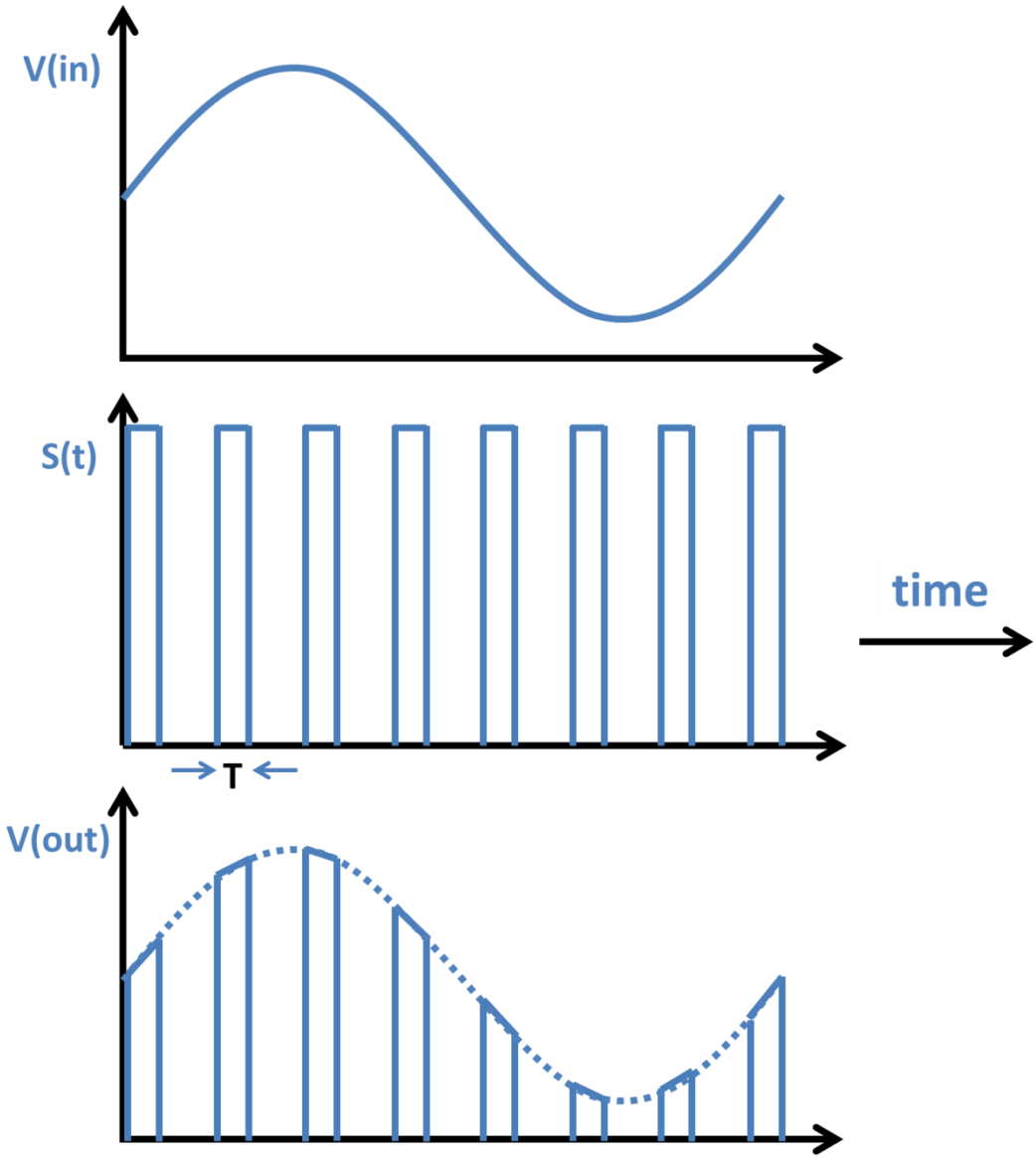
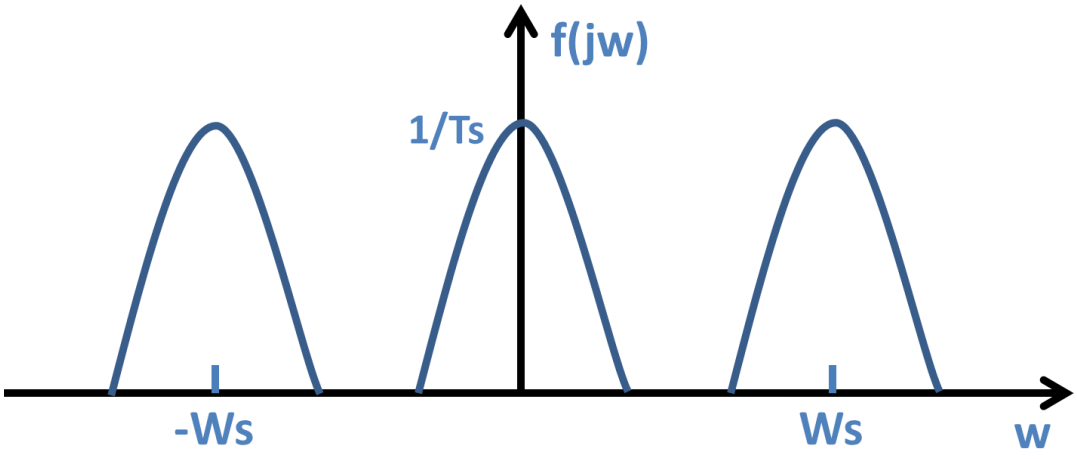


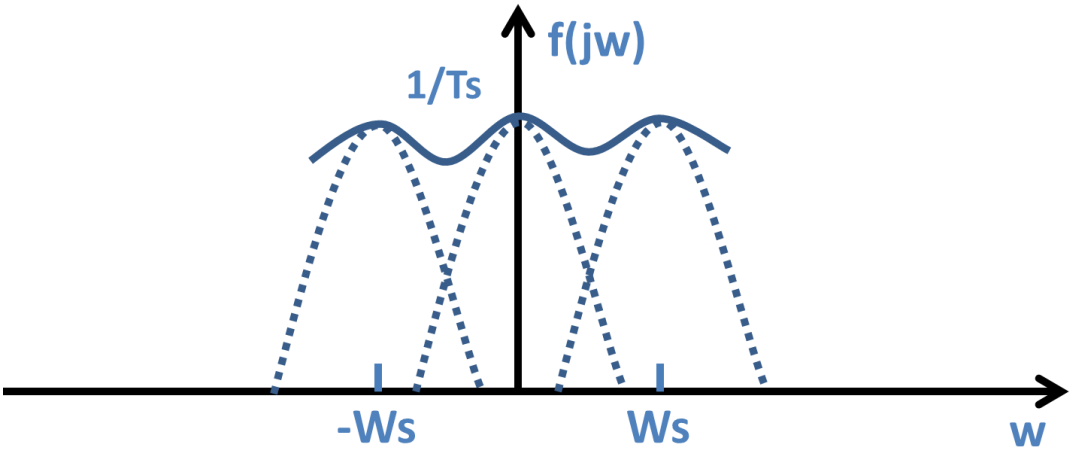
Fig. 4. Signal waveform in sampling circuit

As can be seen from the figure, the faster the frequency f of the sampling signal S(t), the closer the value of the output signal Vout is to the value of the input signal Vin. However, if the frequency f is too fast, the amount of data will be too large, which will affect the efficiency of signal acquisition. Therefore, we need an appropriate frequency to achieve the effect we need. Therefore, frequency sampling theorem needs to be involved here.

According to the Nyquist frequency sampling theorem, the sampling frequency must be greater than twice the signal frequency, that is fs ≧ 2fn, in which the frequency of the sampling signal S(t) is fs and the frequency of the highest frequency component of the input analog signal Vin(t) is fn. The signal can be recovered smoothly through such a sampling method. If not, it cannot be recovered due to spectrum aliasing. As shown in Fig. 5.



(a) Ws ≧ 2Wn



(b) Ws ≦ 2Wn

Fig. 5 Sampling and spectrum folding.

When the analog signal obtained by the sensor is converted into digital signal through the sampling circuit, this process is not instantaneous, but takes a certain time. Since there is a quantization and coding process during conversion, we need to provide a stable value for this process, so at this time, we must use the holding circuit to hold the analog signal obtained each time for a period of time, so as to successfully complete the process of data acquisition.

The holding circuit performs the process of saving the sampled value to the next conversion. The schematic diagram of the holding circuit is shown in Fig. 6.

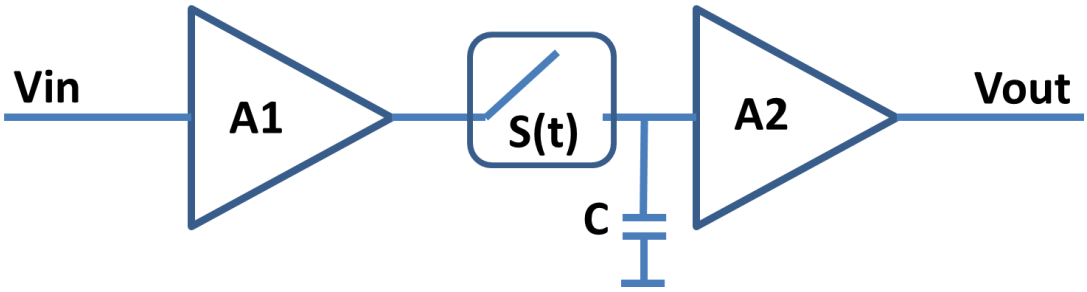


Fig. 6. Sampling-holding circuit

As shown in the figure, its main components are four parts; input amplifier A1, switch drive module, holding capacitor C and output amplifier A2. The input amplifier A1 needs to reduce the impact on the input signal source, so A1 is required to have high input impedance in the circuit. In order to make the charge stored on the capacitor C in the holding stage difficult to discharge, there must also be high input impedance in the output amplifier A2. In addition, in order to improve the load capacity of the circuit, the output impedance of A2 needs to be small. The circuit is also required to meet the condition that the output of V(A1) ·V(A2) is linear to the input. Here we consider the case that V(A1) ·V(A2) = 1, without loss of generality.

We consider the holding phase, as shown in Fig. 7. When time t = T1, the switch at S(t) is closed. At this time, the holding capacitor in the circuit quickly completes the charging process. From V(A1) ·V(A2) = 1, Vout = Vin can be deduced, so sampling is carried out in the time period (T2 - T1). Time t is disconnected at S(t) at T2. When the circuit is in an ideal state, since the input impedance of the output amplifier A2 is infinite, the holding capacitor C cannot discharge, so the voltage at both ends remains Vout unchanged. It can be seen that the voltage remains unchanged in the time period of (T3 - T2).

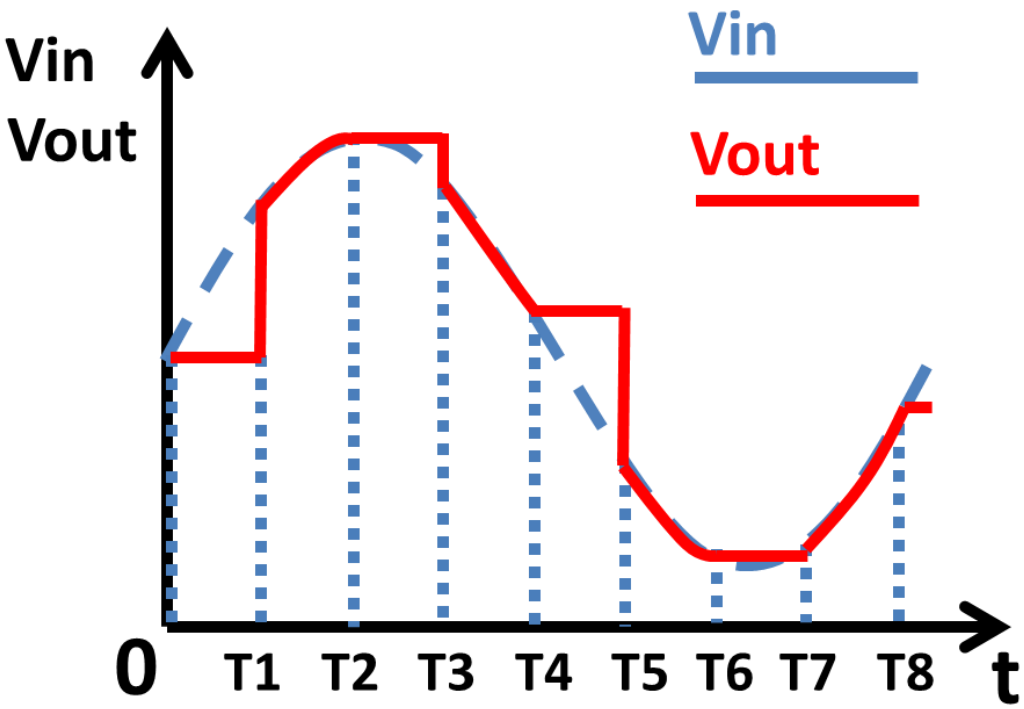


Fig. 7. Waveforms of sampling-holding circuit

2.3 Quantization and Coding

The principle of numerical quantization is as follows. The digital signal converted from analog signal by sampling-holding circuit is different from the original continuous analog quantity. It is discrete in time. At the same time, the amplitude of digital signal is discontinuous. Moreover, after a minimum value is specified, the amplitude of the digital signal can only be an integral multiple of the minimum value. After the sampling in subsection 2.2 above, we set the Vout output level in Fig. 6 to a specific discrete level by approximate quantization.

The digital signal after numerical quantization is converted into a specific digital code through the coding process, such as 1010, etc. The specific digital code after such quantization and coding process is the result of the final conversion of ADC.

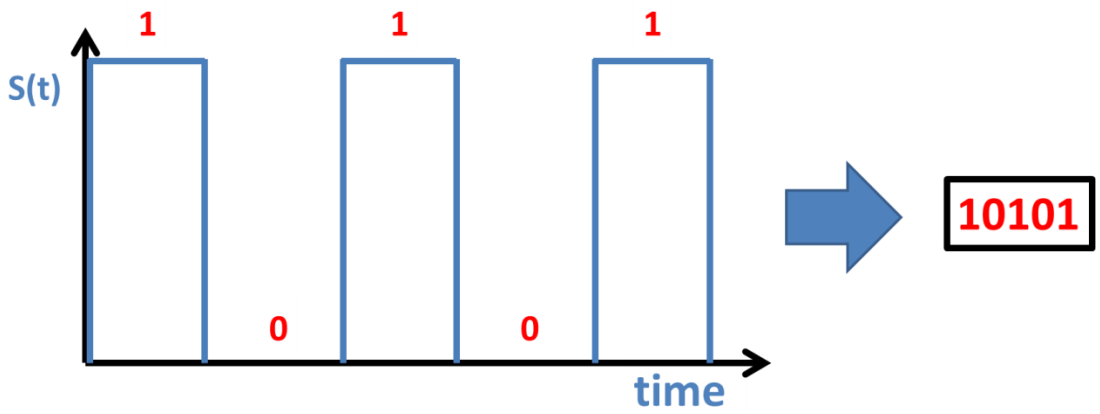


Fig. 8. Coding

The quantization unit is the analog quantity corresponding to the digital signal when the minimum integer value is 1LSB, as shown in Fig. 9.

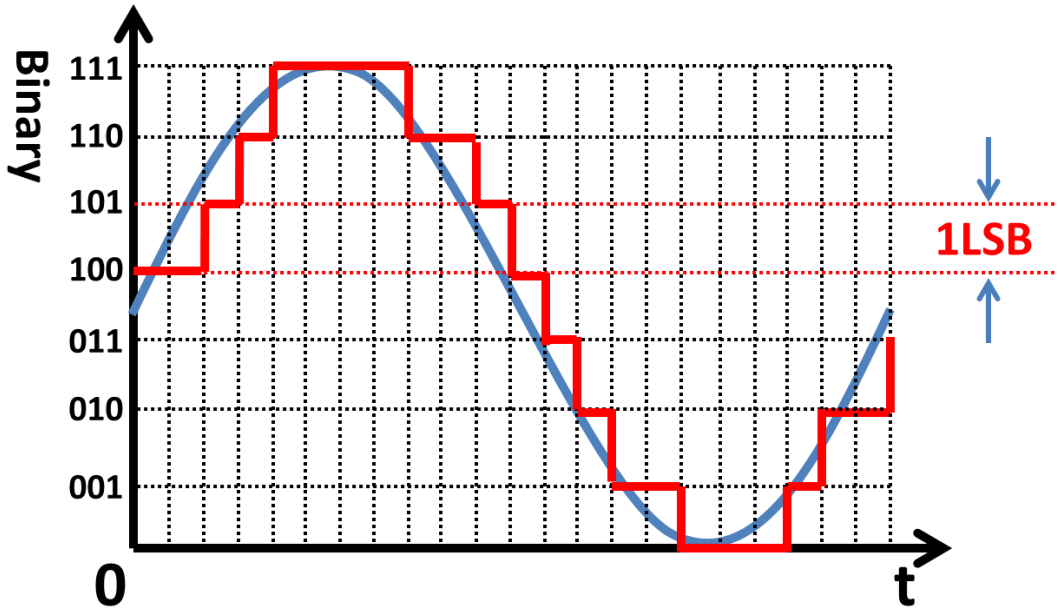


Fig. 9. Quantization error

Quantization error refers to the error caused by quantization of analog signal, which can reach half of the quantization level at most. In the quantization process, since the voltage after sampling may not be divisible, there must be an error after quantization. The quantization error is an essential error and cannot be eliminated. However, the more bits of ADC, the smaller the difference between the quantization result and the quantized analog quantity, and the smaller the quantization error.

2.4 Classification of ADC

With the development of modern society towards intelligence, the demand for integrated circuits has become very strong, and the semiconductor industry has also developed rapidly. Therefore, the new design idea of ADC has also been innovated with the breakthrough of manufacturing technology. According to different detection and control needs, ADC with different structure design and performance came into being.

So far, many kinds of ADC have been developed. There are four kinds of ADCs for main applications: SAR ADC, Flash ADC, Pipelined ADC, ΔΣ ADC.

2.4.1 SAR ADC

SAR ADC is mainly composed of sampling-holding circuit (Sample and hold), comparator (COMP), successive approximation register and control circuit (SAR LOGIC), DA conversion circuit (DAC) and data register, as shown in Fig. 10.

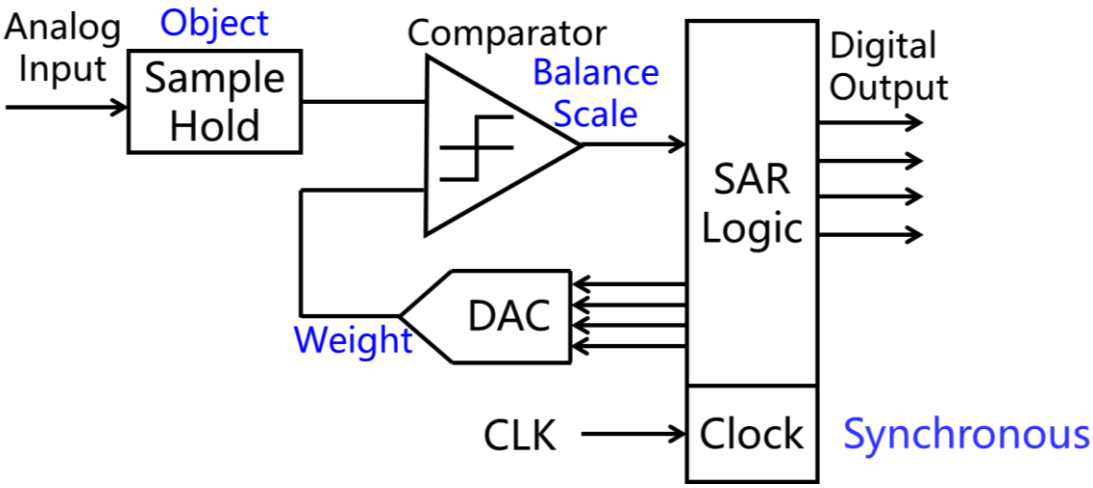


Fig. 10. SAR ADC structure diagram

The analog voltage is input to the inverting input of the comparator, and the output of the DAC is connected to the in-phase input. Through the control of the control circuit, compare the registers one by one, change the numbers one by one, and send the data in the register to the DAC.

First, the highest position 1 of the successive comparison register instructs the DAC to output the corresponding voltage to the inverting end of the comparator for comparison with Vin. If Vin is greater than the voltage, the comparator output is 1, the successive comparison register samples to 1, and the highest bit is 1, otherwise it is 0. Compare until the last bit, and then the stored data will be output.

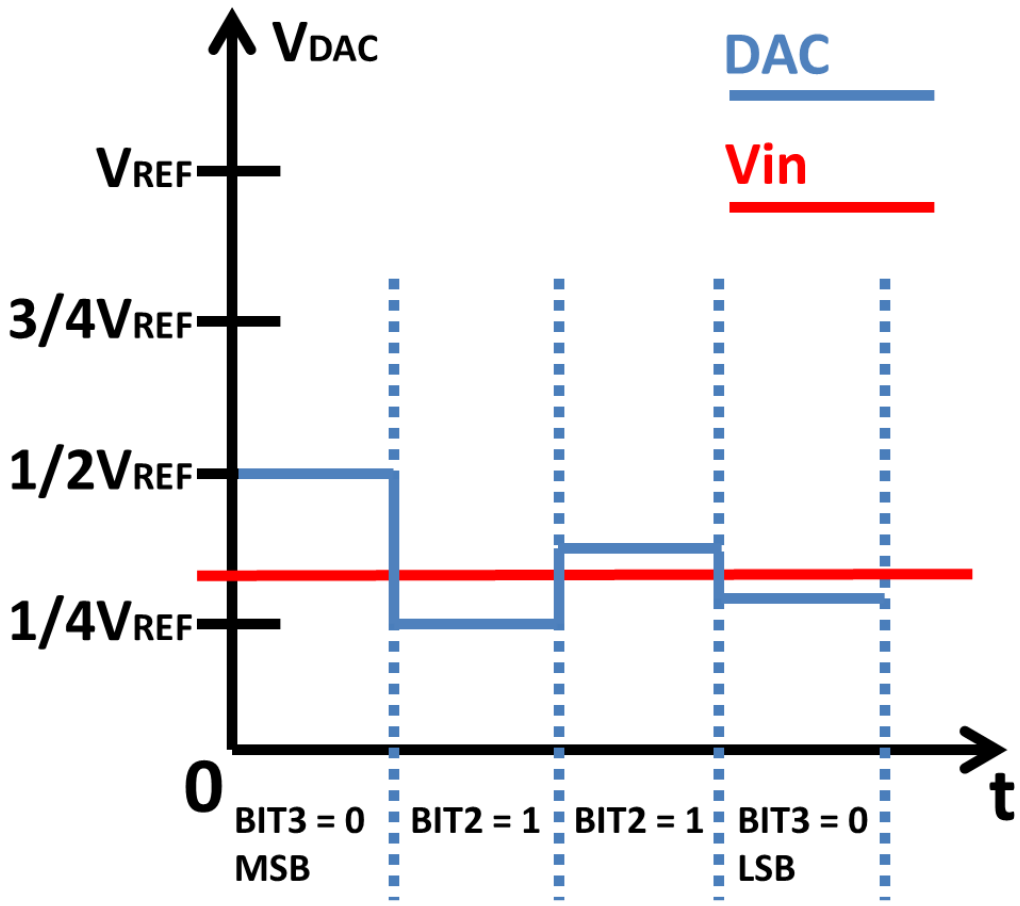


Fig. 11. 4-bit comparison output

It can be seen that this ADC only completes 1-bit conversion in one clock cycle, and n-bit conversion requires n clock cycles, so its sampling rate is not high and its input bandwidth is low. Its advantages are simple circuit structure and principle, small chip area and low power consumption, easy to implement, and there is no delay problem. It is suitable for occasions with medium speed and high resolution requirements.

2.4.2 Flash ADC

Flash ADC has the characteristics of simple structure and full parallel conversion. Because of full parallelism, the conversion can be completed almost at the same time. Therefore, it is the fastest conversion speed among various ADCs. The disadvantage is that 2^n- 1 comparators and 2^n resistors are required, resulting in the increase of chip area and power consumption, which limits the high integration. Therefore, it is usually used in the case of low resolution and high conversion speed.

Fig. 12 shows the structure of flash ADC. It consists of a reference voltage generation network, usually composed of a resistor string for voltage division, a string of comparators and coding logic blocks. For an n-bit fully parallel ADC, 2^n equal resistors are connected in series to provide 2^n- 1 reference voltages with equal spacing of 1 LSB. 2^n- 1 comparators compare the input signal with the reference voltage at the same time. If the input voltage is greater than the reference voltage, the corresponding comparator output is 1. Otherwise, the output is 0. The generated code is then transmitted to the encoder module, which generates the output of binary code according to the internal setting.

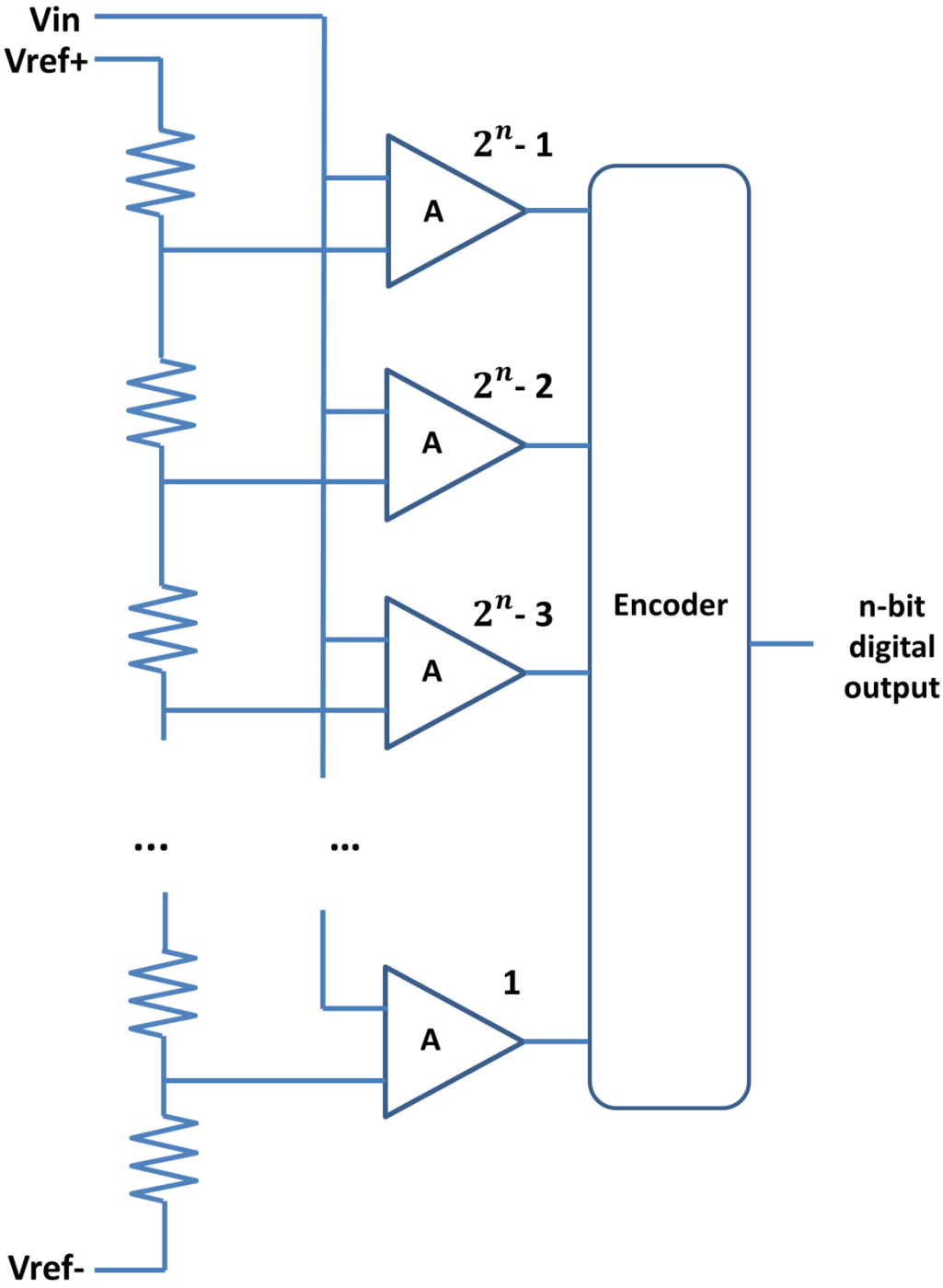


Fig. 12. Structure of Flash ADC

From the above analysis, it can be seen that the Flash ADC is only converted once because of its fully parallel structure, so it does not need to be compared step by step

like SAR ADC. Therefore, its conversion speed is only determined by the speed of the comparator. Through comparison, Flash ADC has the fastest conversion speed among ADCs with various structures, which is its advantage. Another advantage is that the reference power supply adopts resistance series voltage division network, because the monotonicity reduces the occurrence of nonlinearity.

2.4.3 Pipelined ADC

Pipelined ADC is a new high-precision ADC inspired by the pipelining technology of digital system. This kind of ADC circuit can provide high-speed and high-resolution AD conversion. Its working principle is that in several clock cycles, the sampled input signal flows successively along the pipeline circuit, carries out digital coding level by level, and corrects the time error at the same time. Therefore, its conversion mode is to process the input signal through sequential comparison. In some technical fields, it is used in high-speed and low-power systems.

The schematic diagram of Pipelined ADC is shown in Fig. 13. It is composed of several low-precision AD converters. Each stage is composed of a sample and hold circuit, a low resolution AD converter, a DA converter and a summation circuit. The summation circuit also includes an inter amplifier that can provide gain. These individual converters quantize the sampled signals step by step, and then combine their quantization results to form a high-precision quantization output. The number of these stages is equal to the resolution of the ADC.

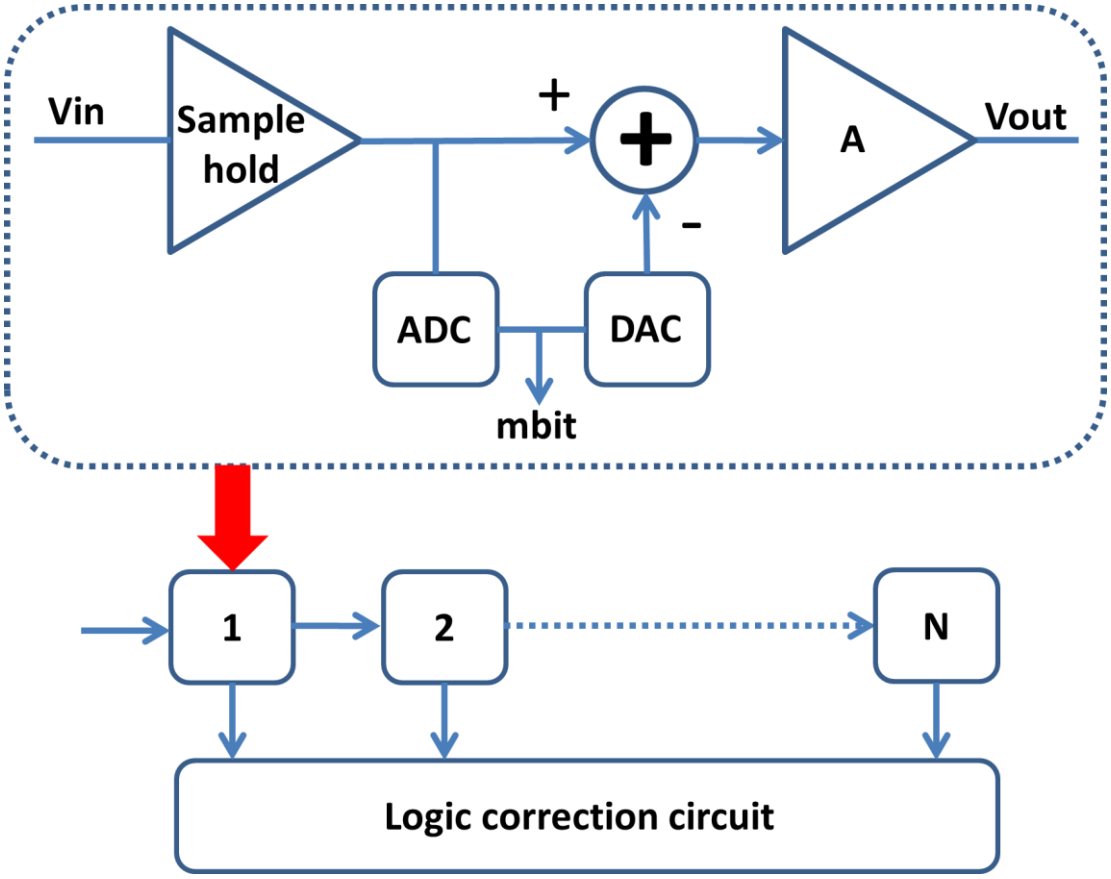


Fig. 13. Schematic diagram of pipelined ADC

Firstly, the analog input is sampled through the sample and hold circuit, and the sampled signal is sent to the sub-ADC for quantization processing to generate m-bit digital quantity. Then, the converted digital signal is sent to the sub-DAC to generate the corresponding analog level, and then the analog level is sent to the summation circuit for processing. The analog level is subtracted from the sampled input signal to obtain the residual signal. After amplification, the residual signal is output to the next stage as a new input signal.

In the n-pipeline structure, this process needs to be repeated n-1 times. Generally, the n stage is a standard flash ADC structure. In order to overcome the internal imbalance and nonlinearity of each stage sub-ADC, each stage pipeline adopts digital correction technology, and there are corresponding redundant bits in the output bits of each stage, so the output bits of each stage together constitute the final converted output after correction.

In the n-pipeline structure, this process needs to be repeated n-1 times. Generally, the n-th stage is a standard flash ADC structure. Each stage pipeline adopts digital correction technology to overcome the internal nonlinearity and other errors of each stage sub-ADC. After this processing, there are corresponding redundant bits in the output bits of each stage. After correcting the output bits of each stage, they are combined as the final output result.

By optimizing the circuit and adding digital correction circuit, it has the advantages of series parallel converter and algorithm correction converter at the same time. First, the accuracy is improved, and the performance requirements of the circuit are not high. Second, the number of components required is directly proportional to the number of conversion bits, which can reduce the number of hardware and control power consumption. Third, due to the parallel and multi-stage processing of analog signals, it can not only realize high-speed conversion, but also improve the resolution of AD converter. Fourth, because each stage has its own sample and hold amplifier, although the conversion of analog signals requires multiple levels, the sample and hold of the previous stage circuit can process the next sampling in time, so each stage of the

pipeline can process multiple sampling signals at the same time to improve the conversion speed. The disadvantages are also obvious. The input signal must pass through the pipeline processing of several stages of circuits in turn, resulting in delay. The reference circuit and bias structure is complex. All outputs need to be synchronized, resulting in strict latch timing.

2.4.4 ΔΣ ADC

ΔΣ ADC is mainly composed of simple analog circuit and complex digital signal processing circuit. The main parts are shown in Fig.14, which are analog ΔΣ modulator and digital filter, in which analog ΔΣ modulator is composed of an integrator, a comparator, a 1-bit DAC and etc. Generally, its sampling rate is several times of Nyquist sampling frequency, and its function is mainly realized by digital circuit combined with algorithm.

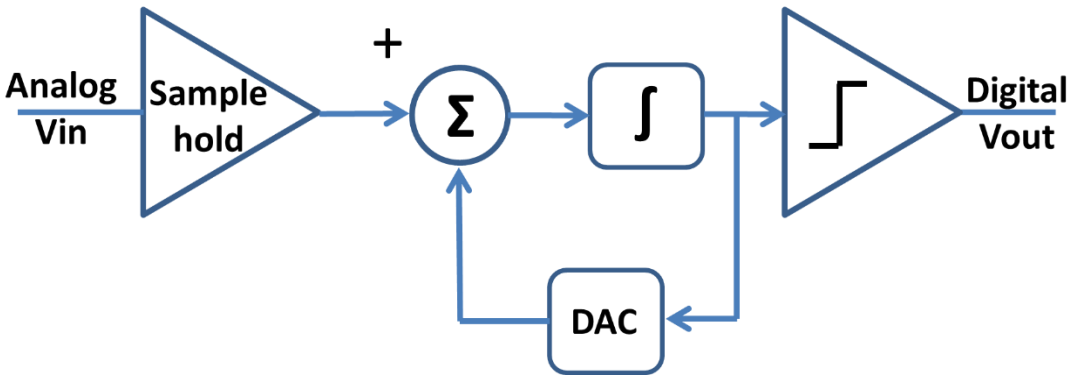


Fig. 14. ΔΣ AD modulator

ΔΣ ADC does not directly encode the amplitude of the signal, but quantizes and encodes according to the increment between the value of the previous sampling and the value of the next sampling. ΔΣ ADC samples the analog input signal at a very high sampling frequency, and then quantizes the difference between the two samples in low order to obtain the digital signal represented by low order digital. Then the processed digital signal is transmitted to the digital decimation filter for decimation filtering to obtain a high-resolution linear pulse digital signal.

2.5 Performance Parameters of ADC

How to test the performance of ADC? It is mainly described by static characteristic index and dynamic characteristic index.

2.5.1 Static Characteristic Index

The input of ADC is analog signal and the output is digital coding. The analog input is any value between Vref^{+} and Vref^{-}, while the digital coding is limited to a fixed or discrete amplitude. Each value of the output digital code has its corresponding analog voltage distinguished by LSB. Therefore, for each additional 1LSB in the input, the output code of the ideal ADC will increase by 1-bit.

LSB is defined as:

$$1\mathrm{LSB} = (\mathrm{Vref}^{+} - \mathrm{Vref}^{-}) / 2^{n}$$

The two main static characteristics of ADC are Differential Non-Linearity (DNL) and Integral Non-Linearity (INL).

Differential Non-Linearity (DNL) is the distance between adjacent codes measured on the vertical step, that is the difference between the actual quantization step and the ideal value corresponding to 1LSB, in percentage of the full-scale range or LSB.

DNL of an ideal ADC is 0LSB. That is each analog quantization step is equal to 1LSB. The DNL of ADC relative to digital output coding is shown as Fig. 15.

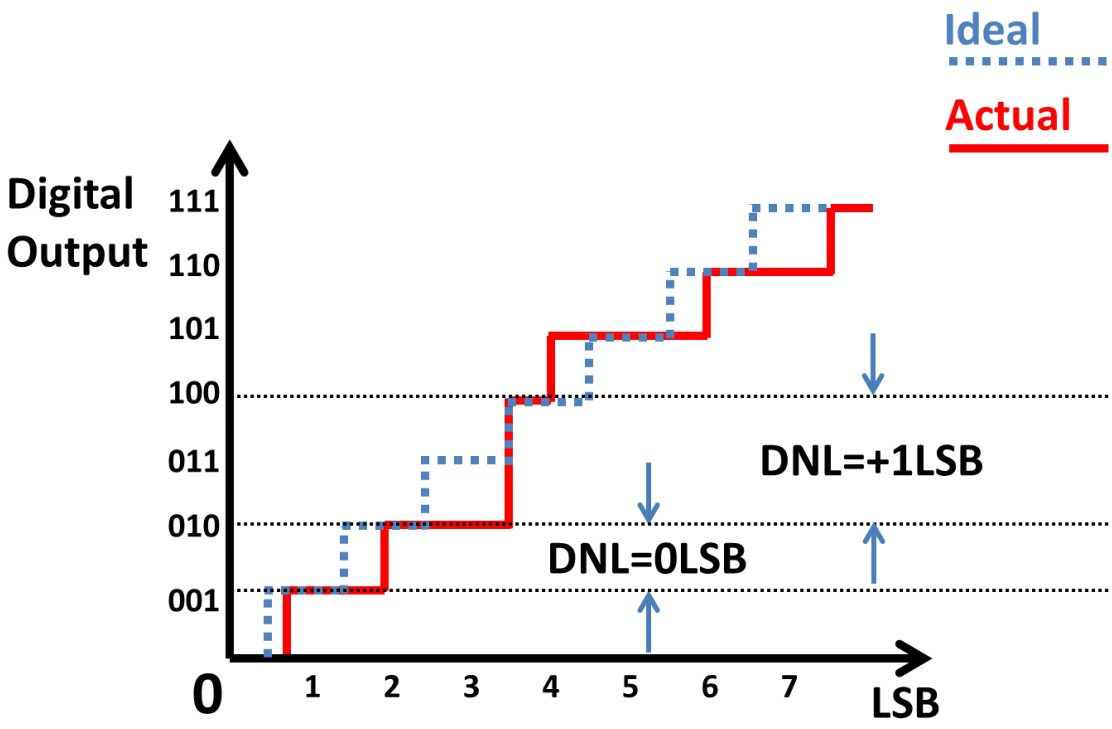


Fig. 15. DNL of ADC

According to Fig. 15, the maximum value of DNL is + 1LSB and the minimum value is 0LSB. If error index of DNL ≦ 1LSB, it means monotonicity and no code loss. When the digital output of an ADC increases with the increase of analog input signal, or remains unchanged, the corresponding function curve is said to be

monotonic. Therefore, to ensure no code loss and monotonic function curve, the DNL of ADC must be less than 1LSB.

Integral Non-Linearity (INL) is the maximum difference between the actual finite precision curve and the ideal finite precision curve in the vertical direction, in percentage of the full-scale range or LSB.

The INL of ADC is shown in Fig. 16. According to Fig. 16, the maximum value of INL is +1LSB and the minimum value is -1LSB.

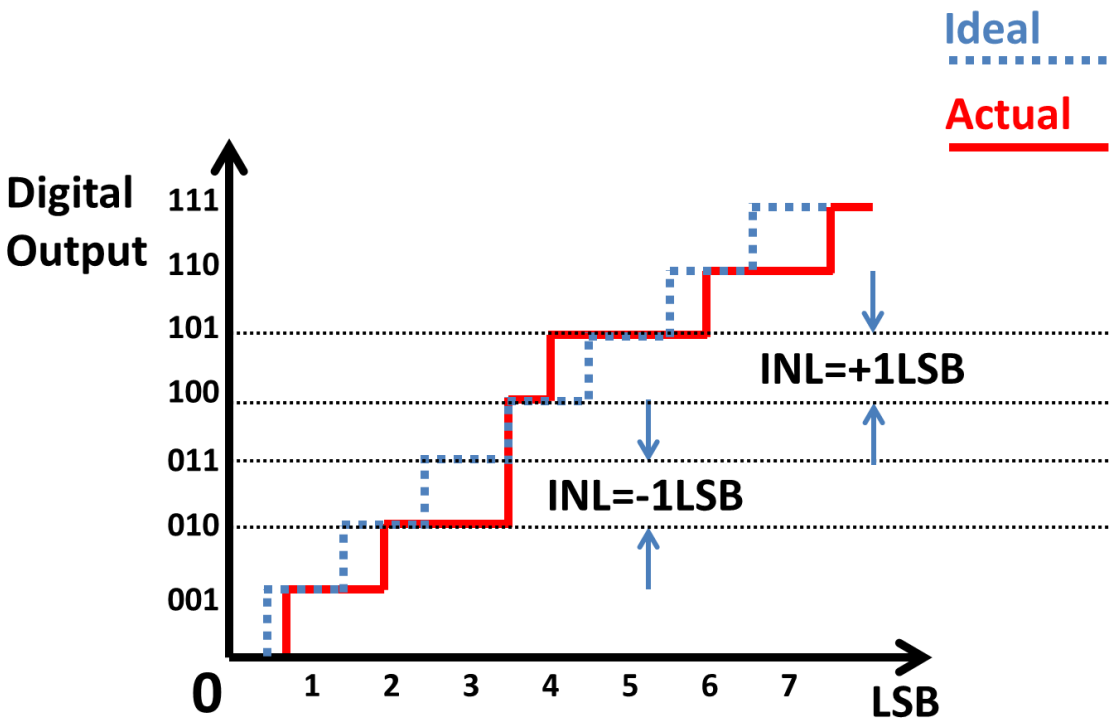


Fig. 16. INL of ADC

2.5.2 Dynamic Characteristic Index

Signal-Noise Ratio (SNR) refers to the ratio of signal power to noise power. The internal noise of the system will make the SNR deviate or exceed the range of theoretical value. The possible causes of errors include: device quantization error, device internal noise and nonlinear noise generated by sampling-holding source.

This parameter describes the ability to suppress noise during the period. The quantization noise is related to the resolution of the converter. The noise in the converter is mainly related to the perfection of the input comparator. The maximum SNR required by ADC is:

$$\mathrm{SNR(dB)} = (\,6.02\mathrm{N} + \,1.76)\ \mathrm{dB}$$

Effective Number of Bits (ENOB), which describes the error free bits of ADC output. ENOB is calculated based on the signal-to-noise ratio of ADC device. It converts the transmission signal quality into equivalent bit resolution. In fact, the system noise distorts the output signal, and the distortion is reflected in the signal-to-noise ratio. The relevant formula is:

$$\mathrm{N} = (\,\mathrm{SNR} - \,1.76)/6.02$$

Spurious free dynamic range (SFDR) refers to the ratio of the amplitude of the fundamental component to the amplitude of the maximum harmonic signal. SFDR shows the ability of the AD converter to detect the smallest signal while inputting a large signal.

3. Traditional Hopfield Neural Network ADC

3.1 Analysis of Traditional Hopfield Neural Network ADC

Hopfield network (Fig.17) [1] is a feedback neural network proposed by American physicist J. Hopfield in 1982. It is a neural network model that simulates the memory function of human brain. As an artificial intelligence network, neural network model has advantages in large-scale pattern recognition because of its parallel processing and high autonomy. It has important potential in nonlinear function approximation, intelligent automatic control and so on.

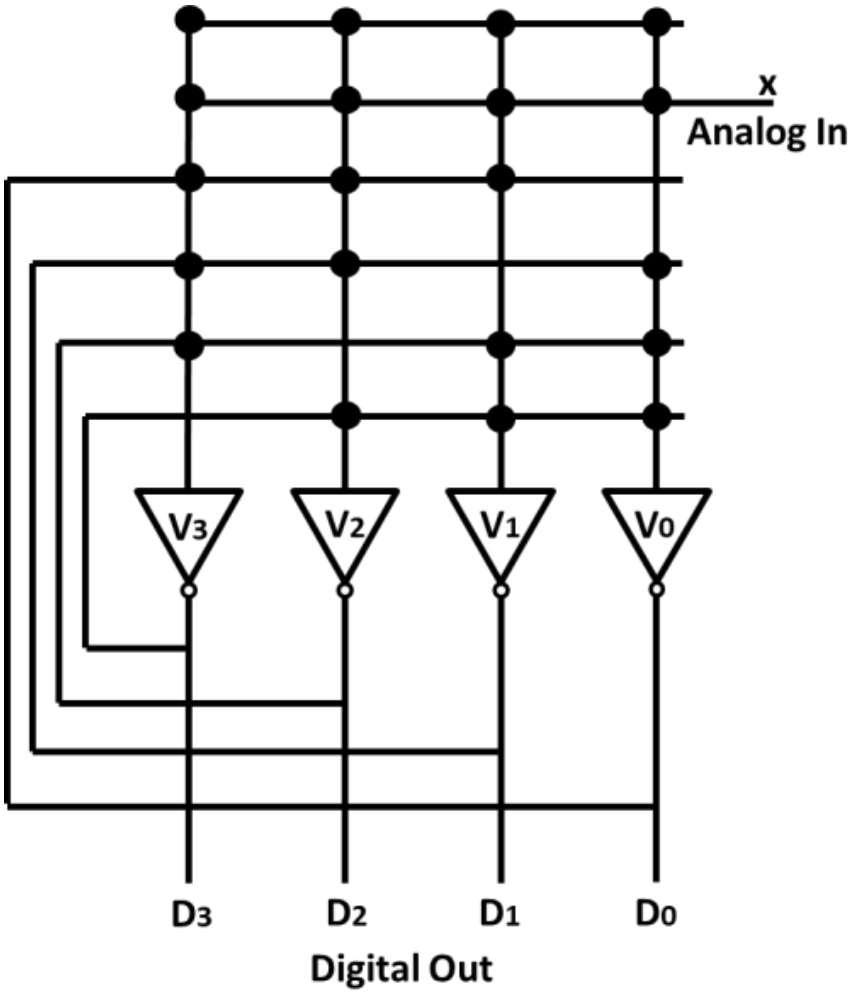


Fig. 17. Traditional Hopfield neural network ADC

For the i-th neuron, the equation of the continuous Hopfield neural network is described as

$$C\frac{dx_{\mathrm{i}}}{dt} = -\frac{x_{\mathrm{i}}}{R_{\mathrm{i}}} + \sum_{j=1}^{N} T_{\mathrm{ij}} f\,(x_{\mathrm{i}}) + I_{\mathrm{i}}$$

Here x_i is the analog input. R_i is the gain. T_{ij} is the conductance value, which is the synaptic characteristic of neurons I and j, that is the feedback coefficient of the amplifier. An operational amplifier is used to simulate the nonlinear characteristics of neurons. The input/output characteristics of the operational amplifier are Sigmoid function. $f(x_i)$ is the output of the i-th neuron. I_i is the threshold.

Hopfield network has a structure that introduces the energy function [1] into the feedback network. The energy function is used as the criterion of network stability. When the operational amplifier is ideal, the energy function is defined as

$$E = -\frac{1}{2}\sum_{i=1}^{N}\sum_{j=1}^{N} T_{\mathrm{ij}} V_{\mathrm{i}} V_{\mathrm{j}} - \sum_{i=1}^{N} V_{\mathrm{j}} I_{\mathrm{i}}$$

The minimum point of energy function is on the stable point of network convergence. Each neuron in the network can be connected with other neurons in two directions, which makes the output of each neuron in the network can be fed back to other neurons in the same layer. Therefore, the relationship function between input and output applied to the continuous Hopfield network is a continuous differentiable and monotonic increasing function. In this way, if the circuit parameters are correctly selected, the equilibrium point of the circuit can be exactly the minimum point of the energy function, so as to realize AD conversion.

3.2 Problem of Traditional Hopfield Neural Network ADC

It is well-known that the ADC based on the traditional Hopfield neural network has a problem of local minima (Fig.18), which sometimes leads to wrong output. Its reason is that there are feedback paths from the lower bits. Fig. 18 explains the local minima problem. Consider the case that we would like to obtain the parameter where the potential energy is at minimum using the gradient calculation of the potential energy. However, the potential energy gradient calculation may fall into the local minima; in such a case, it cannot reach to the minimal potential energy and the correct parameter value cannot be obtained.

When the input analog quantity increases continuously and then decreases continuously, the corresponding digital quantity is not unique, resulting in ADC error. The reason is that when the analog quantity is selected, there are multiple minima in the energy function of this circuit, of which only one is the global minimum and the others are the local minimum. When the coefficient converges to the local minimum, the error corresponding to analog quantity and digital quantity may occur.

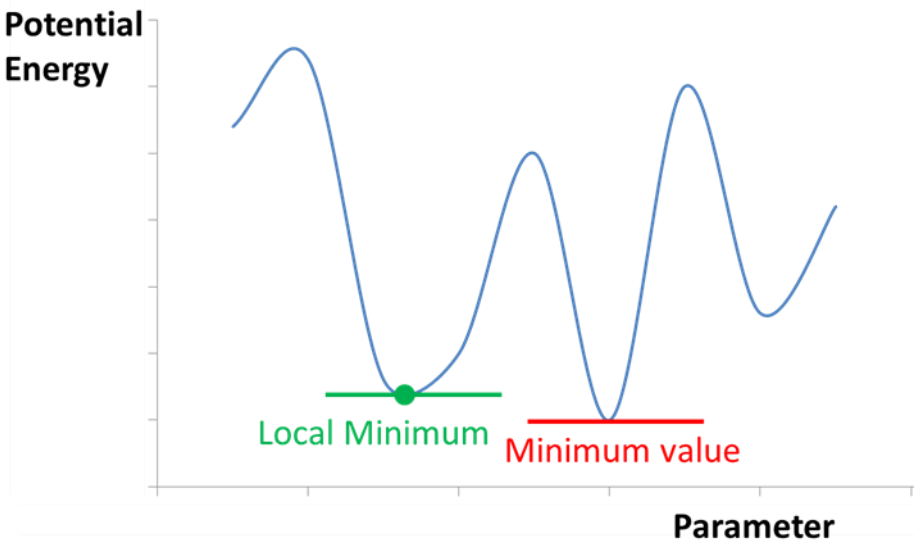
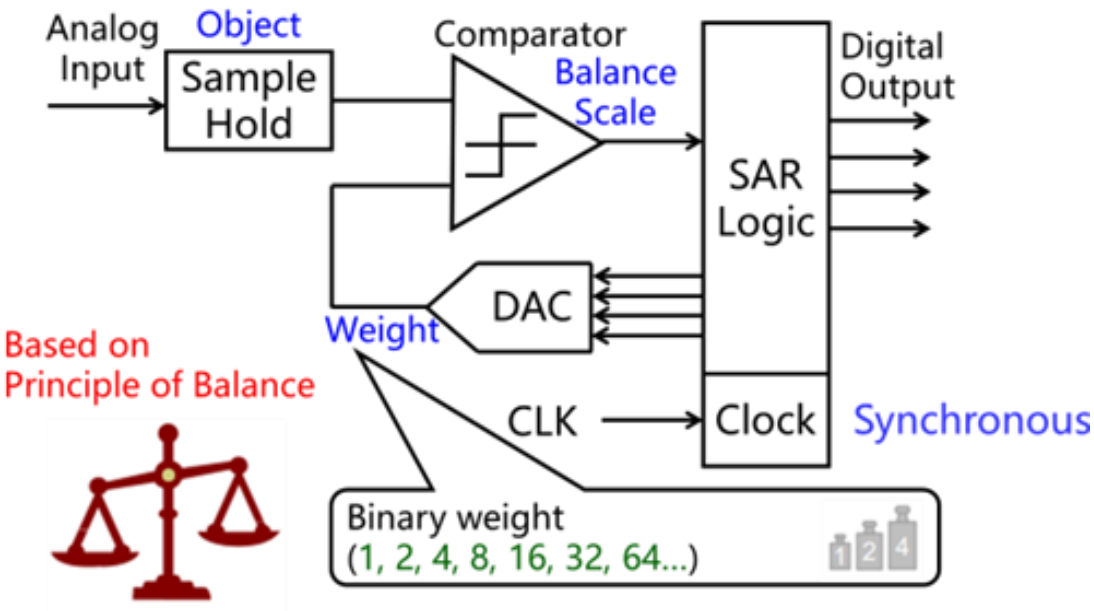


Fig. 18. Problem of local minima. The vertical axis shows potential energy and the horizontal axis shows parameters.

4. Proposed Hopfield Network ADC

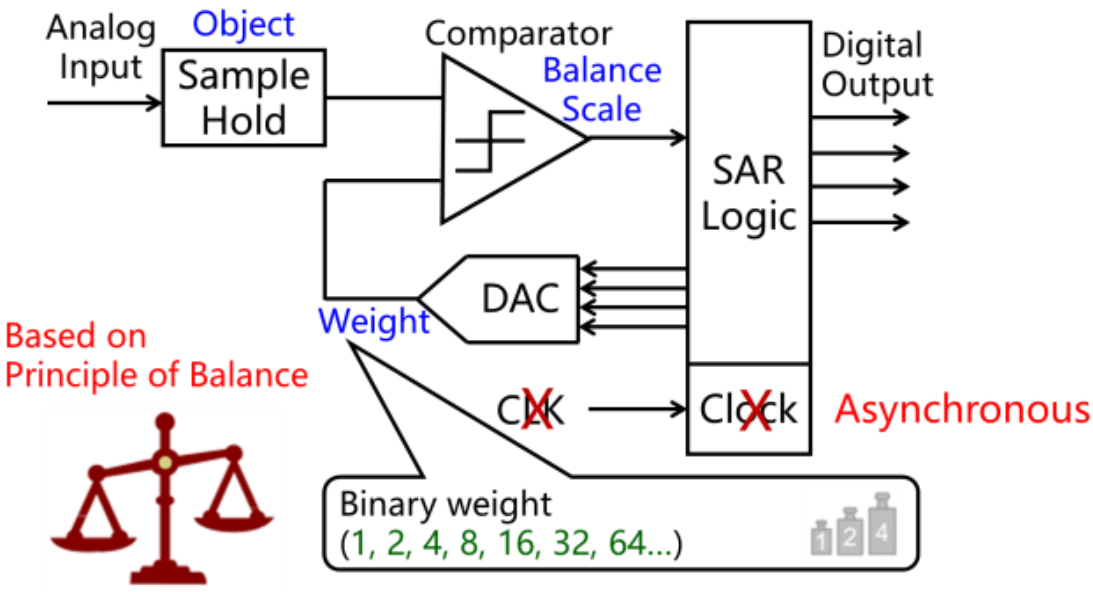
4.1 Binary Asynchronous SAR ADC

Fig. 19 (a) explains the binary-weighted synchronous SAR ADC while Fig. 19 (b) illustrates the asynchronous one. A typical 10-bit 150 MHz synchronous SAR ADC requires 1.8GHz (= (10+2) x 150MHz) clock internally, while asynchronous one needs only 150MHz clock; this is an advantage of asynchronous one.



(a)

Fig. 19. Binary weighted SAR ADC. (a) Synchronous one.



(b)

Fig. 19. (b) Asynchronous one.

Our improved Hopfield network asynchronous SAR ADC is shown in Fig. 20; this is the 6-bit case, but extension to higher bit case is straightforward. The network in Fig. 20 discards feedback paths from lower bits to higher bits and uses all feed forward configuration; then there is no local minimum. Also notice that the inverter circuit is used as a comparator. The advantages of the Hopfield network asynchronous SAR ADC are fast operation, no high frequency clock, no SAR logic and very simple design.

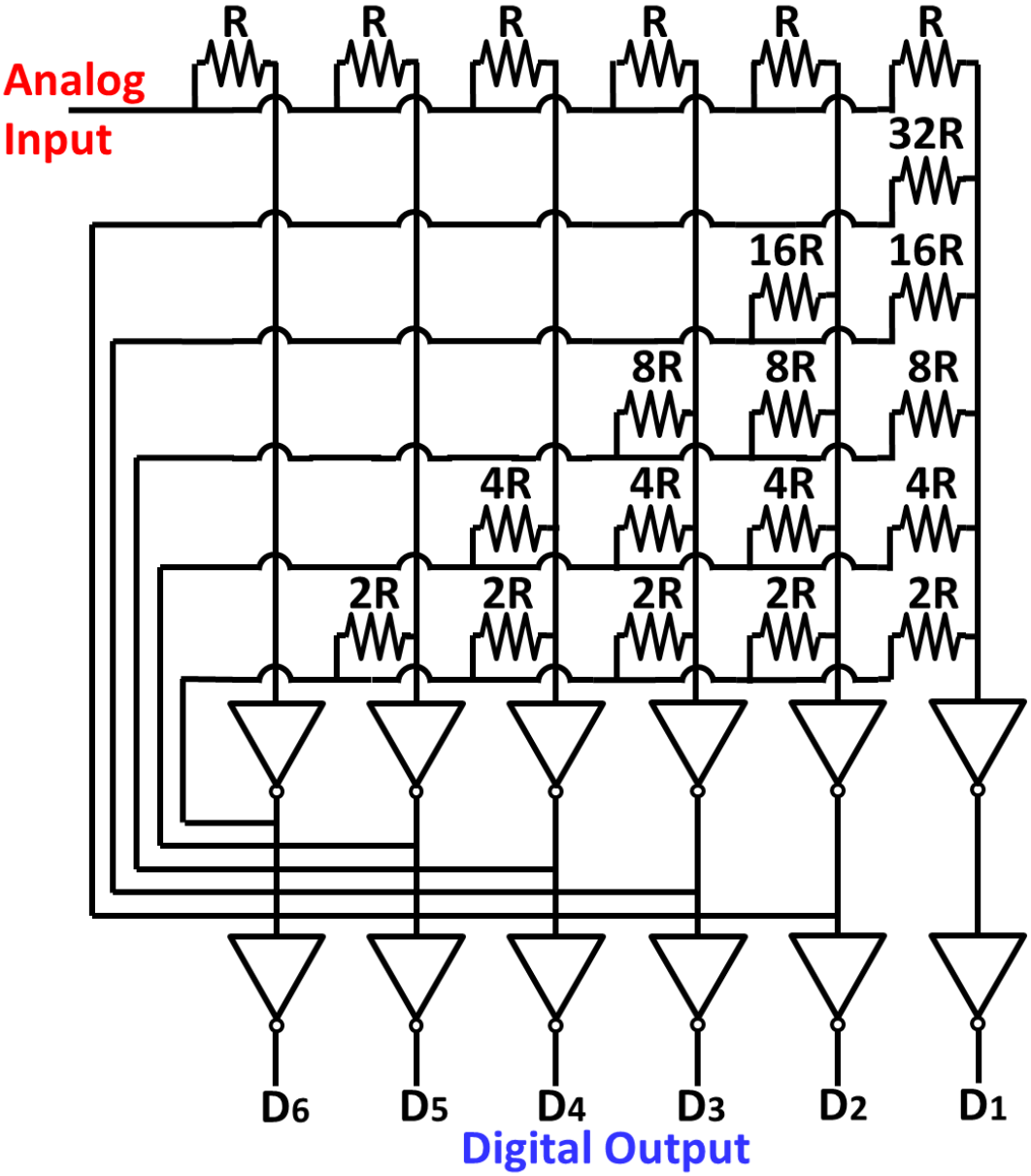


Fig. 20. Investigated binary-weighted asynchronous SAR ADC based on improved Hopfield network in 6-bit case.

We have investigated a 10-bit binary-weighted SAR ADC in Fig. 18 and we have the following decimal digital output from the inverter outputs of D_10…. D_1:

$$\mathrm{Data} = \left(\frac{1}{R_{10}}\right) D_{10} + \left(\frac{1}{R_9}\right) D_9 + \left(\frac{1}{R_8}\right) D_8 + \left(\frac{1}{R_7}\right) D_7 + \left(\frac{1}{R_6}\right) D_6 + \left(\frac{1}{R_5}\right) D_5 + \left(\frac{1}{R_4}\right) D_4 + \left(\frac{1}{R_3}\right) D_3 + \left(\frac{1}{R_2}\right) D_2 + \left(\frac{1}{R_1}\right) D_1$$

Here,

$\frac{1}{R_{10}} = 512, \frac{1}{R_9} = 256, \frac{1}{R_8} = 128, \frac{1}{R_7} = 64, \frac{1}{R_6} = 32, \frac{1}{R_5} = 16, \frac{1}{R_4} = 8, \frac{1}{R_3} = 4, \frac{1}{R_2} = 2, \frac{1}{R_1} = 1.$

SPICE simulation results are shown in Fig. 21, and the operation of the 10-bit binary weighted asynchronous SAR ADC has been confirmed.

The ADC based on continuous Hopfield Network is faster than the general serial AD conversion circuit, requires less operational amplifiers than the general parallel AD conversion circuit, and the circuit structure is simple. The corresponding relationship between analog quantity and digital quantity during normal operation of 10-bit binary weighted asynchronous SAR ADC is shown in Fig. 22.

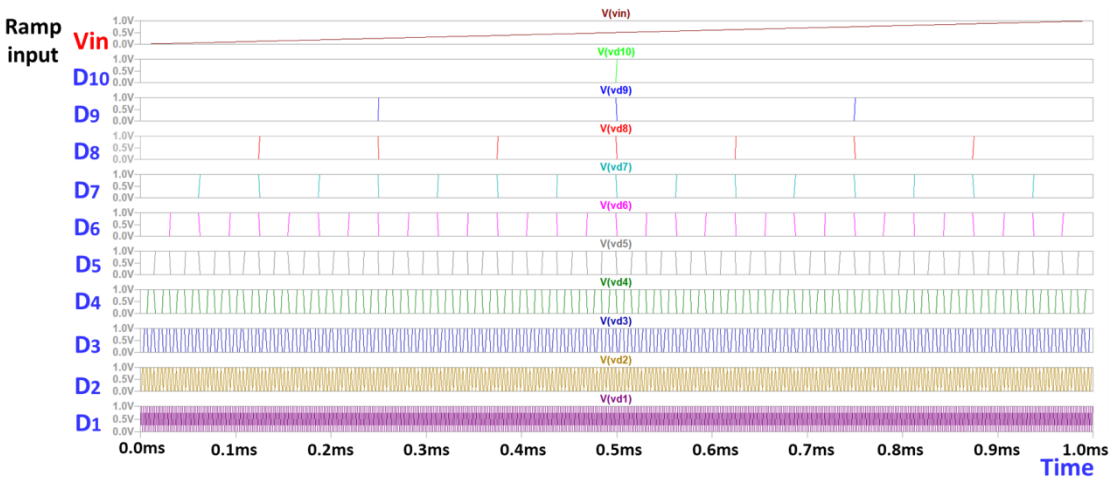


Fig. 21. SPICE simulation results of the10-bit binary-weighted asynchronous SAR ADC with the improved Hopfield network.

Fig. 22. Decimal data calculation result of 10-bit binary-weighted SAR ADC.

4.2. Non-binary Asynchronous SAR ADC

Fibonacci sequence definition is given as follows:

$$F_0 = 0$$

$$F_1 = 1$$

$$F_{n+2} = F_n + F_{n+1}$$

Then Fibonacci numbers are given as follows:

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, \ldots$$

Notice that the radix of the Fibonacci number sequence is approximately 1.62. Hence, by using Fibonacci number weights, non-binary weight SAR ADC with the radix of approximately 1.62 can be realized. Fig. 23(a) explains the Fibonacci number weighted asynchronous SAR ADC conceptually while Fig. 23(b) shows its implementation with the improved Hopfield network. Also notice that the non-binary weighted SAR ADC including the Fibonacci number weighted SAR ADC is discussed in [7, 8, 9].

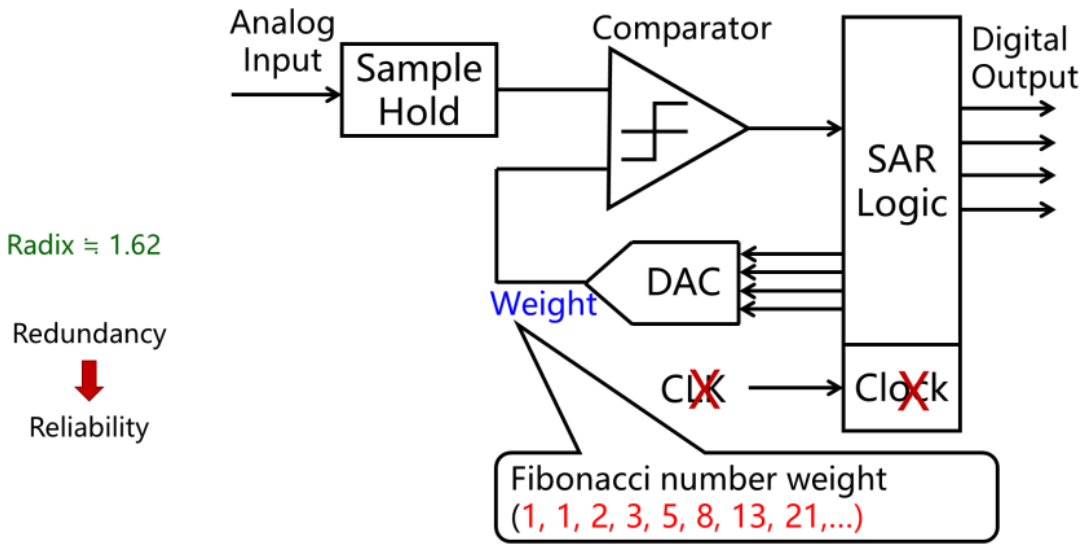
We have the following decimal digital output from the inverter outputs of D_10…. D_1 in the improved Hopfield network ADC:

$$\text{Data} = \left(\frac{1}{R_{10}}\right) D_{10} + \left(\frac{1}{R_9}\right) D_9 + \left(\frac{1}{R_8}\right) D_8 + \left(\frac{1}{R_7}\right) D_7 + \left(\frac{1}{R_6}\right) D_6 + \left(\frac{1}{R_5}\right) D_5 + \left(\frac{1}{R_4}\right) D_4 + \left(\frac{1}{R_3}\right) D_3 + \left(\frac{1}{R_2}\right) D_2 + \left(\frac{1}{R_1}\right) D_1$$

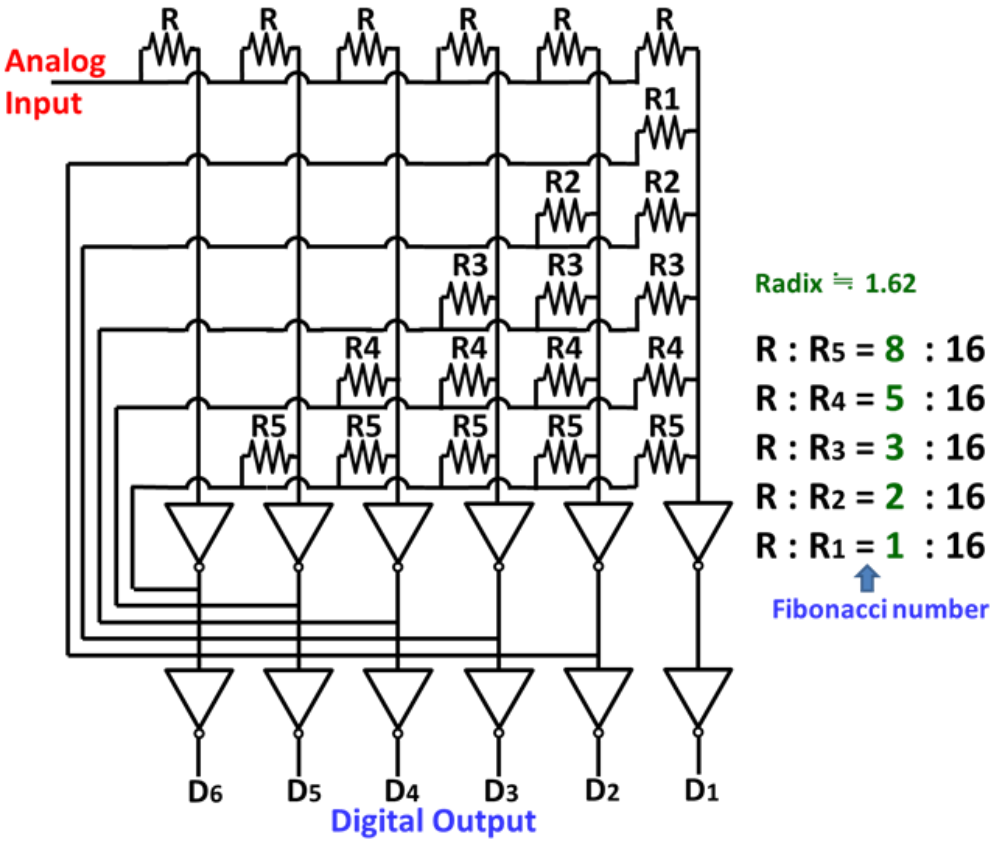
Here,

$$\frac{1}{R_{10}} = 89, \frac{1}{R_9} = 55, \frac{1}{R_8} = 34, \frac{1}{R_7} = 21, \frac{1}{R_6} = 13, \frac{1}{R_5} = 8, \frac{1}{R_4} = 5, \frac{1}{R_3} = 3, \frac{1}{R_2} = 2, \frac{1}{R_1} = 1,$$

SPICE simulation results are shown in Fig. 24, and the operation of the 10-bit Fibonacci number weighted SAR ADC has been confirmed, as shown in Fig. 25.

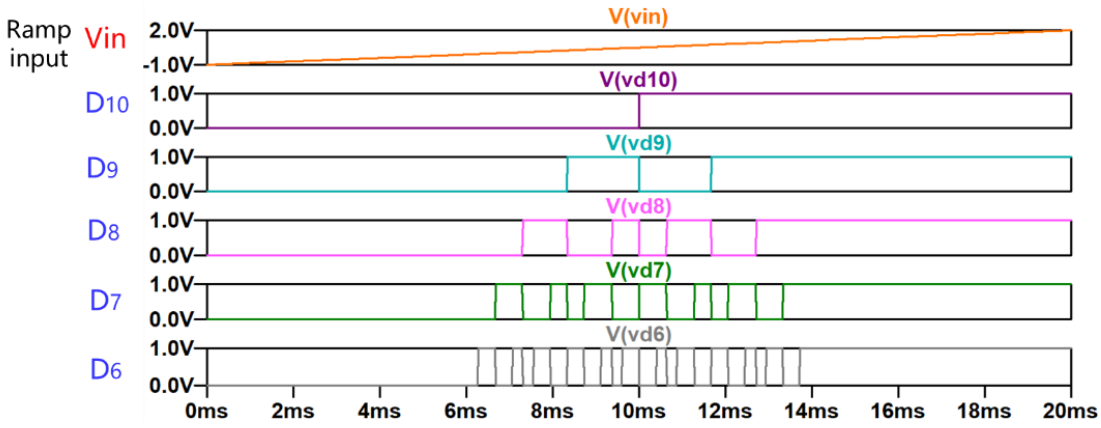


(a)

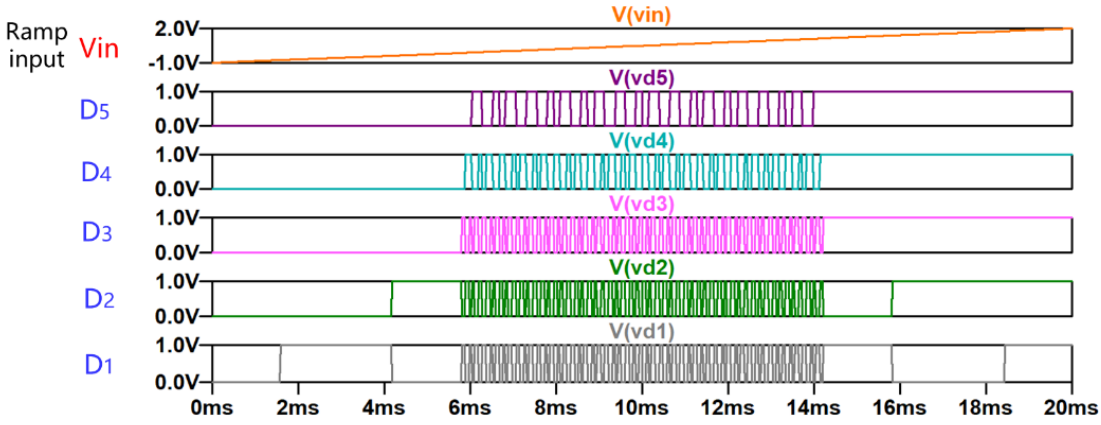


(b)

Fig. 23. Fibonacci number weighted asynchronous SAR ADC. (a) Conceptual explanation. Implementation with the improved Hopfield network (6-bit case).



(a)



(a)

Fig. 24. SPICE simulation results of the 10-bit Fibonacci number weighted asynchronous SAR ADC based on the improved Hopfield network.

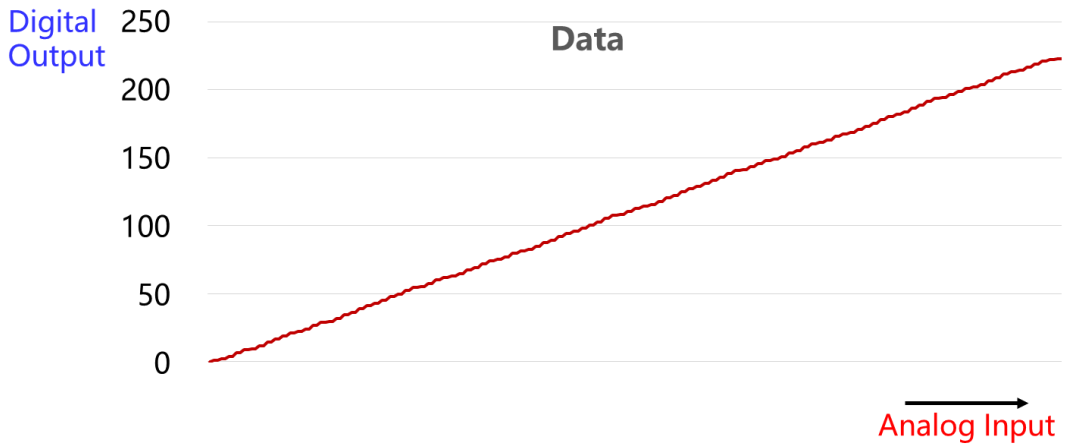
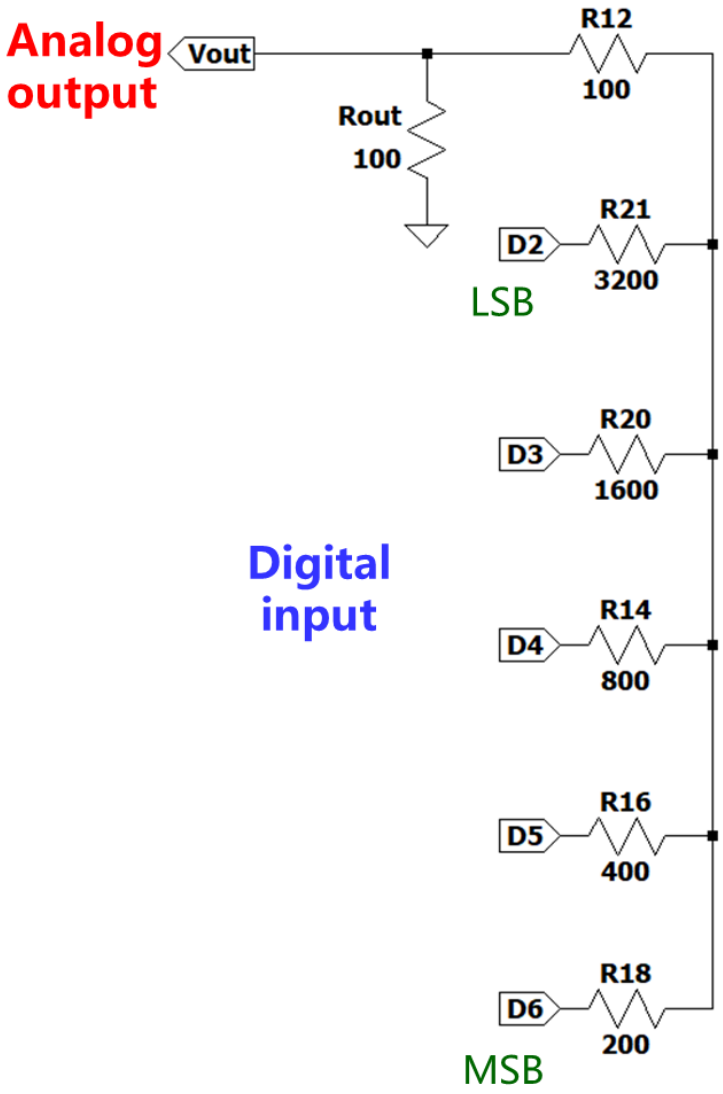


Fig. 25. Decimal data calculation of the10-bit Fibonacci number weighted asynchronous SAR ADC based on the improved Hopfield network.

4.3. DAC Array inside Improved Hopfield Network ADC

Fig. 26 shows the resistive network DAC and its SPICE simulation result, while Fig. 27 explains that the improved Hopfield network ADC has a DAC array.



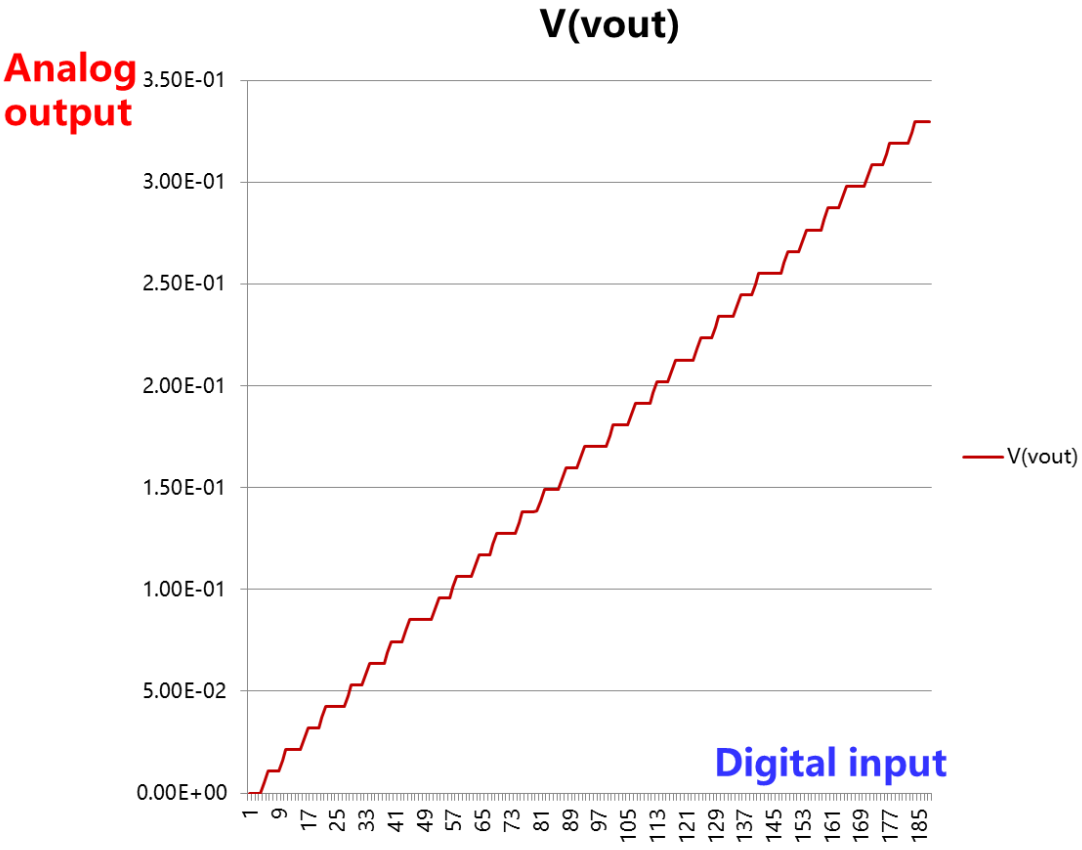


Fig. 26. DAC inside the Hopfield network

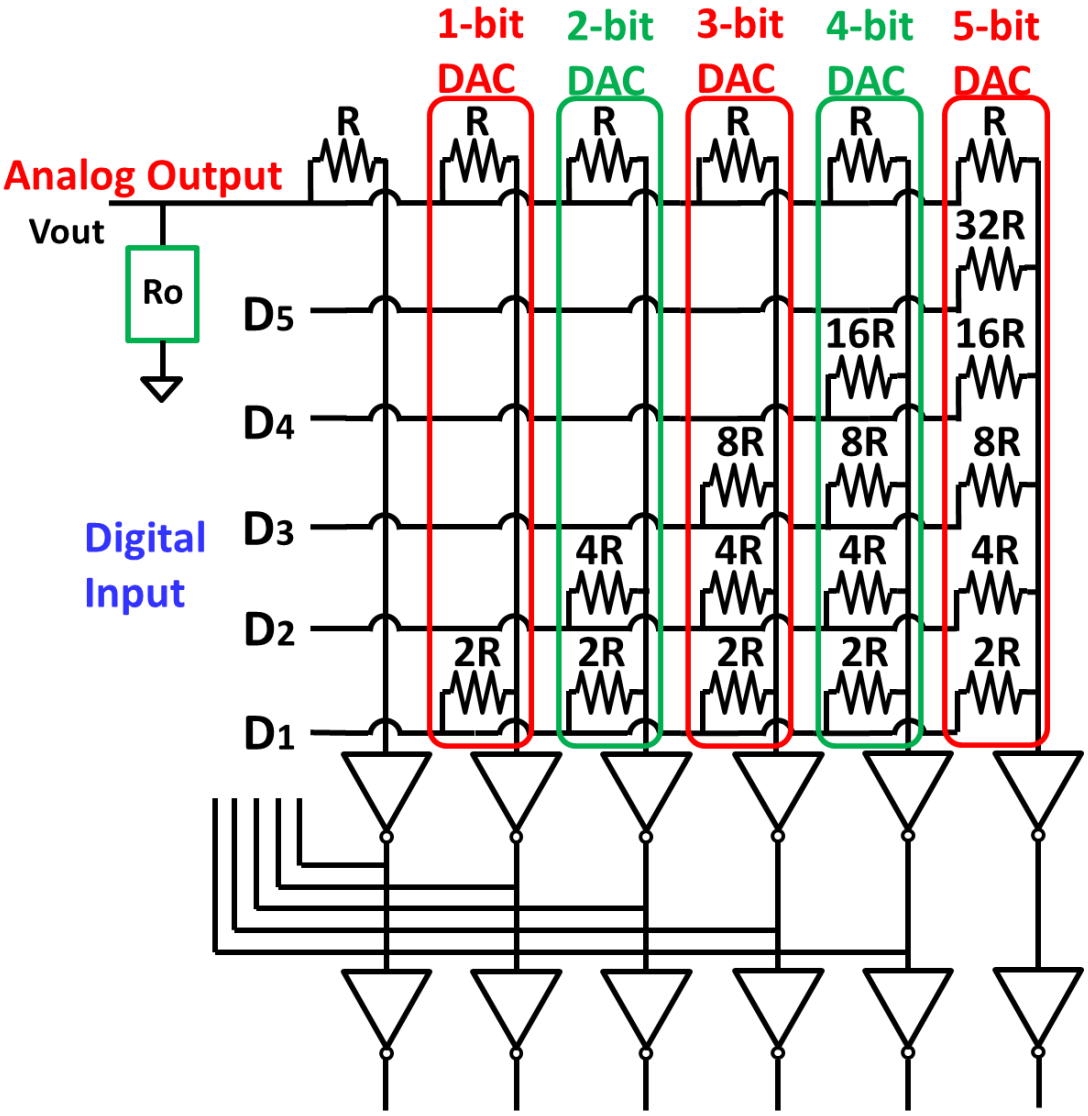


Fig. 27. DAC array inside the improved Hopfield network

5. Conclusion and Discussion

5.1 Discussion

1) Improved Hopfield network ADC.

2) Asynchronous SAR ADC.

   - Very fast

   - Simple design

   - Non-binary as well as binary configurations

   - Competitive to state-of-the-art SAR ADC

   - Verified by SPICE simulation

3) Large resistors with good matching and small chip area.

   ⇒ Technology development is expected.

5.2. Conclusion

This thesis has proposed an improved Hopfield network ADC which does not have feedback paths from lower bits to higher bits. It can avoid the local minima problem and realize an asynchronous SAR ADC with the following advantages: very fast operation, simple design, non-binary as well as binary configurations. Its operation was verified with SPICE simulations. Technology development of large resistors with good matching and small chip area is expected for the proposed SAR ADC to be competitive to the state-of-the-art SAR ADC.

We conclude this paper by remarking that our proposed Hopfield network ADC can be used as a stand-alone SAR ADC competitive to its state-of-the-art, but one of its killer applications would be the multi-bit ADC inside the ΔΣ AD modulator, where high-speed and low-power are mandatory but the nonlinearity due to device mismatches (such as inverter threshold voltage variations) does not matter, thanks to the noise-shaping effects of the modulator.

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List of Publications

[1] Zifei Xu, Xueyan Bai, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Revisit to Hopfield Network for Asynchronous SAR ADC and DAC". 2021 IEEE 3rd International Conference on Circuits and Systems(IEEE ICCS 2021), Chengdu, China (Oct.30-Nov.2, 2021)

[2] Zifei Xu, Xueyan Bai, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Revival of Asynchronous SAR ADC based on Hopfield Network". International Conference on Technology and Social Science 2021(ICTSS 2021), Kiryu, Japan (Dec.7-Dec.9, 2021)

Award

Best Student Presentation Award

Zifei Xu, Xueyan Bai, Dan Yao, Anna Kuwana, Haruo Kobayashi, "Revival of Asynchronous SAR ADC based on Hopfield Network". International Conference on Technology and Social Science 2021 (ICTSS 2021), Kiryu, Japan (Dec.7-Dec.9, 2021)