

DRACO: Co-Optimizing Hardware Utilization, and Performance of DNNs on Systolic Accelerator

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Abstract—The number of processing elements (PEs) in a fixed-sized systolic accelerator is well matched for large and compute-bound DNNs; whereas, memory-bound DNNs suffer from PE underutilization and fail to achieve peak performance and energy efficiency. To mitigate this, specialized dataflow and/or micro-architectural techniques have been proposed. However, due to the longer development cycle and the rapid pace of evolution in the deep learning fields, these hardware-based solutions can be obsolete and ineffective in dealing with PE underutilization for state-of-the-art DNNs. In this work, we address the challenge of PE underutilization at the algorithm front and propose data reuse aware co-optimization (DRACO). This improves the PE utilization of memory-bound DNNs without any additional need for dataflow/micro-architecture modifications. Furthermore, unlike the previous co-optimization methods, DRACO not only maximizes performance and energy efficiency but also improves the predictive performance of DNNs. To the best of our knowledge, DRACO is the first work that resolves the resource underutilization challenge at the algorithm level and demonstrates a trade-off between computational efficiency, PE utilization, and predictive performance of DNN. Compared to the state-of-the-art row stationary dataflow, DRACO achieves 41.8% and 42.6% improvement in average PE utilization and inference latency (respectively) with negligible loss in predictive performance in MobileNetV1 on a 64×64 systolic array. DRACO provides seminal insights for utilization-aware DNN design methodologies that can fully leverage the computation power of systolic array-based hardware accelerators.

Index Terms—Deep neural networks (DNNs), systolic array, PE utilization, latency, energy-efficiency.

Systolic array has become mainstay in hardware-based Deep Neural Network (DNN) accelerators deployed in both edge devices [1] and servers used in data-centers [2], [3]. The systolic array-based architectures enable local communication between neighboring processing elements (PEs) which exploits the inherent parallelism in DNN and adds one extra level in the memory hierarchy of accelerators. This, together with the distributed control logic in systolic architecture, offers an efficient solution for DNN's processing [4].

Concurrently, on the DNN algorithm side, depthwise convolution (DWConv) [5]–[7] has been devised to reduce the number of computations (measured in terms of multiply-accumulation or MAC operations) and parameters. Unlike standard convolution (SConv), where entire channels in a filter are convolved with all input feature maps (ifmaps) and produce one output feature map (ofmap), DWConv allows one

filter-channel to convolve with only one ifmap. Consequently, DWConv exhibits low data reuse and parallelism, which makes DNNs with DWConv as memory-bandwidth bound [8]. The performance and energy efficiency of systolic array-based DNN accelerators rely heavily on certain pre-determined dimensions of convolution (conv) layers and/or feature maps, which helps exploiting high parallelism in large and compute-bound DNNs [9]. However, the reduced shape and size of conv layers, including DWConv, in compact DNNs render most of the PEs underutilized in a fixed-sized systolic accelerator that are designed for large and compute-bound DNNs.

The low PE utilization in systolic array poses three-fold challenges. First, it increases the stall cycles and hence prediction latency, which prohibits inference in real-time. Second, the accelerator does not attain its peak performance and energy-efficiency. Third, the PE underutilization becomes more significant in the larger array sizes and exacerbates the scalability challenge. Fig. 1 shows the experimental results (refer Section III for details on experimental setup) for layer-wise PE utilization on a 64×64 systolic array for MobileNetV1 (MV1). Evidently, the utilization is very high for 1×1 pointwise conv. However, utilization of the 3×3 DWConv is low in initial layers (only $\approx 4\%$) and decreases further in deeper layers due to the reduced size of fmaps. The *key observation* here is, PE utilization depends on both the number of channels in groups and the spatial size of fmaps.

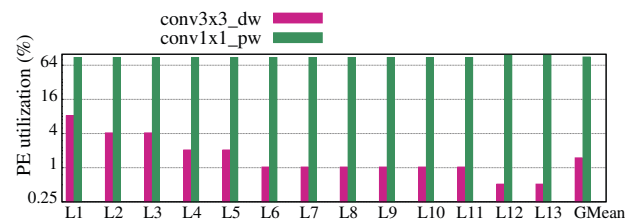


Fig. 1: Layer-wise PE utilization in MobileNetV1

To deal with the aforementioned challenges in DWConv, specialized micro-architecture [2], [9] and dataflow techniques [10], [11] have been proposed. From the general perception in the realm of co-design, a hardware-based solution yields lower return on investment due to prolonged development cycle and lack of flexibility, hence it is used as a last resort. Therefore, we resolve the issue of PE underutilization at the algorithm level and provide generic guidelines for utilization-

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aware DNN design. We seek to answer *whether we can change the architecture of DNN itself such that memory-bound DNNs can efficiently run on the accelerators conventionally designed for large and compute-bound DNNs without any micro-architecture/dataflow modifications?*

In this paper, we propose data reuse aware co-optimization (DRACO) where the number of channels in the groups of fmaps are set to optimize the PE utilization on systolic-array based DNN accelerators. Moreover, by merely fine-tuning the number of channels in the groups of fmaps, DRACO can easily adapt to various sizes of systolic array. Through our extensive experiments, we demonstrate that DRACO *enables substantial improvement in PE utilization on a wide range of systolic array size with a minimal increase in the number of MAC operations and parameters*. We also examine the energy-efficiency implication of DRACO. We find that due to better data reuse in DRACO, the increase in computation increases the access to only local memory (register file or RF) rather than off-chip DRAM. Thus, the increase in total energy consumption is meager. *Interestingly*, we observe that DRACO not only preserves the accuracy of the baseline model, but it can also boost the predictive performance with an appropriate number of channels in the groups of fmaps.

DRACO is applicable to a wide range of DNNs which employ either DWConv or group convolution with a lesser number of channels per group of fmaps. Moreover, it can also be used in the lighter (mobile) version of large DNNs. For instance, in the bottleneck modules of ResNet, 3×3 SConv can be replaced with 3×3 group convolution with an optimal number of channels per group and it can be used as a mobile version of ResNet with high PE utilization on different scales of PEs. Our **contributions** are as follows.

- We implement the DRACO technique to mitigate the low data reuse and PE underutilization in DWConv of memory-bound DNNs.
- We perform an extensive experimentation to understand the interplay of computational complexity and PE utilization with (inference) latency. We reveal that increasing PE utilization at the expense of high computational cost negates the effect of improved utilization and results in suboptimal inference latency.
- We demonstrate the efficacy of DRACO by performing experiments with four different array sizes.
- We perform accuracy experiments on imagenette [12] to show the predictive performance implication of DRACO.

I. RELATED WORK

In Eyeriss v2 [9], hierarchical mesh NoC has been proposed to cater to the high bandwidth requirement for DNNs with low data reuse. Simba [2] deployed Global PE, which performs the near-memory computation for the DNN's layer with low data reuse. The authors in [13] developed an analytical model to efficiently explore the design space and maximize the resource utilization in a systolic array. Liu et al. [11] propose flexible mappings for computation in conv layers to attain high PE utilization. Similarly, Wu et al. [10] implement an

optimized execution order for tiled matrix multiplication to maximize the data reuse in depthwise separable convolution. Kung et al. [14] employ adaptive tiling to reduce the number of tiles required for inference in sparse (unstructured) DNNs. Unlike the aforementioned ad hoc solutions, we change the architecture of DNN itself to achieve a significant gain in PE utilization with a minimum increase in computations and energy consumption. We also study the effect of the proposed algorithmic change on the predictive performance of DNNs.

II. PROPOSED APPROACH

Notations The spatial size of filter (kernel) and fmap are denoted as $d_k \times d_k$ and $d_f \times d_f$ respectively (Table I). For simplicity, we assume the spatial size of ifmap and ofmap are equal. n and m are the number of ifmaps and ofmaps, respectively. The number of ifmaps, and channels in a filter; and the number of filters, and ofmaps are equal. The number of channels (ifmaps) in a group of filters (fmaps) is denoted as G , and the total number of such groups in a conv layer is $\frac{m}{G}$. The number of parameters and activations (input and output together) are denoted as $\#Param$ and $\#Act$, respectively. In Table I, data reuse is estimated as arithmetic intensity of the layer ($DataReuse = \frac{\#MACs}{\#Param + \#Act}$). We separately calculate the data reuse for filter-weights as $W_{reu} = \frac{\#MACs}{\#Param}$. Also, data reuse for input/output activations is $A_{reu} = \frac{\#MACs}{\#Act}$.

A. Data Reuse Bottleneck in Depthwise Convolution

In comparison with standard convolution (SConv), DWConv ($G=1$) reduces both the number of MAC operations and parameters by a factor of n (Table I) which is significant especially in deeper layers where n is very high. However, the data reuse of DWConv is very low compared to SConv. As shown in Table I, the W_{reu} is the same in DWConv and SConv; whereas, A_{reu} of the former is reduced by a factor of n . For example, as illustrated in Fig. 2, W_{reu} of 3×3 DWConv and 1×1 SConv in MobileNetV1 are same; however, A_{reu} in the former is significantly lower than the latter. Also, this disparity in A_{reu} grows in deeper layers. Note that A_{reu} is *more critical* than W_{reu} because W_{reu} increases with increasing input batch size, while A_{reu} does not [8].

TABLE I: Data reuse comparison

Metric	SConv	DWConv	DRACO
#MACs	$m \times n \times d_k^2 \times d_f^2$	$m \times d_k^2 \times d_f^2$	$G \times (n \times d_k^2 \times d_f^2)$
#Param	$m \times n \times d_k^2$	$m \times d_k^2$	$G \times (n \times d_k^2)$
#Act	$(m+n) \times d_f^2$	$(m+n) \times d_f^2$	$(m+n) \times d_f^2$
DataReuse	$\frac{m \times n \times d_k^2 \times d_f^2}{m \times n \times d_k^2 + (m+n) \times d_f^2}$	$\frac{m \times d_k^2 \times d_f^2}{m \times d_k^2 + (m+n) \times d_f^2}$	$\frac{m \times d_k^2 \times d_f^2}{m \times d_k^2 + \frac{(m+n)}{G} \times d_f^2}$
W_{reu}	$\frac{d_f^2}{d_k^2}$	$\frac{d_f^2}{d_k^2}$	$\frac{d_f^2}{d_k^2}$
A_{reu}	$n \times \left(\frac{m}{m+n}\right) d_k^2$	$\left(\frac{m}{m+n}\right) d_k^2$	$G \times \left(\frac{n}{m+n}\right) d_k^2$

Dataflow techniques are selected to maximize the data reuse of a particular data type in DNN. For example, weights and partial sum reuse are maximized in weight stationary and output stationary dataflow [4]. In initial layers, W_{reu} is higher and decreases in the deeper layer, whereas A_{reu} is higher in deeper layers and decreases in layers towards input. Consequently, none of the dataflows can be optimal for all the layers in a DNN. In other words, due to the lower number

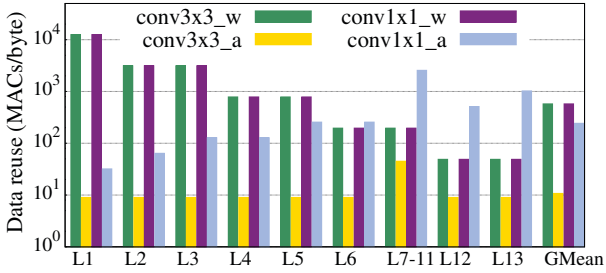


Fig. 2: Weight reuse in 3×3 DWConv (conv3x3_w), and 1×1 convolution (conv1x1_w); activation reuse in 3×3 DWConv (conv3x3_a), and 1×1 convolution (conv1x1_a)

of filter-channels (or ifmaps) in the initial layers and smaller fmap size in deeper layers, PE underutilization happens in the respective layers. This underutilization is further aggravated in DWConv due to the very low A_{reu} .

B. Data Reuse Aware Co-optimization (DRACO)

First, we employed state-of-the-art dataflow, *row stationary* [4], which is adaptable to different shapes and sizes of filters/ifmaps, thus, enables optimal energy-efficiency and throughput for a DNN. As illustrated in Fig. 1, the PE utilization of 1×1 conv with row stationary dataflow is well-above of $\approx 80\%$ and independent of the layer's position in DNN. However, in the case of DWConv, PE utilization is substantially lower ($\leq 4\%$) on large array size (64×64) and *more importantly, it reduces in deeper layers*. That is, even with row stationary dataflow, when the number of channels in a group is deficient, then PE utilization depends on the spatial size of fmaps, and hence it decreases in deeper layers.

To address the shortcomings of row stationary dataflow and to enable high PE utilization in DWConv, we propose data reuse aware co-optimization (DRACO) where we increase the G , which in turn increases A_{reu} (Table I). Since PE underutilization becomes more significant with larger array size, by fine-tuning G , DRACO can adapt to larger array size. Increasing G also increases the number of MAC operations, but, increases the data reuse and decreases the bandwidth pressure. In other words, DRACO adds more #MACs to a bandwidth bound DNN without increasing the bandwidth demand and substantially improves the PE utilization.

III. EXPERIMENTAL EVALUATION

In this section, we detail the experimental setup and elaborate on our findings. We present the insights as key takeaway messages, which can enable a better methodology for latency optimization in DNNs.

A. Experimental Setup

Eyeriss simulator We take Eyeriss, a systolic array-based inference accelerator for DNNs [1], as a baseline architecture and modify the Eyeriss simulator [15], [16] to perform our experiments. Table II shows the on-chip memory (global buffer and register file) sizes for different PE array sizes. Consistent with Chen et al. [4], the memory cost for accessing the DRAM

(off-chip), global buffer (on-chip SRAM), array (inter-PE), and register file (local scratch-pad) are modeled as $\{200, 6, 2, 1\} \times 10^{-12}$ joules, respectively. Since inference is latency-critical, we take batch size as one for all the experiments. TABLE II: Configuration of on-chip memories in Eyeriss simulator for different array sizes

Memory size	16x16	32x32	64x64	128x128
GBuf (KiB)	128	256	512	1024
RF per PE (KiB)	0.5	0.5	0.5	0.5
Total RF size (KiB)	128	512	2048	8192

Baseline model and dataset DWConv ($G=1$) is a popular technique to reduce the computation in both manual design and automated design of DNNs [17]. We use MobileNetV1 [5], widely deployed on mobile platforms, as a baseline model because all of its layers with 3×3 conv (except very first layer) employ DWConv. In MobileNetV1, all 3×3 conv layers are followed by a 1×1 conv layer, and it bears a resemblance to a widely deployed building block: bottleneck module [18]. Therefore, the findings obtained for MobileNetV1 also apply to an extensive range of DNNs.

To understand the interplay of compute efficiency and PE utilization with inference latency, we perform experiments on MobileNetV1 with different values of width multiplier (α) and input resolution multiplier (ρ) [5]. The physical significance of α , ρ , and G are illustrated in Fig. 3. Changing α changes both the number of parameters and MACs whereas ρ changes only the number of MACs. As the number of channels in first 3×3 DWConv layer of MobileNetV1 is 32, we perform our experiments for $G=1$ to $G=16$ for $\alpha=0.5$, $G=1$ to $G=32$ for $\alpha=1$ and $G=1$ to $G=64$ for $\alpha=2$. Table III shows the number of MACs and parameters with different values of α and ρ . Note that to accommodate larger fmaps in the case of MobileNetV1 with $\rho=2$, we double the on-chip memory (GBuf and RF per PE) capacity shown in Table II.

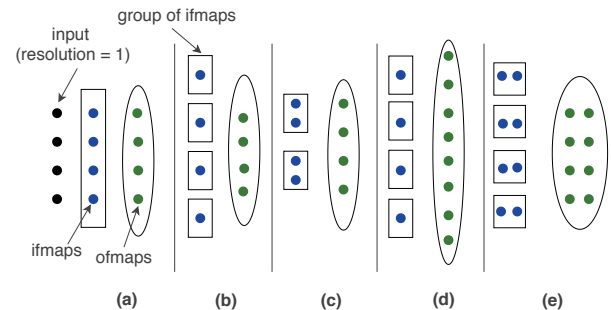


Fig. 3: Comparison of (a) SConv with (b) MobileNetV1 ($\alpha=1$, $\rho=1$, $G=1$); and other MobileNetV1 variants with (c) $\{\alpha=1, \rho=1, G=2\}$, (d) $\{\alpha=2, \rho=1, G=1\}$, and (e) $\{\alpha=1, \rho=2, G=1\}$

We measure the predictive performance of DNNs as the prediction accuracy on the image classification task. We train our models from scratch (i.e. no pre-training), without any data augmentation techniques, on Imagenette dataset [12] with input crop size 224×224 for 150 epochs. Imagenette is a subset of 10 classes from the popular benchmark dataset ImageNet. Note that all the reported top-1 accuracy are average of three runs to avoid the effect on noise on accuracy.

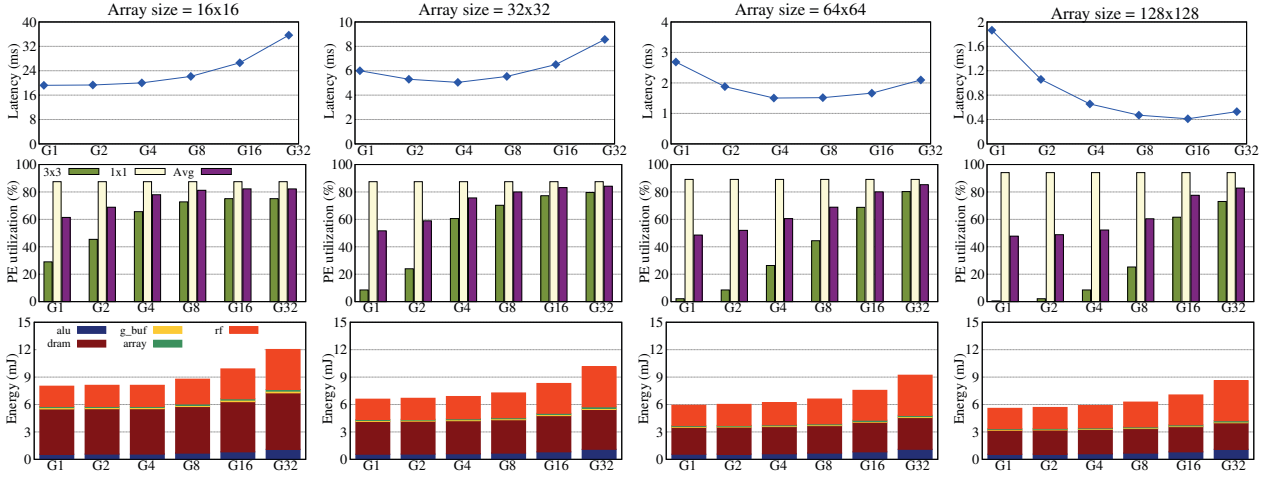


Fig. 4: Results for MobileNetV1 ($\alpha=1, \rho=1$): In top row latency; in middle row PE utilization for 3×3 conv, 1×1 conv, and average utilization; and in bottom row total energy consumption in terms of ALU (alu), DRAM (dram), global buffer (g_buf), systolic array (array), and register file (rf) accesses energy with variations in G and systolic array size are shown.

TABLE III: MACs (in Millions) and param (#parameters in Millions) variations in MobileNetV1 with different α and ρ

	Metric	G1	G2	G4	G8	G16	G32	G64
(a) Baseline MobileNetV1 ($\alpha=1, \rho=1$)								
	MACs	569	586	621	690	830	1108	-
	Param	4.21	4.25	4.34	4.52	4.88	5.59	-
(b) MobileNetV1 with different values of α (ρ set to 1)								
$\alpha=0.5$	MACs	147	156	173	208	278	-	-
	Param	1.82	1.83	1.85	1.9	1.99	-	-
$\alpha=2$	MACs	2237	2272	2341	2481	2759	3315	4428
	Param	13.76	13.94	14.3	15.01	16.44	19.3	25.01
(c) MobileNetV1 with different values of ρ (α set to 1)								
$\rho=0.5$	MACs	143	147	156	173	208	278	-
	Param	4.21	4.25	4.34	4.52	4.88	5.59	-
$\rho=2$	MACs	2272	2341	2481	2759	3315	4428	-
	Params	4.21	4.25	4.34	4.52	4.88	5.59	-

B. Results

PE utilization and latency In middle row of Fig. 4, we show utilization for 1×1 and 3×3 convolutions separately. The reported “average” PE utilization is arithmetic mean of that of the all conv, FC, pooling layers in MobileNetV1. At $G=1$, the PE utilization of MobileNetV1 on the smaller array is well above 50%; however, it reduces on scaling up the array size. For example, the average PE utilization of MobileNetV1 on 16×16 array is 61.4% while that on 128×128 array is 47.8%. Across all the array sizes, the PE utilization for 1×1 conv is well above 80%, however, it is substantially low for 3×3 conv and further decreases with higher array size (e.g., 29% on 16×16 array, and only 2.1% on 64×64 array). Increasing the number of channels in each group (i.e., G) of 3×3 DWConv improves PE utilization. The overall utilization reaches $\approx 80\%$ on 16×16 and 32×32 arrays at $G=8$. By contrast, on 64×64 and 128×128 arrays, utilization reaches $\approx 80\%$ at $G=16$.

As shown in Table III(a), increasing G increases the number of computations and hence, the latency on 16×16 array increases with higher G . However, on larger array sizes, the latency first decreases and reaches minima and further increases with an increase in G . On larger array sizes, PE underutilization becomes significant, and utilization improves

with an increase in G . Hence, the latency starts decreasing initially and reaches a minimum value; however, it further increases as the number of MACs becomes significantly higher. Clearly, at lower G , PE underutilization is significant, and once the utilization is sufficiently high ($\approx 80\%$), the latency is driven by the computational complexity of DNN. Notice that with the increase in array sizes, the minima in latency curve shifts towards the right, i.e., towards higher G . This happens because a higher number of channels is required to utilize the higher number of PEs on a larger array. Hence, the latency is driven by PE utilization, and better PE utilization overweighs the effect of the increase in computational complexity, up to a certain value of G .

Key takeaway 1: *The optimum latency is driven by both the PE utilization as well as the computational complexity of DNN, and the effect of PE utilization on latency depends on PE array size in the systolic accelerator.*

We plot the total energy consumption with different G values to see the energy overhead of increasing G (bottom row in Fig. 4). Since increasing G leads to a gradual increase in the number of computations, there is a negligible increase in the inference energy up to a group size of $G=8$. Moreover, increasing G causes better data locality, and hence, the increase in computation results only in more number of access to RF rather than DRAM. Thus, even at a higher G , the overall increase in energy is not substantial.

Effects of changing the number of filters We set $\alpha = 0.5$ to halve the number of filters in all the layers and set $\alpha = 2$ to double the number of filters. Since changing α does not change the number of channels per group, the PE utilization remains the same across different values of α (middle row in Fig. 5). For $\alpha=0.5$, latency decreases sharply at initial values of G and remains constant at higher G . However, for $\alpha=2$, latency decreases gradually and starts increasing at higher G . Since the number of MACs in MobileNetV1 with $\alpha=0.5$ is quite

low (Table III(b)), the latency is driven only by PE utilization and it remains constant at higher G . However, at higher G with $\alpha=2$, the number of MACs is very high, which results in increased latency. For all values of G , the absolute values of latency and energy are significantly higher at $\alpha=2$ compared to those at $\alpha=0.5$. This is because the number of MACs and parameters are much higher for $\alpha=2$ (Table III(b)).

Key takeaway 2: *The extent to which PE utilization affects the latency also depends on the total number of MACs in DNN. In a DNN with very few MACs, the latency depends only on PE utilization.*

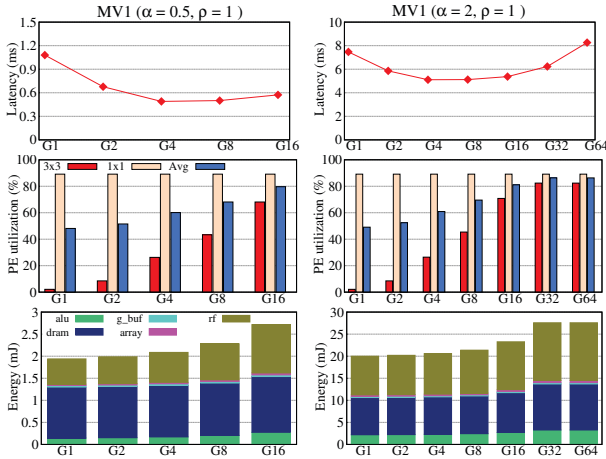


Fig. 5: Results for MobileNetV1 with $\alpha = 0.5$ (left column), and $\alpha = 2$ (right column) on 64×64 PE array: In top row latency; in middle row PE utilization; and in bottom row total energy consumption variations with different G are shown.

Effects of changing input resolution We change ρ to 0.5 and 2 to increase and decrease (respectively) the spatial size of the input image. Changing the input resolution changes the spatial size of fmaps in all the layers, which, in turn, affects the PE utilization. As shown in Fig. 6, due to the higher spatial size of fmaps at $\rho=2$, PE utilization is higher than that at $\rho=0.5$. With $\rho=0.5$, the latency decreases sharply at lower G , then reaches the minimum value at $G=8$ and $G=16$, and then starts increasing at higher G . However, with $\rho=2$, latency decreases gradually at lower G , then reaches a minimum at $G=4$, and then starts increasing sharply at higher G . In other words, with an increasing value of ρ (from 0.5 to 2), the minima in the latency curve shift towards left (i.e., towards lower G).

Thus, when utilization is improved by employing fmap with larger spatial size in a DNN ($\rho=2$), then benefit of better PE utilization is overshadowed by a substantial increase in computation (Table III(c)). For instance, even when a gain in PE utilization from $G=4$ to $G=16$ is $\approx 27\%$, the latency is increased by $\approx 23\%$. However, with $\rho=0.5$, the number of MACs is quite low, and the effect of PE utilization on latency is noticeable. The absolute latency and energy values with $\rho=2$ are substantially higher than those with $\rho=0.5$ due to the higher computational complexity in the former.

Key takeaway 3: *Increasing PE utilization at the expense of*

a substantial increase in the number of computations does not lead to lower latency, and the effect of higher PE utilization is dominated by the number of computations.

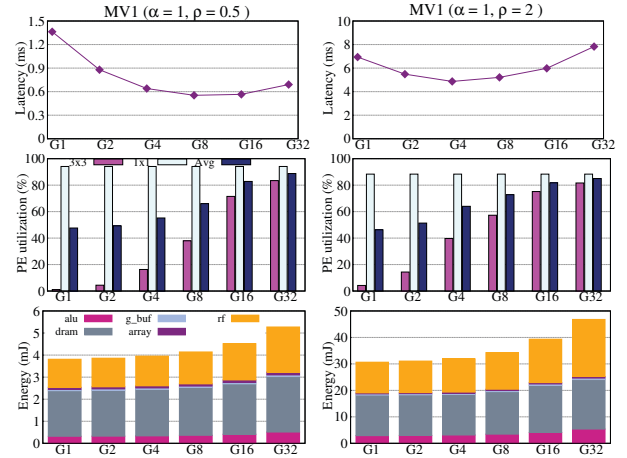


Fig. 6: Results for MobileNetV1 with $\rho = 0.5$ (left column), and $\rho = 2$ (right column) on 64×64 PE array: In top row latency; in middle row PE utilization; and in bottom row total energy consumption variations with different G are shown.

C. Proposed Alternative for Latency Optimization

So far, we have seen that increasing PE utilization by employing more number of channels in each group of a DNN decreases the latency at the cost of a gradual increase in computations. However, increasing PE utilization at the expense of a substantial increase in computation (e.g., MobileNetV1 with $\rho=2$) does not effectively reduce the latency of a DNN. Now, we propose a better alternative for increasing PE utilization, which also reduces the latency more effectively.

MobileNetV1 with $\alpha=0.5$ and $\rho=2$ The PE utilization depends on the number of channels and the spatial size of fmaps in a group. Hence, scaling the number of filters (using α) in the layers of a DNN changes only the computational complexity and does not alter the PE utilization. We propose to use α to reduce the computational complexity of MobileNetV1 with higher ρ . The appropriate value of α depends on the additional gain in computational complexity, i.e., in a proportion of ρ . Here, we set $\alpha=0.5$ to offset the gain in computational complexity in MobileNetV1 with $\rho=2$ without hampering the PE utilization. This reduces the number of MACs by $\approx 4\times$ and the number of parameter by a factor of $\approx 2.5\times$ (Table III(c) and Table IV). The substantial reduction in both the number of MACs and parameters leads to an improvement in both energy efficiency and latency for all the values of G (Table V). This improvement is higher on smaller array sizes because the effect of computational complexity on latency is significant when the array size is smaller. However, the effect of PE utilization on latency is significant on a larger array.

Key takeaway 4: *The computational complexity of a DNN can be reduced without affecting the PE utilization. At constant PE utilization, the effect of computational complexity on latency is quite significant on smaller array sizes.*

TABLE IV: Number of MACs and parameters in MobileNetV1 with $\alpha = 0.5$, and $\rho = 2$

Metric	G1	G2	G4	G8	G16
#MACs (M)	586	621	690	830	1108
#Params (M)	1.82	1.83	1.85	1.90	1.99

TABLE V: Performance comparison of MobileNetV1 versions $\{\alpha = 1$, and $\rho = 2\}$ and $\{\alpha = 0.5$, and $\rho = 2\}$

Model	Array size	Metric	G1	G2	G4	G8	G16
MV1 $\alpha=1$, $\rho=2$	16x16	PE util. (%)	68	77	79	79	80
		Latency (ms)	66.5	67.7	72.1	81.1	99.2
		Energy (mJ)	59.7	60.1	61.0	63.7	69.3
	32x32	PE util. (%)	56	65	77	82	83
		Latency (ms)	18.8	17.8	18.2	20.1	24.4
		Energy (mJ)	37.2	37.6	38.4	41.1	46.6
	64x64	PE util. (%)	50	55	66	74	83
		Latency (ms)	6.9	5.5	4.9	5.2	6.0
		Energy (mJ)	30.6	31.1	31.9	34.3	39.3
	128x128	PE util. (%)	46	48	54	64	77
		Latency (ms)	4.0	2.5	1.7	1.5	1.6
		Energy (mJ)	27.2	27.6	28.5	30.2	33.9
MV1 $\alpha=0.5$, $\rho=2$	16x16	PE util. (%)	68	76	79	79	80
		Latency (ms)	17.8	18.3	20.5	25.1	34.1
		Energy (mJ)	17.5	17.7	18.2	19.5	21.6
	32x32	PE util. (%)	55	65	77	82	83
		Latency (ms)	5.5	5.0	5.2	6.2	8.3
		Energy (mJ)	11.9	12.1	12.5	13.9	15.9
	64x64	PE util. (%)	49	54	66	73	81
		Latency (ms)	2.5	1.8	1.5	1.7	2.1
		Energy (mJ)	10.3	10.5	10.9	12.1	14.1
	128x128	PE util. (%)	45	47	52	63	76
		Latency (ms)	1.8	1.0	0.6	0.5	0.5
		Energy (mJ)	9.2	9.4	9.8	10.7	12.4

D. Implication on Prediction Accuracy

We now investigate the ramification of changing G on the predictive performance of DNN. As shown in Table VI, the top-1 accuracy of baseline MobileNetV1 ($\alpha=1$, $\rho=1$) increases for lower values of G , reaches a maximum value at $G=4$, then starts decreasing at higher G . The DWConv only captures the spatial correlation, and the following 1×1 convolution captures the channel correlation [19]. That is, employing only one channel in a group (in DWConv) captures only one variation of a visual concept in the ofmaps. By contrast, increasing the number of channels in the groups of a filter captures more variations of a single visual concept, which, in turn, boosts the representational power of the network and improves the accuracy [20]. Also, at lower G , each ofmap is connected to very few ifmaps and serves as a strong regularizer, which in turn improves the generalization in DNN. Therefore, once the groups get a sufficient number of channels to capture the variations of the visual concepts, the effect of regularization becomes significant. Hence, at higher G , top-1 accuracy starts decreasing due to weaker regularization.

TABLE VI: Top-1 accuracy (on Imagenette) for MobileNetV1 with different α and ρ

Models	G1	G2	G4	G8	G16	G32
MV1 ($\alpha=1$ $\rho=1$)	84.08	84.55	84.65	83.46	83.40	79.94
MV1 ($\alpha=1$ $\rho=2$)	84.76	84.55	84.17	84.81	83.29	82.90
MV1 ($\alpha=0.5$ $\rho=2$)	82.61	83.54	83.70	82.71	82.29	-

Note that for larger input size higher G is required to capture more variations of a visual concept. Therefore, top-1 accuracy

in MobileNet-V1 with $\rho=2$ is maximum at $G=8$ (Table VI). However, DNNs with very few parameters result in underfitting at $G = 1$, hence top-1 accuracy in MobileNet-V1 with $\alpha=0.5$, and $\rho=2$ is lower at $G=1$ and starts increasing from $G=2$. The difference between the top-1 accuracy of MobileNetV1 with $\{\alpha, \rho\} = \{0.5, 2\}$, and $\{1, 2\}$ is minimum at $G=4$. Also, the latency is minimum at same G on a 64×64 array (Table V). Hence, $G=4$ is a sweet spot for both optimum latency and prediction accuracy. In summary, our proposed alternative for latency optimization in MobileNetV1 with $\rho=2$ does not hamper the accuracy, provided groups in DNN have sufficient G to capture the variations in concepts.

IV. CONCLUSION

In this paper, we presented a data reuse aware co-optimization approach (DRACO) for improving the PE utilization on systolic accelerators for memory-bound DNNs. We explained the role of computational complexity, PE utilization, and array size of the systolic accelerators on (inference) latency optimization. We demonstrated that improving PE utilization does not always improve the performance of a DNN; it also depends on the computational overhead of improving PE utilization. Our approach to improving PE utilization also boosts the predictive performance of DNNs.

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