J Comput Electron (2012) 11:303–314
DOI 10.1007/s10825-012-0406-y

Semi-analytical modeling of Ag and Au nanoparticles and fullerene (C60) embedded gate oxide compound semiconductor MOSFET memory devices

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Published online: 24 May 2012
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Abstract In this paper we present an analytical simulation study of Non-volatile MOSFET memory devices with Ag/Au nanoparticles/fullerene (C60) embedded gate dielectric stacks. We considered a long channel planar MOSFET, having a multilayer SiO_2–HfO_2 (7.5 nm)–Ag/Au nc/C60 embedded HfO_2 (6 nm)–HfO_2 (30 nm) gate dielectric stack. We considered three substrate materials GaN, InP and the conventional Si substrate, for use in such MOSFET NVM devices. From a semi-analytic solution of the Poisson equation, the potential and the electric fields in the substrate and the different layers of the gate oxide stack were derived. Thereafter using the WKB approximation, we have investigated the Fowler-Nordheim tunneling currents from the Si inversion layer to the embedded nanocrystal states in such devices. From our model, we simulated the write-erase characteristics, gate tunneling currents, and the transient threshold voltage shifts of the MOSFET NVM devices. The results from our model were compared with recent experimental results for Au nc and Ag nc embedded gate dielectric MOSFET memories. From the studies, the C60 embedded devices showed faster charging performance and higher charge storage, than both the metallic nc embedded devices. The nc Au embedded device displayed superior characteristics compared to the nc Ag embedded device. From the model GaN emerged as the overall better substrate material than Si and InP in terms of higher threshold voltage shift, lesser write programming voltage and better charge retention capabilities.

Keywords Long channel MOSFET · Non-volatile memory · C60 · Ag nanocrystal · Au nanocrystal

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1 Introduction

The application of nanocrystals embedded in the gate dielectrics of MOS memory devices, to improve the performance has been a topic of continued interest [1–4]. The embedding of various semiconducting (like Si, Ge) and metallic (like Ni, Ag, W, Au) nanocrystals in the gate dielectrics of MOS NVMs have been studied in this regard [2, 3]. The physically separated nanoparticles/nanocrystals (ncs) present within the host dielectric, act as a charge trap sites, effectively working as a floating gate, in such devices. These nc embedded oxides have shown superior performance, in terms of better programming-erase performance, higher Fowler-Nordheim (F-N) currents, lesser write voltages and longer charge retention compared to conventional MOS memories [1–6].

From the various experimental studies, it has been firmly established that metallic nanoparticles offer more advantages than semiconducting ones, for this sort of devices. In recent studies Ag and Au ncs have shown good performance and reliability as embedded nanoparticles in MOS NVMs. With the emergence of carbon based nanomaterial

like fullerenes (C60), CNTs, Carbon nanofibres etc. as potential electronic materials, study is needed on the applicability of such ncs in the gate dielectrics of MOS NVMs. Though there have been reports on CNT embedded gate oxide MOS memories [7], the use of such high aspect ratio cylindrical/wire shaped nanomaterials poses a serious challenge from the fabrication and the reliability perspective. One of the most difficult aspect of using CNTs or nanowires in gate dielectric of MOS NVMs is to prevent them from touching each other, which is essential for minimizing the charge leakage via lateral diffusion. Among the carbon based nanomaterial, C60 can be a fit candidate for embedding in gate oxide stacks of memory devices. This is due to its spherical size and smaller diameter, high work function and possible compatibility with ion-implantation process for embedding in the gate dielectric. Therefore it can be of significant interest to study and compare the performance of a C60 embedded gate oxide MOSFET memory device, with their metallic nc (Ag and Au) embedded counterparts.

Also a number of experimental and theoretical studies in recent years have shown interest in the use of compound semiconductors like InGaAs, GaN, InP etc. as substrate materials to potentially replace the Silicon substrate in certain MOSFET applications [8–11]. The compound semiconductors show certain advantages over Si MOSFETs owing to their higher electron mobility, higher density of states in the conduction band, possibility of band-gap engineering etc. However, the memory performance of such compound semiconductor MOSFETs, are a rather less explored area. Only very few reports are available to date on the application of compound semiconductors for memory applications [12–15]. In fact there has been little/no work done in the area of comparative performance of compound semiconductor MOSFET NVMs having C60 embedded gate dielectric. Therefore computational studies on the application of nanocrystal embedded gate dielectric compound semiconductor NVM devices, could act as a pointer for further experimental studies in this area.

In this work we study and compare the performance of nc-Ag/Au/C60 embedded multilayer gate dielectric long channel planar MOSFET NVM devices, using Si/GaN /InP/InGaAs as the substrate materials. The MOSFET NVM has been considered to have a multilayer gate dielectric with a stacked 5 nm SiO_2–2.5 nm HfO_2 tunnel oxide (7.5 nm), 6 nm nc-Ag/Au/C60 embedded HfO_2 layer, followed by a 30 nm HfO_2 layer working as a control oxide. The device dimensions for our studies have been chosen so as to in the same range with recently fabricated advanced MOSFET memories [5, 6]. In our work we evaluated the MOSFET surface potentials, the energy band diagram of the NVM, the electron tunneling characteristics (and from this the write/programming voltage), and the transient threshold voltage shifts of the device under consideration. We also modeled how the applied gate voltage impacts the threshold voltage shift due to nanocrystal charging, and investigated the erasing characteristics under a suitable reverse gate bias.

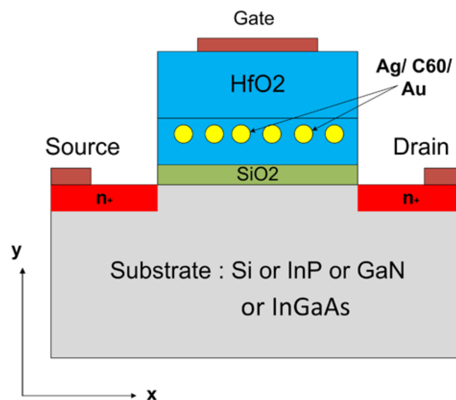

Fig. 1 Schematic diagram (not to scale) of the device under consideration

2 Analytical modeling

In Fig. 1 we have shown the schematic diagram (not to scale) of the device under consideration. We consider a long channel MOSFET, having $n+$ source and drain. The channel thickness was considered to be 20 nm (d_{Si}) and the channel length (L) was 100 nm. The positions of the SiO_2 tunnel oxide (d_1), HfO_2 tunnel oxide (d_2), nc embedded nitride (d_3) and the SiO_2 control oxide (d_4) were considered to be 25 nm, 27.5 nm, 33.5 nm, and 63.5 nm respectively. Which gives the thicknesses of the consecutive layers to be 5 nm (t_1), 2.5 nm (t_2), 6 nm (t_3) and 30 nm (t_4) respectively. The nanocrystals of 5 nm diameter were assumed to lie uniformly distributed within the 6 nm nc embedded HfO_2 layer. On top of it we considered an Aluminum metal gate. The device dimensions used in this paper have been chosen so as to be in the same range as with recently fabricated MOSFET memories [5, 6].

2.1 Surface potential evaluation

We now move towards finding out the surface potential in the Si substrate which would act as the starting point. For $y < d_{Si}$, considering only the mobile charge carriers in the Silicon the Quasi-1D Poisson's equation is given by [16–18]

$$\frac{\partial^2 \varphi_0(y)}{\partial y^2} = \frac{q n_i}{\epsilon_{Si}} \cdot \exp\left[\frac{q(\varphi_0(y) - V)}{kT}\right] \tag{1}$$

where $\varphi_0(y)$ stands for the potential in the Si substrate, n_i is the intrinsic carrier concentration in the channel, $V = 0$ at the source end ($x = 0$) and $V = V_{DS}$ at the drain ($x = L$)

and ϵ_{Si} being the dielectric constant of the Si substrate. The other symbols having their usual meanings in the above equation. The boundary conditions for the above equation are given by

$$\varphi_0(y)|_{y=d_{Si}} = \varphi_S \tag{2}$$

$$\left.\frac{d\varphi_0(y)}{dy}\right|_{y=d_{Si}} = -\frac{C_{eff}}{\epsilon_{Si}}\left[V_G - \frac{q\Lambda_C(\tau)}{\epsilon_{ox}} - \Phi_{ms} - \varphi_S\right] \tag{3}$$

In (2)–(3) the term φ_S represents the surface potential, V_G is the applied gate voltage, $q\Lambda_C(\tau)$ stands for the areal charge density (Coul/m^2) accumulated in the nc embedded layer in time τ, Φ_{ms} stands for the gate metal-oxide work function difference. The capacitance C_{eff}, denotes the effective capacitance of the multilayer gate oxide stack. To compute C_{eff}, we apply the Maxwell-Garnett effective medium approximation to evaluate the effective dielectric constant of the gate oxide stack. Considering the nanocrystals to be spherical in shape and to be uniformly dispersed within the HfO_2 layer, the effective dielectric constant of embedded layer comes out to be [19]

$$\epsilon'_{embed} = \frac{\epsilon_{HfO_2} \times \{2\nu(\epsilon_{nc} - \epsilon_{HfO_2}) + (\epsilon_{nc} + 2\epsilon_{HfO_2})\}}{\epsilon_{nc} + 2\epsilon_{HfO_2} - \nu(\epsilon_{nc} - \epsilon_{HfO_2})} \tag{4}$$

where υ stands for volume fraction of nanocrystal in the nitride layer, ϵ_{nc} stands for the nanocrystal dielectric constant of nc Si or nc Au. Here, ϵ_{HfO_2} stands for the nitride dielectric constant. From this we have the capacitance of the nc embedded layer as

$$C_{embed} = \frac{\epsilon_{embed}}{t_3} \tag{5}$$

Thereafter considering the capacitances of the different layers of dielectrics, we calculate the effective gate dielectric capacitance as

$$C_{eff} = \left[\frac{1}{C_{tox1}} + \frac{1}{C_{tox2}} + \frac{1}{C_{embed}} + \frac{1}{C_{cox}}\right]^{-1} \tag{6}$$

In (7) C_{tox1}, C_{tox2} and C_{cox} stand for the capacitances of the tunnel oxide (SiO_2 layer), tunnel oxide (HfO_2 layer) and the control oxide layers respectively. In order to evaluate the electron effective mass in the composite gate dielectric, we may consider the electron effective mass of the nc-Ag/Au or C60 embedded layer to be,

$$m_{embed} = m_{NC} \cdot \upsilon + m_{HfO_2} \cdot (1 - \upsilon) \tag{7}$$

m_{NC} is the electron effective mass in the nc-Ag/nc-Au/C60, whereas m_{HfO_2} is the electron effective mass in the HfO_2. Thereafter, considering a single electron relaxation time throughout the entire gate dielectric, we get the effective mass of the composite gate dielectric [19],

$$m_{eff} = m_{embed} \cdot \frac{t_{embed}}{t_{total}} + m_{SiO2} \cdot \frac{t_c + t_{tox1}}{t_{total}} + m_{HfO2/La2O3} \cdot \frac{t_{tox2}}{t_{total}} \tag{8}$$

We now proceed to solve (1) using the boundary conditions (2)–(4). Initially considering the nanocrystal embedded layer to contain a constant charge $N'_c = N_C(\tau_0)$ at a certain instant of time τ_0, and following Langevelde [17], and Chen [18] we arrive at the implicit relation

$$V_{GB} - \Phi_{ms} - \frac{qN_C(\tau)}{t_3} - \varphi_s = \gamma\left[\varphi_s + \upsilon_t\left(e^{-\varphi_s/\upsilon_t} - 1\right) + \upsilon_t \cdot \exp\left(-\frac{V - 2\varphi_F}{\upsilon_t}\right) \cdot \left(e^{\varphi_s/\upsilon_t} - 1\right)\right]^{1/2} \tag{9}$$

where $\upsilon_t = (k_B T/q)$ is the thermal potential, and φ_F is the bulk Fermi potential, and γ is the body factor, defined by $\gamma = \sqrt{2q\epsilon_{eff}N_A}/C_{eff}$. Thereafter, we arrive at the expression for the surface potential

$$\varphi_S = 2\varphi_F + V + \upsilon_t \cdot \ln\left[\frac{1}{\upsilon_t} \cdot \left\{\left(\frac{V_{GB} - \Phi_{ms} - \frac{qN_C(\tau)}{t_3} - \phi'}{\gamma}\right)^2 - 2\varphi_F - V + \upsilon_t\right\}\right] \tag{10}$$

where ϕ' stands for

$$\phi' = 2\varphi_F + V + \frac{(\sqrt{V_{GB} - \Phi_{ms} - \frac{qN_C(\tau)}{t_3} + \frac{\gamma^2}{4}} - \frac{\gamma}{2})^2 - 2\varphi_F - V}{\sqrt{1 + [(\sqrt{V_{GB} - \Phi_{ms} - \frac{qN_C(\tau)}{t_3} + \frac{\gamma^2}{4}} - \frac{\gamma}{2})^2/4\upsilon_t]^2}} \tag{11}$$

2.2 Field in the multilayer gate dielectric

We now turn our focus on evaluating the potential at different layers of the gate stack. For this, we consider the Poisson equations in the different layers,

$$\frac{d^2\varphi_1(y)}{dy^2} = 0 \tag{12}$$

$$\frac{d^2\varphi_2(y)}{dy^2} = 0 \tag{13}$$

$$\frac{d^2\varphi_3(y)}{dy^2} = \frac{qN_C(\tau)}{\epsilon_{embed}} \tag{14}$$

$$\frac{d^2\varphi_4(y)}{dy^2} = 0 \tag{15}$$

Here, $\varphi_1(y)$, $\varphi_2(y)$, $\varphi_3(y)$ and $\varphi_4(y)$ represent the potentials in the tunnel oxide (two layers), nc embedded nitride layer and the control oxide regions, respectively. The solutions of (15) to (17) are obtained to be respectively

$$\varphi_1(y) = A_1 y + A_2 \tag{16}$$

$$\varphi_2(y) = A_3 y + A_4 \tag{17}$$

$$\varphi_3(y) = \frac{qN_C(\tau)}{2t_3} y^2 + A_5 y + A_6 \tag{18}$$

$$\varphi_4(y) = V_G - A_7 y - A_8 \tag{19}$$

$A_1, A_2, \ldots, A_8$ are constants which can be determined by applying Gauss' Law at the interfaces of the layers. The values are evaluated to be

$$A_1 = \sqrt{\frac{2kTn_i\epsilon_{Si}}{\epsilon_{eff}}} \cdot \sqrt{e^{(\varphi_S - V)/\upsilon_t}} \tag{20}$$

$$A_2 = \varphi_S - A_1 d_{Si} \tag{21}$$

$$A_3 = \frac{\epsilon_{tox1}}{\epsilon_{tox2}} \cdot A_1 \tag{22}$$

$$A_4 = \left(1 - \frac{\epsilon_{tox1}}{\epsilon_{tox2}}\right) \cdot A_1 d_1 + A_2 \tag{23}$$

$$A_5 = \frac{\epsilon_{tox2}}{\epsilon_{embed}} \cdot A_3 - \frac{qN_C(\tau)}{t_3} \cdot d_2 \tag{24}$$

$$A_6 = \frac{qN_C(\tau)d_2^2}{2t_3} - A_3 d_2 + A_2 - A_3 d_2 \tag{25}$$

$$A_7 = \frac{\epsilon_{embed}}{\epsilon_{cox}} \cdot \left[qN_C(\tau) + A_5\right] \tag{26}$$

$$A_8 = \frac{qN_C(\tau)d_3^2}{2t_3} + A_5 \cdot d_3 + A_6 - V_G + A_7 \cdot d_3 \tag{27}$$

Thus, the fields $F_1(x)$, $F_2(x)$ and $F_3(x)$ in the different regions of the gate dielectric can be found from (18)–(20) to be

$$F_1(x) = -A_1 \tag{28}$$

$$F_2(y) = -A_3 \tag{29}$$

$$F_3(y) = -\frac{qN_C(\tau)}{t_3} y - A_6 \tag{30}$$

$$F_4(y) = A_7 \tag{31}$$

2.3 Evaluation of tunneling currents and nanocrystal charging

To get the tunneling currents responsible for nanocrystal charging, we first assume a neutral nc embedded layer and solve for the surface potential as described in Sect. 2.1. Thereafter we go on to evaluate the electric fields in the different regions of the gate dielectric stack, as described in Sect. 2.2.

In such devices, there exist two types of electron tunneling, the direct tunneling (occurring at low applied electric fields) and the Fowler-Nordheim (F-N) tunneling (for high applied fields). It is the F-N tunneling mechanism that is chiefly responsible for nanocrystal charging in these type of NVM. For evaluating the direct tunneling and the F-N tunneling currents, we employ a WKB approximation based model to our system [19, 20]. Upon the application of a gate bias, a triangular potential well is created in the substrate side of the semiconductor-oxide interface. The quantized energy levels of this triangular potential well may be found using

$$E_{n,\ell} = \left(\frac{\hbar^2}{2 \cdot m_{X\ell}}\right)^{1/3} \cdot \left(\frac{3}{2}\pi q F_{Sub} \cdot \left(n - \frac{1}{4}\right)\right)^{2/3} \tag{32}$$

Here $E_{n,\ell}$ is the energy of the electron in the ℓ-th valley of the n-th level ($n = 1, 2, 3, \ldots$), q is the electronic charge, F_{Sub} is the electric field in the substrate, $m_{X-\ell}$ is the effective mass of the electron in the ℓ-th valley in the direction perpendicular to the Si–SiO_2 interface.

Assuming the embedded nanocrystals and C60 to be roughly spherical in shape, their energy states are can be obtained by solving for the wave vector values of the spherical Bessel function [21]

$$\varepsilon_{i,k} = \varepsilon_g + \frac{\hbar^2}{2m_e} \cdot \left(\frac{\beta_{i,k}}{a}\right)^2 \tag{33}$$

In the above expression $\varepsilon_{i,j}$, is the k-th sub-band of the i-th energy state of the nanocrystal, ε_g is the energy band gap, $\beta_{i,k}$ is the i-th zero of the k-th order spherical Bessel function, a being the nanocrystal size.

In order to calculate the nanocrystal charging, we consider both the direct and the F-N components of the substrate to nc (J_{in}) and nc to metal gate tunneling (J_{out}) currents. The net charging current density (J_{Ch}) being the difference between them [19]. The F-N component of the current densities can be written as

$$J_{in}^F = \sum_{n,\ell} \wp(\varepsilon_{n,\ell}) \cdot \left(\frac{q^3 m_{Sub}}{16\pi^2 m_{eff}\hbar}\right) \cdot \frac{(\bar{F}_1)^2}{(\Phi_{B1} - E_{n,\ell})} \times \exp\left\{-\left(\frac{2\sqrt{8m_{eff}q}}{3\hbar}\right)\frac{(\Phi_{B1} - E_{n,\ell})^{3/2}}{\bar{F}_1}\right\} \tag{34}$$

$$J_{out}^F = \sum_{i,k}\left(\frac{q^3 m_{nc}}{16\pi^2 m_{eff}\hbar}\right)\cdot\frac{(\bar{F}_3)^2}{(\Phi_{B2}-\varepsilon_{i,k})} \times \exp\left\{-\left(\frac{2\sqrt{8m_{eff}q}}{3\hbar}\right)\frac{(\Phi_{B2}-\varepsilon_{i,k})^{3/2}}{\bar{F}_3}\right\} \quad (35)$$

In (32)–(33), Φ_{B1}, Φ_{B2} are the intrinsic Si–SiO_2 electron tunneling barrier height, and the nanocrystal-control oxide interface barrier height. $\bar{F}_1$ and $\bar{F}_3$ are the equivalent fields in the region $d_{Si} < y < d_1$ and $d_3 < r < d_4$, respectively. The density of final states in the spherical nc is expressed as [21],

$$\wp(\varepsilon_{n,\ell}) = \frac{2a^3}{3\pi}\frac{\sqrt{2}m_{nc}^{3/2}}{\hbar^3}(\varepsilon_{n,\ell}-\varepsilon_F)^{1/2} \quad (36)$$

ε_F being the Fermi energy of the nc, (n and ℓ are free indices), other symbols have their usual meanings. The direct tunneling current components are given by

$$J_{in}^D = \sum_{n,\ell}\wp(\varepsilon_{n,\ell})\cdot\frac{\{2m_{eff}(\Phi_{B1}-E_{n,\ell})\}^{1/2}\lambda q^2\bar{F}_1}{\hbar^2} \times \exp\left(\frac{2\lambda\sqrt{2m_{eff}(\Phi_{B1}-E_{n,\ell})}}{\hbar}(t_1+t_2)\right) \quad (37)$$

$$J_{out}^D = \sum_{i,k}\frac{\{2m_{eff}(\Phi_{B2}-\varepsilon_{i,k})\}^{1/2}\lambda q^2\bar{F}_3}{\hbar^2} \times \exp\left(\frac{2\lambda\sqrt{2m_{eff}(\Phi_{B2}-\varepsilon_{i,k})}}{\hbar}t_4\right) \quad (38)$$

The current densities J_{in} and J_{out} can thus be expressed as the sums of their direct and F-N components respectively. From these, the time evolution of charge stored in the nanocrystal layer, can be evaluated to be

$$\frac{dQ}{d\tau} = J_{in} - J_{out} \quad (39)$$

From (37), we can easily get the amount of charge stored in the nanocrystal embedded layer, which gives the stored charge density in the nanocrystal embedded layer as

$$Q(\tau) = \int_{\tau_1}^{\tau_2}(J_{in}-J_{out})d\tau \quad (40)$$

Equations (32)–(38) give us the write mechanism of the MOSFET device. The erase characteristics can be similarly described by considering electron tunneling from the nc states back into the Si substrate, under a negative gate bias. The erase mechanism under a negative bias is owing to the tunneling current density

$$J_{erase} = \sum_{n,\ell}\gamma(E_{n,\ell})\cdot\left(\frac{q^3 m_{Sub}}{16\pi^2 m_{eff}\hbar}\right)\cdot\frac{(\bar{F}_{1rev})^2}{(\Phi_B'-\varepsilon_{n,\ell})} \times \exp\left\{-\left(\frac{2\sqrt{8m_{eff}q}}{3\hbar}\right)\frac{(\Phi_B'-\varepsilon_{n,\ell})^{3/2}}{\bar{F}_{1rev}}\right\} \quad (41)$$

Φ_B' is the nanocrystal-tunnel oxide barrier height, $\bar{F}_{1rev}$ is the reverse effective (erasing) electric field density. The density of states in the substrate being

$$\gamma(E_{n,\ell}) = \sqrt{\left(\frac{4\eta_v m_d^*}{\pi\hbar^2}\right)kT}\cdot\left[1+\exp\left(\frac{E_F-E_{n,\ell}}{kT}\right)\right]^{-1} \quad (42)$$

where η_v is the valley degeneracy, m_d^* is the state density effective mass $m_d^* = (m_z m_y)^{1/2}$ where m_z and m_y are effective masses parallel to the semiconductor-oxide interface. k denote the Boltzmann constant and E_F the substrate Fermi energy.

Here, it is worth mentioning that in our model the defects in the SiO_2 tunnel oxide—compound semiconductor interface have not been included. The presence of such interface states could induce effects such as a larger hysteresis behavior and interface trap generation, thereby hindering the performance of compound semiconductor NVMs. A solution may be offered by applying PECVD grown SiO_2 as observed by Cha et al. [12] or by the application of other dielectrics like $LiNbO_3$ or Gd_2O_3 in combination with GaN/AlGaN, as shown by Hao et al. [13] and Chang et al. [14] respectively.

2.4 Threshold voltage shifts

From Sect. 2.3, we have the value of stored charge density in the nc embedded layer. Now, we proceed to evaluate the threshold voltage shifts due to charging of the nanocrystals, following a simple method proposed by Amoroso et al. [22]. Here we consider that the charge is stored in the nc embedded layer only. If the stored charged densities at times τ and τ' be given by $Nc(\tau)$ and $Nc(\tau')$, and their associated values of the constants A_3 and A_4 (23)–(24) be taken as A_3, A_4 and A_3', A_4' then the threshold voltage shift can be simply written as

$$\Delta V_T = \frac{q(N_C(\tau')-N_C(\tau))}{4\epsilon_{nc}}\cdot d_3^2 + (A_5'-A_5)\cdot d_3 + (A_6'-A_6) \quad (43)$$

3 Modeling results and discussions

In Figs. 2(a)–(b), we have shown the modeled surface potential with respect to a varying gate bias for the different MOSFET memory devices. For Fig. 2(a), we have assumed a fixed nanocrystal (nc-Ag) and varied the substrate. From the results it is seen that the GaN MOSFET device has a slightly higher surface potential compared to the other substrates. InP and InGaAs MOSFETs however seem to show a

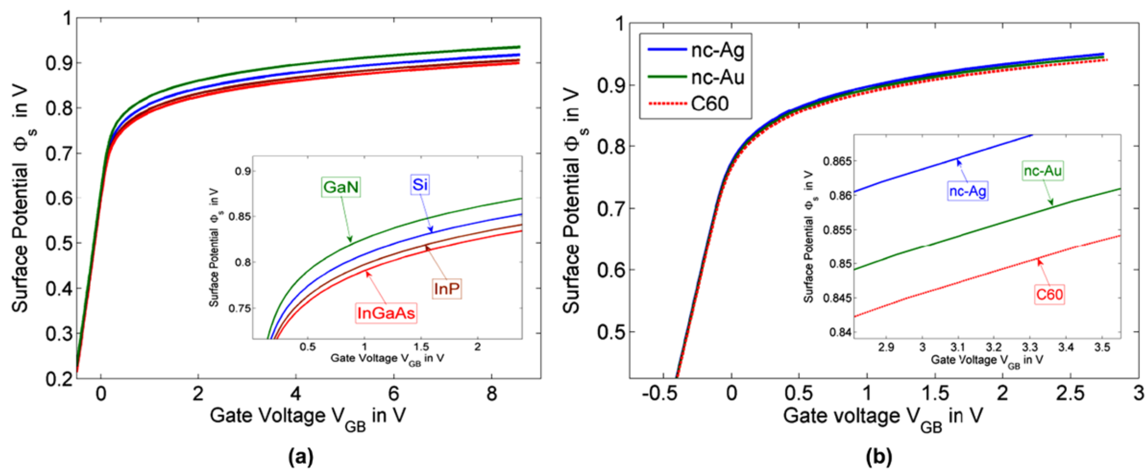

Fig. 2 Surface potentials for different gate voltages for (**a**) different substrate materials, (**b**) comparison of the three nc embedded devices for a Si MOSFET NVM (*insets*: zoomed view)

slightly lesser surface potential than the Si MOSFET NVM. This nature could be attributed to the relative permittivity of the substrates under consideration, GaN having a lesser k value of 8.90 compared to 11.9 of Si and 12.50 of InP and 13 of InGaAs. A lesser k-value results in a higher surface potential for the same applied gate bias.

In Fig. 2(b), we have shown the surface potentials for the Si substrate MOSFET, with different ncs embedded in the gate dielectric. There doesn't seem to be much to choose from the different embedded ncs in this regard, as the difference in surface potential due to nc variation seems rather negligible. However, a critical look shows an ever so slightly lesser potential for the C60 embedded Si MOSFET compared to that of the nc-Au and the nc-Ag embedded ones. This may be due to the slight difference in the effective dielectric constants of the composite gate dielectrics, for the different cases. However, this effect is rather negligible, and hence we have not further shown the surface potential variations with a varying nc for all the three substrates, in our results.

Figure 3 shows the energy band diagrams derived from our model with an (assumed) neutral nc embedded layer and a fixed gate bias of $V_G = +5$ Volts with $V_{DS} = 0$ V. Since the electron tunneling characteristics of the metallic ncs depend on their Fermi level, hence only the conduction band profile of all the cases has been shown in Fig. 3. From the band diagram it is clear that, the nanocrystals act as charge trapping sites in the multilayer gate dielectric. Here it is seen that C60 forms the deepest potential well for charge trapping, compared to the nc-Au and the nc-Ag. This is owing to the higher work function of C60 (∼5.65 eV) compared to that of the nc-Au (∼5.108 eV) and the nc-Ag (∼4.6 eV). The impact of the applied field in the writing process is also evident from the figures. In all three cases, the initiation of a triangular well formation in the substrate-tunnel SiO_2 interface can also be observed. The band-diagrams seem quite similar to each other. This is simply because of the semiconductors chosen are of electron affinity of a similar value (4.05, 4.14, 3.9 and 4.19 eV for Si, GaN, InP and InGaAs respectively). However a closer inspection shows a slight difference in the magnitude of the semiconductor-SiO_2 tunneling barriers for each of the systems. The InP substrate shows the least substrate to nc tunneling barrier of 2.95 eV, followed by the Si (∼3.15 eV), GaN (∼3.20 eV), and the InGaAs (∼3.24 eV) substrates.

In Fig. 4 we have shown the tunneling currents responsible for charging the nanocrystals (as derived from Sect. 2.3). As is evident from the curves, there exist two distinct regions in the gate voltage-charging current characteristics. It is the direct tunneling component of the charging current that is prominent in the low applied field region. Whereas in the high applied field region the Fowler-Nordheim currents seem to be the dominant component. Though nanocrystal charging can take place in both the domains, it is the F-N tunneling mechanism for nc charging that is more preferred due to shorter charging times and better charge pumping. However if the applied F-N stress is too high, there exists the reliability issue of device degradation. Usually it's the onset voltage of the F-N tunneling, which acts as the write/programming voltage in such devices. In all the three substrates, the C60 embedded MOSFET NVMs shows an earlier onset of the F-N tunneling mechanism. As for the substrate variation, in general the compound semiconductor devices show lesser F-N onset voltages, than the Si MOSFET. Among the compound semiconductors InGaAs is the better performer. In Table 1 we have shown the write voltages, and the typical values of F-N tunneling currents and the direct tunneling currents in the MOSFET NVM devices under consideration.

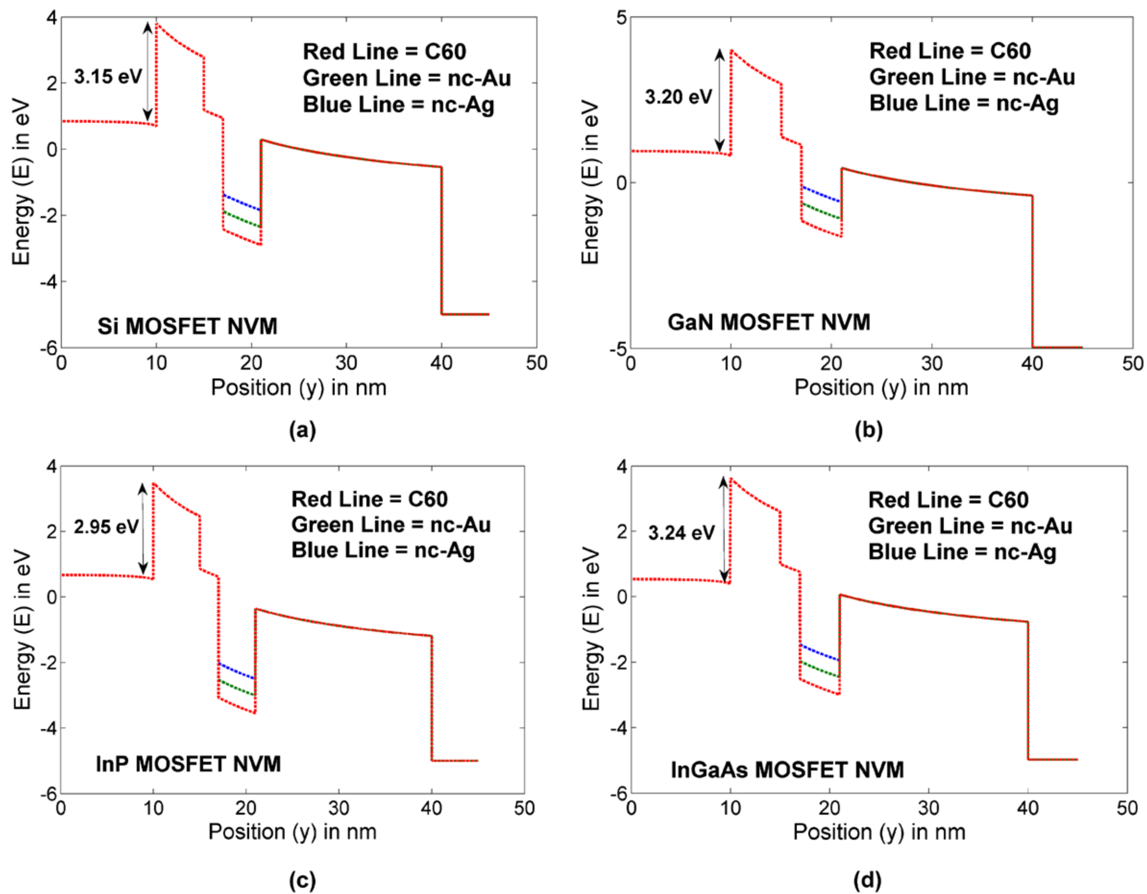

Fig. 3 Energy band diagram of the different nc embedded gate dielectric MOSFET NVM Devices for (**a**) Si substrate, (**b**) GaN substrate, (**c**) InP substrate, (**d**) InGaAs

Table 1 Write/programming voltages of the different devices

Substrate	nc embedded	Write voltage (V)	F-N tunneling current (Amp) at +10 V	Direct tunneling current (Amp) at +4.5 V
Si MOSFET NVM	nc-Ag	9.305	6.993×10^{-16}	9.576×10^{-21}
	nc-Au	8.027	6.993×10^{-13}	9.434×10^{-21}
	C60	7.804	1.22×10^{-12}	9.212×10^{-21}
GaN MOSFET NVM	nc-Ag	8.303	1.062×10^{-13}	9.640×10^{-21}
	nc-Au	7.311	4.035×10^{-11}	9.542×10^{-21}
	C60	7.082	1.012×10^{-9}	9.223×10^{-21}
InP MOSFET NVM	nc-Ag	8.320	4.882×10^{-13}	9.352×10^{-21}
	nc-Au	7.450	3.411×10^{-10}	9.165×10^{-21}
	C60	7.226	1.002×10^{-9}	9.023×10^{-21}
InGaAs MOSFET NVM	nc-Ag	7.965	5.243×10^{-13}	9.106×10^{-21}
	nc-Au	7.142	4.216×10^{-10}	9.032×10^{-21}
	C60	6.996	1.339×10^{-9}	9.003×10^{-21}

From Table 1, it is quite clear that the C60 embedded InGaAs MOSFET NVM has the lowest write voltage, and the highest F-N tunneling currents (for a fixed applied voltage of +10 V). The performance of InGaAs is very closely followed by the GaN device. The superior performance of the compound semiconductors over Si substrate, in terms of lesser write voltages and higher F-N tunneling currents is despite a higher substrate to nc tunneling barrier. This is expected to have been originated from the higher Density of States (DOS) in the conduction band, and the higher elec-

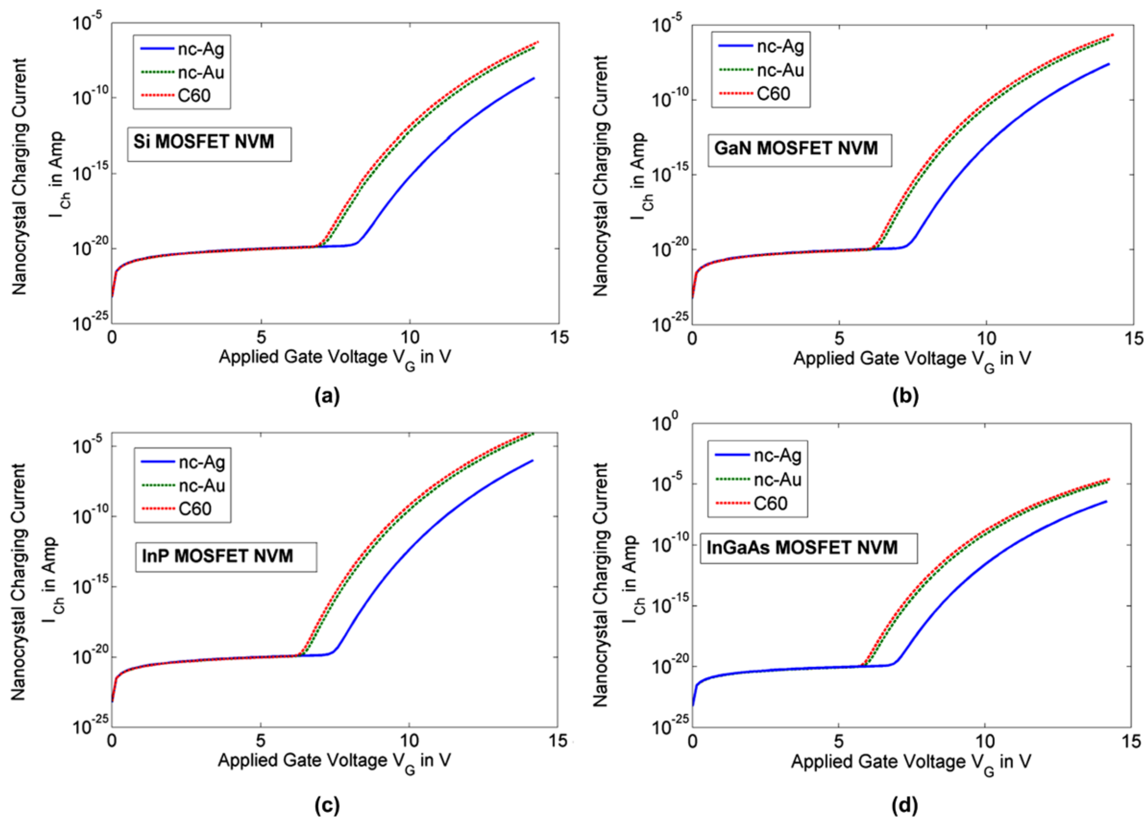

Fig. 4 Charging currents at different gate voltages for the different nc embedded MOSFET NVMs under consideration for (**a**) Si substrate, (**b**) GaN substrate, (**c**) InP substrate, (**d**) InGaAs

tron mobilities of the compound semiconductor substrates, compared to the conventional Si substrates. As for C60, it is the deeper potential well (Figs. 3(a)–(d)), that makes for a lesser nc to metal gate tunneling current (J_{out}), thereby resulting in better charging compared to the other embedded ncs. The same may be said for the superior charging performance of the Au ncs compared to the nc Ag embedded dielectrics.

At this point, it is worth mentioning that, is in this work we have considered metal ncs of 5 nm diameter (which is the standard average size of nanoclusters used in nc embedded gate dielectric MOS NVMs) [1–9]. Using a smaller sized metallic ncs (say ∼2 nm diameter) may result in improvement of the charging and the leakage suppression performance of MOS NVMs by virtue of the work-function enhancement of the ncs. Such effects have also been studied in our earlier work on Si MOSCAP NVM [23]. Since the focus of the present article is on the performance of compound semiconductor MOSFET NVMs, therefore a thorough study on the size variation of ncs on the NVM performance are beyond the scope of this work.

In MOSFET NVMs, the most important parameter is the threshold voltage shift. It is by this parameter that the 0 and 1 state of a MOSFET memory device may be understood. The higher the threshold shift for a given condition, the better is the performance of the NVM. In Fig. 5, we have shown the variations of the threshold voltage shifts, with different applied gate voltages. We have assumed a fixed charging time of 10^{-2} seconds. Owing to the lesser write voltages and a higher Density of States (DOS), the C60 embedded devices seem to offer the best performance followed by nc-Au and nc-Ag embedded NVMs. For similar reasons, the compound semiconductor MOSFETs perform better than the Si MOSFETs, in terms of obtaining higher threshold voltage shifts for the same applied gate voltage. In Fig. 6, we have shown a comparison of the threshold voltage shifts evaluated from our model, with experimental results of Mikhelashvili et al. [5] for nc-Au embedded Si MOSFET NVM device reported recently. For the comparison, we have plugged into our model, the exact device dimensions as for the fabricated device [6].

In Figs. 7(a)–(d), we have shown the transient threshold voltage shifts of the various devices under consideration, for a fixed applied gate voltage of +9 Volts. As evident from the results, the compound semiconductor MOSFET memories seem to show not only higher magnitude of threshold voltage shifts, but they also seem to charge significantly faster. This is owing to the higher magnitude of F-N tunneling currents for the compound semiconductor MOSFETs, in

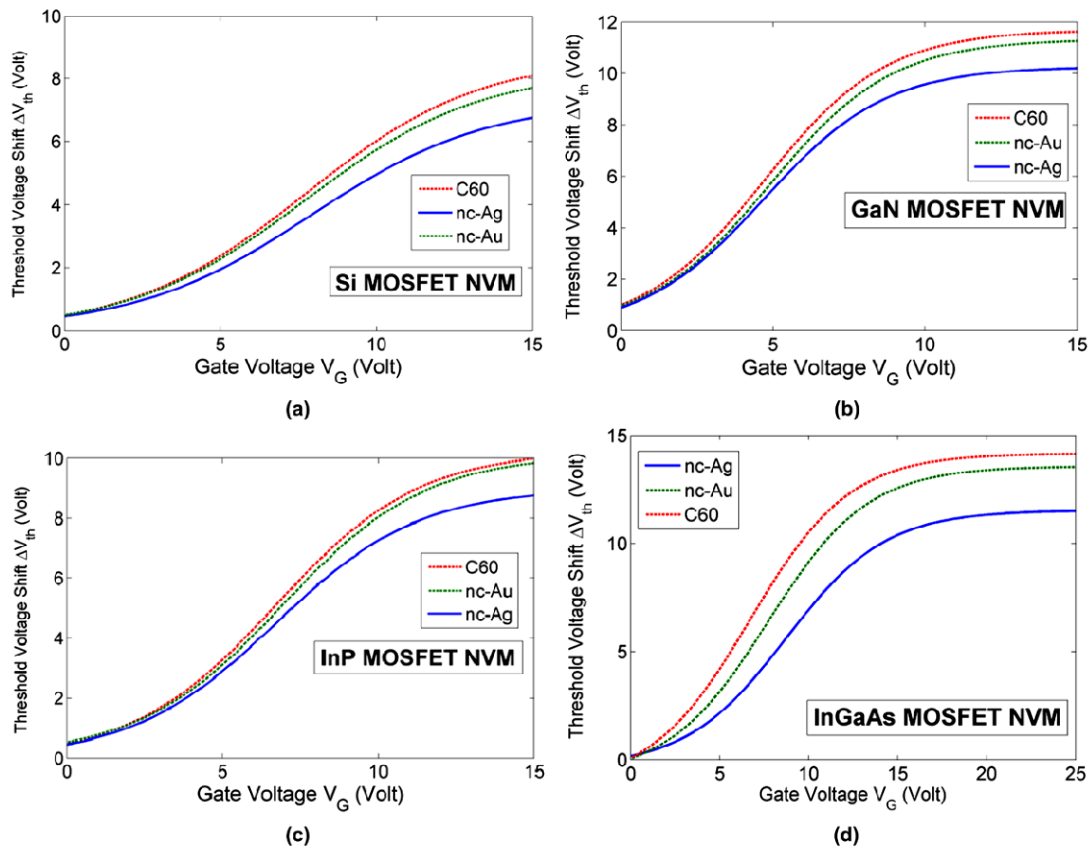

Fig. 5 The threshold voltage shifts of the devices under consideration for different writing voltages for (**a**) Si substrate, (**b**) GaN substrate, (**c**) InP substrate, (**d**) InGaAs

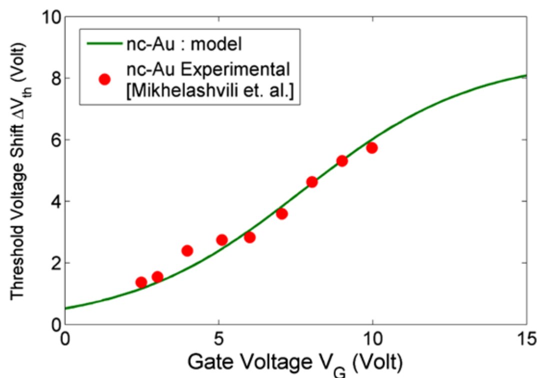

Fig. 6 Comparison of threshold voltage shift results of our model with experimental data of Mikhelashvili et al. [5]

comparison to the Si MOSFET. Also, the lower write voltage, and the slightly higher density of final states in the C60 enable them to fare better than the other ncs under consideration.

In Figs. 8(a)–(c), we have shown the comparison of results of our model for transient threshold shifts, with experimental data of recently fabricated nc-Ag embedded MOSFET NVM by Ryu et al. [6] and that of nc-Au embedded MOSFET NVMs by Mikhelashvili et al. [5].

Here, we have considered both the electron charging and the hole charging cases of the devices under consideration, and used device dimensions identical to those reported by the aforesaid groups [5, 6]. The results seem to show good agreement with the experimental data.

Finally in Figs. 9(a)–(d) we have shown the modeled erase characteristics of different nc embedded gate dielectric MOSFET NVMs, for a fixed erasing voltage of -8.5 V. All the devices were considered to initially charge at an applied gate bias of $+9$ V for 10^{-2} s. The C60 embedded devices show to take longer time to erase, owing to their deeper potential well (which effectively suppresses nc to substrate tunneling currents), followed by the nc-Au and nc-Ag embedded devices. Among the compound semiconductor MOSFETs, it is the InP MOS that shows slightly longer erase times compared to the GaN. From the point of view of the erase time the InGaAs MOS NVM shows the fastest erase characteristics. For the Si MOSFET, however the erase time is the more. This can be attributed to the fact that the compound semiconductor MOSFET NVM acquires more charge than the Si substrate MOSFET. This higher amount of stored

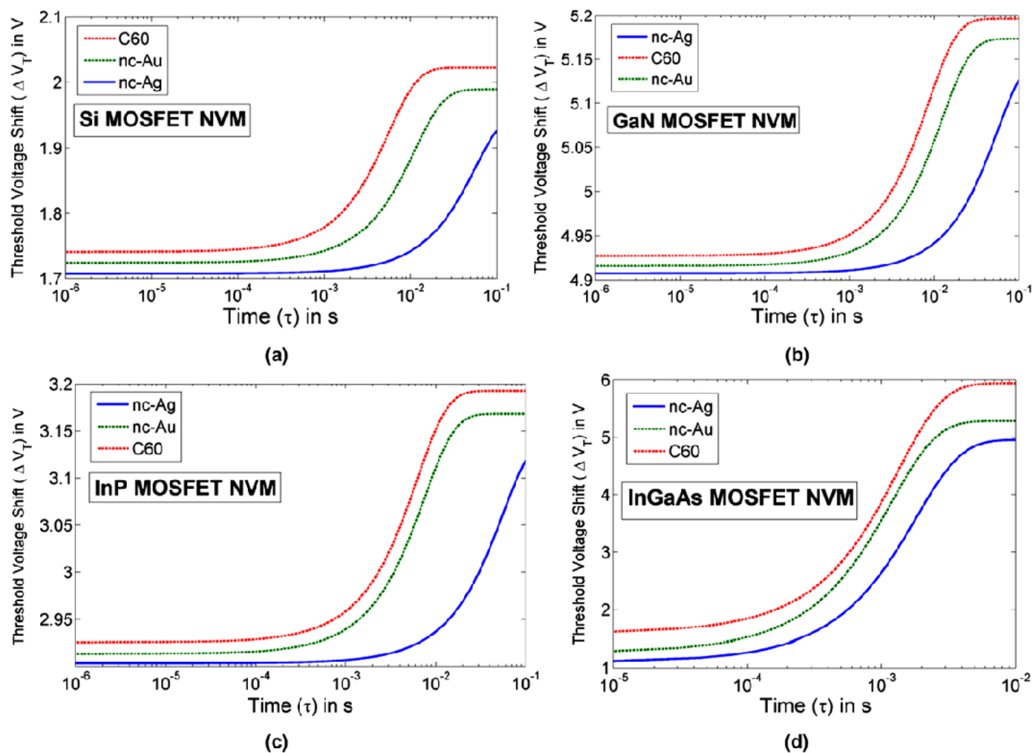

Fig. 7 The transient threshold voltage shifts for a fixed gate bias of +9 V for (**a**) Si substrate, (**b**) GaN substrate, (**c**) InP substrate, (**d**) InGaAs

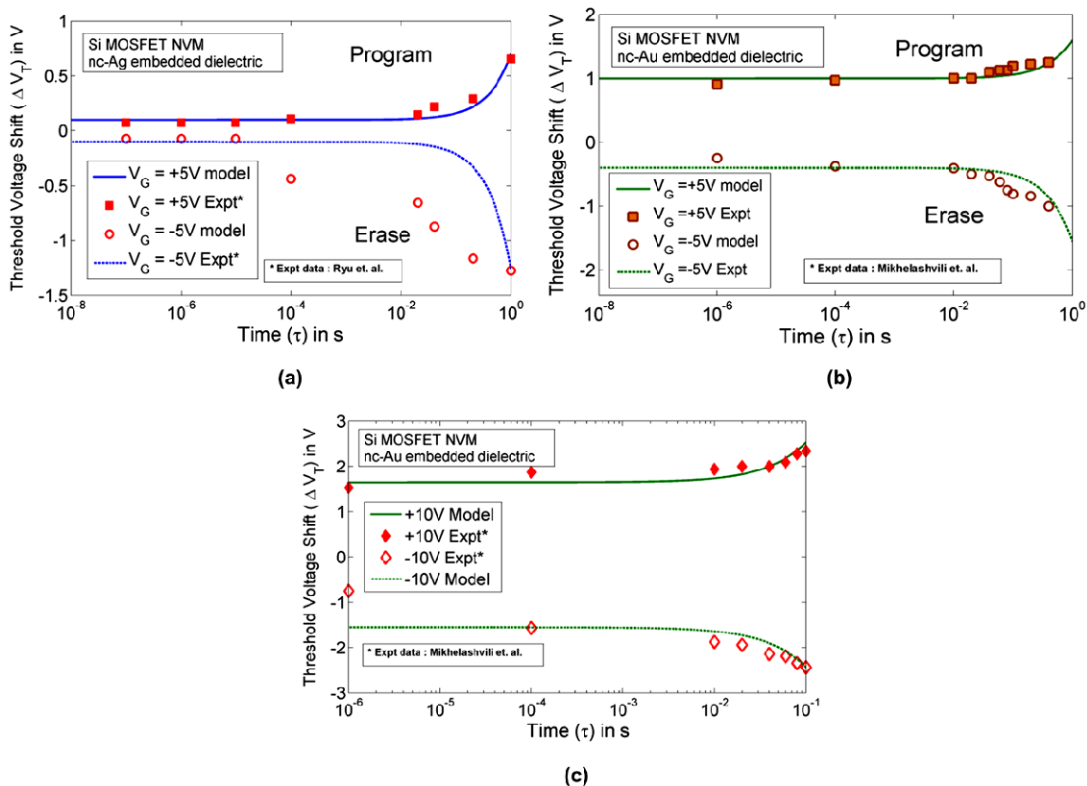

Fig. 8 Comparison of the transient threshold voltage shifts of our model with experimental results of (**a**) Ryu et al. [6] and (**b**) & (**c**) Mikhelashvili et al. [5]

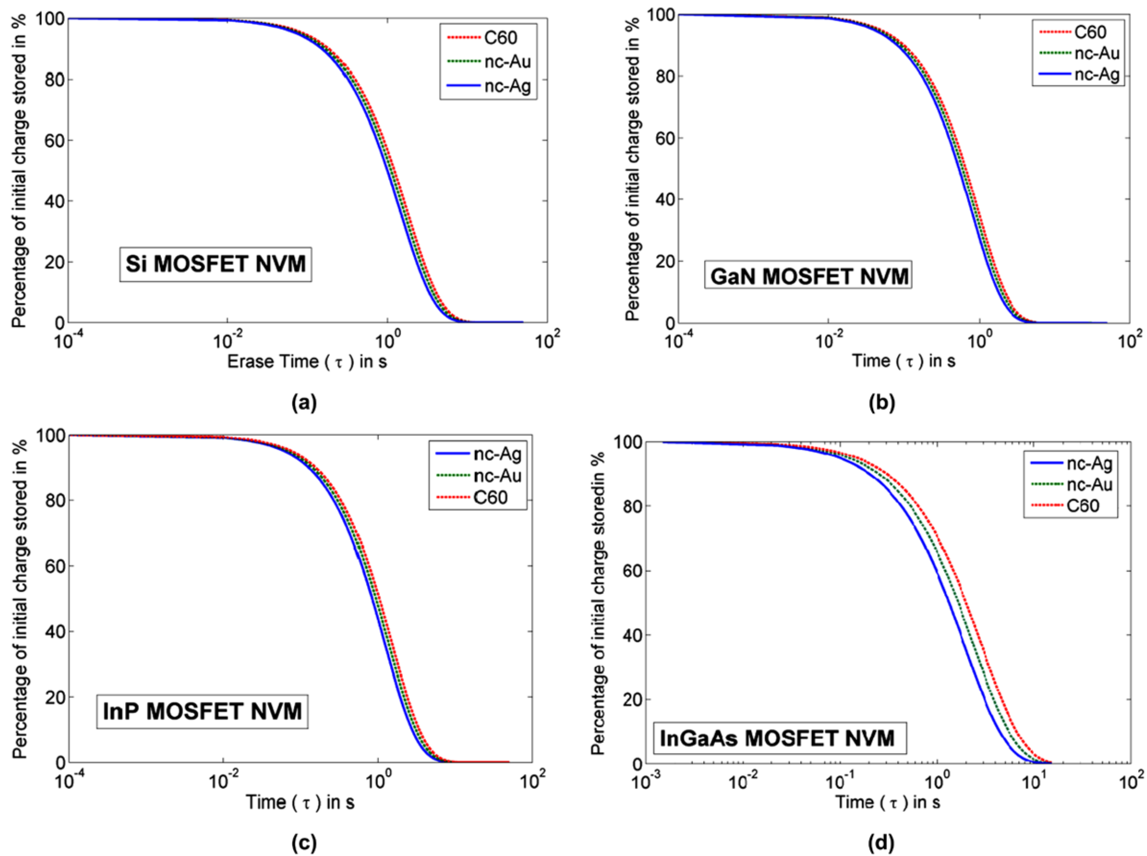

Fig. 9 The modeled erase characteristics (at −8.5 V) of the for (**a**) Si substrate, (**b**) GaN substrate, (**c**) InP substrate, (**d**) InGaAs

charge can act to cause a faster erase mechanism by enhancing the reverse (erasing) gate bias.

4 Conclusion

In this work we study and compare the performance of different nanocrystal (nc-Ag/nc-Au/C60) embedded multilayer gate dielectric long channel MOSFET NVM devices. We compared two compound semiconductors namely, GaN and InP for use as proposed substrate materials in such NVMs, with the conventional Si substrate in our study. From a semi-analytic solution of the Poisson equation, the potential and the electric fields in the substrate and the different layers of the gate oxide stack were derived. Thereafter we have investigated the Fowler Nordheim and the direct tunneling currents from the substrate inversion layer to the embedded nanocrystal states in such devices, using following a trap-like model using a WKB approximation based method. We simulated the write-erase characteristics, gate tunneling currents, transient threshold voltage shifts of the NVM devices from our analytical model. The results of the simulations were also compared with recently reported experimental results for nc-Ag and nc-Au embedded MOSFET NVMs.

From the studies, the C60 embedded gate dielectric devices showed better performance than the ones embedded with nc-Ag and nc-Au, in terms of lower write/programming voltages, higher magnitude of threshold voltage shift and faster charging, for the same applied gate voltage and better charge retention properties. These results stem from the fact that C60 has a higher work-function than the metallic ncs, which forms deeper potential well in the gate dielectric, helping in better charging performance and charge storage. Among the two metallic ncs the nc-Au embedded device emerged as the better performer from our simulations. The comparison between the different substrates shows an overall superior memory performance of the compound semiconductor MOSFETs, with GaN emerging as the best choice. The results predicted by our model seems to be in good agreement with available data on metallic ncs embedded gate dielectric MOSFET memories.

From these we could propose C60 embedded GaN MOSFET to be a better replacement of the currently used metallic nc-Ag or nc-Au embedded conventional Si MOSFET memory devices.

Acknowledgements AS wishes to thank DST, Govt. of India for INSPIRE Fellowship. CKS wishes to thank the UGC, Govt. of India, for the major research project and TWAS support as an Associate, to visit UNLP, Argentina, where part of the work was carried out.

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