Porphyrin-Based Metal–Organic Frameworks for Neuromorphic Electronics

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Porphyrin-based metal–organic frameworks (PP-MOFs) have some special features beyond ordinary MOFs, including superior optoelectronic characteristics, the ability to form 2D layered structure, and customizability, which prompt the increasing attention of PP-MOFs in the field of neuromorphic electronics. The related application research is in the initial stage, and a timely summary and guidance are necessary. The PP-MOFs fabrication should be shifted from powder synthesis in a chemistry laboratory to high-quality film preparation under a clean environment to ensure device performance. This article highlights the PP-MOFs film preparation methods and the application advances in neuromorphic electronics, performs comparative analysis in detail, and puts forward the challenges and future research directions, with the aim to attract the attention of experts in various areas (e.g., chemists, materials scientists, and engineers) and promote the application of PP-MOFs in neuromorphic electronics.

1. Introduction

Metal–organic frameworks (MOFs) are crystalline nanoporous materials with supra-molecular structures built out of metal nodes and organic ligands through coordination bonds.[1] In the past decades, MOFs were well-known for their features of customizable crystal lattices with variable node and linkers, high stability, short- and long-range ordering, high-surface-area, versatile host–guest chemistries, intrinsic pore with tunable size, and broad response to environmental stimuli, offering a unique choice for building and fine-tuning different structure–property relationships and filling the gap between organic and inorganic materials.[1b,2] As a result, related research and commercial interests are increasing, with the widespread applications in various areas and MOFs-based customized services provided by some companies.

Porphyrins are a kind of macromolecular heterocyclic compounds widely found in nature (e.g., chlorophylls, hemoglobins, cytochromes, catalase, and vitamin B12), demonstrate superior performances in catalysis, optoelectronics, and photodynamic therapy (PDT), and can be obtained through substituting the β- and meso-positions of porphin ($C_{20}H_{14}N_4$) by using various functional groups.[3] Integrating porphyrins into MOF crystal lattices as linkers to prepare porphyrin-based MOFs (PP-MOFs) can gain more versatile features and promising characteristics on the basis of their intrinsic performances,[4] such as porous low-dimension nanostructures,[5] high solution stability,[6] and enhanced optoelectronic properties,[4,7] which have been applied in the areas of sensing, photocatalysis, biomedicine, energy harvesting and conversion, electrochemistry, and so on.[5,8]

In addition to the aforementioned applications, the PP-MOFs have been applied in the areas of neuromorphic electronics since 2018.[9] Neuromorphic electronics can emulate the critical human brain functionalities (e.g., memory and learning), mainly involving two categories of devices: field effect transistor (FET) and memristor.[10] Undoubtedly, after decades of development, now the semiconductor industry is at a historical turning point, and electronic devices are developing to miniaturization, intelligent, and low power consumption. In the upcoming era of the Internet of Things (IoTs), facing the challenges from data explosion, the failure of Moore's Law, von Neumann bottleneck, and the increasing demand for data processing efficiency. Under this circumstance, a novel neuromorphic/cognitive computing strategy based on neuromorphic electronics has been proposed.[11] This computing strategy has no distinguishable boundary between memory and logic, showing an entirely different architecture from conventional computing with separated memory and logic operations rely on von Neumann architecture, and can break the memory wall by building artificial neural networks

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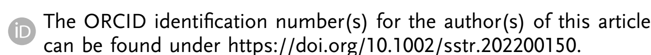
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(ANNs) on a hardware level to realize in-memory computing for processing information with high efficiency and low power consumption.[11a,12] Therefore, the research and exploration of high-performance neuromorphic electronics are of the utmost importance. For this purpose, various materials, including small molecules,[13] oxides,[14] chalcogenides,[15] quantum dots (QDs),[14c,16] 2D materials,[14c,17] perovskites,[18] and biomaterials,[19] have been applied in semiconductor devices (e.g., two-terminal memristor,[11a,12c,e,17f,20] three-terminal memory/ synaptic transistor,[10a,21] and memtransistor[22]) for developing high performance neuromorphic electronics. Organic or organic–inorganic hybrid materials with low dimensions or/ and special features (e.g., optoelectronic characteristics and unique energy band structure) have gotten lots of interest in these functional devices. As a kind of typical organic–inorganic hybrid materials, MOFs exhibit comprehensive characteristics between conventional inorganic and organic materials (including the mechanical properties between inorganics and polymers, adjustable electrical properties, and intrinsic porosity to the benefit of ion transport and storage of functional guest molecules) and are considered as one of the promising candidate materials for future electronic devices.[1b,2,23] As the sub-class of MOFs, PP-MOFs have several special characteristics: 1) the superior optoelectronic characteristic due to the existence of porphyrin linkers; 2) the ability to form 2D layered structure; 3) more powerful customizability obtained by pre-changing the metal ions at the center of the porphyrin ring. Compared to other materials, such as perovskites, BN, and transition metal dichalcogenides (TMDs), the high stability, superior optoelectronic characteristic and powerful customizability of PP-MOFs can be the distinct advantages. These characteristics prompt the increasing attention of PP-MOFs in the field of neuromorphic electronics. The research about PP-MOFs-based neuromorphic electronics is in the initial stage, but the preliminary research layout has been basically completed, involving FETs, two- and three-terminal memory, and synaptic devices (**Figure 1**). Therefore, a timely and comprehensive summary of the application of PP-MOFs in neuromorphic electronics is essential and beneficial to promote the in-depth study.

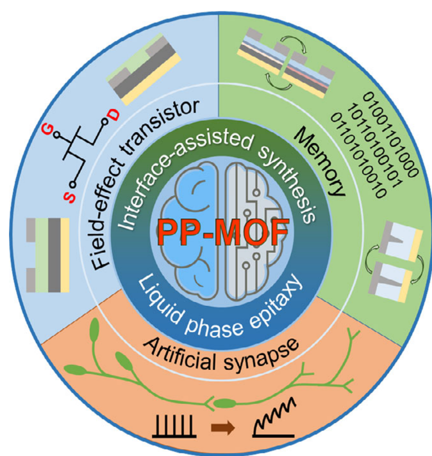

Figure 1. The porphyrin-based metal–organic frameworks (PP-MOFs) film preparation methods and applications in neuromorphic electronics.

Different from traditional application fields (e.g., gas separation and catalysis), in neuromorphic electronics, the PP-MOFs fabrication should be shifted from powder synthesis in a chemistry laboratory to high-quality film preparation in a clean room. The quality of the film directly affects the performance of the device. Even if PP-MOFs have the ability to form a 2D layered structure, it is not easy to prepare a film with a large size, highly uniform orientation, controllable thickness, low roughness, high homogeneity, and compactness. The difficulty in preparing high-quality thin films limits the application of PP-MOFs in neuromorphic electronics to some degree. Therefore, it is necessary to discuss and analyze the film preparation methods that have the potential for developing high-performance neuromorphic electronics [such as interface-assisted synthesis and liquid phase epitaxy (LPE), Figure 1] for deepening the understanding of film growth and promoting the application of PP-MOF in neuromorphic electronics.

In this article, both PP-MOF film preparation methods and applications in neuromorphic electronics are highlighted. Section 2 provides an overview of the film preparation of PP-MOFs, mainly involving two methods: interface-assisted synthesis and LPE. At the end of this section, the comparison and analysis of each fabrication strategy are performed. Section 3 addresses in detail the advances of PP-MOFs in transistors and neuromorphic electronics. At last, section 4 puts forward the challenges and future research directions of film preparation and PP-MOFs based neuromorphic electronics.

2. Preparation of PP-MOF Films

The first step for fabricating PP-MOFs-based devices is depositing a film on a substrate [e.g., Au, SiO_2, and indium tin oxide (ITO)]. For various specific applications, the requirements for the films in the aspects of homogeneity, morphology, structure, stability, and mechanical robustness are different. To be specific in neuromorphic electronics, the homogeneity, compactness, surface smoothness, thickness controllability, and size should be more focused on meeting the requirements of devices with high yield, low variability, and large array. Therefore, some commonly used MOF synthetic methods are not suitable for developing neuromorphic electronics, such as solvothermal synthesis, which will result in relatively random orientation, rough film surface, and low homogeneity.[24] With different metal–ligand connection dimensionality and topology, the PP-MOF films can be divided into two categories: 2D MOF [or 2D metal–organic layers (2D MOLs)] and 3D MOF films, even if they are formed by similar metal–oxo clusters. 3D MOF films are not proper for neuromorphic electronics since their crystallinity, surface morphology, and orientation are far from satisfactory. Therefore, in this section, we strictly limit the discussion to the pure 2D PP-MOF film fabricating methods that have the potential for developing high-performance neuromorphic electronics, including interface-assisted synthesis and LPE. The film fabricating methods for PP-MOF composites (e.g., PP-MOF/polymer composite) are not discussed here.

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2.1. Interface-Assisted Synthesis

Interface-assisted synthesis is a common method for fabricating MOF films and performed by the self-coordination of organic ligands and metal ions at air–liquid (A–L), liquid–liquid (L–L), or liquid–solid (L–S) interface (**Figure 2**a).

2.1.1. A–L Interface

Coupled with Langmuir–Blodgett (LB) method, Makiura et al. fabricated a highly crystalline-oriented PP-MOF film, NAFS-1 (NAFS-1: nanofilm of metal–organic frameworks on surfaces no. 1), at the A–L interface by using metalloporphyrin (5,10,15,20-tetrakis(4-carboxyphenyl)porphyrinato-cobalt(II), CoTCPP), pyridine and $CuCl_2{\cdot}2H_2O$ as organic ligand, capping agent and metal node, respectively.[25] In this process, once the CoTCPP and pyridine are dispersed on the $CuCl_2{\cdot}2H_2O$ aqueous solution (Figure 2b), the 2D layered CoTCPP–py–Cu nanosheets (NSs) are formed immediately at the A–L interface.[26] With the compressing of the container's walls, the CoTCPP–py–Cu NSs array is formed. Keeping a suitable surface pressure, the NSs array can be transferred onto a substrate after several dipping and washing cycles to fabricate NAFS-1 (Figure 2b). The obtained NAFS-1 shows high homogeneity and low surface roughness, and its thickness can be adjusted on a nanoscale by repeating the dipping/washing cycles. This method is universal for various substrates from standard substrates (e.g., Si, Au, quartz glass) to nonconventional substrates (e.g., ferromagnetic Permalloy[27]), and has been used for developing a series of PP-MOF films (e.g., NAFS-2,[28] NAFS-13,[26b] NAFS-21,[29] NAFS-31,[30] and NAFS-41[30]). Due to the fast interfacial reaction between metal nodes and organic ligands, the NAFS-1 shows a small lateral crystalline domain size of 20 nm.[26b] Subsequently, a post-injection method (i.e., injecting the metal node solution after the dispersion of organic ligand) was developed to improve lateral crystalline domain size to about 200 nm.[26b] Using neutral pyridyl groups to replace carboxylic groups as the peripheral porphyrin substituents, the interfacial reaction was effectively regulated, which increased the domain size to 410 nm.[29] However, this LB-assisted film synthesis technique needs a professional deposition equipment, which is quite expensive.

A "modular assembly" method was developed by Xu et al. to fabricate PP-MOF film based on normal laboratory instruments, which can solve the problem of expensive equipment.[31] In this method, the film fabrication can be divided into two steps: "chemical synthesis" and "framework assembly". In the "chemical synthesis" step, any mature synthetic technique, such

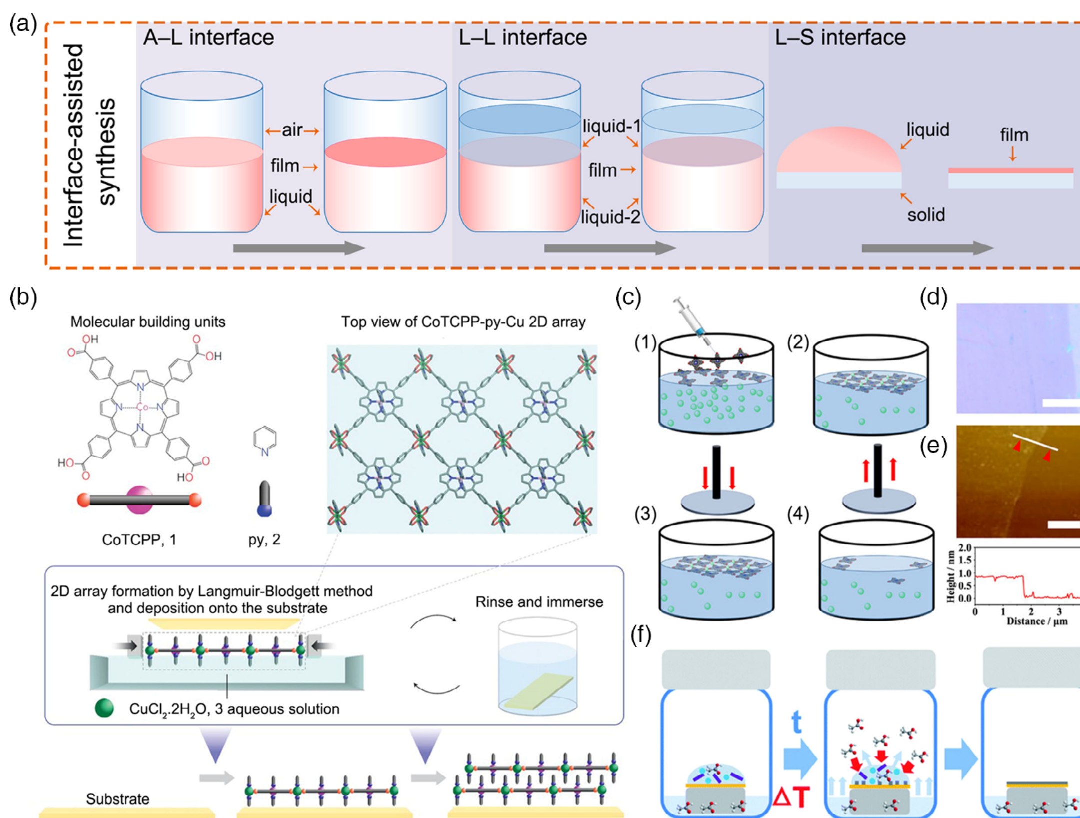

Figure 2. The examples of interface-assisted synthesis for fabricating PP-MOFs films. a) The schematic illustrations of the fabrication of MOF films at the A–L, L–L, and S–L interfaces. b) The schematic illustration of Langmuir–Blodgett (LB)-assisted film synthesis for fabricating NASF-1. Reproduced with permission.[25] Copyright 2010, Springer Nature. c) The schematic illustration of fabricating Cu-THPP film by using standard A–L interface assisted synthesis. d,e) The optical (d) and atomic force microscopy (AFM) (e) images of single layer Cu-THPP, scale bar: 10 (d) and 2 (e) μm. (c–e) Reproduced with permission.[37] Copyright 2021, Wiley-VCH GmbH. f) The schematic illustration of vapor assisted conversion method. Reproduced with permission.[24] Copyright 2020, The Royal Society of Chemistry.

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as solvothermal and surfactant-assisted methods, can be used for preparing highly crystalline "MOF modules."[31,32] Then the MOF film can form at the A–L interface through a simple "framework assembly" process. At last, the MOF film can be easily transferred onto various solid substrates by a convenient "stamping" process. The film thickness can be controlled by repeating the "stamping" process. The "modular assembly" is a convenient and rapid PP-MOF film fabrication method, and can be used in conjunction with traditional 2D MOF NSs synthetic techniques which have been summarized by many excellent reviews.[20b,23b,31,33] In this kind of film, the connections of NS–NS and NS–substrate are realized through the van der Waals (vdW)' force. This unique connection structure is a double-edged sword. On the one hand, the surface/interface (e.g., surface dangling bonds and micro-channels between NSs) in films can induce some interesting properties not found in bulk materials,[34] such as super-proton conductivity,[35] which can be used for developing protonic FETs.[36] However, on the other hand, this weak vdW force may result in the layered peeling phenomenon of MOF film.

Recently, Liu et al. successfully fabricated a wafer-level PP-MOF (Cu-THPP) thin film at the A–L (air–dichloromethane) interface by using 5,10,15,20-Tetrakis(4-hydroxyphenyl)-21H,23H-porphine (THPP) and copper acetylacetonate as organic ligand and metal node agents, respectively (Figure 2c).[37] The THPP was dissolved in NaOH aqueous solution and then added dropwise on the copper acetylacetonate dichloromethane solution surface. As the water evaporated, the film formed and covered the whole liquid surface. The MOF film could be transferred to a solid substrate by a stamping process. The film thickness can be adjusted by the amount of THPP. Different from LB-assisted synthesis and modular assembly methods, this method can directly induce a large-scale PP-MOF film with a smoother surface and better homogeneity, preferred "face-on" orientation, and excellent crystallinity.[37] This method can also produce a continuous and large-size single-layer MOF film (Figure 2d,e). These merits of the obtained PP-MOF film are beneficial for developing high-performance optoelectronic artificial synapses.[37] However, this method still has some shortcomings. First, the film formation process may need a relatively long reaction (assembly) time due to the weak volatility of water. Second, the wrinkle and folding of the film may be unavoidable during the stamping process, which is adverse for large-area device integration. Third, the film thickness adjustable range is relatively small (about 1–7 nm). The third shortcoming can be overcome by repeated stamping operation, but the multi-deposition approach can bring some other problems, such as lattice mismatch and film peeling during the repeating process.

2.1.2. L–L Interface

The PP-MOF films can also form at L–L interface. Sakamoto et al. prepared a bis(dipyrrinato)zinc(II) PP-MOF film at water–dichloromethane interface by using $(CH_3COO)_2Zn$ and lab-synthesized [(5,10,15,20-tetrakis(4'-((*Z*)-(5-methyl-1H-pyrrol-2-yl)(5-methyl-2H-pyrrol-2-ylidene)methyl)-[1,1'-biphenyl]-4-yl) porphyrinato)]zinc(II) as metal node and organic ligand agents.[38] In this synthesis technology, pyridine was added into dichloromethane to provide axial coordination with the porphyrinic zinc center and improve the solubility of ligand. The film can be obtained after 2 days of quiescence since the gentle addition of the water phase [$(CH_3COO)_2Zn$ aqueous solution] on the surface of the organic phase. The obtained film can be transferred on a substrate by a modified Langmuir–Schäfer method and its thickness can be controlled by ligand concentration. This method can generate film with a smooth surface, good homogeneity, and excellent crystallinity, but some limitations such as long reaction time and folding during the stamping process still exist.

2.1.3. L–S Interface

During the synthesis process of 2D MOFs, modulators with the same functional groups as organic ligands (e.g., carboxylic acid and pyridine) are always added into the reaction system to competitively coordinate with metal ions, adjusting the coordination interaction between organic ligands and metal nodes, blocking the MOF growth in a specific direction, and resulting in the anisotropic growth and 2D nature.[33a,39] By combining this modulation strategy with steam-assisted conversion (SAC) and dry–gel conversion (DGC) which are the well-known techniques for the film's synthesis of zeolites and their related materials (e.g., zeolitic imidazolate framework), a vapor-assisted conversion (VAC) method has been developed and can induce the formation of highly oriented MOF films at L–S interface.[24,40] Based on the VAC method, Fischer et al. fabricated a Zn_2(ZnTCPP) film on various substrates, including ITO, Au, and Si, by using 5,10,15,20-tetrakis(4-carboxyphenyl)porphyrin (H_2TCPP), $Zn(NO_3)_2{\cdot}6H_2O$ and acetic acid as organic ligand, metal node, and modulator agents, respectively.[24] In a typical synthesis process, the vapor solution [the mixture of *N,N*-dimethylformamide (DMF) and acetic acid] was added into a glass vial with a sealing cap, and a droplet of PP-MOF precursor solution (the mixed solution of H_2TCPP, $Zn(NO_3)_2{\cdot}6H_2O$ and acetic acid) was added on the substrate placed on a platform in a vial. Through a series of operations, including sealing, heating, cooling, and washing, the Zn_2(ZnTCPP) film was synthesized on the substrate (Figure 2f). The obtained Zn_2(ZnTCPP) film by VAC has a relatively low roughness, tuned thickness, and homogeneous distribution.[24] In the VAC method, many factors, including the substrate, the precursor concentration, the droplet volume, the modulator concentration, and the reaction temperature and time, can affect the orientated growth of MOF film.[24,40a] The film thickness can be controlled by the precursor droplet volume. The film growing on the substrates functionalized with -COOH/-OH shows a better crystallinity than that on non-functionalized substrates. The combination of low-concentration precursor and high-concentration modulator is important for nucleation and crystallization.[40a] The addition of acetic acid into the vapor source is necessary. The acetic acid vapor can slowly diffuse into the precursor droplet to promote the orientated growth of the PP-MOF film.[40a] Therefore, by changing these factors, the MOF film nucleation and crystallization processes can be precisely controlled for obtaining optimal morphology and thickness. However, due to these reasons, the fabrication of MOF film with

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high quality based on the VAC method becomes relatively difficult, especially for the researchers lacking experience in material preparation.

2.2. LPE

LPE can provide well-controlled thickness and crystalline orientation, and is one of the most frequently used techniques for MOF film preparation.[41] In the LPE method, the choice of metal nodes is restricted to those that can form paddle–wheel structure, such as $(CH_3COO)_2Zn$ and $(CH_3COO)_2Cu$, while the use of organic ligands is unlimited.[42] The unique feature of the LPE method is that the substrates are immersed successively into a single solution (ligand or node) instead of a mixture reactant like solvothermal synthesis.[17e,42] Besides, the reactant concentration in LPE is usually lower than that in solvothermal synthesis for better crystallization.[43] The substrates should be clean and dry, and in most cases surface modifications should be carried out by functional groups, such as –COOH, NH_2, and OH. After each immersing step, the unreacted precursor ions or organic molecules should be removed by soaking substrate/film into corresponding solvents. After a certain number of immersing cycles, the MOFs film can be formed on the substrate layer by layer, and its thickness can be controlled by immersing cycle numbers. Sometimes, depending on the situation, various assisted techniques, such as automated pumping, spraying, and spin-coating systems, can be applied for the purposes of labor and time saving (**Figure 3**a).

2.2.1. Pumping-Assisted LPE

The first PP-MOF film prepared by LPE was reported by Hupp et al. in 2013 for the application of solar energy conversion.[44] In this study, they applied Zn_2^{4+} as a metal ion node, 3-aminopropyl-trimethoxysilane (3-APTMS) functionalized Si or ITO as a substrate to fabricate PP-MOF films based on an automated pumping system (Figure 3b).[44,45] The porphyrin-type ligands were introduced as antenna chromophore and functional light harvester to expand the spectral absorption range and improve the energy conversion efficiency.[7b,44,46] The surface roughness of the formed film shows a negative correlation with the immersing cycle number and can be decreased to 3 nm after 120 cycles. The authors believe that the film initially nucleated and displayed at the 3-APTMS regions, and the nucleated film patched overlaps gradually with the proceeding of immersing process. It's worth noting that they introduced two kinds of organic ligands in one MOF structure (Figure 3b), which provided the structure foundation to obtain new or modified PP-MOFs film by post-assembly

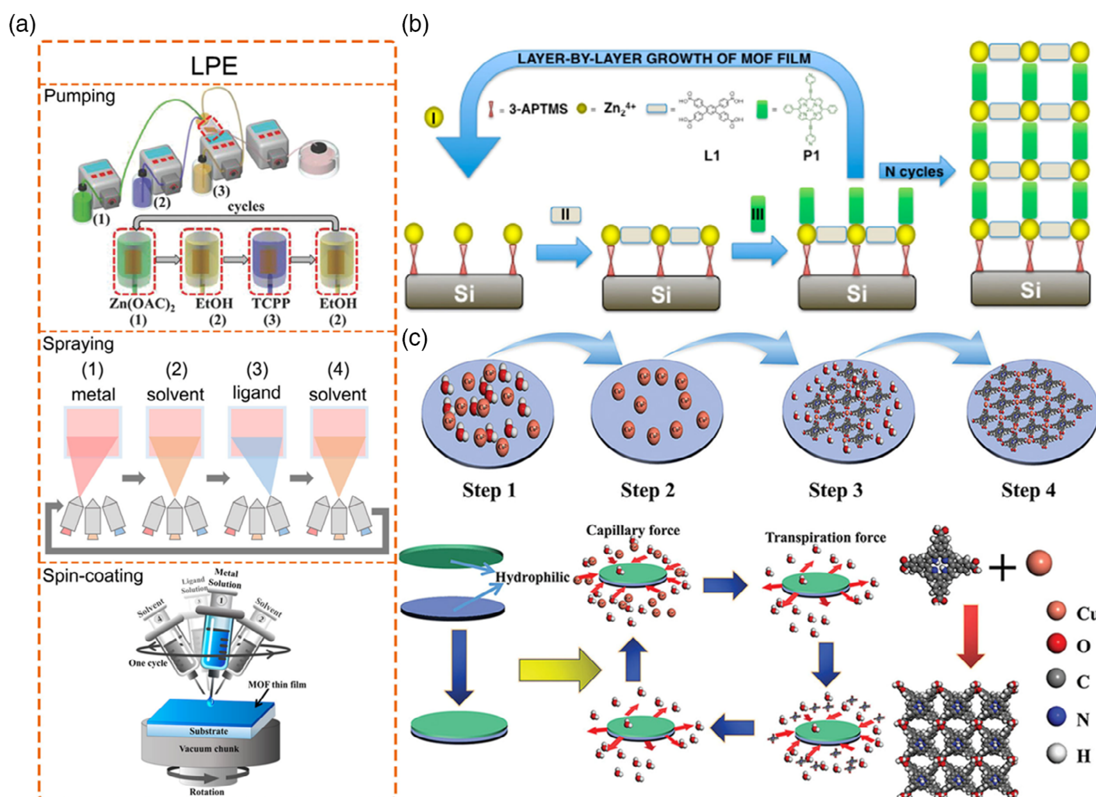

Figure 3. The examples of liquid phase epitaxy (LPE) methods for synthesizing PP-MOFs films. a) The schematic illustrations of the fabrication of MOF films by using pumping, spraying and spin-coating assisted LPE methods. Pumping: reproduced with permission.[48a] Copyright 2018, Wiley-VCH GmbH; spraying: Reproduced with permission.[51b] Copyright 2017, Wiley-VCH GmbH; spin-coating: Reproduced with permission.[52] Copyright 2016, American Chemical Society. b) The schematic diagram of the step-by-step growth of PP-MOF film with two different organic ligands on 3-aminopropyl-trimethoxysilane (3-APTMS) functionalized substrate. Reproduced with permission.[44] Copyright 2013, American Chemical Society. c) The schematic diagram of face-to-face confinement growth method for Cu_2(TCPP) film. Reproduced with permission.[54] Copyright 2021, Wiley-VCH GmbH.

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transformation (e.g., post-assembly linker metalation or solvent-assisted linker exchange),[47] and reflect the highly customizable feature. Different from the conventional LPE (dipping substrate into reactant solution), in this pumping-assisted LPE method, the reactant and washing solutions are pumped into a reactor sequentially to complete the cycle process. One of the advantages of pumping-assisted LPE method is that the film growth process can proceed under a relatively high temperature by introducing a reflux or heating unit around the reactor.[43,44] Using this pumping-assisted LPE method, Zn-TCPP films were fabricated by Zhang et al., and then treated by heating in an N_2 atmosphere or doped with Pt atoms to improve conductivity and applied as counter electrodes in the development of high-performance solar cells.[48] The introduction of automated pumping can simplify synthesis operation, but the film fabricating time is still relatively long, which needs above 25 min in one growth cycle. Besides, a large quantity of solvents and chemicals are needed, causing waste and pollution.

2.2.2. Spraying-Assisted LPE

Spraying-assisted LPE is another commonly used method for fabricating PP-MOF films. Compared to the pumping method, spraying-assisted LPE can shorten one growth cycle time to ≈1.5 min and greatly improve the film preparation efficiency.[49] Based on spraying-assisted LPE, Wöll et al. fabricated two kinds of PP-MOF films (free base porphyrin Zn-SURMOF 2 and Pd-porphyrin Zn-SURMOFs 2). The obtained PP films not only show large size, controllable thickness, and good morphology, but also have a small indirect bandgap and large charge–carrier mobility and generation efficiency, which is suitable for developing photovoltaic device.[49,50] Besides, PP-MOF film PIZA-1 can also be obtained by spraying-assisted LPE and used for selective adsorption of volatile organic compounds and electrocatalysts in oxygen evolution reaction.[51] However, unfortunately, the surface roughness film from spraying is not ideal compared to that from the pumping method (about several nanometers), which results in the need to deposit relatively thick metal electrodes (above 100 nm).[50] Moreover, the issue of large consumption of solvents and reagents still needs to be solved.

2.2.3. Spin-Coating-Assisted LPE

To address the problem of large chemical reagent consumption, Eddaoudi et al. developed the spin-coating assisted LPE method to fabricate MOF film.[52] Typically, the metal nodes and organic ligands solutions are added successively on a substrate that is pre-adsorbed on a vacuum chuck and subsequently spin-coated continuously during the adding process. The substrate should be pretreated with functional groups and washed with a pure solvent (e.g., ethanol) after each step. This method is universal for diverse MOF films and substrates.[52] The obtained film is homogeneous and highly crystalline, whose thickness can be controlled by growth cycle times. Using this method, the growth time and chemical solution in one cycle were decreased to about 1 min and 200 μL, respectively, greatly improving the efficiency and reducing the chemical pollution.[52] Heinke et al. further prepared two kinds of PP-MOF films, Zn(TPP) and Zn(DAP), by using 5,15-bis-(3,4,5-trimethoxyphenyl)-10,20-bis-(4-carboxyphenyl)porphyrinato zinc(II) and [10,20-bis(4-carboxyphenyl)-5,15-diazaporphyrinato]zinc(II) as ligands, respectively.[53] This study showed another merit of spin-coating assisted LPE, that is, this method allows guest molecules (e.g., C60) to be easily and evenly added to the PP-MOF film during the growth process for improving the film performance (e.g., conductivity and photo-responsive).[53] However, there is not much improvement in the aspect of film surface smoothness compared to pumping/spraying-assisted LPE.

2.2.4. Confinement Growth

Recently, Liu et al. proposed a face-to-face confinement growth method to fabricate PP-MOF thin film [Cu_2(TCPP)] based on LPE and capillary action.[54] They first pretreated the substrates using O_2 plasma, ultraviolet ozone, or piranha solution to improve the surface hydrophilicity, and then parallelly fixed two highly hydrophilic pretreated substrates to form a microporous interface between two substrates for mimicking the microporous channel of the capillary. The procedure of face-to-face confinement growth was as follows: 1) inserting fixed substrates into low-concentration $CuSO_4$ aqueous solution (1 h); 2) removing the solvent by heating (0.5 h); 3) inserting fixed substrates into low-concentration organic ligand solution [meso-tetra (4-carboxyphenyl)porphine (H4TCPP), 1 h]; 4) removing the solvent by heating (0.5 h); 5) repeating steps 1 to 4 until the desired film thickness is attained (Figure 3c).

In this process, due to the strong capillary action, the reactant solutions are driven into the confined area and can disperse on the whole substrate surface, and form the Cu_2(TCPP) film layer by layer. This method has the generality and can be used for fabricating other MOF films [e.g., $Cu_3(HHTP)_2$, HHTP: 2,3,6,7,10,11-hexahydroxytriphenylene]. The obtained Cu_2(TCPP) film has many excellent features, including wafer-scale size, high crystallinity and orientation, continuous in large scale, homogeneous and nanoscale thickness, and smooth surface [root-mean square (RMS) roughness: 4.6–8.2 nm in different substrates].[54] Benefitting from these features (e.g., continuous on large scale), the Cu_2(TCPP) film fabricated by confinement growth has higher conductivity (0.007 S cm^{-1}) than the film fabricated by LB-assisted interface (5.4×10^{-4} S cm^{-1}) and VAT (1.1×10^{-4} S cm^{-1}) methods.[54] Besides, the Cu_2(TCPP) films fabricated by this confinement growth method have a specific A–A stacking structure.[54] which can induce lots of regular and straight pores. These pores can allow the molecules and ions with suitable sizes to pass, which is important and attractive for the design of novel neuromorphic electronics, such as memristors. However, this method still needs to be improved owing to a long time for the film confinement growth (>3 h for one cycle).

2.3. Comparison of Different Film Preparation Strategies

Here, we perform a comparison between different 2D PP-MOF film preparation methods mainly in three aspects: 1) the application potential in large neuromorphic electronic device array which has a desire for the film with smooth surface, relatively high compactness and homogeneity, and adjustable thickness;

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2) the method universality, for example, whether the method can be applied in heating condition? 3) whether the method is easy to implement (including film fabrication time and the requirements for professional skills and apparatuses)? According to the comparison results in **Table 1**, up to now, it's difficult to find a fabrication method that can be satisfactory in all respects. For example, the confinement growth can generate high-quality 2D PP-MOF film and show low requirements for professional competencies and apparatuses, but it cannot be applied in high reaction temperatures and needs a really long film fabrication time. Therefore, continuous efforts are needed in developing universal, simple, and efficient fabrication methods for high-quality 2D PP-MOF films. Besides, some special preparation methods used in other 2D MOF films [e.g., chemical vapor deposition (CVD)][1b,17e,40c,42,43,55] can also be introduced in the preparation of 2D PP-MOF films for neuromorphic electronics.

3. PP-MOFs for Neuromorphic Electronics

In this section, the applications of PP-MOFs in transistor and neuromorphic electronics are summarized, involving FET, memory, and artificial synapse. Here, we focus on the application where PP-MOFs are applied as an active layer. For example, in the subsection about FETs, only the related works of applying PP-MOF as a semiconductor layer are discussed.

3.1. PP-MOFs for FETs

FETs are considered the most important kind of microelectronic devices in modern large-scale integrated chips for the functions of logic, amplification, switching, and so on. A typical FET mainly has four components: 1) source/drain (S/D) electrodes for controlling the channel current; 2) semiconductor layer whose conductivity can be changed under the vertical electrical field; 3) insulating layer; 4) a gate electrode (**Figure 4**a). The schematic illustration of channel length (L) and width (W) can be found in Figure 4a. The voltage applied on the gate electrode (V_{GS}) can lead to the enhancement or depletion of the carrier in the semiconductor layer, thereby adjusting the charge flow between S/D electrodes (I_{DS}) under drain voltage (V_{DS}), that is, the device ON/OFF state. The V_{GS} required for just switching on the FET is called threshold voltage (V_{th}). The FETs can not only be used in the actual circuit, but also be as highly valuable experimental tools for in-depth investigating the performance of semiconductor materials.

According to the relative location of the gate and S/D electrodes, FETs can be divided into four types, bottom gate (BG) or top gate (TG) combined with the top contact (TC) or bottom contact (BC) of S/D electrodes (Figure 4a). Each one of these four FET structures has merits and demerits in the aspects of electrical performance, device stability, and fabrication technology. The contact barrier between the semiconductor and S/D electrodes can largely affect the flow of channel current and device performance. Compared to TGTC and BGBC, the TGBC and BGTC structures can induce a relatively low contact barrier. By modifying the surface of S/D electrodes, e.g., depositing a thin metal oxide or an organic layer, the contact barrier in TGTC and BGBC can be optimized.[56] However, the device preparation process may become complicated. For environment-unstable semiconductor materials, the TGTC and TGBC structures can be the appropriate choices, since the dielectric can act as the self-encapsulation layer for providing protection. The TGBC and BGBC structures allow the large-scale preparation of small molecule/polymer semiconductors, especially for materials incompatible with photolithography. For FETs with special functions (light or gas sensitivity), the BGTC and BGBC structures can be selected, and particularly BGBC structure can lead to better performance. In organic FETs (OFETs) with TGTC and BGTC structures, the direct deposition (e.g., thermal evaporation) of metal electrodes may damage the organic semiconductor

Table 1. Comparison of the preparation methods for 2D PP-MOF films.

Method[a)]	Interface-assisted synthesis					LPE			
	A–L			L–L	L–S				
	LB-assisted	modular assembly	standard		VAC	pumping	spraying	spin-coating	confinement growth
Film surface smoothness	low	low	high	high	middle	high	middle	middle	high
Film thickness adjustability	middle	middle	middle	middle	low	high	high	high	high
Film homogeneity	middle	middle	high	high	low	high	middle	middle	high
Film compactness	low	low	middle	middle	middle	middle	middle	middle	high
Heating condition[b)]	no	no	no	no	yes	yes	no	no	no
Film fabrication time	short	short	long	long	short	middle	short	short	long
Apparatus requirement	high	low	low	low	middle	high	middle	middle	low
Professional requirement[c)]	middle	middle	low	low	high	low	low	low	low
References	[25,26b,27–30]	[31,32]	[37]	[38]	[24]	[44,48]	[49–51]	[53]	[54]

[a)]This comparison only includes the methods summarized in this article. Therefore, the results of "low", "middle", and "high" are the relative comparison results between these methods. For example, the "low" surface smoothness of LB-assisted interface synthesis just means relatively lower film surface smoothness compared to other methods in this table (e.g., confinement growth); [b)]"Heating condition" means whether this method can be used in heating condition (i.e., high temperature); [c)]"Professional equipment" means the requirements for professional competence in materials synthesis.

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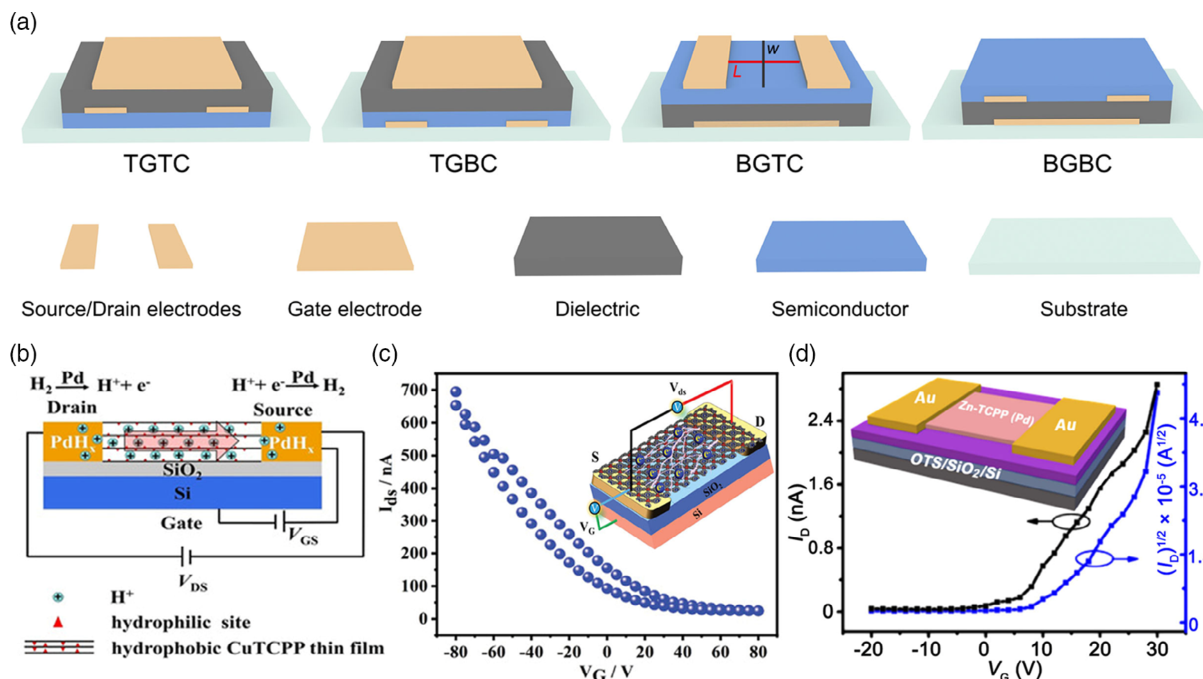

Figure 4. PP-MOFs-based field effect transistor (FETs). a) Schematic diagrams of FETs with different structures (TGTC, TGBC, BGTC, and BGBC). b) The mechanism diagram of CuTCPP film based protonic FET device with BGBC; CuTCPP film was obtained by modular assembly. Reproduced with permission.[36] Copyright 2021, Wiley-VCH GmbH. c) The transfer curves of Cu_2(TCPP) film based FET with BGBC structure, inset: the schematic diagram of the device; Cu_2(TCPP) film was obtained by confinement growth. Reproduced with permission.[54] Copyright 2021, Wiley-VCH GmbH. d) The transfer curves of Zn-TCPP(Pd) NS-based FET with BGTC structure under dark and illumination conditions (light density: 274.2 mW cm^{-2}); the Zn-TCPP(Pd) NS was obtained by crystal dissolution-growth method. Reproduced with permission.[62] Copyright 2022, American Chemical Society.

materials. Therefore, the overall considerations of material features, fabrication techniques, and applications are needed for selecting the suitable FET structure. For PP-MOF-based FETs, two kinds of device structures, BGBC and BGTC have been applied up to now.

To investigate FETs, the transfer characteristic curves (showing I_{DS} as the function of V_{GS}; I_{DS} in a logarithmic or linear scale) are usually tested for extracting valuable performance parameters. The I_{DS} value is generally manipulated by many factors (including carrier mobility, dielectric capacitance, channel length, and width), and can be described in saturation region as follows

$$I_{DS} = \frac{W}{2L}\mu C_i (V_{GS} - V_{th})^2 \quad (1)$$

where L and W are the channel length and width; μ is the mobility; C_i is the dielectric film capacitance per unit area; V_{th} is the threshold voltage.

Some important FET performance parameters, including off current (I_{off}), device on/off ratio, $V_{th,}$ and μ, can be extracted from transfer curves directly or through Equation (1).

As discussed in subsection 2.1.1, the PP-MOF film obtained by the "modular assembly" method has abundant microchannels and surface dangling bonds, which can help absorb water and form a hydrogen bonding network, thereby providing a continuous transfer path for protons.[35,36] Taking advantage of this feature, Xu et al. fabricated a protonic FET device with BGBC structure by using MOF material (CuTCPP film) as an active layer for the first time (Figure 4b).[36] The metal Pd (80 nm) was pre-deposited on the substrate as S/D electrodes and provided a proton by forming PdH_x under an H_2 atmosphere (Figure 4b).[57] The film conductivity shows a positive correlation trend with relative humidity, and can be largely improved by the existence of H_2, which is essential for this FET function. There is no additional proton for injecting the active layer without an H_2 atmosphere, that is, no field effect regulated current. This protonic FET shows slightly higher mobility (9.5×10^{-3} $cm^2 V^{-1} s^{-1}$) compared to other protonic FET based on typical materials [e.g., porous organic polymer: 5.7×10^{-3} $cm^2 V^{-1} s^{-1}$, obtained by direct synthesis based on 1,3,5-tris(4-aminophenyl)benzene (TAPB) and 1,4-diisothiocyanatobenzene (DSAB);[57c] reflectin: 7.3×10^{-3} $cm^2 V^{-1} s^{-1}$;[57b] maleic chitosan: 4.9×10^{-3} $cm^2 V^{-1} s^{-1}$].[57a]

Liu et al. fabricated a Cu_2(TCPP)-based FET with BGBC structure using confinement growth method. The FET device shows a typical p-type behavior (Figure 4c) with an on/off ratio of 40 and mobility of 0.026 $cm^2 V^{-1} s^{-1}$.[54] The confinement growth method induces a high film quality and a relatively higher conductivity (0.007 S cm^{-1}) of the Cu_2(TCPP) film than other fabrication methods. This conductivity is much higher than that of typical MOFs ($<10^{-8}$ S cm^{-1}),[58] and even comparable with that of some conductive 2D conjugated MOFs (e.g., Cu_3HHTP_2[59] and Ni_3HTTP_2[60,61]).

The PP-MOF NS can also be used for FET devices. Recently, Huo et al. developed a Zn-TCPP (Pd) NS-based FET with BGTC

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structure (Figure 4d).[62] The PP-MOF NSs and S/D electrodes are fabricated by a crystal dissolution-growth method and thermal evaporation with an organic belt shadow mask, respectively.[62] The obtained Zn-TCPP (Pd)-based FET exhibits n-type behavior and obvious photo-response characteristics. Under illumination conditions (light density: $274.2\,mW\,cm^{-2}$), the device mobility ($3.9 \times 10^{-4}\,cm^2\,V^{-1}\,s^{-1}$) and on/off ratio (321) are obviously higher than those in the dark (mobility: $1.2 \times 10^{-4}\,cm^2\,V^{-1}\,s^{-1}$; on/off ratio: 74).[62] However, compared to large-size film, the NS is not decent for device integration.

Up to now, there are few studies about 2D PP-MOF-based FETs. The key structure and performance parameters of currently reported 2D PP-MOF-based FETs are summarized in **Table 2**. In the field of MOF-based FETs, the brilliant works are mainly based on the 2D conjugated MOF materials [e.g., Cu-BHT and $Ni_3(HITP)_2$], which usually show relatively high conductivity and I_{off} (Table 2). However, the high I_{off} goes against the goal of low energy consumption. As a kind of typical carboxylic acid-based MOFs, PP-MOF can induce relatively low I_{off} in FET device, indicating the potential for low-power consumption devices. However, compared to the typical FETs based on conjugated MOFs, 2D PP-MOF-based FETs show a relatively low mobility and on/off ratio. This phenomenon may be caused by the inherent difference in the MOF structures. Therefore, it is very urgent to improve the mobility and on/off ratio of PP-MOF FET devices on the basis of low I_{off} by utilizing the material's inherent features, such as the introduction of guest molecules (or nanostructures) by utilizing the porous feature. In contrast, as one of the most important features, the optoelectronic characteristic of PP-MOF FETs should also be paid attention and strengthened.

3.2. PP-MOFs for Memory Devices

Based on whether the stored information will be lost after the power outage, the electronic memory device can be categorized into two sorts: volatile and nonvolatile devices. The nonvolatile devices are always used for storing data securely for a long time, while the volatile device can be used for static/dynamic random access memory (SRAM/DRAM) and steep sub-threshold slope transistor, etc. In consideration of the practical application of PP-MOFs in memory devices, only the most common nonvolatile devices [floating-gate transistor memory (FGTM) and memristor] are involved in this part.

3.2.1. PP-MOFs for FGTMs

The FGTM has a similar device structure to FET (**Figure** 4a and **5**a; taking BGTC structure as an example). The only structural difference of FGTM is the existence of a floating gate between the semiconductor and dielectric layers (Figure 5a). A typical working process of FGTM can be roughly described as follows (taking a p-type device as an example): 1) programming: under the action of negative V_{GS}, the holes are driven from the semiconductor to the floating gate (FG) and stored; the stored holes can play the role of shielding the gate electric field, leading to the decrease of I_{DS} compared to the initial state under same V_{GS} value, that is, the shift of transfer curve to negative V_{GS} direction; under normal conditions, this charge injecting and storing process is called programming. 2) erasing: after the programming process, under positive V_{GS}, the holes are released from FG (or to say that the electrons are driven to FG to neutralize the holes), which can result in the increase of I_{DS} compared to the programmed state and the transfer curve shifts to the positive V_{GS} direction; this process is called erasing. 3) reading: by applying a suitable V_{GS} (i.e., read voltage, V_{read}), a low or high I_{DS} value can be obtained for judging the device state (programmed or erased state); this low and high I_{DS} values can be defined as binary data "0" and "1" for information storage (Figure 5b). Therefore, utilizing FGTM, the information can be stored, read and erased easily through programming, reading and erasing processes.

In the FGTM structure, the tunneling layer plays the role of blocking the escape of stored charge from FG to semiconductor by providing a tunneling barrier and ensuring the long-term safe storage of data. During the programming and erasing processes, the charges can "across" the tunneling barrier by hot electron injection, direct tunneling, and Fowler–Nordheim tunneling (FNT).[16,63] Therefore, the tunneling layer should have a suitable thickness for realizing the purposes of safe storage (i.e., long data retention), low operating voltage, and fast programming/erasing speed.[63b] The choice of high-k dielectric materials can induce low tunneling leakage current, low operation voltage, and high retention performance.[16,64] The V_{th} difference (ΔV_{th}) between programmed and erased states is an important parameter that

Table 2. The performance comparison of the 2D PP-MOF FETs and other typical MOF FETs.

PP-MOF FETs[a)]	film fabrication	Structure	Behavior	Mobility [$cm^2\,V^{-1}\,s^{-1}$]	ON/off ratio	I_{off} [A]	Ref.
Pd/CuTCPP/Pd[b)]	modular assembly	BGBC	protonic FET	9.5×10^{-3}	4.1	35×10^{-10}	[36]
Au/Cu_2(TCPP)/Au	confinement growth	BGBC	p-type	0.026	40	–	[54]
Au/Zn-TCPP(Pd)/Au[c)]	crystal dissolution-growth	BGTC	n-type	3.9×10^{-4} (1.2×10^{-4})[d)]	321 (74)[d)]	–	[62]
Other MOF FETs	film fabrication	structure	behavior	mobility ($cm^2\,V^{-1}\,s^{-1}$)	on/off ratio	I_{off} (A)	ref.
Cu-BHT[b),e)]	L–L interface	BGBC	ambipolar	99 (h)/116 (e)	≈10	$\approx 2 \times 10^{-5}$	[126]
Au/$Ni_3(HITP)_2$/Au[b),f)]	A–L interfacial	BGTC	p-type	48.6	2×10^3	$\approx 1 \times 10^{-7}$	[127]

[a)] V_{TH} is not summarized in this table due to the lack of data; [b)] The I_{off} values are taken indirectly according to the corresponding references; [c)] The active layer is Zn-TCPP(Pd) NS obtained by crystal dissolution-growth method; [d)] The data inside and out of parentheses are obtained under dark and illumination (light density: $274.2\,mW\,cm^{-2}$) conditions, respectively; [e)] BHT: benzenehexathiol; [f)] HITP: 2,3,6,7,10,11-hexaiminotriphenylenesemiquinonate.

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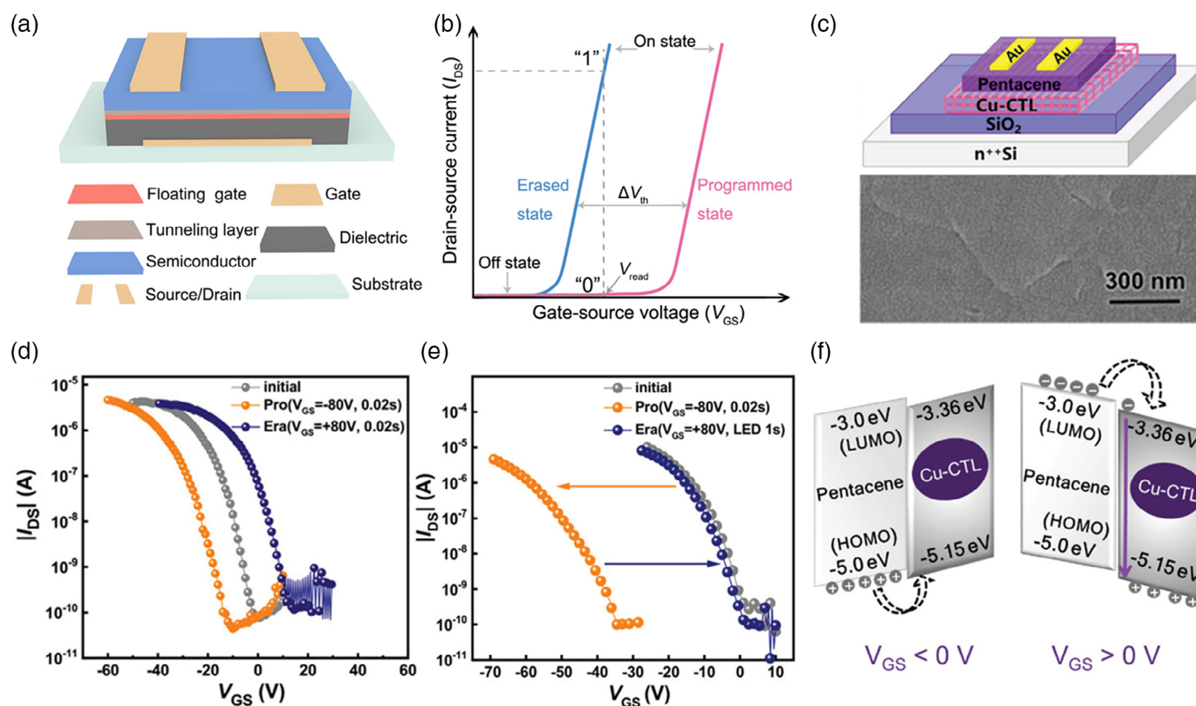

Figure 5. The PP-MOF based floating-gate transistor memory (FGTM). a) The diagram of typical FGTM. b) Typical transfer curves of FGTM under programmed and erased states. c) The diagram of Cu-CTL based FGTM (upper) and the scanning electron microscope (SEM) image of FG layer (bottom). d,e) The transfer curves of Cu-CTL based FGTM without (d) and with (e) PS blocking layer after the programming and erasing operations ($V_{DS} = -30$ V). f) The band diagrams of Cu-CTL based FGTM under programming ($V_{GS} < 0$) and erasing ($V_{GS} > 0$) operations. c–f) Reproduced with permission.[32b] Copyright 2021, Wiley-VCH GmbH.

depicts the memory ability of the FGTM (i.e., memory window, Figure 5b). Besides, retention, endurance, operating voltage/current, etc. are also the concerned parameters and describe the FGTM performances in aspects of information storage time, operating tolerance, power consumption, and so on. Only the key concepts and mechanisms are involved here, more in-depth discussion about FGTM can be found in other excellent relevant reviews.[16,63b,d,65]

For FGTM, FG is a crucial part. Up to now, various materials, including metal nanoparticles (NPs),[63d] small molecules,[13] perovskite,[18a,c] semiconductor QDs,[16] and 2D materials,[17b,h,66] have been applied as FG for trapping charges. These materials can be applied either directly or in combination with polymer as an FG layer.[21a,65,67] The porous structures of the FG layer (e.g., resulting from thermal annealing of polymers) can produce a large number of trapping sites and benefit the efficient injection of charge carriers.[68] As typical porous materials, MOFs can be used as FG layer materials for developing high-performance FGTM.

Recently, for the first time to apply Cu-CTL NSs as FG material, Shi et al. developed an FGTM device with a memory window of ≈37.5 V (Figure 5c, upper).[32b] The Cu-CTL NSs are fabricated based on SDS (sodium dodecyl sulfate)-directed solution synthetic method by using $Cu(NO_3)_2{\cdot}3H_2O$ and H_2TCPP as the metal node and organic ligand agents.[32b,69] The Cu-CTL film was prepared by the modular assembly for the FG layer (Figure 5c, bottom). Applying pentacene as a semiconductor layer, the FGTM shows a typical p-type behavior. The insulation characteristic of MOFs prompts the direct application of Cu-CTL film as a charge trapping layer without a tunneling layer. Under the negative V_{GS} bias (programming), holes are injected from pentacene to the Cu-CTL layer and trapped (Figure 5f), resulting in the negative direction shift of V_{th} from −8.65 to −22.34 V (Figure 5d). After the erasing process under positive V_{GS} bias, electrons are trapped by the FG layer, which leads to the positive direction shift of V_{th} from −22.34 to 4.74 V and a memory window of 27.08 V. The device also shows 100 programming/erasing (P/E) endurance cycles. However, the direct contact between the semiconductor and the FG layer leads to the easy escape of captured charges from Cu-CTL to pentacene and the relatively poor retention performance and small memory window. To solve this problem, a polystyrene (PS) blocking layer was introduced into the device structure. The Cu-CTL-based FGTM with PS tunneling layer shows an obvious improved retention and memory window ($\Delta V_{th} = 37.48$ V, Figure 5e). By regulating erasing voltage amplitude and introducing extra light illumination, Cu-CTL-based FGTM can realize the progressive erasing process, indicating the ability of multilevel data storage. The large memory window comes from the excellent charge trapping property which show the larger MP value (memory window/programming voltage) of 0.47 (37.48/80) than CuPc-PS4 (0.36),[70] ferritin NPs (0.14)[71] and 6FDA-DBA-SP (0.37).[72] Moreover, the author also compared the charge-trapping abilities of Cu-CTL NSs and TCPP molecules. The Cu-CTL/PS device shows an obviously higher charge–storage density (2.21×10^{12}) than TCPP-based FGTM (3.79×10^{11}). This phenomenon

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may be attributed to the porous structure and proper interlayer spacing (4.05 Å) of Cu-CTL NSs, which are beneficial to the charges tunneling across the layered structure and trapping, leading to the high charge–storage ability.[32b,68] This research is the first work on MOFs-based FGTM device and has important guiding significance. Unfortunately, the effect of light with different intensities and wavelengths have not been studied systematically. The structure–function relationship between PP-MOFs and charge trapping ability (e.g., the size of PP-MOF NSs and type of metal nodes) has not been thoroughly studied.

3.2.2. PP-MOFs for Memristor

In consideration of the inherent device's physical structure, FGTM cannot solve the coexistence problem between the size miniaturization and high-performance information storage. Memristor developed in this context has the merits of scalable architecture and high-density storage and is considered one of the most potential next-generation memory devices. The concept and real physical device demonstration of a memristor were first developed by Chua in 1971[73] and HP researchers in 2008,[74] respectively. The typical structure of a memristor is a capacitor-like device obtained by inserting a switching active layer (usually an insulator) into two electrodes (i.e., metal–insulator–metal, MIM structure, **Figure 6**a). Cross-bar is the most recommended architecture which facilitates the circuit design and 3D stack to realize high-density storage (Figure 6a, upper). For the sake of simplifying the device fabricating process and studying the resistance switching (RS) performance of active materials, cross point and parallel structures can also be applied in academic research of memristors, although they are disadvantageous to actual industrial production in consideration of device integration and circuit design.

Memristor is the portmanteau "memory resistor" whose conductance is determined by the external stimulus history which can usually cause the physical or chemical reconfiguration of the switching layer and the change of resistance. After the external stimulus (e.g., electrical, light and mechanical), the reconfiguration change of active material can induce two or more resistance states. Typically, logic states "0" and "1" are defined to represent high and low resistance states (HRS and LRS). Clearly, more resistance states are beneficial to data multilevel storage. The switching from HRS to LRS is commonly called SET, and the vice versa is called RESET process. Depending on the direction of the applied SET and RESET voltages (V_{SET} and V_{RESET}), the I–V behavior can be divided into unipolar and bipolar (Figure 6b). The current ratio between LRS and HRS is on/off ratio ($I_{on/off}$) which depicts the distinction degree of logic states. The larger $I_{on/off}$ indicates the better accuracy of the information stored, which is also conducive to the realization of information multilevel storage by setting external conditions, such as compliance current (I_{CC}).

The memory function of a memristor is in essence the reliable and controlled resistance changes that are caused by one or more switching mechanisms, such as ionic migration, charge trapping/de-trapping, and redox reactions, affected by the active material categories, type of electrodes, external stimulus mode, etc. Based on the space occupied by the atomic rearrangements during the physical or chemical reconfiguration process, the switching mechanisms can be divided into two groups: filamentary and area-dependent.[75] Usually, the RS caused by atomic rearrangements that are confined in a small area ($<100\,nm^2$) can be called filamentary. On the contrary, the RS that has a homogeneous characteristic and happens at the locations laterally displaced (same depth) in the switching layer or interface can be called area-dependent. The filamentary type memristors always show fast switching speed, large $I_{on/off}$, and excellent scalability, but have obvious shortcomings of the uncontrollable variability and relatively high power consumption due to the stochastic nature of filament formation and large LRS current (I_{LRS}). The area-dependent memristors show low power consumption, but are not satisfactory in $I_{on/off}$ and switching speed.

The filamentary mechanisms are commonly dominated by the ionic migration processes which can be divided into two categories:[76] 1) the anionic type based on the migration of VIA element ions (e.g., oxygen and sulfur) with the rearrangements of charged vacancies; 2) the cationic type based on the oxidation, migration and reduction processes of active electrodes (e.g., Ag, Cu, Al). In anionic-type memristors, the positively charged vacancies are driven to form the conductive paths (CPs) during the SET process, and combine with negative ions during RESET process to switch the memristors from LRS to HRS. The active layers with a deficiency of VIA elements can function as ion reservoirs for ion storage during SET/RESET processes. In cationic-type memristors, applied positive voltage bias can induce the redox reaction of active electrode atoms to generate metal cations. These cations are driven to counter electrode direction under positive bias, and then a reduction reaction happens. As the processes of oxidation, migration, and reduction go on, active electrode atoms gradually accumulate in the switching layer and form the conductive filaments (CFs) to switch the device from HRS to LRS. This process is reversed under the electric field with opposite polarity, that is, the RESET process. The morphology and initial formation position of CFs can be different for various switching layers that show diverse cation migration and reduction rates.[77]

Besides the memristors with ionic migration (filamentary) mechanism, there is another device in which the RS behaviors are considered to be based on purely electronic mechanism.[12e,78] The typical example is charge trapping/detrapping mechanism-based memristor. Under the voltage stress, the carriers from electrodes can be captured by the traps stemming from the doped nanostructures, interface between the electrodes and active layer, and vacancies/defects in the active materials, resulting in the RS behaviors.[79] For the device dominated by interface traps, the charge trapping/detrapping can change the height of Schottky barriers and lead to the switching of device resistance. The trap sites from vacancies/defects are usually "atom-level" and randomly distributed, and nanostructures can be introduced into the active layer to adjust the amount and distribution (random or layered) of traps (Figure 6c).[9,17j,79,80] For the device dominated by the traps distributed in random and/or layered, some famous models, including trap-controlled space charge-limited current (SCLC) (Figure 6d)[9,18i,80b,81] and trap-assisted tunneling (TAT),[82] have been used for explaining the

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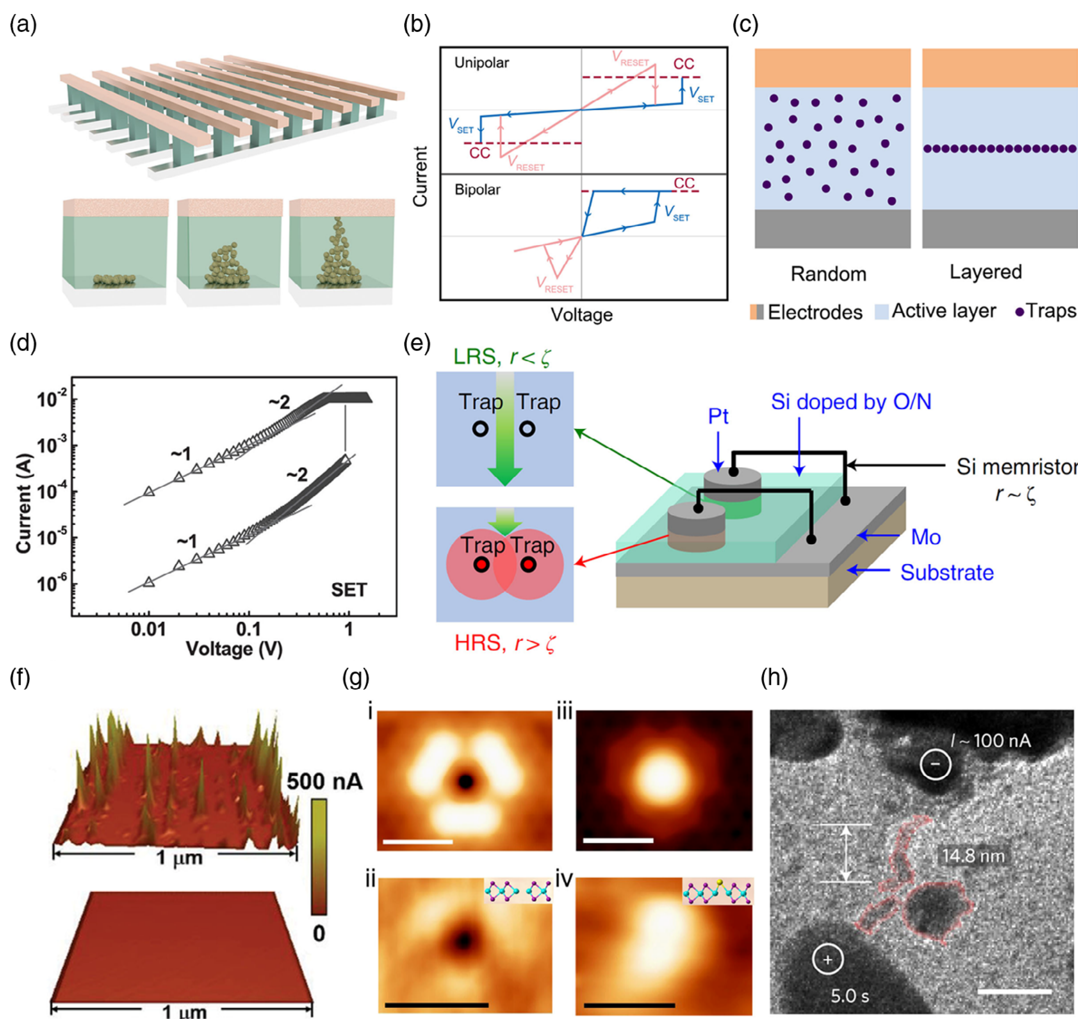

Figure 6. The mechanism of memristor. a) The diagrams of typical memristor (upper) and filamentary RS mechanism (bottom). b) Typical I–V curves of unipolar and bipolar memristors. c) The diagrams of charge trapping/detrapping mechanism with random and layered trapping sites. d) The trap-controlled space-charge-limited current (SCLC) model. The region of slope ≈2, coincident with the Mott–Gurney equation or Child's law, is an important characteristic of SCLC. Reproduced with Permission.[81a] Copyright 2016, AIP Publishing. e) The diagrams of nanometallic memristor. Right: the structure of Si based nanometallic memristor. Left: schematic of trap-electron-regulated RS from low resistance state (LRS) ($\zeta > r$, empty traps) to high resistance state (HRS) ($\zeta < r$, filled traps); ζ is localization length; r is electron transport distance; δ is film thickness. Reproduced with Permission.[85] Copyright 2019, Springer Nature. f) The current maps of LRS (up) and HRS (bottom) obtained by using in situ C-AFM technique. Reproduced with Permission.[18i] Copyright 2019, Wiley-VCH GmbH. g) The scanning tunneling microscopy (STM) images of single layer MoS_2-based memristor obtained by using in situ technique. i and ii indicate the sulfur divacancy (V_{S2}) under HRS, i: experimental image, ii: simulated image; iii and iv indicate the Au atom substitution on the top V_{S2} defect, resulting in the LRS, iii: experimental image, iv: simulated image; S, Mo, and Au atoms are shown in purple, cyan, and yellow balls in the inset picture in ii and iv. Reproduced with Permission.[88a] Copyright 2021, Springer Nature. h) The TEM image of Ag CFs obtained by using in situ technique. Reproduced with Permission.[89a] Copyright 2017, Springer Nature.

RS behaviors. The common charge trapping/detrapping-based memristor suffers from the voltage–time dilemma, that is, a memristor is less likely to meet simultaneously the requirements of fast switching time, small switching voltage, and long retention time, because there is the same barrier need to be overcome during writing/erasing and retention processes.[83] The nanometallic memristor can avoid this dilemma due to its ultrathin amorphous insulator and deformable "soft spots".[83] In the amorphous insulator, the nanometallicity can be observed when the electron transport distance (r) falls below the localization length (ζ).[84] In a nanometallic memristor with ultrathin amorphous insulator film (δ–r–ζ, δ: film thickness, Figure 6e), the metal–insulator transitions can be realized by tuning ζ which can be decreased/increased by trapping/detrapping the charge carriers under the voltage bias.[83b,84] Therefore, the initial state of the nanometallic memristor is always LRS. Under the voltage bias, the charge carriers are captured by the trap sites, which can decrease the effective ζ by Coulomb blockade and lead to HRS (Figure 6e).[83b,85] In a nanometallic memristor, the large electric field (>1 MV cm^{-1}) during the writing or erasing process can

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lead to atomic or bonding distortions, which can cause a much lower barrier and faster field-assisted tunneling (i.e., small switching voltage and fast switching time), and then avoid the voltage–time dilemma.[83b] Moreover, in this kind of purely electronic memristor, the electrons follow a 3D and isotropic pathway, providing a high device uniformity.[83b,85]

It is crucial to in-depth study the device's working mechanism to figure out the dynamic RS behaviors for further guiding the optimization of device performances.[86] For this purpose, many in situ techniques have been developed, including conductive atomic force microscopy (C-AFM),[9,18i,80b,87] scanning tunneling microscopy (STM),[88] transmission electron microscopy (TEM),[77,89] scanning transmission X-ray microscopy (STXM),[90] and Raman.[18h,89b,91] Each technique has its scope, advantages, and disadvantages, and the choice of the right technique is very important for the accurate and efficient study of the device working mechanism, which has been well-reviewed by Sun et al.[86] Moreover, the thorough study of the device electrical properties (e.g., different cell sizes and different temperatures) to make an initial assessment of the device working mechanism is also important for choosing the appropriate in situ technique. Here, the C-AFM, STM, and TEM techniques are briefly discussed. C-AFM can be used to identify the switching location with high accuracy, generate RS (I–V curves) in a nano-scale area, obtain the current maps of the switching active layer (Figure 6f), and even observe the 3D topography of CFs.[87] Performing the write, erase and read operations to obtain the corresponding current maps, especially read current maps, is important to demonstrate device state and memory performance during the RS mechanism study of a nonvolatile memristor. Limited by the tip radius, the spatial scale of C-AFM is usually beyond 10 nm, which cannot be applied to study the device's working mechanism on an atomic scale. In this respect, STM has a small spatial scale of nm–100 nm and a significantly better resolution than C-AFM, which is well-suited for the working mechanism study of ultrathin crystalline materials based memristor, such as TMDs (Figure 6g).[88a] Both C-AFM and STM can realize the nondestructive test, but they have the obvious disadvantage of extensive temporal scale (100 ms days) and narrow sample type (only tip-based structure). The TEM technique has a fine temporal scale (μs h) and can be used in various sample types, including vertical, lateral, and tip-based structures, to study the dynamic procedure of device RS behavior (Figure 6h).[89a] By connecting the spectroscopy technique, such as energy dispersive spectroscopy (EDS) and electron energy loss spectroscopy (EELS), TEM can intuitively observe the formation and rupture of CFs constituted by various elements,[77,86,89a,92] and can be the most widely used in situ technique at present.

Memristors have been developed rapidly in the past decade with fast switching speed (sub-nanosecond), extremely low power consumption (sub-pJ per transition), excellent scalability (10 nm), lone retention (>10 years), superior endurance (>10^{12} cycles), and workable 3D integration in academia and industry.[11b,17c,75b,93] One of the most urgent problems of memristors is the relatively large temporal (cycle-to-cycle) and spatial (device-to-device) variability resulting from intrinsic stochastic RS process. To solve this problem, electrode engineering, filament confinement, and some purely electronic memristors, have been developed.[83,85,94] Besides, exploring novel functional materials as active layers and taking a comprehensive understanding of the switching physics and material properties are required for developing high-performance memristors.

The first MOF-based memristor was reported by Grzybowski et al. in 2014.[95] Since then various MOFs, including famous ZIF-8,[96] HKUST-1,[97] and MIL-53,[98] have been applied in the development of memristors (**Table 3**).[1b,2,23a,42] The initial porous feature of MOFs is beneficial to the RS performance modulation and optimization of memristors by adsorbing the guest molecules (e.g., alcohol,[96a] water,[97d,99] ferrocene[97b]). Benefiting from the convenient and mature fabrication methods, some MOFs can also be coated on the nano-materials as active switching layers in memristors.[100] The switching mechanisms of these MOF based memristors involve ion migration,[95,96c,98,99b,101] charge trapping/detrapping,[9,100a,102] ferroelectric transition,[99a] trap-limited SCLC,[100b] and redox (Table 3).[96b]

In 2018, Ding et al. reported a PP-MOF-based memristor with a typical electroforming free bipolar RS behavior for nonvolatile data storage by using the composite of Zn-TCPP NSs and polyvinylpyrrolidone (PVPy) as a switching active layer for the first time (**Figure 7**a, upper).[9] The Zn-TCPP NSs were prepared by surfactant-assisted synthesis method and showed ultrathin thickness (≈10 nm) with micron-level lateral size (Figure 7a, bottom). Compared to other MOF-based memristors, the obtained PP-MOF-based device shows relatively high comprehensive performance with large $I_{on/off}$ (10^3); low operation voltage ($V_{SET} = -0.54$ V; $V_{RESET} = 2.4$ V), long retention (10^4 s), and superior endurance (1000 cycles) (Table 3). The obtained device can also realize multilevel information storage by controlling the I_{CC} values (Figure 7c). The switching mechanism is considered as charge trapping assisted hopping, as confirmed by the results of conductive atomic force microscopy (C-AFM) and Kelvin probe force microscope (KPFM). Specifically, the charge carriers filled the capture sites on the Zn-TCPP NSs and formed the CPs by hopping (Figure 7b) as the applied voltage increased, which switched the device from HRS to LRS. On the contrary, the CPs were ruptured and the trapped carriers were released under the opposite voltage, resulting in the RESET process. Besides, the memristor I–t curves of SET and RESET processes were tested for investigating the probability of turn-on/off under a particular voltage pulse. The time values needed to switch on/off ($t_{turn\text{-}on}$ or $t_{turn\text{-}off}$) under a specific voltage stress were collected for calculating the cumulative probability (Figure 7d,e). Based on the percolation conducting path model and Weibull distribution, the probabilities of turn-on/off under different pulse biases were obtained, which can help the researchers choose the reasonable operating voltages.[103] For example, under the pulse of -0.1 V and 1 ms, the device turn-on probability is 4.10×10^{-10}%, which indicates that it is almost impossible to switch the device on and perfectly reasonable to choose this pulse for reading the device resistance state. Unfortunately, in this study, the active layer is a Zn-TCPP@PVPy composite with low content of PP-MOF, which is not conducive to studying the inherent properties of Zn-TCPP, such as porous and photoelectric properties. Besides, compared to mature materials, especially TMOs, the performance of MOFs-based memristors still have room to improve.

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Table 3. The performance comparison of the MOF based memristor for nonvolatile information storage.

structure	Material type	Behavior	$I_{on/off}$	V_{SET}/V_{RESET} [V]	Retention [s]	Endurance	Mechanism	ref.
Ag/Rb-CD-MOF/Ag	Single crystal	Bipolar	150	2/−2	600	20	Ions transport assisted redox	[95]
Pt/RSMOF-1/W[a)]	Single crystal	Bipolar	30	±7.5/±1.5	6×10^3	50	Water assisted ferroelectric transition	[99a]
Ag/FJU-23-H_2O/Ag	Single crystal	Bipolar	10^5	0.2/≈−0.8	10^4	100	Proton transport	[99b]
rGO/MoS_2@ZIF-8/rGO	Film	WORM	7.0×10^4	3.3/--	1.5×10^3	–	Trap-limited SCLC	[100b]
Au/HKUST-1/Au[b)]	Film	Bipolar	18.5	0.79/−0.53	10^4	10^7	Ions migration assisted linker pyrolysis	[97a]
Ag/ZIF-8/Si	Film	Bipolar	10^7	1.8–2.6/–0.80–2.45	1.8×10^3	25	Ion migration	[96a]
Au/HKUST-1/Cu/Au	Film	Bipolar	10	0.7/–1	–	–	–	[97b]
Au/ZIF-8/Al	Film	Bipolar	10^4	–1.9/2.5	4×10^3	100	Redox	[96b]
Ag/AuNPs@Cd-MOF-1/ITO[c)]	Film	Bipolar	10^3	–2.1/2.1	–	200	CHARGE trapping/detrapping	[100a]
Ag/AuNPs@Cd-MOF-2/ITO[d)]	Film	Bipolar	10^4	–2.5/1.5	–	200	charge trapping/detrapping	[100a]
Ag/AgNPs@Cd-MOF-1/ITO[c)]	Film	Bipolar	10^2	–4.8/2.1	–	200	Charge trapping/detrapping	[100a]
Ag/AgNPs@Cd-MOF-2/ITO[d)]	Film	Bipolar	10^3	–3.8/3.8	–	200	Charge trapping/detrapping	[100a]
Ag/MIL-53/GaInSn@PDMS[e)]	Film	Bipolar	10^2	–1.2/0.3	10^5	200	Ion migration	[98]
Au/MHA-HKUST-1/Au tube[f)]	Film	Ambipolar	1.7×10^7	0.7–1/--	2×10^3	10	Water promoted electronic structure tuning	[97d]
Ag/ZIF-8@PVPy/ITO[g)]	Film	Bipolar	7.8×10^3	1.24/–2.75	1.3×10^4	500	Ion migration and trapping	[96c]
Ag/UiO-66@PVA/FTO[h)]	Film	Bipolar	10	1.5/–1.2	–	40	Ion migration	[101]
Au/$Cu_3(HHTP)_2$/ITO	Film	Bipolar	10^2	1/–1	1.2×10^4	120	Charge trapping/detrapping	[102]
Al/Zn-TCPP@PVPy/ITO	Film	Bipolar	10^3	−0.54/2.4	10^4	1000	Charge trapping assisted hopping	[9]

[a)]RSMOF-1: $[InC_{16}H_{11}N_2O_8]\cdot 1.5H_2O$; [b)]The device need a forming process under the voltage of 15 V ($V_{forming}$ = 15 V); [c)]Cd-MOF-1: $[Cd(tib)_2]\cdot(ClO_4)_2\cdot(DMF)_4$; [d)]Cd-MOF-2: $[Cd(tib)(Tdc)]\cdot(DMA)_3$; [e)]PDMS: Polydimethylsiloxane; [f)]MHA: 6-mercaptohexanoic acid; [g)]The device need a forming process under the voltage of 1.82 V ($V_{forming}$ = 1.82 V); [h)]PVA: polyvinyl alcohol; The device switching behavior can be transferred form threshold volatile to bipolar nonvolatile RS mode by improving the applied voltage range. The relevant data in Table 3 is extracted according to the bipolar nonvolatile RS mode.

3.3. PP-MOFs for Artificial Synaptic Devices

The data has seen explosive growth in this age of 5G and IoT. According to the white paper of International Data Corporation (IDC), global data generation will reach 175 ZB in 2025 from 33 ZB in 2018.[104] To deal with the situation, devices with a high ability for processing data steadily and efficiently are of great necessity. In the past decades, the generated data was processed by conventional computers based on silicon technology and von Neumann architecture, whose computing performance improvement largely relies on the scaling-down strategy. However, this scaling-down strategy seems to have come to an end because Moore's law is approaching its physical limits. In contrast, in conventional computers, the central processing unit (CPU) and memory are separated, and the data is transferred back and forth between them. This operation principle leads to low data processing efficiency and high energy consumption due to the limited bandwidth and frequent data transfer, that is, the von Neumann bottleneck. Therefore, searching for novel computing strategies is necessary.

In recent years, inspired by the human brain, neural network computing based on neuromorphic electronic devices has been developed and considered the most promising and effective way to deal with the von Neumann bottleneck.[10c,11a,b,d,12a,d,e] Human brain is a supercomputer based on close-connected spiking networks with low energy consumption (20 W) and small volume (2 L), which is composed of 10^{11} neurons and 10^{15} synapses and can parallelly accomplish the tasks of memory and data processing. Two adjacent neurons are connected by a synapse, and the connection strength is referred to as synaptic weight. The typical information (active potentials, APs) transmission between neurons can be divided into two steps (**Figure 8**a): 1) the APs from pre-neuron inducing the release of neurotransmitters to form synaptic vesicle to the synaptic cleft; 2) the neurotransmitters in synaptic cleft are received by the receptor on the postsynaptic membrane and prompt the generation of APs on the post-neuron. The synaptic weight can be adjusted by this transmission process, and this adjustability is called synaptic plasticity, which is thought to be the neural basis of memory and learning.[105] Based on the duration time of synaptic weight variation, synaptic plasticity falls into two categories: short-term plasticity (STP, millisecond to minute scale) and long-term plasticity (LTP, minute to month or year scale), which endow the computing and memory/learning functions, respectively.

Up to now, the neuromorphic devices for mimicking biological synaptic behaviors, i.e., artificial synapse devices, can be broadly divided into two categories: two-terminal devices (e.g., memristor) and three-terminal devices (e.g., FGMT). In a two-terminal synaptic device, voltage stimulus (APs) applied on

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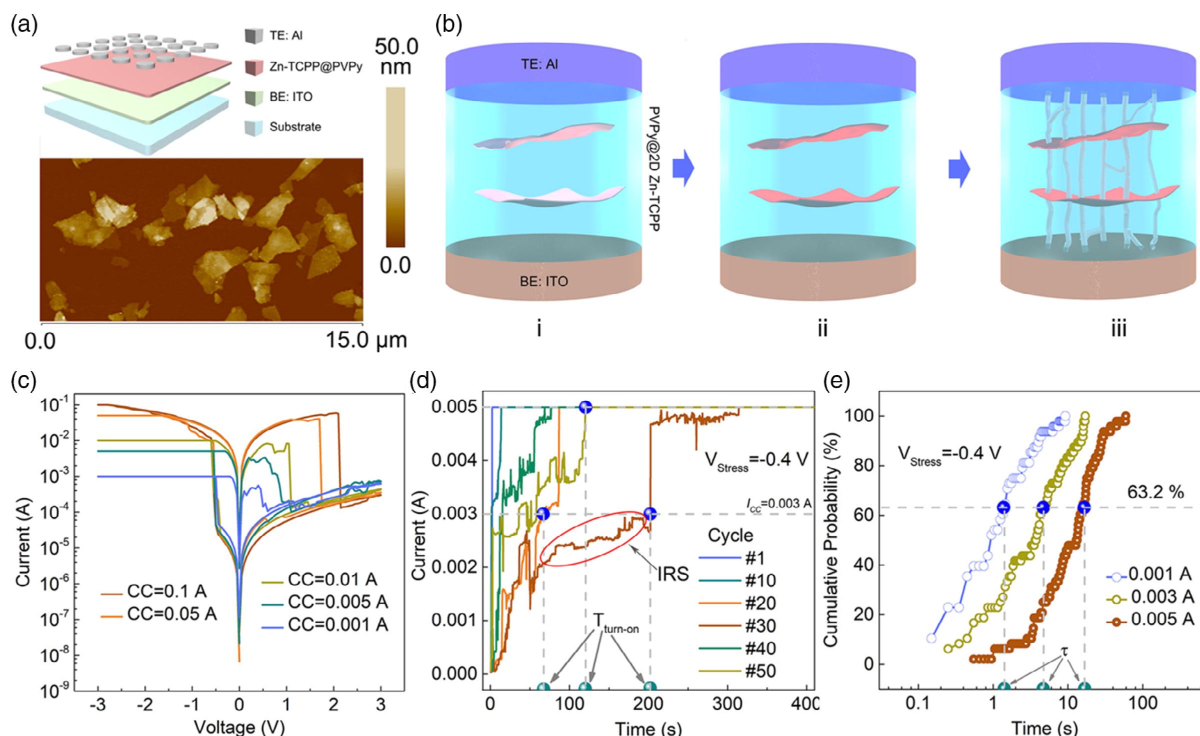

Figure 7. The PP-MOF-based memristor. a) The diagram of Zn-TCPP-based memristor (upper) and the AFM image of Zn-TCPP NSs (bottom). b) The RS mechanism diagrams of Zn-TCPP based memristor (i: initial state; ii: charge filled state; iii: above V_{SET} state. c) The *I–V* curves of Zn-TCPP based memristor under different CC values. d) The turn-on *I–T* curves of Zn-TCPP based memristor. e) The cumulative probabilities under different CC values. a–e) Reproduced with permission.[9] Copyright 2018, Wiley-VCH GmbH.

the top electrode (TE, presynaptic membrane) can induce the conductivity (synaptic weight) changes of the active switching layer which will be detected by the bottom electrode (BE, postsynaptic membrane). The active layers can simultaneously store synaptic weight status and modulate signal transmission. In a three-terminal synaptic device, the presynaptic spike is applied to the gate electrode (pre-synapse) and can result in the change of I_{DS} (post-synapse). Two-terminal and three-terminal artificial synapses have their own advantages. In a two-terminal architecture, computing and memory processes are integrated into the same space−time, which can avoid cumbersome information transfer, improve efficiency, and reduce energy consumption. In addition, the synapse-like two-terminal structure is beneficial for scale-down and layer-by-layer 3D stacking. The three-terminal architecture provides more flexibility in the aspects of signal transmission and synaptic weight modulation, which is beneficial for performing specific multiple tasks and complex behaviors. After several years of development, some recommended metrics of neuromorphic systems have been raised, such as small size ($<1\ \mu m^2$) for integration, fast write/read speed ($<1\ \mu s$), low variations, excellent write endurance [$>10^9$ (online learning)], low switching noise ($<0.5\%$) and a large number of separable resistance states (>100) with high linearity and symmetry.[10c,11b−d,12c] For realizing these merits, various functional materials, including oxides,[14a,c,e,14,106] chalcogenides,[15b−e,106b] QDs,[14c,16] 2D materials,[14c,17d−g] MXene,[17j,107] perovskite,[18b,c,e,108] and biomaterial,[19,109] have been developed and utilized for mimicking the common synaptic behaviors, such as paired-pulse facilitation (PPF), paired-pulse depression (PPD), transition of STP to LTP, spiking rate dependent plasticity (SRDP) and spike-timing-dependent plasticity (STDP). These synaptic behaviors have been explained in detail in previous reviews.[11d,17g,110] In the field of MOF-based artificial synaptic devices, the relevant research is in the initial stage.

At present, MOF-based artificial synapses have been reported, involving three kinds of materials, ZIF-8,[96c] Cu-THPP,[37] and Zn-TCPP.[111] Kim et al. fabricated a two-terminal memristor with the vertical structure of Ag/ZIF-8@PVPy/ITO and the switching mechanism of Ag^+ migration and trapping.[96c] Under the voltage bias, the oxidized Ag^+s migrate and are trapped by ZIF-8, and then reduced to formed CFs, leading to the resistive switching. The device not only shows decent data storage performance (Table 3), but also provides the potential application in the artificial synapse. Under the positive (negative) pulse train, the device shows a continuous increase (decrease) of postsynaptic current (PSC). This potentiation and depression process can be repeated several times in different devices with low variation, indicating highly reliable performance. Moreover, the STP to LTP transition and typical asymmetric STDP can be realized by increasing the pulse number and setting the suitable pulse stimuli (e.g., shape and sequence of pre- and post-synaptic spikes).[96c]

As mentioned earlier, porphyrins have excellent optoelectronic characteristics and can be used as a photosensitizer in

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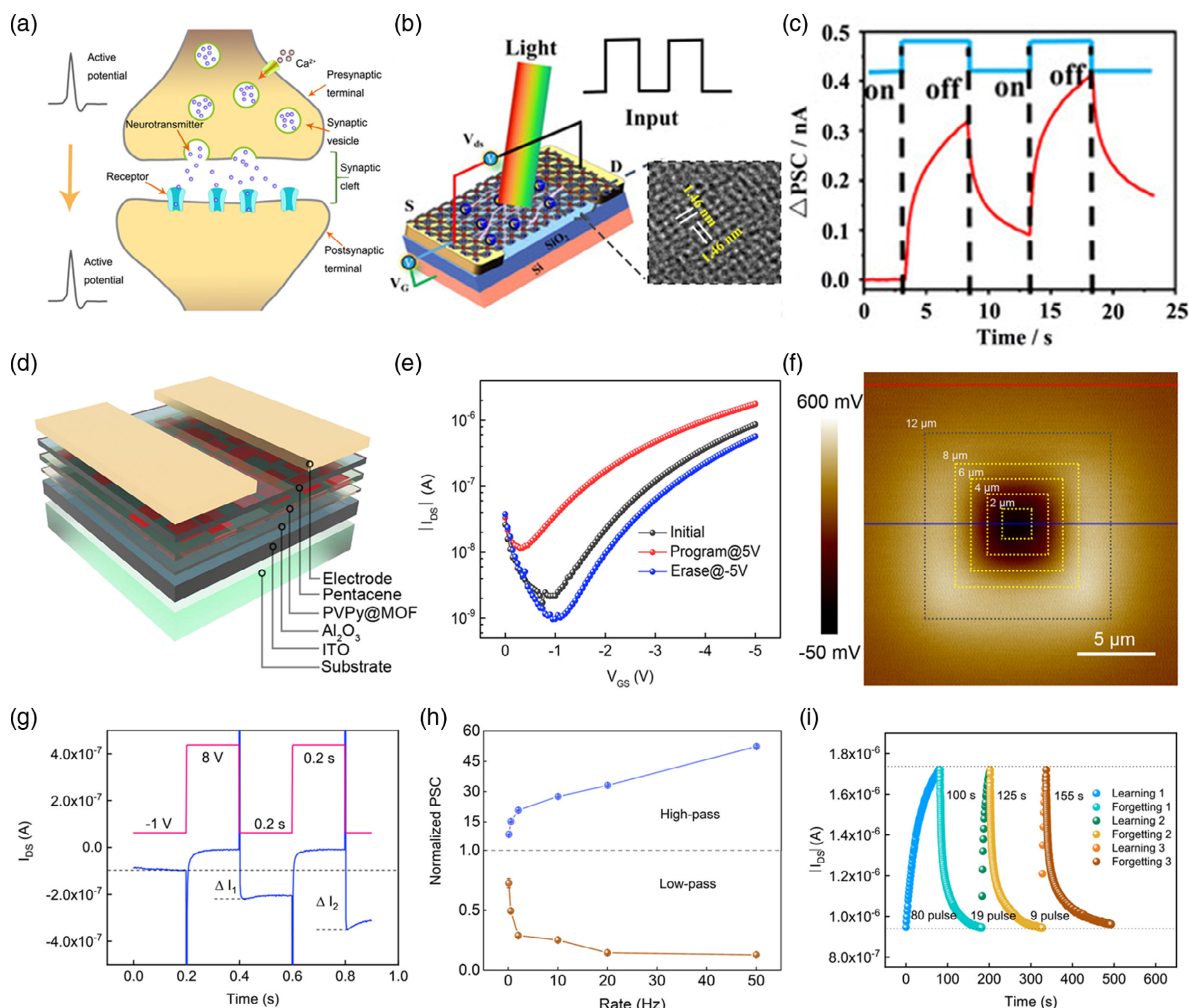

Figure 8. The PP-MOF-based artificial synapse. a) The schematic illustration of biological synapse and APs transmission. b) The schematic illustration of Cu-THPP based artificial synaptic device with lateral two-terminal structure. c) The ΔPSC variation of Cu-THPP based artificial synaptic device under two continuous pulses (420 nm). (b and c) Reproduced with permission.[37] Copyright 2021, Wiley-VCH GmbH. d) The schematic illustration of Zn-TCPP NSs based three-terminal synaptic FGMT. e) The transfer curves of Zn-TCPP NSs based synaptic FGMT under initial, programed and erased states. f) The surface potential distribution of Zn-TCPP@PVPy film obtained Kelvin probe force microscope (KPFM) after programming operation (+6 V, 12 μm) followed by continuous erasing operation (−2 V; 8, 6, 4, 2 μm). g) The PPF behavior realized by Zn-TCPP NSs based synaptic FGMT. h) The filtering behavior realized by Zn-TCPP NSs-based synaptic FGMT. i) The learning–forgetting–relearning process of Zn-TCPP NSs-based synaptic FGMT. (d–i) Reproduced with permission.[111] Copyright 2020, Wiley-VCH GmbH.

optoelectronic artificial synapses to realize low operation voltage and power consumption.[112] Wang et al. fabricated a highly photo-sensitive artificial synaptic transistor by using 5,15-(2-hydroxyphenyl)-10,20-(4-nitrophenyl)porphyrin (TPP) as a photo-active layer. Under the assistance of light stimulation (450 nm), the device exhibited high photosensitivity (1 μW cm^{-2}), small operation voltage (−70 μV), and low power consumption (1.4 fJ), and can also realize the accurate identification of visual information.[112a] Moreover, the porphyrins with specific functional groups can be linked with other materials or molecules by chemical reaction to develop a photosensitive switching layer for optoelectronic electronics.[113] Zhang et al. recently developed a porphyrin–graphene covalent hybrids-based photonic synaptic transistor by linking monolayer graphene with 5,10,15,20-tetrakis (4-aminophenyl)-21H,23H-porphine through the diazo addition reaction. With the help of light (430 nm), the synaptic transistor can realize a low operation voltage of (−10 mV), which is lower than most other reported photonic synaptic devices.[113a]

On the basis of the A–L interface-assisted synthesis and stamping method, Liu et al. fabricated a Cu-THPP-based two-terminal optoelectronic artificial synapse with a lateral structure (Figure 8b).[37] Under light illumination, the photo-induced hole–electron pairs promote the gradual increase of the current without voltage stimulus. Once the light is removed, the holes cannot recombine with electrons instantly, causing gradual decay rather than an instant reduction of the current (Figure 8c). By applying continuous optical pulse, the device can successfully mimic the PPF with the index of 125%, which is comparable with the PPF indices obtained from other optoelectronic material based artificial synapses, such as MoS_2 (120–130%),[114] C_3N_4 (120%),[115]

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and $CsPbBr_3$ (130%).[116] The STP to LTP transition can be successfully mimicked by increasing the illumination stimulus intensity, radiation time, and stimulus frequency. The Cu-THPP-based artificial synapse showed high structure and operational stability which was verified by the PSC tests of the same device after 50 days and 20 different devices, exhibiting the potential application in image recognition. Moreover, the lateral structure of the device allows the modulation of V_{GS} to the PSC for mimicking the different memory and learning abilities of various humans. The optoelectronic artificial synapse with both optical and electrical stimuli can decrease the power consumption to some extent, but still has room for improvement, such as the replacement of integrated stimulation of optical and electrical by all-optically controlled (AOC).[117] In an AOC device, both the increase (writing process) and decrease (erasing process) of conductance can be realized by light irradiation.[117a–c] This AOC switching mode can largely decrease the power consumption compared to the optical and electrical integrated stimulation in traditional optoelectronic devices due to the absence of electrical stimulus, whose power consumption is largely dominated by read energy.[117a,c] Therefore, AOC artificial synapse can be an important and promising development direction for PP-based optoelectronic artificial synapse.

By using Zn-TCPP@PVPy as a charge trapping layer and pentacene as a semiconductor layer, Ding et al. fabricated a three-terminal FGMT for mimicking common synapse behaviors (Figure 8d).[111] The synaptic FGMT shows a typical p-type behavior with $\Delta V_{th} = 1.44$ V (Figure 8e), indicating the charge trapping ability of Zn-TCPP NSs for both holes and electrons, which has been proved by KPFM. Moreover, the trapped charge carriers can be erased step by step by applying small opposite voltages, indicating the performance of multiple conductive states (Figure 8f). The ΔPSCs show a positive correlation with intensity, duration time, and frequency of the pulse stimuli on the gate electrode. By applying suitable pulse stimuli, the excitatory/inhibitory PSC (EPSC/IPSC), PPF/PPD, STP to LTP transition, SRDP, and filtering can be emulated (Figure 8g,i). Moreover, the learning–forgetting–relearning processes are also mimicked. The first, second, and third learning processes need 80, 19, and 9 pulses, while the spontaneous decay times of the first, second, and third forgetting processes are 100, 125, and 155 s, respectively, which is similar to the learning–review process of the human brain.

More efforts are needed for developing MOF-based neuromorphic devices. In the terms of device performance, there is a long way to achieve the current recommended metrics. Exploring and developing new MOF materials and device structure/composition (e.g., pure MOF active layer without polymer matrix and vertical cross-bar structure with small size, and AOC artificial synapse) can be the effective ways for improving device performance. In contrast, the studies about artificial neural networks and neuromorphic computing are still blank.

4. Summary and Outlook

In this article, we discussed the film preparation methods and the applications of PP-MOFs in neuromorphic electronics. We have emphatically summarized the synthesis methods of 2D PP-MOF films, which mainly include interface-assisted synthesis and LPE. The strengths and weaknesses in the terms of film quality and operation difficulty of each method have been discussed for the comprehensive selection in future research. The application of PP-MOFs in neuromorphic electronics is in the initial stage, but the related preliminary layout has been basically completed based on these pioneering studies, involving various aspects (FETs, two- and three-terminal memory and artificial

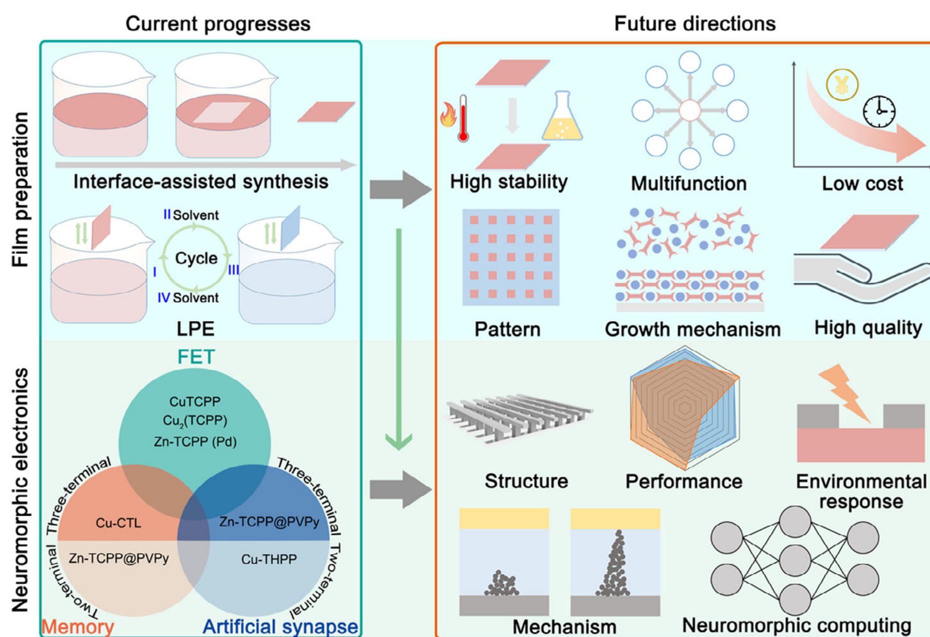

Figure 9. The current progresses and recommended future research directions of PP-MOFs film preparation methods and applications in neuromorphic electronics.

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synapse devices, **Figure 9**), which can provide references for the follow-up researches. However, the breadth and depth of related research are far from enough (Figure 9).

4.1. Film Preparation

For the need for high performance of neuromorphic electronics, the PP-MOF preparation should focus on thin film fabrication. The conventional solvothermal method has the greatest universality, but cannot produce thin films with highly uniform orientation, controllable thickness, low roughness, high homogeneity, and compactness. Current interface-assisted synthesis and LPE strategies are not compatible between film quality and operation difficulty. Specifically, the following challenges should be addressed in future film preparation studies. 1) More kinds of PP-MOF films should be developed, especially those films with high chemical, mechanical and thermal stability that can endure harsh lithographic processes and high-temperature "burn in" step in the CMOS technique. 2) More functions should be improved or introduced, especially the electronic or ionic charge transport properties and optoelectronic characteristics. Referring to the successful experience of other kinds of MOFs, building 2D close stacking and conjugated architecture, introducing guest molecules, ions, conductive polymers or nanostructures, bonding chemical functional groups, and mixing multi-ligands can be the effective ways.[44,55f,118] 3) The synthesis methods for highly homogeneous, compact, and surface smooth thin film should be developed. The film quality directly affects the device's performances, especially yield and variability. Large-scale single-crystalline PP-MOF films are highly recommended. 4) The costs and requirements of film synthesis should be decreased on the basis of quality assurance. The high costs and requirements, including time costs and the requirements for instrumentation and expertise, can limit the application of PP-MOFs in neuromorphic electronics, especially for researchers who are just starting out. Therefore, the simple and efficient methods that can produce high-quality PP-MOF thin films will be very attractive. 5) The systematic and in-depth investigations of film growth mechanisms and parameters are highly recommended. Only a few works focus on the MOF film growth mechanisms,[42,55e,119] whose in-depth understanding can help in fabricating high-quality PP-MOF films (even single-crystalline film), and take the lead in developing new PP-MOF films. Optimizing the growth parameters of some specific potential PP-MOF films is an effective approach to obtaining high-quality films, which can also offer references. 6) The pattern techniques should be developed for further improving performance (e.g., reducing the cross-talk current) in the future large-scale device array. In this aspect, some strategies used in other kinds of MOF materials, such as photolithographic etching and microcontact printing, can be used for reference.[1b,119,120]

4.2. Neuromorphic Electronics Application

4.2.1. Device structure

The existing research about PP-MOF-based memristors involves lateral and vertical common bottom electrode structures, missing the cross-bar structure which is the most recommended architecture due to its big potential in realistic products.[75b] In three-terminal PP-MOF neuromorphic electronics, only FET-like (i.e., FGMT) structure is studied. Based on some specific characteristics of PP-MOFs, other device structures can also be developed. For example, taking advantage of the ion transport property of PP-MOF,[36] the electrolyte-gate synaptic transistors can be developed.[10a] The discovery of new kinds of PP-MOF films with unique characters (e.g., ferroelectric and magnetic) can give birth to novel device functionalities. The AOC device is a promising direction to develop neuromorphic electronics with ultra-low power consumption. Moreover, the single device size of existing related research is micron-scale and needs to be reduced to nano scale. In contrast, fabricating single-crystal devices to investigate the intrinsic property of PP-MOFs is also attractive. Thanks to the large conjugate structure in porphyrin ligands, 2D layered PP-MOF single crystal materials can be easily synthesized,[121] which provides the possibility to fabricate devices based on mechanical exfoliation materials, just like TMDs.

4.2.2. Device Performance

Each kind of neuromorphic electronic device has its own set of essential parameters to evaluate device performance and the potential as practical products. However, some core parameters are not investigated thoroughly in current PP-MOF-related researches, such as I_{off} and V_{th} in FETs, and switching speed and energy consumption in memory and artificial synapses. Performing a comprehensive evaluation of devices is necessary.[11c,75b] In contrast, choosing a suitable and rigorous testing method is also important according to specific device characteristics. For example, the current-visible pulsed voltage stress method is highly recommended in the endurance test, especially for prototype devices based on novel materials.[93b] Some recommended testing methods have been summarized by previous reviews.[75b,93b] The reported performance of present PP-MOF-based neuromorphic electronics is not striking. This can be for two reasons: 1) the limitation of testing, that is, the device may have better performance but not tested, which can be solved by choosing a suitable testing method according to the technical requirements as recommended earlier; 2) limitations of the material itself or device structure, in the face of such situation, the choice of film preparation methods, the optimization of device fabricating techniques, and the design of device structure need to be strictly controlled according to the specific characteristics of PP-MOFs. Exploring more kinds of PP-MOFs for neuromorphic electronics is also important.

4.2.3. Environmental Response

One of the most successful application areas of PP-MOFs is sensing, including gas, light, and ions.[8a] Therefore, PP-MOFs have huge potential for developing environmental response neuromorphic electronics, like other reticular materials (e.g., ZIF-8[96a] and COF-5[122]). Moreover, introducing guest molecules or nanostructures can endow some unique performances to MOFs, which can be used as an optimizing strategy

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for developing environmental response PP-MOFs based on neuromorphic electronics. The optoelectronic characteristic is an inherent feature of PP-MOF, but it is rarely studied in neuromorphic electronics. One of the reasons is the less content of PP-MOFs in the active layer, which causes weak photo-response.[9,111] Therefore, fabricating neuromorphic electronics based on pure PP-MOF active layer and systematically studying their photo-response performance will be fascinating.

4.2.4. Device Mechanism

Obtaining in-depth insights into the device working mechanism is of paramount importance for the targeted optimization of device performance and the design of the same type of devices, and is therefore recommended. The diversification of PP-MOFs, device variability, effects of environmental conditions, and complexity of the mechanism make it very difficult to investigate the working mechanism. Besides the electrical test under a strictly controlled environment, the in situ characterizations, such as TEM and SEM,[77,89a] and device modeling, such as molecular dynamics simulation,[123] are highly recommended.[75b,86]

4.2.5. Neuromorphic Computing

Building a neuromorphic computing system at the hardware level on the basis of neuromorphic devices is a promising way to break through the von Neumann bottleneck, and realize in-memory computing and parallel data processing with low energy consumption. Unfortunately, the research about PP-MOF-based neuromorphic computing systems is still blank. High-performance PP-MOF-based neuromorphic devices are needed. The low device variability, vast number of conductance states with highly linear and symmetric, and low switching noise are vital and necessary for accurate, stable, and reliable computing.[11c,d] Moreover, the PP-MOF memristor with volatile switching, especially threshold switching, is another attractive neuromorphic electronic device, which can be used for developing artificial neurons and sensory nerves,[124] but is not reported yet. In contrast, the artificial in-sensor computing system (e.g., retinal) can also be realized by combining the PP-MOF-based neuromorphic electronics with their environmental response characteristics (e.g., light).[110,125]

To conclude, not excluding the challenges of film fabrication and application mentioned above, the PP-MOFs remain an exciting possibility for neuromorphic electronics. Besides the common features of other MOFs, such as structure/composition customizability, rich porosity, and high stability, PP-MOFs have the unique optoelectronic characteristic and the ability for forming high-quality 2D thin film, which is extremely attractive in the scope of electronic devices. With the deepening of research and resolution of challenges, it seems plausible that many breakthroughs will appear in the near future.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial synapses, data storage, film preparations, metal–organic frameworks, transistors

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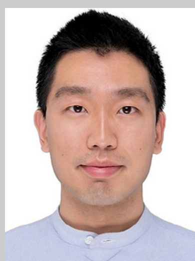

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