別紙様式５(Attached Form 5)

学位論文要旨 Abstract of Thesis

所属専攻 Field: Computer Science/ Computer Architecture 専攻(Field)
氏　名 Name: Hendarmawan（ヘンダルマワン）

Title of Thesis

Design Framework for Streaming Accelerator in Heterogeneous Computing
(ヘテロジニアスコンピューティングにおけるストリーミングアクセラレータの設計フレームワーク)

Abstract（within 1600 words）

Software development on processors is well documented and supported by the libraries provided by high level programming languages like C/C++ and Python. However, the performance of streaming data processing on processors are considerably lower performance and higher energy consumption compared to Hardware (HW) in chips implementation. On the other hand, FPGA have demonstrated great speed performance and power efficiency advantages over conventional computers in various domains, such as image processing, communication, and data analysis. In reality, design and implementation of hardware on FPGA normally take longer period of time due to its complexity for core development and it requires understanding and skills for circuit design to use tools to develop accelerator application on FPGA. This disadvantageous attribute makes development cost on FPGA become expensive and often become obstacles for software developers to design and deploy their applications on HW level.

Objective of this research are to make experiment for rules to apply regular expression pattern as template into hardware logic and to be supported on High Level Synthesis methodology. Secondly, to provide some evidence whether FPGA and Processors as a hybrid can be utilized into solution for High Performance Computing or other fields where energy consumption is the main limiting factor to comply with. The result of this research will provide information of performance, energy consumption and high productivity in term of HW-SW co-design. Moreover, we are investigating overall performance each case study and its power consumption. Furthermore, we attempt to combine the usage CPU cores along with drawbacks on these heterogeneous FPGA using Pynq Hardware and explore the capabilities of FPGA embedded platform and processors by

taking execution metrics using sets of stream processing case studies. In order to get best practices with high performance, high productivity and low power consumption, the above will be explained in this thesis. The evaluation results will be mentioned throughout the entire thesis.

This doctoral thesis is organized with six chapters. In chapter one, we introduced the research background, research objectives, contributions and thesis organization. While in chapter two, we explained various types of FPGA, FPGA architecture, and FPGA design flow. The challenges and problems of stream processing and pattern matching also described in this chapter.

In Chapter Three, we successfully applied Hardware Streaming Framework to achieve high productivity and maintain high performance. In our system, we adopt developed hCODE development kit and High Level Synthesis (HLS) to improve HW design efficiency and IP management, which allows us create more complex processors in relatively short time. For Streaming application with Email pattern matching case study, we evaluate both software and hardware for regular expression pattern matching with our framework. In addition, we utilize RE2C for software evaluation and we improve the work for High Level Synthesis for initial step for hardware evaluation. According to the evaluation results, HW/SW co-design acceleration can be achieved with our framework even though some optimization required for better performance.

In Chapter Four, we implemented and conducting evaluation using optimized software library with C/C++ and Python programming language for pattern matching and feature extraction from event stream data set with use cases for evaluation with different scenarios and implementations. Existing libraries provided by high level programming languages like C/C++ and Python and other conventional toolkits for pattern matching and feature extractions are considered as low performance compared to DFA compiler.

In Chapter Five, we presented rules and methods towards translation of regular expression pattern into supported hardware code. For evaluation we perform pattern matching and feature extraction from data stream with 5 different use-cases on 7 different implementations. We able to get better performance on HW chips compared with existing high-level programming common used libraries (C/C++ and Python regex library) and RE2C toolkit on embedded platform and processors. Our translation rules for hardware accelerator are proven with higher performance compared to other implementations on optimized software regex for both CPU and ARM processors. The performance evaluation shows that the utilization of FPGAs enable to speed up data streaming applications and at the same time significantly the energy consumption.

Finally, Chapter Six describe concluding and remarks.