An efficient reconfigurable peak cancellation model for peak to average power ratio reduction in orthogonal frequency division multiplexing communication system

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ABSTRACT

The peak to average power ratio (PAPR) in orthogonal frequency division multiplexing (OFDM) communication system will be reduced using reconfigurable peak cancellation (RPC). RPC will also aid in improves the error vector magnitude (EVM) and reduces adjacent channel leakage ratio (ACLR) in OFDM communication system. The proposed RPC design methodology and practical implementation using field programmable gate array (FPGA) are discussed. The proposed RPC has been demonstrated using VIRTEX-7 XC7Z100 dual-core FPGA device with less hardware difficulty and minimum utilization of FPGA resources. The proposed RPC improves the efficiency of OFDM communication process by reducing complementary cumulative distribution function (CCDF) with respect to instantaneous power in dB. A comparison analysis was done between the existing selective mapping (SLM) method with proposed RPS method with respect FPGA resource utilization. The proposed RPC is implemented using VIRTEX-7 XC7Z100 dual-core FPGA device. Its effectively utilizing sub-carriers, fast Fourier transform (FFT) filter, bandwidth, and sampling frequency. Due to parallel switching operation, it reduces the PAPR, ACLR and improves EVM in OFDM signal with less hardware complexity.

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1. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) waves or in other words orthogonal frequency division multiplexing waves are extensively accepted in contemporary wireless transportations schemes to provide significant benefits like flexible distribution of assets and large spectrum consumption. Since such signals are fundamentally a total of numerous signals in whichever time sphere or the given frequency, their probability density functions (PDFs) or alternatively probability density functions estimate Gaussian dissemination that has a bulky peak to average power ratio (PAPR). These stances stringent challenges over

the active variety of converters of the given data and exclusively restricts well organized procedure of the power amplifiers (PA). PAPR dipping is thus significant for enhancing the PA productivity by letting advanced average input power much earlier to the happening of saturation. The lone restraint is considered such that the adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) of consequential signal must be placed below an agreed level [1], [2].

Although the renowned probabilistic methods like selected mapping (SLM) and partial transmit sequence (PTS) methods are distortion-less, such methods show a growing calculational intricacy as additional unconventional signal arrangements are produced for assortment. It deters the execution of such methods in a high-speed real time system (HSRT) and also deters operations which are standard-compliant. Inspired by the explanations done above, modest methods like, spatial modulation (SM) and peak cancellation (PC), which have very lesser complication, can be deliberated as further truthful methods from the practical execution point of view. SM that is instituted by a clipper and a filter is the naivest procedure for lessening of PAPR. A disadvantage of SM is the regrowth of peak subsequent to filtering and the quantity of regrowth is normally not traceable [3], [4].

Many investigators recommend repetitive practice of SLM. Such thing is done to have replica of the SM blocks and there by moves towards the difficulty upsurge of many-fold. In distinction, PC is treated as a very much unnoticed method which actually has benefits in many facets. PC actually utilizes autonomous pulses which are cancelling in nature in order to abandon the values which are in peak to the threshold. Besides, PC is effortlessly constructed to do acquiescent procedure for signals of diverse communiqué principles. This is due to the fact that the pulses which are cancelling could be rationalized to assist diversity of carrier structures and bandwidths. In this context, PC can be considered to be more appropriate for real-world submissions [5], [6]. In the stiff execution space for PAPR reduction, an uneven adaptive mode PAPR lessening method in cognitive radio which shows alternate hardware execution of SLM procedure in OFDM scheme. So as to examine the viability of PC, one hardware design technique is explained with specific emphasis on field programmable gate array (FPGA) execution in contrast with the very famous SM in this work [7]–[9].

2. PEAK REDUCTION DONE BY PC

Figure 1 represents the fundamental PC outline. Pulse generators that are cancelling in nature are empowered during occurrence time when peaks which are greater than the given threshold are established. The produced pulses are surmounted and moved as per the peak angles and amplitude and deducted from indigenous signals which is represented in Figure 1.



Figure 1. Fundamental block diagram of peak cancellation

2.1. Peak cancelling method

The earmark signal must be oversampled in order to accomplish PC because of the fact that the sampled signals of Nyquist cannot properly epitomize the incessant time signal of the real peak power. The OFDM signal which uses baseband N-subcarrier through J times oversampling is articulated in the paper [10], [11].

$$a_n \triangleq \frac{1}{\sqrt{X}} \sum_{i=0}^{x-1} P_i e^{\frac{k2\pi ni}{JX}}$$
(1)

Where P_i is the quadrature amplitude modulator (QAM) it is considered as an independent distributed variable and a_n be the uncorrelated variable at J=[1, 0], then (1) can be represented as (2).

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$$a_n = |a_n|e^{j\varphi_n} \tag{2}$$

Where $|a_n|$ is the time-variant amplitude and φ_n phase variation with repect to time, if the input signal peak value reaches above the optimized threshold level p^{th} at k_p . The mathematical model of the above condition is represented by (3):

$$\overline{a_n} = a_n - q_n = a_n - \left(\sum_{k_p=0}^{N_p-1} \left(\left| a_{k_p} \right| - P_{th} \right) e^{j\varphi_{k_p}} \cdot \rho(n - k_p) \right) * D_n, 0 \le k_p \le N_p$$
(3)

where N_p represents the number of peack detection in OFDM signals at specified period.

As the cancellation pulse is deducted within the initial signal, it lessens the magnitude of signal peak to the corresponding threshold value [12]–[14]. PC situation is portrayed in Figure 2 to expedite the accepting of the given calculation.

$$\overline{a_n} = a_n \sum_{k_{p=0}}^{N_p - 1} \left(\left| a_{k_p} \right| - P_{th} \right) \cdot D_n - i_p e^{j\varphi_{i_p}}$$

$$\tag{4}$$

There is a detached filter and each and every time a peak is noticed, the cancelling pulse is produced [15].



Figure 2. Fundamental delta function signal impact on peak cancellation process

2.2. Mathematical model for cancelling pulse scheme

The PC process is a nonlinear procedure that leads to the off-target distortion and destructive induced spatial incoherence (ISI). On the idea of such anticipated results, the scheme of cancelling pulse, naturally, would be the finest cancelling pulse and thorough explorations would be essential to discover the appropriate cancelling pulse for a definite signal to fulfill the scheme necessities [16]–[18]. Largely, the incidence retort of the pulse which is cancelling in nature must adapt to the spectrum like signal so as to the scheme of cancelling pulse is basically comparable with the design of a finite-impulse-response (FIR). In order to lessen the adjacent symbol error effect and decrease realization complexity, trimming the pulses that are cancelling in nature leads to a normal result. Nevertheless, straight truncation of the canceling pulse goes towards huge off-target radiation. Thus, window function is done as a competent way to attain pulses that are having sensible frequency reaction [19], [20]. Considering the sinc wave for instance, the resultant pulse which is windowed then it represents in (5):

$$D_n = \begin{cases} Win_n sinc(\beta n), -\frac{LN-1}{2} \le n \le \frac{LN-1}{2} \\ 0, Otherwise. \end{cases}$$
(5)

where Win_n the function of a window, α represents is the form of sinc pulse and L_N depicts the window length and pulse also. In this work, Kaiser window is utilized, that is shown in (6).

$$Win_n = \frac{J_0(\sqrt[\alpha]{1-\left(\frac{2n}{LN}\right)^2})}{J_0(\alpha)} \tag{6}$$

2.3. Reduction of PAPR using conventional SM

Here, a modest SM scheme revealed in Figure 3 will be deliberated. Initially, the amplitude which is oversampled immediate OFDM signal would be delivered over a soft envelop limiter in order to accomplish the role of clipping [21]–[23]. Presuming a predefined threshold P_{th} , the n_{th} output sample is shown as in (7) and then clipping ratio is represented in (8):

$$\overline{a_n} \triangleq \begin{cases} a_n & \text{for } |s_n| < P_{th} \\ P_{th \, e^{j\varphi_n}} & \text{for } |s_n| \ge P_{th} \end{cases}$$
(7)

where $0 \le n < JN$ and $\varphi_n = \angle a_n$;

$$\tau \triangleq \frac{P_{th}}{\sqrt{P_{in}}} \tag{8}$$

where P_{in} is the input power mean value of OFDM unclipped signal.



Figure 3. Basic fundamental block functional blocks of selective mapping system

2.4. Proposed peak cancellation execution method

Knowing the elementary case of PC, the effort remaining is to understand it with judicious hardware. An arrangement to PC realization is represented in Figure 4. The immediate magnitude and stage of the intricate signal are calculated with coastal observing research and development center (CORDC) algorithm [24]-[26]. The peak identify chunk, which has few registers and comparators, detects the magnitude peak which is greater compared to the given threshold. When we notice a peak, the equivalent stage and the magnitude quantity greater compared to the threshold are actually latched and transformed to method I/Q considering alternative CORDC. There is first counter in the cancelling pulse generator chunk, which is unswervingly associated with the reduced-order models (ROM) address port. The already found cancelling pulse, that actually is amenable compared to the final signal spectrum, is deposited in the ROM. Then the given counter is activated once one peak is found, and when it becomes L, it is reset. To handle the existence of rigorous peaks, numerous cancelling pulse generators are essential to produce autonomous pulses that are cancelling in nature and we can see this in Figure 5, where the dissemination will happen from left to right for the given signal. In the left, when we notice a primary peak, the initial generator would be enabled for L clocks to produce the primary cancelling pulse [27]-[29]. When we notice second and the third peaks and when the first generator is on only, the second and third generators are produced, in order, to trigger the second and third cancelling pulses. When ROM 1 is free and in case the fourth peak is noticed, the first generator will be reprocessed to produce the fourth cancelling pulse. This process lasts till no peak which is greater compared to the threshold is established. All cancelling pulse generator outputs are totaled and lastly deducted from the deferred signal which is original. It is understood that the complication of resources in this method is confined by the quantity of obtainable cancelling pulse generators and the generators in top part of Figure 4 which has greater possibility to be utilized when the cancelling pulse generators in the foot could be sluggish many of the time [30], [31]. Hence few negotiations would be essential in order to find the quantity of how much cancelling pulse generators are actually utilized [32]-[34].



Figure 4. Internal hardware architecture of proposed reconfigurable peak cancellation



Figure 5. OFDM signal implementation using multiple cancelling pulse

3. SIMULATION RESULTS

3.1. Execution procedure

Note that using the Xilinx ISE 14.7 evaluation board, the scheme of reconfigurable peak cancellation (RPC) is executed which has a Virtex-7 XC7Z100 dual core FPGA device. 32 QAM signal is taken into account and the 3,250 fast Fourier transform (FFT) size is used with the amount of sub-carriers' equivalent to 1,500 that shows an employed bandwidth of 20 MHz and a fundamental sampling frequency of 32.78 MHz. So as to get an exact peak value, we fix the oversampling ratio which is equal to 8. Thus, the

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total sampling rate is 255.78 MHz. The assessment panel has a local oscillator of 220 MHz that is used to produce the system clock which is having the on-chip clock supervisor resources.

3.2. Investigational outcomes

With respect to this work, we mention the PAPR as the measured instant power standardized average power beneath an assured probability. Figure 6 represents the subsequent CCDF or in other words called complementary cumulative distribution function for RPC and SM schemes both. In the research, though CCDF outcomes with final PAPR from 5 dB to 9 dB are computed, the CCDF curves of final PAPR equivalent to 7 dB and 9 dB are portrayed for the intention of demo. To assess the efficacy of PAPR lessening, we display the realized PAPR versus over average power of threshold in Figure 7. It indicates the fact like RPC contributes stable PAPR lessening when the final PAPR is greater compared to 7 dB. Alternatively, the SM depicts a clear breach among the realized PAPR and final PAPR, due to the even effect of the filter after clipping.

In Figure 8, for various realized PAPRs, ACLR is drawn. With the similar realized PAPR, we can examine and explain that PC depicts improved ACLR enactment. Improved outcome is acquired for PC also in the test of EVM that is shown in Figure 9. This outcome is because of the point that the filtering process is prepared on every signal point in time area, while PC merely provides outcome to restricted length of the signal as debated previously.



Figure 6. Comparison analysis of CCDF response with respect OFDM signal range from 7 dB to 9 dB



Figure 8. ACLR simulated comparison analysis between SLM and RPC



Figure 7. Attained PAPR simulated comparison analysis between SLM and RPC



Figure 9. EVM simulated comparison analysis between SLM and RPC

3.3. Comparison of employment of resources

Table 1 shows the overview of FPGA resource utilization during execution process of proposed RPC scheme and conventional SM scheme. Its effortlessly found that demonstrates very less hardware difficulty with respect to the necessary utilization number of 64 bits flip flops (FFs), 64-bit look-up table (LUTs) and DSP48E2 Xilinx multipliers in mode consumptions. Alternatively, PC wants extra memory for keeping the anticipated cancelling pulses in the storage.

Table 1. FPGA resources utilization analysis between RPC and SM							
		RPC			SM		
SI.NO	Resource	Used	Available	Utilization (%)	Used	Available	Utilization (%)
1	Programmable I/O	26	400	6.5	72	400	18
2	Global Buffer	1	25	4	2	25	8
3	Function	5	11800	0.0423	5	20	25
	Generator						
4	LUTs Slices	4250	13250	32.075	11,250	13000	86.538
5	Flip flop (FFs)	4500	20000	22.5	12250	20000	61.25
6	Block RAM	5	10	50	0	0	0
7	Block Multiplexer	15	500	3	175	500	35

4. CONCLUSION

The proposed RPC more efficiently reduces the complexity of hardware implementation and its overheads. A reconfigurable peak cancellation design methodology and practical implementation using FPGA are discussed and specific attention on the resource utilization during the communication process is made. As per performance analysis, it shows the proposed method has a better efficiency of 2.5% compared to the conventional methods. Due to the reconfigurable parallel operation of the proposed method, it is efficiently capable to handle multicarrier wireless transmitter with lower hardware complexity of about 9%, lower ACLR of 2.33% and improved EVM of 1.88% compared to conventional methods. With respect to further investigation, theoretically, we can examine the RPC methods through further accurate design standard which may affect optimal enactment for specified PAPR values. Also, the system-level examination is essential to see the outcomes of channel coding and frequency discerning fading channels. Limitation: loss of information occurs when communication takes place in the highly restricted and remote region having high bandwidth in 5G technology. Future scope: infield of FPGA, many innovations are being carried out, due to this a high-speed switch operation performed parallelly without overhead in 5G communication process.

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