A Cascaded Multilevel Inverter Based on New Basic Units

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Abstract

Due to the ever-increasing importance of multilevel inverters, researchers try to offer new structures for this type of inverters to improve their performance and reduce their costs. In this paper, a new topology has been proposed for cascaded multilevel inverters. This inverter is formed by the series connection of new basic units which utilize fewer power switches in their structure. The reduction in the number of components used in this new inverter has resulted in lower economic costs and installation area. Also, four different methods have been proposed to determine the magnitudes of the input voltage sources enabling the proposed inverter to operate in both symmetric and asymmetric modes. To show the advantages of the inverter, it is compared with the conventional cascaded H-bridge inverter and other similar ones. The simulation and experimental results confirm the performance accuracy of the proposed inverter and also its ability to generate different voltage levels at the output.

Keywords: Cascaded inverter, Basic Unit, Voltage source, Modular, Multilevel Inverter (MLI).

1. Introduction

Traditionally, the conversion of DC power to AC was done by two-level inverters, but recently, multilevel inverters have become popular due to their abundant advantages over the two-level ones and as a result, they are being extensively used in different industrial fields such as active power filters, renewable energy source interface circuits, static compensators, flexible AC transmission systems (FACTS) and High Voltage DC (HVDC) systems (Gupta *et al.*, 2016; Khodaparast *et al.*, 2020). The most important advantage of multilevel inverters (MLIs) is their high output power quality (Siddique *et al.*, 2019). This valuable feature is acquired by generating stepped and multilevel voltage at the output (Can, 2020a). By increasing the number of voltage levels, the total harmonic distortion (THD) of the output will be decreased (Azimi *et al.*, 2021). Furthermore, by changing the switching strategy in MLIs, like switching at high frequency or using filters in the circuit (Shuvo *et al.*, 2019), using selective harmonic elimination (Siddique *et al.*, 2019), optimizing firing angles by genetic algorithm (Farokhnia *et al.*, 2012), or other optimization techniques, the THD can be further reduced (Can, 2020b).

Some other remarkable advantages of multilevel inverters to mention are: less voltage stress on switches, less dv/dt at the output, ability to operate in higher voltage and power rates, and better electromagnetic compatibility (Farokhnia *et al.*, 2012; Nilkar, Babaei and Sabahi, 2012). These inverters are categorized as Diode Clamped, Flying Capacitor (FC), and cascaded H-Bridge (CHB) (Gupta *et al.*, 2016; Khodaparast *et al.*, 2020). To produce N number of voltage levels at the output by using a single-phase diode clamped inverter, $(N-1)(N-2)$ clamped diodes, 2(N-1) switching components and N-1 number of DC link capacitors are required (Colak, Kabalci and Bayindir, 2011). In this inverter, by increasing the number of output levels, the number of circuit components increases, significantly. Unlike diode clamped inverters, FC-MLIs use flying

capacitors instead of clamped diodes. In one N-level single-phase FC inverter, N-1 number of DC link capacitors and $(N-1)(N-2)/2$ number of auxiliary capacitors are required. The accurate control of charging and discharging of the capacitors becomes more and more difficult as the number of voltage levels increases (Colak, Kabalci and Bayindir, 2011; Azimi *et al.*, 2021). Also, there is another type of MLIs called Switched Capacitor (SC) MLIs. In the structure of these converters, several capacitors are utilized which facilitates producing the output voltage levels. Based on the required output voltage waveform and circuit design, several capacitors, usually one input source and in some topologies more than one source are utilized (Khodaparast, Adabi and Rezanejad, 2018). However, the noticeable advantages for these inverters are about their operation simplicity that unlike FC and NPC ones, they require neither any external sensors nor external auxiliary controllers for voltage balancing of the capacitors (Azimi *et al.*, 2020). Besides, SC-MLIs benefit from lower voltage stress on semiconductor devices; on the other hand, due to utilization of several capacitors in their structure, they suffer from the spikes of the input current which restricts their industrial application (Mehrasa *et al.*, 2020).

The fourth category is conventional CHB (CCHB). This inverter is formed by series connection of H-Bridges. Among multilevel inverters, cascaded inverter uses the lowest number of components in its structure for generating certain voltage levels (Colak, Kabalci and Bayindir, 2011). Also, this inverter reaches higher voltage, power and reliability levels in comparison to the others (Tsang and Chan, 2014). Since the voltage sources used in this inverter should be isolated, then it is possible to replace them with capacitors, photovoltaic cells, fuel-cells and so on. In terms of the magnitudes of input sources, this inverter is divided into symmetric and asymmetric topologies (Babaei *et al.*, 2016; Lee *et al.*, 2018; Ponnusamy *et al.*, 2020). In symmetric topology, the magnitudes of input voltage sources are the same. In this type, in the case of the existence of

N voltage sources at the input, 2N+1 number of levels could be generated in the output phase voltage (Samadaei *et al.*, 2016). Symmetric inverters have high levels of modularity and this remarkable feature makes it possible to increase the number of voltage levels without increasing the complexity of circuit and only by adding similar cells to the inverter structure (Babaei *et al.*, 2016). This topology has a high reliability and all the switching components used in its structure are identical. But the major defect of it is: with an increase in the number of voltage levels, the required number of components increases significantly and as a result, the volume of the circuit and its costs rise. One way to solve this problem is to use asymmetric structure (Babaei *et al.*, 2016; Lee *et al.*, 2018). In this topology, the magnitudes of input voltage sources are not equal. This topology loses mentioned modularity, although obtains the ability to generate more voltage levels compared to symmetric topology which means achievement of higher power quality and less cost (Gupta *et al.*, 2016). The most important concern of designers in this area is that as the number of circuit components rises, the control complexity of the inverter increases. Also, the increment of circuit devices leads to an increase in the manufacturing cost while decreases the converter reliability. As a solution, several new topologies have been proposed that require fewer number of components in their structures (Manjrekar and Lipo, 1998; Babaei and Hosseini, 2007; Laali, Abbaszadeh and Lesani, 2010; Colak, Kabalci and Bayindir, 2011; Debnath *et al.*, 2015; Gupta *et al.*, 2016; Siddique *et al.*, 2019, 2020). In some cases, several novel switching schemes have been proposed which by implementing them, total switching or conduction loss or even the control complexity of the circuit is reduced (Debnath *et al.*, 2015; Gupta *et al.*, 2016).

Based on the mentioned issues, this paper deals with proposing a new topology with reduced number of power switches based on CHB-MLI concept. This structure is comprised a series connection of new basic units. Unit based topologies have kind of special reliability means

defective units could be bypassed and inverter continues to operate without shutting down or losing the load. Accordingly, the organization of this article is as follows: Section 2 explains the proposed topology and its features in detail. Comparison between the proposed topology and CCHBI in terms of the number of required switches and input sources is conducted in Section 3. Section 4 reports the simulation and experimental results of a single-phase 15-level multilevel converter based on proposed topology, which prototype outputs verify the theoretical discussions. Finally, the present study is concluded in Section 5.

2. The proposed structure

The proposed basic unit of this study consists of three isolated DC voltage sources and eight power switches, which is illustrated in Figure 1. By using an accurate and precise switching algorithm, input sources can be connected to the output individually or in series and generate desired stepped voltage which is the basic principle of multilevel inverters. To avoid $V_{1,1}$ of being short circuited, switches $S_{1,1}$, $S_{1,2}$ and $S_{1,3}$ never turn on simultaneously. This point is considered for other sources, too. Table 1 shows the state of switches in the basic unit for generating different voltage levels at the output. In this table, 0 means the switch is OFF and 1 means it is ON.

To generate more levels at the output, it is possible to connect a number of basic units in series. Figure 2 shows the general form of the proposed inverter. As an example, if two units are connected in series, there would be six input sources and 16 power switches. More number of sources, means more magnitude summations which also means more voltage levels could be generated and the output gets closer to a sinusoidal waveform. Hence, the concept of series units is used for achieving more steps and higher voltages with lower THD. An H-bridge is connected to the inverter which is vital to produce negative voltage polarity. In the bridge, T_1, T_4 in positive and T_2, T_3 in negative half-period of voltage turn on, simultaneously. It means over one period;

these switches turn on and off just one time. According to Table 1, during one voltage cycle, $S_{1,1}$ seven times, $S_{2,1}$ six times, $S_{3,1}$ and $S_{6,1}$ three times, $S_{4,1}$ four times, $S_{5,1}$ one time, $S_{7,1}$ and $S_{8,1}$ two times, are switched on. The naming convention for components is as follows: the voltage sources and switches are shown by $V_{i,j}$ and $S_{k,j}$, respectively which i (i=1,2,3,) and k (k=1,2,…,8) used for numbering them and j(j=1,2,…n) shows the unit number. For instance, $V_{3,2}$ is the third voltage source in the second unit and or $S_{5,3}$ is the fifth power switch in the third unit. When the switch $S_{8,j}$ is ON, the j^{th} unit is bypassed and zero voltage level is generated. $S_{2,j}$ is a bidirectional switch while the others are unidirectional one.

The proposed inverter can operate in both symmetric and asymmetric modes. Accordingly, four procedures have been proposed to determine magnitudes of input sources. For each of these procedures, number of voltage levels and maximum output voltage that can be generated are calculated in the following. Also, the number of switches and maximum blocked voltage by them are given.

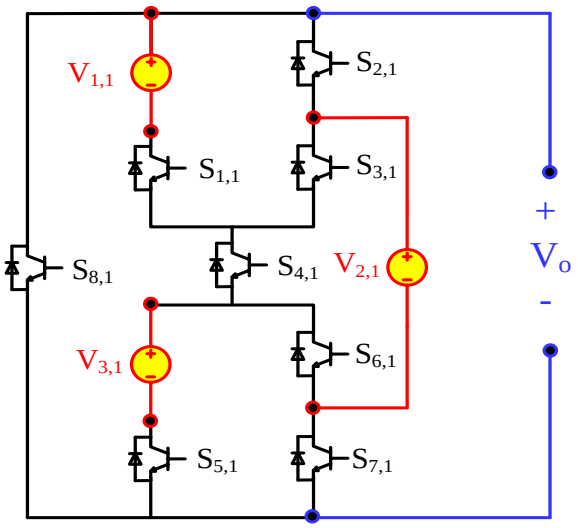


Figure 1. Proposed basic unit

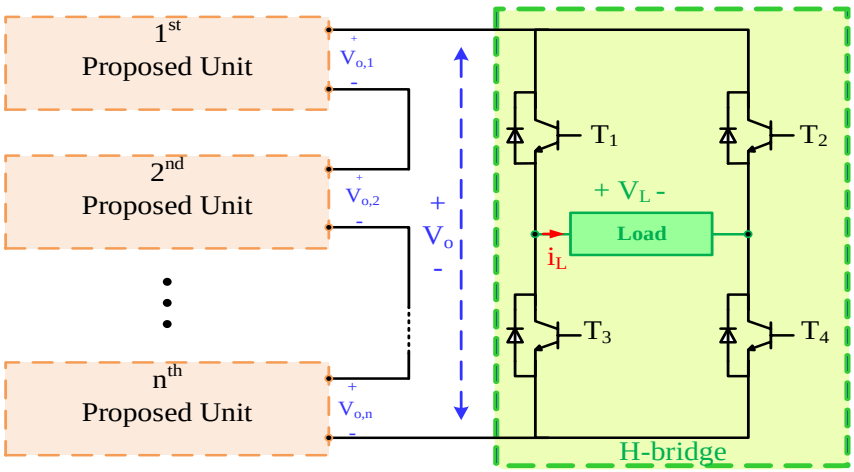


Figure 2. Proposed topology in general

Table 1. State of switches to produce different voltage levels in the basic unit

$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{6,1}$	$S_{7,1}$	$S_{8,1}$	Vo
0	0	0	0	0	0	0	1	0
1	0	0	1	0	1	1	0	$V_{1,1}$
0	1	0	0	0	0	1	0	$V_{2,1}$
1	0	1	0	0	0	1	0	$V_{1,1}+V_{2,1}$
0	1	1	1	1	0	0	0	$V_{3,1}$
1	0	0	1	1	0	0	0	$V_{1,1}+V_{3,1}$
0	1	0	0	1	1	0	0	$V_{2,1}+V_{3,1}$
1	0	1	0	1	1	0	0	$V_{1,1}+V_{2,1}+V_{3,1}$

These two recent mentioned parameters are really determinant in the manufacturing cost of the inverter. Maximum blocked voltage is obtained by sum of the maximum blocked voltages by each of the switches and it can be calculated as follows:

$$(V_{block})_{S8,j} = V_{1,j} + V_{2,j} + V_{3,j} \quad (1)$$

$$(V_{block})_{S1,j} = (V_{block})_{S2,j} = 2(V_{block})_{S3,j} = V_{1,j} \quad (2)$$

$$(V_{block})_{S4,j} = V_{2,j} \quad (3)$$

$$(V_{block})_{S5,j} = 2(V_{block})_{S6,j} = (V_{block})_{S7,j} = V_{3,j} \quad (4)$$

According to above equations, in each unit, $S_{8,j}$ blocks highest voltage so this switch should have highest voltage tolerance. For the switches of the H-bridge, blocked voltages are given as the following:

$$\frac{(V_{block})_{H-bridge}}{4} = (V_{block})_{T1} = (V_{block})_{T2} = (V_{block})_{T3} = (V_{block})_{T4} = Vo_{max} \quad (5)$$

Regarding equation (5), the bridge blocks $4Vo_{max}$ and Vo_{max} is the peak voltage at the output and it is sum of the magnitude of all input voltage sources. Hence, each of bridge switches must be able to block peak voltage. Then, the total blocked voltage for proposed inverter can be obtained from the equation (6),

$$(V_{block})_{Total} = 3.5\sum_{j=1}^{n} V_{1,j} + 2\sum_{j=1}^{n} V_{2,j} + 3.5\sum_{j=1}^{n} V_{3,j} + (V_{block})_{H-bridge} \quad (6)$$

Where 'n' is the number of units. Here, four procedures named as P_1 to P_4 have been proposed to determine magnitudes of required input sources. Implementing these schemes make the operators capable to face different situations in the operation of inverter. In P_1 the magnitude of the input sources is equal, therefore:

$$V_{1,j} = V_{2,j} = V_{3,j} = V_{dc} \quad (7)$$

Then:

$$N_{level} = 6n + 1 \quad (8)$$

$$N_{switch} = 8n + 4 \quad (9)$$

$$Vo_{max} = (3n)V_{dc} \quad (10)$$

$$V_{block} = (21n)V_{dc} \quad (11)$$

Where 'n' is the number of units, N_{level} is the maximum number of voltage levels and

N_{switch} is the number of required switches considering H-bridge. According to equation (7) all input sources are the same which means the inverter is symmetric using P_1. Thus, to have a versatile inverter which can work in asymmetric mode, P_2, P_3 and P_4 are defined in the following. P_2 is defined as;

$$V_{1,j} = 2^{3j-3}V_{dc} \tag{12}$$

$$V_{2,j} = 2^{3j-2}V_{dc} \tag{13}$$

$$V_{3,j} = 2^{3j-1}V_{dc} \tag{14}$$

$$N_{level} = 2^{3n+1} - 1 \tag{15}$$

$$N_{switch} = 8n + 4 \tag{16}$$

$$Vo_{max} = 7V_{dc}\sum_{j=1}^{n} 2^{3j-3} \tag{17}$$

$$V_{block} = (\frac{49.5}{8})V_{dc}\sum_{j=1}^{n} 2^{3j} \tag{18}$$

P_2 is actually a binary incremental scheme. To be clear, in first unit, the source magnitudes are V_{dc}, $2V_{dc}$ and $4V_{dc}$.

Another scheme is P_3 which by using it, the calculation of parameters would be:

$$V_{1,1} = V_{2,1} = V_{3,1} = V_{dc} \tag{19}$$

$$V_{1,j} = V_{2,j} = V_{3,j} = 2^{j}V_{dc} \qquad for \;\; j > 1 \tag{20}$$

$$N_{level} = \begin{cases} 7 & for \quad n = 1 \\ (24\sum_{j=2}^{n} 2^{j-2}) + 7 & for \quad n > 1 \end{cases} \tag{21}$$

$$N_{switch} = 8n + 4 \tag{22}$$

$$Vo_{max} = \begin{cases} 3V_{dc} & for \quad n = 1 \\ 3V_{dc}\left(1 + \sum_{j=2}^{n} 2^{j}\right) & for \quad n > 1 \end{cases} \tag{23}$$

$$V_{block} = \begin{cases} 21V_{dc} & for \quad n = 1 \\ 21V_{dc}\left(1 + \sum_{j=2}^{n} 2^{j}\right) & for \quad n > 1 \end{cases} \tag{24}$$

Finally, P_4 is defined as below:

$$V_{1,j} = (3j - 2)V_{dc} \tag{25}$$

$$V_{2,j} = (3j - 1)V_{dc} \tag{26}$$

$$V_{3,j} = (3j)V_{dc} \tag{27}$$

$$N_{level} = 3n(3n + 1) + 1 \tag{28}$$

$$N_{switch} = 8n + 4 \tag{29}$$

$$Vo_{max} = 3V_{dc}\sum_{j=1}^{n}(3j - 1) \tag{30}$$

$$V_{block} = V_{dc}\sum_{j=1}^{n}(63j - 21) \tag{31}$$

The use of these four methods gives a special flexibility to the inverter and possibility to generate different voltage levels.

3. Comparative Study

In this section, the proposed inverter is compared with the CCHBI in terms of the number of required switches and voltage sources. Considering CCHBI as symmetric and assuming that there are N number of voltage sources in its structure, then method M_1 would be:

$$V_1 = V_2 = \cdots = V_N = V_{dc} \tag{32}$$

$$N_{level} = 2\mathrm{N} + 1 \tag{33}$$

$$N_{switch} = 4N \tag{34}$$

That, N_{level} and N_{switch} are the number of voltage levels and required switches, respectively. In (Manjrekar and Lipo, 1998; Babaei and Hosseini, 2007; Laali, Abbaszadeh and Lesani, 2010) three other methods are given to determine the magnitudes of CCHBI input sources which are shown by M_2-M_4, respectively. According to M_2:

$$V_1 = \frac{V_2}{2} = \frac{V_3}{2} = \cdots = \frac{V_N}{2} = V_{dc} \tag{35}$$

$$N_{level} = 4N - 1 \tag{36}$$

$$N_{switch} = 4N \tag{37}$$

Also, calculations of M_3 are as follows:

$$V_1 = \frac{V_2}{3} = \frac{V_3}{3} = \cdots = \frac{V_N}{3} = V_{dc} \tag{38}$$

$$N_{level} = 6N - 3 \tag{39}$$

$$N_{switch} = 4N \tag{40}$$

Besides, the equations of M_4 are:

$$V_N = 2^{N-1} V_{dc} \tag{41}$$

$$N_{level} = (2^{N+1}) - 1 \quad (42)$$

$$N_{switch} = 4N \quad (43)$$

Finally, a unary incremental scheme of M_5 are as:

$$V_N = NV_{dc} \quad (44)$$

$$N_{level} = N(N+1) + 1 \quad (45)$$

$$N_{switch} = 4N \quad (46)$$

The last one named as M_5, is a very common method that many of designers have used it to determine the magnitude of input sources. Considering the description of each method as well as the proposed ones, the key characteristics of all approaches are summarized in Table 2. According to this table, the number of switches used in M_1-M_5, are identical but number of levels vary. Similarly, the number of required semiconductor devices in P_1-P_4 are the same, while the output voltage levels, and generated voltage differ from each other.

Table 2. Comparative overview of Key characteristics for each topology

REFERENCE	SYMBOL	N LEVEL	V_N	N SWITCH
PROPOSED STRUCTURE	P_1	$6n+1$	$(3n)V_{dc}$	$8n+4$
	P_2	$2^{3n+1}-1$	$7V_{dc}\sum_{j=1}^{n} 2^{3j-3}$	$8n+4$
	P_3	$(24\sum_{j=2}^{n} 2^{j-2})+7$	$3V_{dc}\left(1+\sum_{j=2}^{n} 2^{j}\right)$	$8n+4$
	P_4	$3n(3n+1)+1$	$3V_{dc}\sum_{j=1}^{n}(3j-1)$	$8n+4$
CCHBI	M_1	2N+1	V_{dc}	4N
BABAEI & HOSSEINI, 2007	M_2	4N-1	$2V_{dc}$	4N
LAALI ET AL., 2010	M_3	6N-3	$3V_{dc}$	4N
MANJREKAR & LIPO, 1998	M_4	$(2^{N+1})-1$	$2^{N-1}V_{dc}$	4N
COMMON METHOD	M_5	N(N+1)+1	NV_{dc}	4N

To better clarify the differences mentioned in Table 2, a graphical comparison is conducted in this study. Accordingly, Figure 3 shows a comparison between P_1 and M_1 in terms of the number of switches in different voltage levels. As it is clear from this figure, in the symmetric mode, the proposed inverter needs fewer power switches in its structure for generating certain voltage levels. Figure 4 and 5 show comparisons among P_2-P_4 and M_2-M_5 in terms of the number of required switches and sources in different voltage levels, respectively. As it can be seen in these figures, in asymmetric mode, the proposed inverter uses fewer components compared to CCHBI which results in decreasing inverter control complexity, installation area, and cost. For example, by using 6 isolated DC power supply to generate 13 voltage levels in the output, the proposed inverter (P_1) uses twenty power switches while M_1 requires 24 power switches for the same condition. Requiring four more power switches means further initial cost as well as further gate driver circuits and other auxiliary devices.

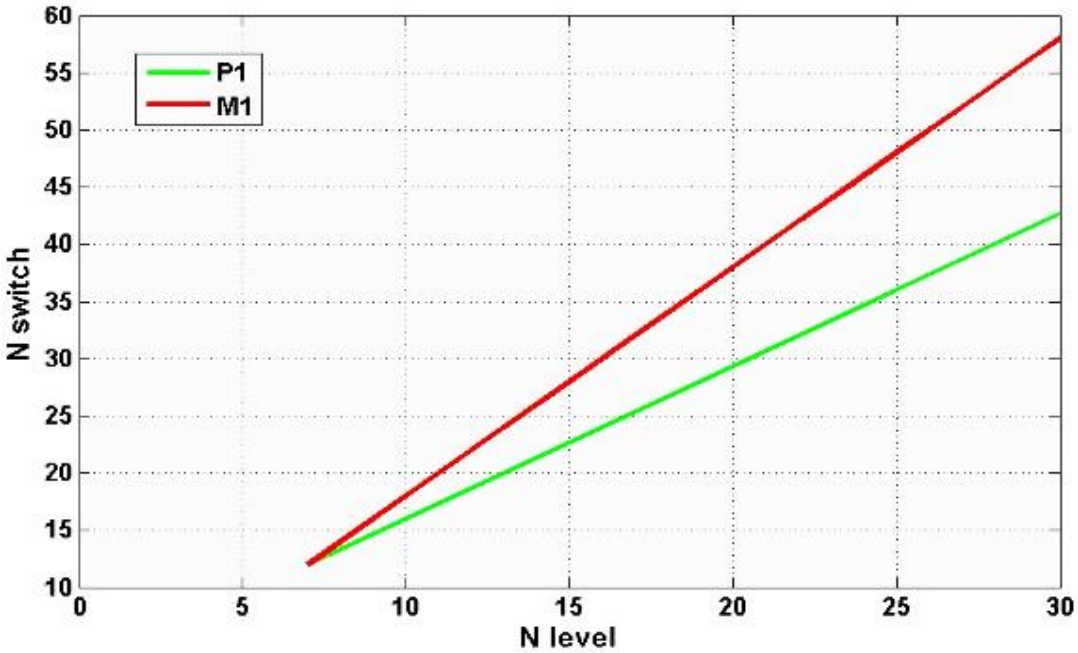


Figure 3. Comparison between P_1 and M_1 in terms of the number of switches versus voltage levels

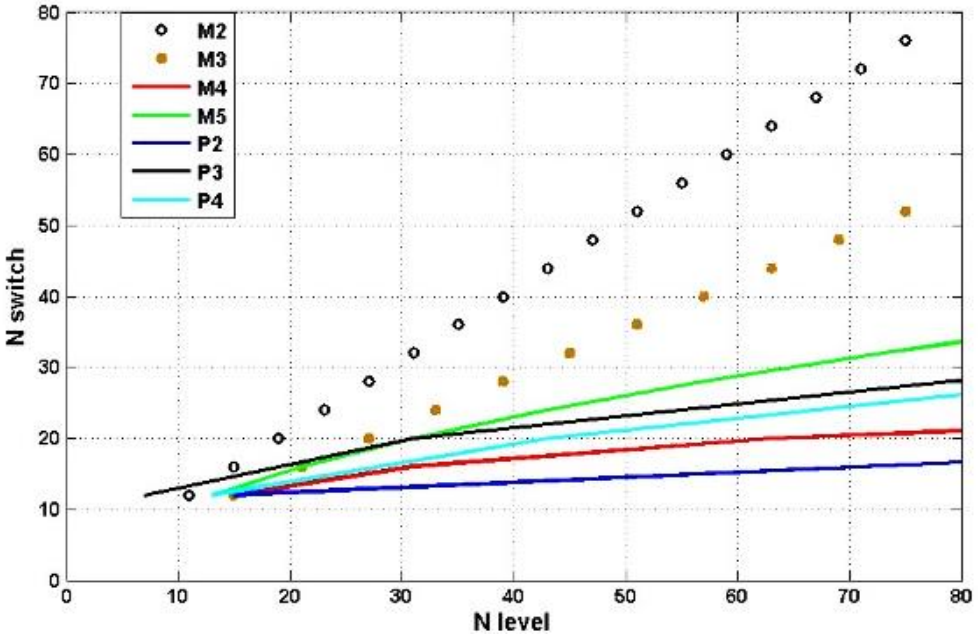


Figure 4. Comparison between P_2-P_4 and M_2-M_5 in terms of the number of switches versus voltage levels

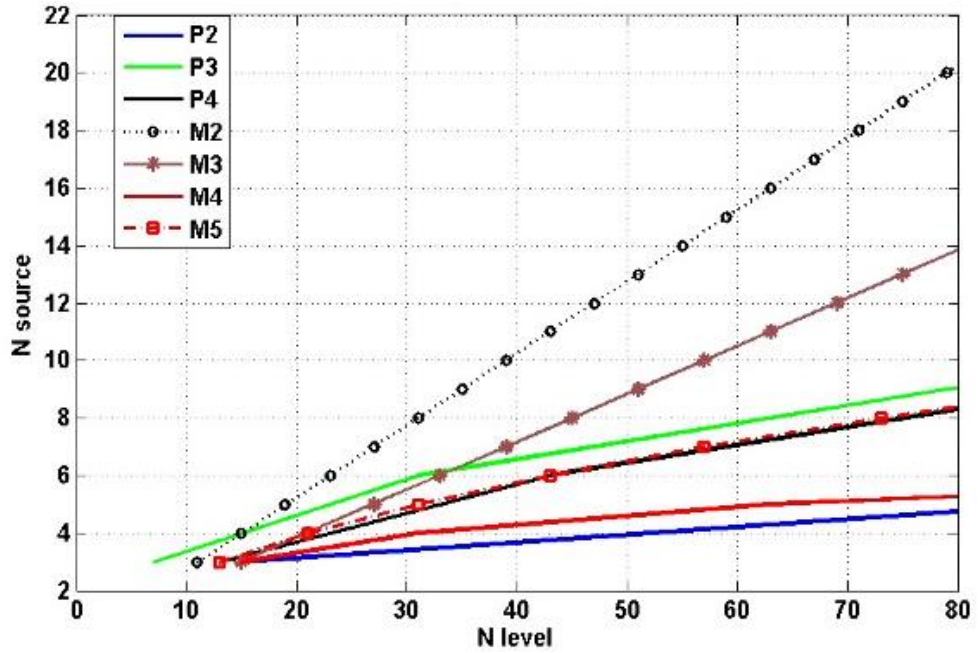


Figure 5. Comparison between P_2-P_4 and M_2-M_5 in terms of the number of sources versus voltage levels

4. Performance Assessment

This section is devoted to the efficacy evaluation of the proposed converter via simulation and experimental results. To reach this goal, one basic unit based on P_2 is simulated in MATLAB/SIMULINK software. The Nearest Level Modulation (NLM) technique is used for the operation control of the proposed inverter (Ponnusamy *et al.*, 2020; Azimi *et al.*, 2021). The overview of the NLM strategy for the proposed inverter is depicted in Figure 6. To generate the desired output 50 Hz voltage waveform, the sampled voltage waveform (V_{sample}) have to follow the reference voltage ($V_{reference}$) so that the sample voltage is always estimated and rounded to the nearest integer value of the reference signal by using (47). Consequently, each voltage level could be shaped in a way that, the active times of each switch is calculated considering the time duration of each output level (T_i).

$$V_{sample} = V_{dc} \times round(\frac{V_{refrence}}{V_{dc}}) \quad (47)$$

Accordingly, the switching times of each level are obtained and presented in Table 3. Afterward, by use of these times and applying them to the inverter with their corresponding switching states, as described in section 2, Table 1, the 15-level output voltage waveform can be achieved. Also, the magnitudes of input sources are $V_{1,1}$=4V, $V_{2,1}$=8V, $V_{3,1}$=16V. Thus, the amplitude of the output peak voltage is 28 volts, which is the sum of all input sources.

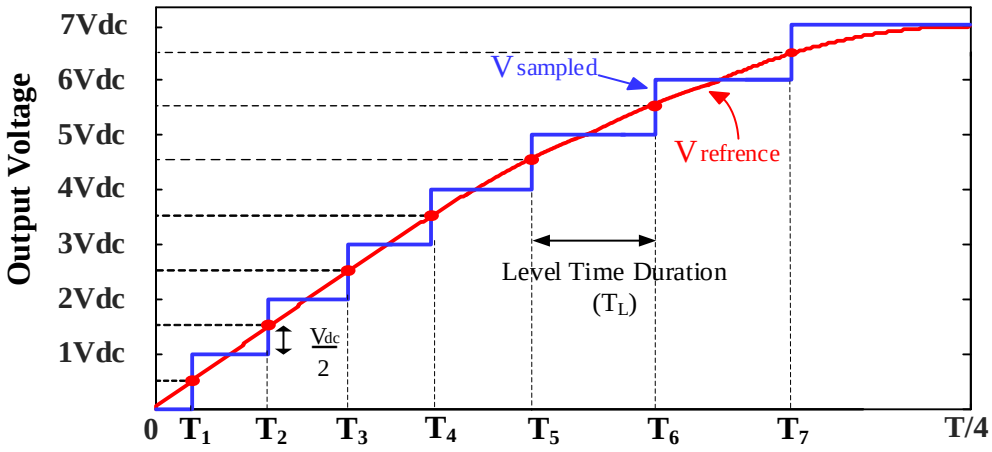


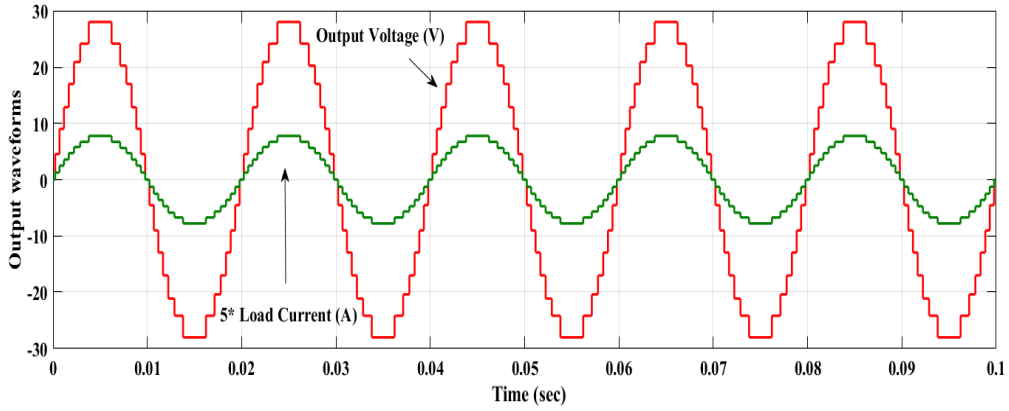
Figure 6. Applying NLM strategy for the proposed inverter

Table 3. Switching times of the NLM for the proposed inverter

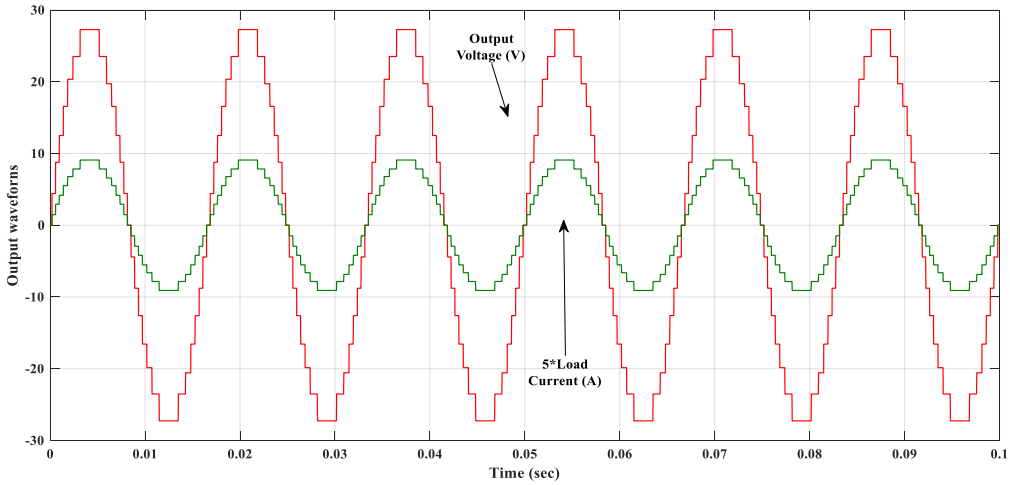
Switching Times (micro second)	
T_1	227
T_2	687
T_3	1162
T_4	1666
T_5	2222
T_6	2877
T_7	3789

A. Simulation Results

To obtain an accurate analysis of the proposed structure's operation, different operating conditions are studied in this part. Initially, sufficient performance of the inverter at different output frequencies is investigated. Accordingly, the operation of the proposed inverter at 50 Hz and 60 Hz operating modes, supplying a pure resistive load (R_1=15 Ω) are presented in Figure 7 ensuring the appropriate performance of the inverter. It should be noted that for more clarification, the current waveforms are multiplied by 5 in all simulations.



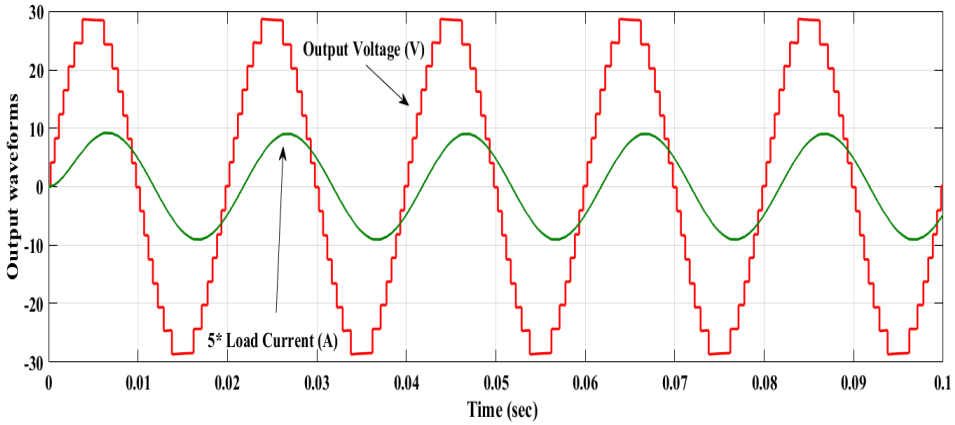
(a)



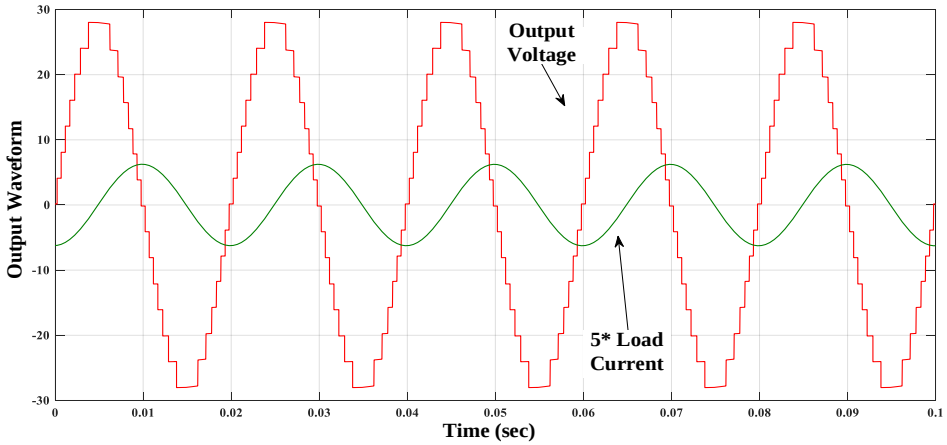
(b)

Figure 7. Output voltage and current waveforms of the inverter supplying a resistive load at: (a) 50 Hz and (b) 60 Hz operating modes

Moreover, the inverter should be able to supply different loads. Hence, the simulation results of the output voltage and load current of the 50Hz converter feeding a resistive-inductive load (R_2=13 Ω + L_2= 24 mH) and a pure inductive load (R_3= 60 mH) are depicted in Figure 8. In addition, the harmonic content of the proposed inverter for the voltage reached 5.47% (Figure 9). According to the Figure 9, all the harmonic spectra stay under five percent, and the overall harmonic content is below eight percent, satisfying the IEEE- Std. 519-2014 requirements.



(a)



(b)

Figure 8. Output voltage and current waveforms of the 50 Hz inverter supplying a: (a) resistive-inductive and (b) pure-inductive load

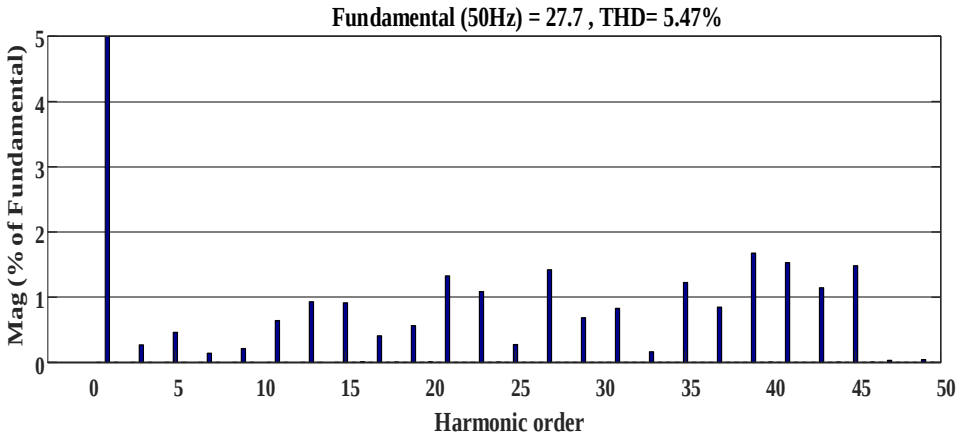
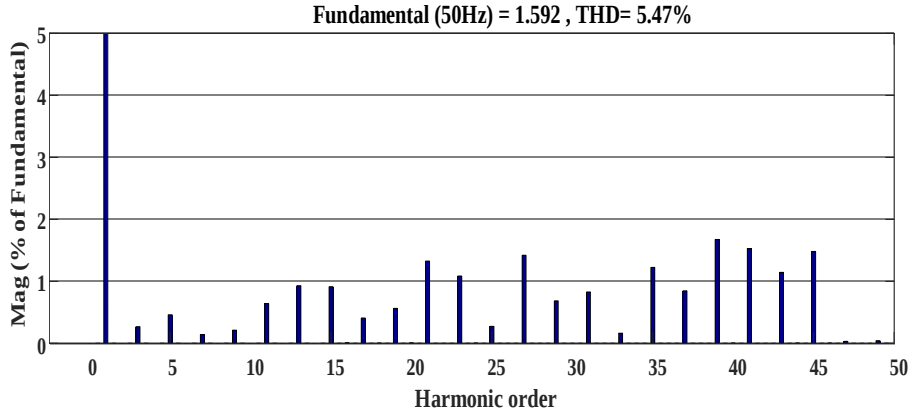
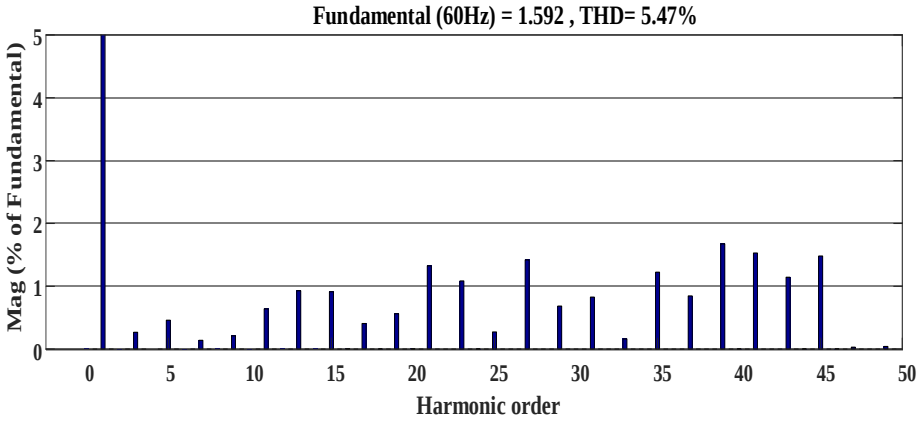


Figure 9. Harmonic content of the proposed inverter's voltage

Furthermore, the harmonic spectrum of the output current for the resistive load (R_1) is included in Figure 10. As it can be seen, the output current waveform properly follows the output voltage despite operating under various frequencies. This results in uniform output waveforms with similar harmonic content. Accordingly, considering the fact that all the individual components of the harmonic content are far below five percent. For example, 39th harmonic order seems to be the dominant spectrum with the value below two percent. In addition, the amount of THD is only 5.47 percent, which is under eight percent, ensuring that the operation of the proposed inverter can sufficiently meet the requirements of the IEEE-std.519-2014 standard.



(a)



(b)

Figure 10. THD of the output current at: (a) 50 Hz and (b) 60 Hz

For more clarification, the THD of the output current when the inverter is supplying the resistive-inductive load (R_2=13 Ω + L_2= 24 mH) is investigated. With regard to the inductive behaviour of the load, it is expected to face a lower amount of THD. Hence, the most important feature of this factor would be the one obtained from a resistive load showing the worst condition of the harmonic contents. The THD of the load current for the mentioned R-L load is presented in Figure 11.

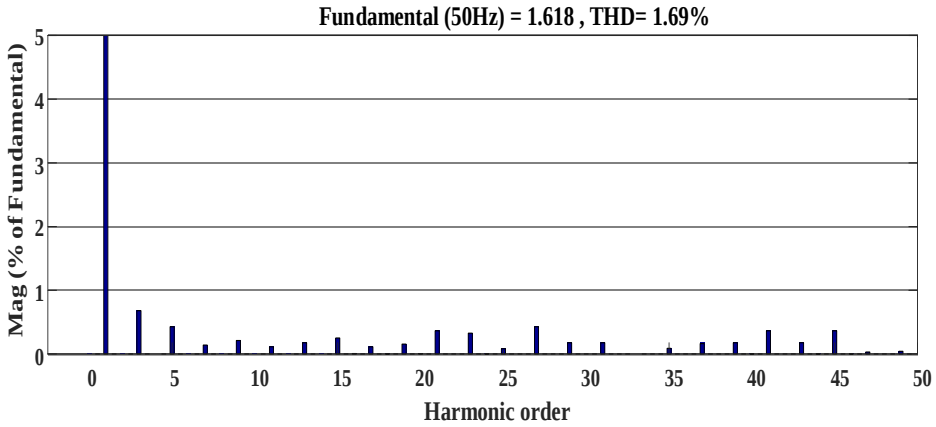


Figure 11. THD of the output current for R-L load

Accordingly, the THD of 1.69 percent is achieved approving the significance of the resistive load behaviour. Finally, the obtained results ensure the sufficiency of the output power quality for the most possible operating point of the inverter for grid-integrated application of the proposed inverter especially, renewable energy applications.

B. Experimental Results

To verify the theoretical and simulation studies, an experimental prototype has been developed. In the inverter prototype, IGBTs manufactured by International Rectifier with model of G4PH50UD are used. To produce the control pulses for the switches, a microcontroller made by ATMEL with model of MEGA256 is applied. The power switch gate driver includes opto-coupler IC with model of 4N27 for electrically decoupling microcontroller and the power switches. Another utilized IC is ULN2003, which is consists of seven open collector Darlington pairs with

common emitters to provide the required current for the gate signals. Also, it should be considered that there is no filter at the load side. The overview of the developed laboratory prototype is displayed in Figure 12. As it is shown, the prototype consists of microcontroller, basic unit, and H-bridge as the inverter main parts.

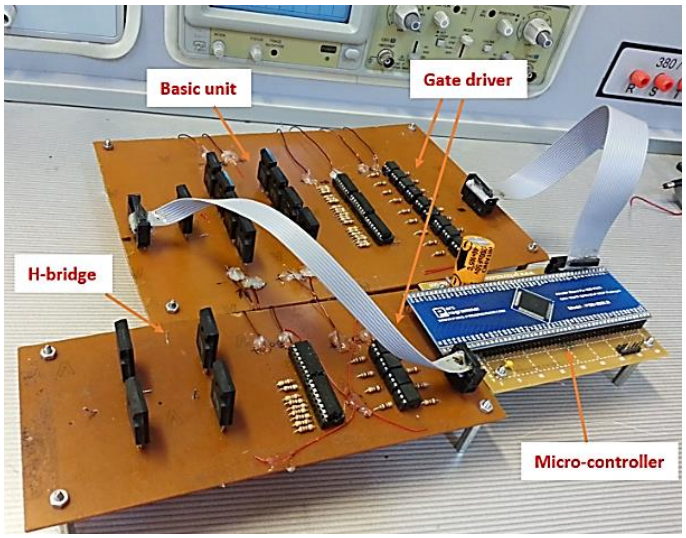
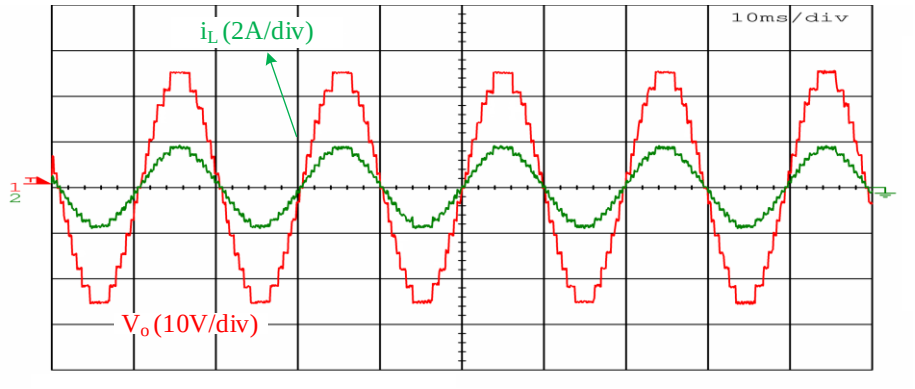
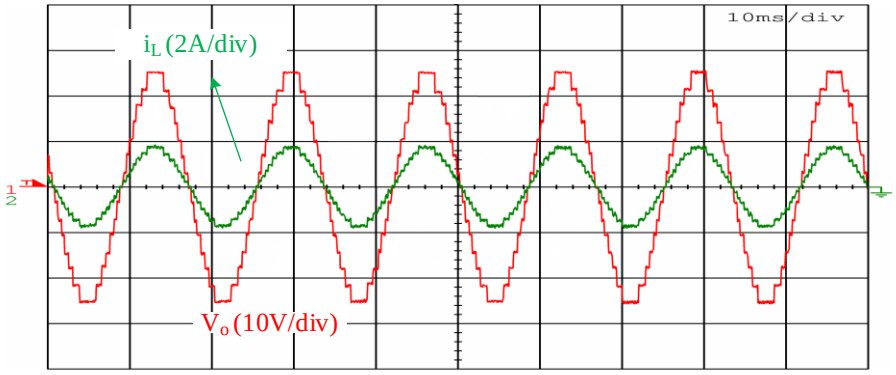


Figure 12. Prototype of proposed inverter

To verify the functionality of the proposed 15-level inverter, presentation of output waveforms at different frequencies and loads as described in simulation part is necessary. Accordingly, the satisfactory behaviour of the proposed inverter supplying a pure resistive load (R_1=15 Ω) at 50 and 60 Hz frequencies are presented in Figure 13. Notably, for more resolution, all the figures are presented in 0.01 sec (10 ms) per division. According to the results, experimental output waveforms match the simulated ones. However, due to the fact that the real elements have internal resistance, noticing slight differences between the simulation and experimental results is normal. Therefore, sufficient behaviour of the proposed inverter for both simulation and experimental results not only confirms the performance accuracy but also approves its functionality.



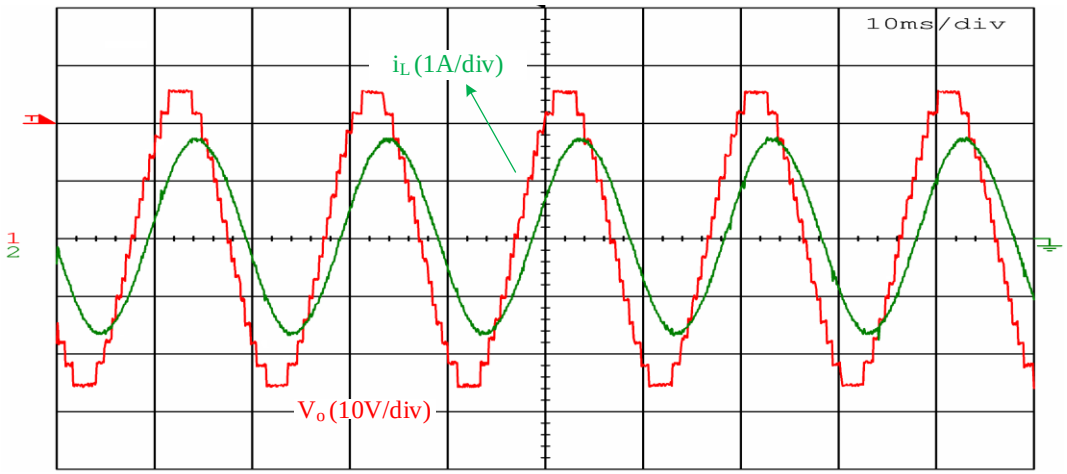
(a)



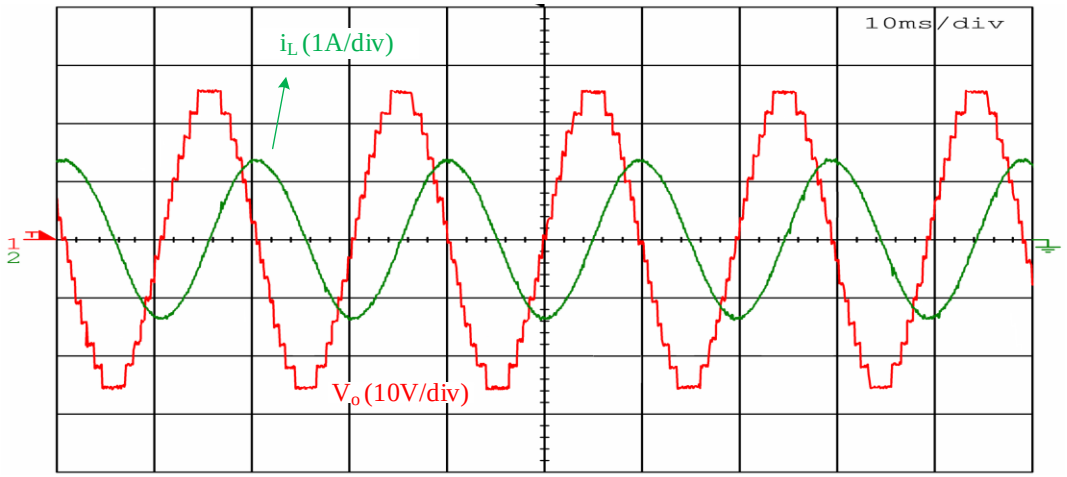
(b)

Figure 13. Experimental results of the proposed inverter supplying a resistive load at: (a) 50 Hz and (b) 60 Hz operating modes

Then, the output 15-level voltage and current waveforms at 50 Hz frequency for the resistive-inductive (R_2=13 Ω + L_2= 24 mH) and a pure inductive load (R_3=60 mH) with regard to the system parameters as described in simulation results section are presented in Figure 14. According to the results, the proposed inverter operates under different types of loads, sufficiently.



(a)



(b)

Figure 14. Experimental results of the inverter supplying a: (a) resistive- inductive load and (b) pure-inductive load

5. Conclusion

In this paper, a new topology formed by new basic units for cascaded multilevel inverters is proposed. Basic unit uses fewer power switches in its structure, compared with different similar structures to generate certain voltage levels. The use of fewer components will result in decreased cost, inverter volume and complexity that thorough technical analyses is reported in the paper. However, the detailed cost analysis is case sensitive (which depends on current and voltage ratio of the converter) and many other factors hence it is beyond scope of the paper and it can be considered as future studies. Moreover, four methods (P_1-P_4) are proposed to determine the

magnitudes of input voltage sources to enable the inverter to operate in both symmetric and asymmetric modes. Correspondingly, without increasing the circuit components, more voltage levels could be generated at the output. Then, one P_2 based unit, which is capable of generating 15-voltage levels by utilizing three input sources and eight power switches, is simulated and an experimental setup is developed. Its performance accuracy according to 5.47% THD and sufficient behaviour at both 50 and 60 Hz frequencies and under various loads is confirmed. As the input sources are isolated and can be replaced by capacitors or batteries, the proposed topology can be considered as a suitable choice for storage and renewable energy interfaces especially, grid-connected large-scale PV cells. Each array of cells could be an input source and as they may have different output voltages, implementing P_1-P_4 is applicable as a part of the solution.

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