Tampereen yliopisto

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MICROCHIP TEST ENVIRONMENT

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ABSTRACT

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With the ever-increasing demand for more powerful chips, it is necessary to integrate multiple circuits inside a chip. These chips are called a system on a chip (SoC). Even though SoCs integrate more and more functionality inside a single chip they still require a printed circuit board which at least provides power and input and output connectors.

Tampere University together with multiple companies started SoC Hub project. The goal of this project is to develop a system on a chip and increase Finnish system on a chip design expertise. The target is to develop one system on a chip in a year with three SoCs in total. The goal of this master's thesis is to design a printed circuit board that can be used to test the first iteration of the SoC.

Printed circuit boards which are designed for testing have three main functions: provide power, provide input and output connectors and their circuitry, and to make testing as easy as possible. This system on a chip requires three different power rails, which must be turned on and off in a sequence and they must also be monitored in case of a fault. For this purpose, a power management system was developed in which a microcontroller monitors and controls the power rails. On the printed circuit board most of the input and output connectors use pin headers. The pin headers make testing easy as most signals are available in simple pin headers. Some signals also have more specialized connectors such as an SD card socket. Testability was also a major concern when deciding the stack up of the printed circuit board. All signals are routed on the outer layers so that they are easily available and can be slightly modified if needed.

Some difficulties were also faced during the design process of the printed circuit board. Of these the biggest was the global chip shortage, because of which most of the chips that could have been used were not available. Due to chip shortage most of the chips had to be changed during the design phase and some chips had to be replaced by alternative means like using ready-made modules. Despite these problems the printed circuit boards were designed and manufactured before the SoCs arrived. The printed circuit boards were tested to be functional after which they could be used for their intended purpose of testing the SoCs.

Keywords: PCB, printed circuit board, SoC

TIIVISTELMÄ

Roope Keskinen: Testiympäristön suunnittelu mikropiirille
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Kasvavien tehovaatimusten takia entistä enemmän useita eri piirejä integroidaan yhdelle mikropiirille. Näitä mikropiirejä kutsutaan järjestelmäpiireiksi. Vaikka järjestelmäpiirit integroivat koko ajan enemmän toimintoja sisäänsä, tarvitsevat ne silti piirilevyn, muun muassa käyttöjännitteitä ja liitäntöjä varten.

Tampereen yliopisto yhteistyössä usean yrityksen kanssa aloitti SoC Hub -projektin. Projektin tarkoituksena on kehittää uusi järjestelmäpiiri ja samalla kehittää järjestelmäpiirien suunnitteluosaamista Suomessa. Tavoitteena on kehittää kolme järjestelmäpiiriä yksi piiri vuodessa. Tämän diplomityön tavoitteena on suunnitella piirilevy, joka mahdollistaa ensimmäisen järjestelmäpiirin testaamisen.

Testaamista varten suunnitellulla piirilevyllä on kolme päätehtävää: tuottaa käyttöjännitteet, tarjota liittimet ja niiden oheispiirit ja tehdä testaaminen mahdollisimman helpoksi. Järjestelmäpiiri tarvitsee kolmet käyttöjännitteet, jotka on käynnistettävä ja sammutettava tietyssä järjestyksessä ja niitä on tarkkailtava. Tätä varten kehitettiin käyttöjännitteiden hallintajärjestelmä, jossa mikrokontrolleri tarkkailee ja ohjaa käyttöjännitteitä. Piirilevyllä suurin osa liitännöistä on tehty käyttäen piikkirimoja. Tämä mahdollistaa helpon testaamisen, sillä lähes kaikki signaalit ovat saatavilla piikkirimoista. Osalla signaaleista kuten SD-kortilla on erikoisempi liitin niiden käyttökohteista riippuen. Helppo testattavuus on otettu huomioon myös piirilevyn rakenteessa. Kaikki signaalit kulkevat piirilevyn uloimmissa kerroksissa, jotta ne ovat tarvittaessa helposti saatavissa ja niihin on mahdollista tehdä pieniä muutoksia.

Työn aikana kohdattiin myös ongelmia. Näistä suurin oli globaali piiripula, jonka takia piirejä, joita olisi voinut käyttää piirilevyllä ei ollut saatavilla. Tämä johti siihen, että osa piireistä jouduttiin vaihtamaan useamman kerran suunnitteluvaiheen aikana ja joidenkin piirien kanssa tarvitsi hyödyntää vaihtoehtoisia tapoja kuten valmiiden moduulien käyttöä. Ongelmista huolimatta piirilevyt saatiin suunniteltua ja valmistettua ennen järjestelmäpiirien saapumista. Testaamisen jälkeen piirilevyt todettiin toimiviksi. Tämän jälkeen piirilevyjä voitiin käyttää niiden tarkoitukseen eli mahdollistamaan järjestelmäpiirin testaaminen.

Avainsanat: PCB, piirilevy, SoC

FOREWORDS

This thesis was written as a part of the SoC HUB project for Tampere University. I would like to thank Professor Karri Palovuori for offering the subject of this thesis for me and helping to guide me through it.

For me this thesis provided a good starting point for high-speed PCB design. This was an excellent opportunity to learn about transmission lines and other high-speed PCB design philosophies which were all new to me. In addition to PCB design, this project was a good opportunity to learn about ASIC and electronics component package design.

In addition, I would like to thank other teachers from Tampere University from whom I had the pleasure to learn from. And most importantly, I want to thank my family and friends for being a great support throughout my studies.

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Roope Keskinen

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ABBREVIATIONS AND MARKINGS

5G	Fifth generation technology standard for broadband cellular networks
AC	Alternating current
ADC	Analog-to-Digital converter
AI	Artificial intelligence
ANSI/VITA	VMEbus International Trade Association
AXI	Advanced eXtensible Interface bus protocol
C2C	Chip-to-Chip connection interface
CAMIF	Camera interface
CDC	Communication device class
CMOS	Complementary metal-oxide semiconductor
COM	Communication port
CPGA	Ceramic pin grid array
CPU	Central processing unit
DC	Direct current
DFU	Device firmware upgrade
DFT	Design for Test
DMA	Direct memory access
EEPROM	Electronically erasable programmable read-only memory
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FMC	FPGA mezzanine card
FPGA	Field-programmable gate array
GPIO	General purpose input/output
HDMI	High-definition multimedia Interface
HID	Human interface class
HPC	High pin count
HPC	High performance computing subsystem
HSMC	High speed mezzanine card interface
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC sound
IC	Integrated circuit
I/O	Input/Output
JTAG	Joint Test Action Group
LDO	Low-dropout regulator
LED	Light emitting diode
LPC	Low pin count
MCU	Microcontroller unit
MOSFET	Metal-oxide-semiconductor field-effect transistor
MPC	Medium performance computing subsystem
NMOS	N-type metal-oxide-semiconductor
NVLDA	NVIDIA deep learning accelerator
OVP	Over voltage protection
PCB	Printed circuit board
PHY	Physical layer transceiver for Ethernet
PLL	Phase locked loop
PM	Power manager
PMBus	Power management bus
PMIC	Power management integrated circuit
PMOS	P-type metal-oxide-semiconductor
RGMII	Reduced gigabit media-independent interface
SD	Secure Digital

SDIO	Secure Digital input output
SMD	Surface mount device
SoC	System on a chip
SPI	Serial peripheral interface
SPIM	Serial peripheral interface master
SysCtrl	System control subsystem
TLP	Top level peripherals subsystem
TQFN	Thin quad flat no-leads package
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
UVP	Under voltage protection
VLIW	Very long instruction word
ZIF	Zero insertion force.

1. INTRODUCTION

Nowadays computational demand for devices is getting higher all the time while the devices themselves are even more space constrained. This has led to using specialized processors in addition to central processing units (CPU). These specialized processors are optimized to perform a single task very efficiently such as artificial intelligence (AI) accelerators or image decoders and encoders. Having multiple different specialized chips leads to better efficiency but they use more space. This is where a system on a chip (SoC) integrated circuits (IC) come in handy. They are chips that integrate most of the required components into a single chip. These components often are CPUs, memories, specialized processors, and other circuits. SoCs can be most easily found in applications that are small and require a lot of processing power such as smartphones.

Because of the highly integrated nature of SoCs their design needs a lot of expertise. To gain said expertise Tampere University launched SoC Hub project which is a joint effort between Tampere university and multiple partner companies to design new SoCs for 6G, artificial intelligence, imaging, and security applications. In addition, SoC Hub aims to collect key players and establish the first world class SoC ecosystem in Finland. This project will also strengthen SoC design competence in Europe.

SoC prototypes will be manufactured one chip a year. The goal is to increase the integration level of the SoCs overtime meaning external components will be integrated in to the SoC. This fast prototyping and testing are made possible by architecture templates. The first iteration of the SoC is called Ballast.

The goal of this Master's thesis is to design a printed circuit board (PCB) called Graniitti on which the Ballast can be mounted on and tested with. The Graniitti PCB must provide power, connectors for input/output (I/O) and rudimentary user interface using buttons and jumpers through which the functionality of the Ballast SoC and the Graniitti PCB can be configured.

2. OVERVIEW OF THE TEST ENVIRONMENT

The Graniitti PCB and an FPGA board together form a test environment which can be used to test the Ballast SoC. As mentioned, this thesis mainly focuses on the design of the Graniitti PCB and not on the Ballast SoC or the FPGA board.

The Graniitti PCB can be divided into three main parts: Ballast SoC and way to attach it to the Graniitti PCB, power management, and I/O. The I/O can still be divided into high and low speed I/O. The high speed I/O is used for a chip-to-chip connection, and it requires different PCB design methods than the lower speed I/O which is used for the other I/O.

2.1 Ballast SoC

The SoC consists of eight different parts. High-performance computing (HPC) sub-system, medium performance computing (MPC) sub-system, System control (SysCtrl) sub-system, top level peripherals (TLP) sub-system, chip-to-chip (C2C) sub-system, AI accelerator sub-system, Ethernet sub-system and digital signal processor (DSP) co-processor sub-system.

HPC is a general-purpose Linux capable multiprocessor subsystem. HPC will heavily rely on external memory attached via C2C. MPC is a general-purpose processor sub-system with peripheral I/O. SysCtrl is a lightweight CPU sub-system responsible for initializing and booting up other systems on the SoC. TLP houses some peripherals which are shared by all cores. C2C is used to connect external chips to the SoC. C2C is shown in better detail in the next Chapter 2.2. AI accelerator is used to accelerate AI applications and it is based on NVIDIA Deep Learning Accelerator (NVDLA). Ethernet sub-system provides 1 Gbit/s Ethernet connectivity trough RGMII interface so it will require an external physical layer (PHY). The last sub-system is the digital signal processing (DSP) which uses VLIW DSP core for pre/post processing tasks in small and energy-constrained scenarios.

The SoC uses a ceramic pin grid array (CPGA) package with 257 pins. This CPGA will be mounted to the test board with a zero-insertion force (ZIF) socket. This socket allows the package to be dropped in without any force and tightened with the use of a lever. This socket type eliminates the possibility of accidentally damaging the pins when trying to insert the SoC.

2.2 C2C and FPGA board

The C2C interface of the Ballast SoC is used as a bridge to connect two devices together over an Advanced eXtensible Interface (AXI). The bridging functions of the C2C convert the wide on-chip AXI signalling to more compact device-to-device interface. This greatly reduces the number of needed I/O making the C2C interface optimal for connecting two high-speed devices together but at the same time requiring fewer I/O pins than full AXI interface. C2C supports up to 1584 Mbit/s bandwidth. In this case C2C is used to connect an FPGA board to the Ballast SoC. The FPGA can be used to increase memory and number of I/O's or act as an accelerator.

From PCB design point of view the most important thing about C2C is the physical connector used for connecting the Graniitti PCB to the FPGA board. There are 36 signals in the C2C interface, and their clock speed is 200MHz so the selected connector should at least fulfil these requirements.

The first option for the connector is just a standard 2.54mm general purpose I/O (GPIO) pin header. This option would be easy to implement, and it should still handle 200MHz signals. Unfortunately, 2.54mm GPIO headers are rare on the high-end FPGA boards and they have been replaced with higher performance connectors.

One of those connectors is the Intel's HSMC connector (high-speed mezzanine card). HSMC is developed to standardize the way in which additional cards are connected to the host board. This connector is mainly used by Intel's FPGA boards. Connector has 172 pins of which 121 are for signals, 39 for power and 12 ground pins so there would be way more than enough pins. The signal pins are designed to operate up to 625 MHz. [1]

FPGA mezzanine card (FMC) is an ANSI/VITA (VMEbus International Trade Association) 57.1 standard. It defines a way to connect I/O modules to an FPGA. FMC is mainly used by Xilinx's FPGA boards, but some Intel based boards also use it. There are two different version sod the FMC available. LPC (low pin count) with 160 pins and HPC (high pin count) with 400 pins. Both of them use the same physical connector but the amount of pins populated is different. [2]

Other requirements for the FPGA-board apart from the connectors are:

- Modern FPGA. For example, Artix-7 or Spartan-7 FPGA
- DDR2/3/4 memory
- Gigabit Ethernet

There are many FPGA boards which fulfil before mentioned requirements, such as Spartan-7 SP701 FPGA Evaluation Kit, but in this case Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit from Xilinx was selected. It was selected because Tampere University already had few of those. The FPGA board uses Zynq UltraScale+ multiprocessor system on chip which has a quad core Arm Cortex-A53 processing system, dual core Arm Cortex-R5 real-time processor and an FPGA fabric [3]. The FPGA board also has on board DDR4 memory and a slot for additional DDR4 memory [3]. It also features a Gigabit Ethernet, and it uses FMC LPC connector for expansion. In addition to the requirement the FPGA-board has multiple other nice to have features such as Universal Serial Bus (USB) and High-Definition Multimedia Interface (HDMI).

2.3 Power management and I/O

Power management is used to fulfil the complex power requirements of SoC. Power management is responsible of sequencing power-ups and power-downs of the SoC and monitoring the power supplies in case of faults. The power management system on Graniitti PCB is made using discrete switch mode converters and linear regulators which are controlled and monitored using a microcontroller.

Most of the I/Os on the Graniitti uses pin headers as connectors because it is not known what will be attached to them it is best to use pin headers which allow attaching pretty much anything to them. Other connectors than pin headers are used for a Secure Digital (SD) card and a USB connector for USB to Joint Test Action Group (JTAG) chip.

3. PCB DESIGN FOR SIGNAL INTEGRITY

Signal integrity is the signal's ability to propagate without distortion. In other words, it is a measurement of a signal's quality in a PCB. A distortion occurs as fluctuations in the signal's voltage. Those fluctuations can cause the signal to be read incorrectly leading to unwanted behaviour. Signal integrity issues usually manifest themself at higher frequencies. High signal frequencies require fast rise and fall times which can lead to signal integrity issues. [4]

Signal integrity issues can be divided in to four different groups: electromagnetic interference (EMI), reflections inside a single net, crosstalk between multiple nets, and power system stability. Primary cause for all these problems is short rise and fall times of signals. [5] In high-speed digital systems it is not feasible to increase the rise time of signals so other measures are needed. The following chapters will show ways to combat the aforementioned different signal integrity issues.

3.1 Electromagnetic interference

In electronics a signal is made of varying voltage or current. When a signal is transmitted, there is a current flow between a transmitter and a receiver. Flowing current will cause a magnetic field, which's strength is proportional to the amount of current, around the trace it is flowing through. On the other hand, according to Faraday's law of induction changing magnetic field can induce current into traces or wires. This means than changing current in one trace can induce changing current into nearby traces. This is desirable for antennae but for many other designs it can cause problems. This means that designs that emit electromagnetic interference do not only cause problems for nearby designs but also are themselves susceptible to EMI.[5]

To reduce susceptibility to EMI it is important to understand how currents flow inside a PCB. Current flows from transmitter to receiver but also according to Kirchhoff's first law the same amount of current must flow back to the transmitter in a closed loop [5][6]. The path that a current flows from transmitter to receiver and back encloses an area known as loop area. The size of the loop area defines how susceptible signal is to EMI. Larger loop area being more susceptible. This means that EMI can be minimized by reducing the loop area which is achieved by having a signal and its return path as close to each other as possible. [5] On a PCB this can be achieved by having a signal and its return traces be on different layers on top of each other.

3.1.1 Current return path

Having a return path directly under signal trace is good for minimizing EMI but it would be laborious and hard to manually route each return path. Instead of routing each return signal a whole layer of a PCB can be dedicated as a reference plane which most commonly is a ground plane. For alternating current (AC) signals power planes can also be used as reference planes.

The path taken by the return current will depend on whether it is direct current (DC) or AC. DC signal will take the path of least resistance and use most of the reference plane. AC signals meaning any signal which changes its state will return through the path of least impedance. The route of the least impedance is directly under the signal trace so AC signals return current will follow the signal trace. This is because according to Faraday's law current will couple from one parallel conductor to other. According to Lenz's law this current will flow in the opposite direction to the signal reinforcing the return current. Since the currents reinforce each other, it means that less energy is needed to move the signal therefore the impedance must be lowest directly under the signal trace. [6] This means that when using a return plane with AC signals, which most signals are, the return current will automatically follow the signal trace which minimizes the loop area and susceptibility to EMI.

3.2 Signal reflections

Any signal will reflect back towards the driver from the receiver or from any other point where it encounters an impedance discontinuity. Reflected signals can also reflect again from the driver leading to a situation in which a signal will reflect multiple times before attenuating if there is little or no loss on the signals path. Reflections will happen even if the receiver end is open or shorted. The reflected signal will superimpose on the transmitted signal and cause over- or undershoots, which is called ringing. Ringing means that the voltage of the signals is out of control which can cause erroneous logic states, false triggering or even cause damage to connected devices in the worst case. [6][7]

Reflection coefficient, ρ, can be used to determine the polarity and magnitude of the reflected signal. For transmission lines, which are shown in the following chapters, the reflection from the receiver end will depend on the load resistors value. Formula for the reflection coefficient ρ is

$$\rho = \frac{R_L - Z_0}{R_L + Z_0} \quad (1)$$

where R_L is the resistance of the load resistor near receiver and Z_0 is the characteristic impedance of the line.

The reflections coefficient can have values between -1 and +1 where sign will determine the polarity of the reflection and the absolute value determines the magnitude. If the coefficient is 1, it means that the signal is fully reflected with the same magnitude and polarity as with the original signal. [6][8] Reflections do not happen when reflection coefficient is zero and that is only possible when the signal path has a constant impedance throughout, and it is terminated with a resistor that equivalent to the line's impedance.

3.2.1 PCB transmission lines

To control reflections, signal traces can be designed to be transmission lines. Transmission lines are traces that have uniform impedance along their whole length, and they are terminated with their characteristic impedance. This is a special case in which there will be no reflections from the receiver to the driver. [6][8]

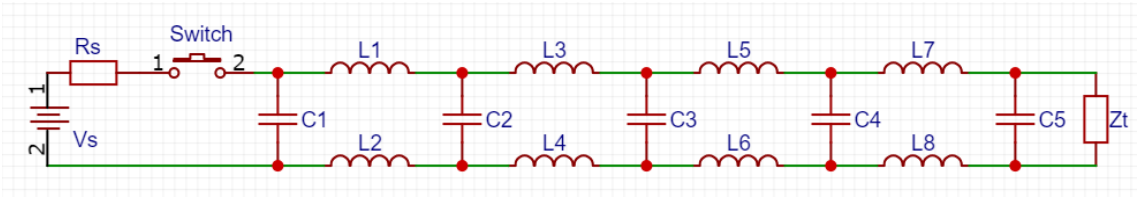


Figure 1. *Lumped-element model of transmission line*

The schematic of an ideal transmission line is shown in the Figure 1 as series of lumped capacitors (*C*) and inductors (*L*). In this lumped-element model it is assumed the resistance is negligibly small and the line is of infinite length. This results into evenly distributed inductance along its length and evenly distributed capacitance between lines. [6][7]

When a signal pulse is transmitted through the transmission line it will first start charging C_1 through source resistance. At first C_1 acts as a short circuit and current only flows through it back to the source. Charging current is limited by source's resistance R_s and is $I = V_s/R_s$. When C_1 charges, it does not act as a short circuit and current starts flowing through L_1. Instantaneous impedance for charging capacitor is $Z_c = V_{line}/I$. Since each inductor pair is mutually coupled, L_1 induces return current in L_2. These currents in turn start charging capacitor C_2. When C_1 is fully charged to voltage $V_{line} = V_s - R_s I$, no current flows through it and it's instantaneous impedance becomes infinite so the impedances for the capacitors are $Z_{c1} = \infty$ and $Z_{c2} = V_{line}/I$. As the signal propagates

trough the transmission line the capacitor being charged will have impedance of $Z_c = V_{line}/I$, charged capacitors have infinite capacitance and the impedance further down the line is unknown. So, from the signal sources point of view the impedance is constant through the whole transmission line. [7]

The characteristic impedance Z_0 of the whole transmission line is

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{2}$$

in which L_0 is the intrinsic inductance and C_0 is the intrinsic capacitance of the line.

Characteristic impedance of a line has no phase sift meaning that it is fully resistive. This allows a resistor to terminate the line. When a transmission line is terminated with a resistor equal to its characteristic impedance the resistor will absorb the energy of a transmitted signal by turning it to heat thus removing any reflections from receiver end.

3.2.2 Transmission line terminations

There are five typical options for terminating a transmission line: parallel, series, AC, Thevenin and diode. Of those termination options parallel and series are the most commonly used and will be explained below. [6]

In parallel termination a resistor which resistance is equal to transmission lines characteristic impedance is placed between signal trace and return trace at the end of the line. This resistor absorbs all of the signal's energy eliminating reflections. Parallel termination is effective and simple as it only requires one resistor in a simple location. Its only downside is that the resistor will continuously dissipate power which can become a problem if there are multiple terminations. [6][8]

Series termination on the other hand is placed in the beginning of the signal line in series with the line and receiver end is left unterminated. The resistor is chosen so that the sum of the driver's impedance and resistor resistance equal to the transmission lines characteristic impedance. With series termination there will be full reflection from receiver to driver, but the resistor will absorb the reflected energy eliminating further reflections. Series terminations advantage is the lack of continuous power dissipation and the need of a single component as in parallel termination. Downside of the series termination is the reflection from receiver to driver and drivers output impedance can be different for different logic states so it can be impossible to perfectly match the impedance. Still the series termination is often good enough.[6][8]

3.2.3 Transmission line impedance

There are two common ways of building a controlled impedance line in a PCB: microstrip and stripline tracking. In microstrip tracking signals are routed on the outer layers of the PCB and in stripline signals are routed on the internal layers of the PCB. Stripline tracking can achieve better signal integrity since the traces are shielded on the inside of the PCB but that makes the PCB design a bit more complicated and the traces can't be probed. For that reason, microstrip tracking was selected for the Graniitti PCB and why only equations for microstrip tracking are presented in this chapter.

In microstrip tracking signal layers are on the outside layers and power planes are on the internal or outer layers depending on layer count. In two-layer PCBs the signals are on one layer and ground plane is on the other layer. In multilayer PCBs the outer layers are used for signals and inner layers for power planes. Figure 2 shows the structure of a two-layer PCB with microstrip tracking.

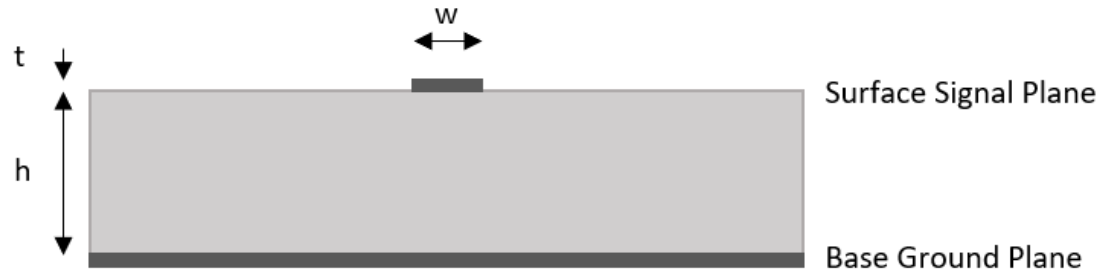


Figure 2. *Microstrip tracking*

Characteristic impedance Z_0 for double or multilayer PCBs with single ground layer can be calculated using (3)

$$Z_0 = \frac{\mathrm{k}}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \tag{3}$$

where k is 87, ε_r is the relative dielectric of the substrate, w is the track width and t is the thickness of the copper trace and h is the height of the PCB substrate between the trace and ground layer. Restrictions for this formula are that relative dielectric of the substrate must be $1 < \varepsilon_r < 15$ and trace width in relation to substrate height must be $0.1 < \frac{w}{h} < 3.0$. [7][8]

More often though, the target characteristic impedance of a trace is known, but the required trace width for that impedance is not known. Trace width w for a given characteristic impedance can be calculated using (4) which was acquired by solving (3) for trace width.

$$w = 7.475h \times e^{(-Z_0\sqrt{\varepsilon_r+1.41})/k} - 1.25t \quad (4)$$

Same restrictions apply for (4) as for (3).

It is clear from the previous equations that a designing a controlled impedance line depends more on geometry than electronics. Track width is the easiest variable to change since a PCB designer will have full control over it. Other variables like laminates dielectric and distances between traces will depend on the used materials and PCB stackup allowing only partial control at best cases.

The previous equations can be used to get a rough idea of the PCBs trace impedances while ignoring multiple variables like solder masks, nearby traces, and varying materials inside the PCB like prepregs and laminates. To get precise results simulation tools or standalone impedance calculators from reliable manufactures can be used. [6] PCB manufactures often offer controlled impedance PCBs in which they can adjust the design to get the most precise impedance control.

3.2.4 Electrically long traces and critical length

In short traces reflections do not cause signal integrity issues, since when the signal is reflected back to the driver, the driver is still driving as signal causing the reflection to be overwhelmed by the driver [6]. In longer traces the propagation time of signal can be too long compared to the rise time of signal which causes reflections and signal integrity issues. When propagation time is too long compared to the rise time, the trace is considered electrically long and must be treated as a transmission line [7]. This means that the line must have controlled impedance over its length and proper termination [7].

Propagation speed of a signal is too long compared to the rise time when propagation time of the signal is longer than one-half of the signals rise time [7]. This means that the trace should be shorter than half of the length that the signal travels in its rise time. This length is called critical length. If length of a trace is longer than signals critical length, then the trace should be treated as a transmission line. Critical length l_c for a signal can be calculated with (7)

$$l_c = \frac{vt_r}{2} \quad (7)$$

where v is the propagation speed of the signal and t_r is the rise time of the signal.

Speed v of an electrical signal in PCB can be calculated using (8)

$$v = \frac{c}{\sqrt{\varepsilon_r}} \quad (8)$$

in which c is the speed of light in vacuum and ε_r is the relative permittivity of the material between signal and return plane. [9] The effective relative permittivity will depend on the used PCB material.

3.3 Crosstalk

Chapter 3.1 was about how traces can be designed so that the amount of electromagnetic interference radiated and susceptibility to it can be minimized. This chapter is about how adjacent traces can couple to each other causing interference. This interference caused by adjacent traces is called crosstalk.

With two adjacent traces current flow in one of them will couple into the other. The trace that causes the interference is called an aggressor and the other trace is called a victim. The current can couple from the aggressor to the victim through two different means known as inductive and capacitive coupling. The coupled current in the victim trace will cause two different noise signals. One of those signals will flow in the same direction as the signal in the aggressor trace known as forward crosstalk and the other noise signal will flow in the opposite direction known as backward crosstalk. [5]

Flowing current in the aggressor trace is made of electrons. These electrons repel other electrons in nearby traces. The repelled electrons will move away from the aggressor lines electrons in both ways along the victim trace. Since the victim traces electrons move to both ways there will be forward and backward crosstalk caused by this reaction known as capacitive coupling. [5]

Flowing current in the aggressor trace will also cause a magnetic field around the trace. When the magnetic field intersects with the victim line it induces a current into the victim trace which flows in the opposite directions as the current in the aggressor trace. This type of coupling is known as inductive coupling, and it only causes backward crosstalk. [5]

3.3.1 Forward and backward crosstalk

Forward and backward crosstalk travel in opposite directions but that is not their only difference. With backwards crosstalk a moving signal in the aggressor trace pushes charged elements backwards in the victim trace. As the aggressor signal propagates it keeps on pushing more victim elements backwards. This ends as a string of victim elements moving backwards whose length is twice the coupled length of the traces. It is important to note that the length of the crosstalk pulse is measured in time and not in

distance. This means that the width of the crosstalk pulse is twice the propagation time of a signal in the coupled region. Magnitude of the backwards crosstalk pulse is somewhat determined by the length of the coupled region. The longer the coupled region, the higher the magnitude of the crosstalk pulse is to a certain degree. With longer coupled regions the magnitude of the crosstalk pulse starts to level off before reaching a maximum value. Maximum magnitude of the crosstalk pulse is reached when the coupled region is equal in length to the critical length mentioned in Chapter 3.2.4. This means that maximum magnitude is reached when the coupled regions length is equal to one half of the rise time of the aggressor signal. [5]

With forward crosstalk the signal in the aggressor trace causes charged elements of the victim line to be pushed forward. These elements get grouped up and this is what causes forward crosstalk. With forward crosstalk the magnitude of the crosstalk pulse keeps increasing with the length of the coupled region without any limit that is likely to be achievable on a PCB. Width of the forward crosstalk pulse is at maximum equal to the rise time of the aggressor signal. In practice though forward crosstalk is not usually significant as it is known to be very small in microstrip environments and almost non-existent in stripline environments. [5]

3.3.2 Crosstalk mitigation

Calculating the amount of crosstalk can be very hard and accurate results require the use of simulation software. Level of the coupling can be estimated between two traces on top of a reference layer with (9). Level of the coupling never exceeds the value given by (9) [5]

$$\frac{1}{1+\left(\frac{D}{H}\right)^2} \; or \; \frac{H^2}{H^2+D^2} \tag{9}$$

where H is the distance between a trace and reference plane, and H is the distance between the two traces [5].

From equation (9) it is clear that the degree of coupling degreases when the distance between the two traces increases or the distance from trace to reference plane degreases. This means that a PCB stackup that places traces as close to reference plane should be used and distancing traces from each other helps at reducing crosstalk.

In typical case the traces are one trace width apart from each other. The spacing works for typical traces but not for traces which are susceptible to crosstalk. These traces should be kept two trace widths apart from each other. This is known as 3*w* rule since

the distance from traces middle to other traces middle is three times the width of a trace. With 3*w* rule the transmission line traces are out of reach for 70% of each other's magnetic fields. [7]

As mentioned in the previous chapter, backwards crosstalk reaches its maximum amplitude if the coupled region is longer or as long as the critical length of a signal. This means that the crosstalk can be mitigated by keeping traces as short as possible or by reducing the rise time of the signal being transmitted.

Finally, traces can be terminated at far end of the victim trace with the victim traces characteristic impedance. Using terminations backwards crosstalk pulses can be fully absorbed so that they do not reflect forward [5]. Using terminations can difficult as it can be hard to calculate the correct value for the termination resistor and incorrect placement of the resistor can have negative consequences for the circuit's operation [5]. For this reason, the best and the simplest way to mitigate crosstalk is to minimize distance from the trace to the reference plane and maximize the distance between the traces.

3.4 Power systems and decoupling

There are two common ways to connect power and ground: series and parallel. In series connection multiple branches share the same common path. In parallel connection on the other hand, the currents are supplied through sperate paths. From schematic point of view, they are identical but in practice they are different since zero resistance conductors exist only in theory. In practise there will be a voltage drop over the shared conductors which means that the different branches will have different voltage over them. Series connection would be easier to route since it requires fewer traces, but the common paths can be problematic at higher frequencies. That means that parallel connection is often preferred over serial, but it can be more difficult to route since there are more paths to be routed. [7]

Aforementioned problem of parallel connection can be solved by dedicating a whole layer of a PCB as a ground plane. As mentioned in Chapter 3 signals current returns through the path of least impedance which is under the signal trace. This would require making current return paths under each signal which would be complicated and laborious. By dedicating a layer as a full ground plane directly under the signal layer all signals will have their optimal return path done automatically.

In addition to ground planes, also a power plane is usually added to PCB designs. In power planes there are one or more power rails which are made as wide as possible.

This minimises the inductance and maximises the capacitance between power and ground traces which is desired for power distribution system. [7]

If even smaller noise is required, power and ground planes can be split. This can be done by separating noise generating components from noise sensitive components and eliminating common return paths by splitting power and ground planes into separate areas. Components should be separated so that analog and digital components are not mixed, and noisiest components should be closest to connectors and least noisy should be farthest away. Plane splitting can be done by creating a moat around a copper area so that it is connected to common areas only from one point. This prevents noises from spreading through the mote to more sensitive areas. Moating can be used around clock generators for example. In addition to moating, splitting can be done by using multiple layers of a PCB as isolated continuous planes. [7]

If the ground plane is split, care must be taken not to route signals over the split area. If a signal trace is routed over those unrelated planes, the return current cannot follow directly under the signal trace. This leads to larger loop area and susceptibility to EMI. For this reason, it is vital to route all high-speed signals over solid reference planes. [5]

3.4.1 Bypass capacitors

Though power and ground planes are great for reducing noise they are not immune to it. One such type of a noise is switching noise caused by high-speed digital systems. Switching noise happens when digital system’s gates switch from one state to another. In Complementary metal-oxide semiconductor (CMOS) technology when the gates switches state it draws a significant amount of current for a brief moment. Depending on if the gate turns on or off it can lead either to voltage drop in power rail or to voltage increase in ground plane. These voltage changes are known as rail collapse and ground bounce. Switching noise can cause problems with digital systems but more importantly it can be detrimental to analog systems which usually require a low-noise environment. [7]

Switching noise can be mitigated by using a bypass capacitors. Bypass capacitors are small capacitors which promote stable power distribution by acting as local power storages for fast switching gates and act as lowpass filters by shorting power supply noise. [7] There are two different approaches for bypass capacitor decoupling: traditional approach and power system impedance approach.

3.4.2 Traditional bypass capacitor approach

In traditional approach bypass capacitors are viewed as local fast charge storages. Fast changing gates of an IC can source their required charge quickly from nearby capacitors instead of the required charge having to transition from the power supply which is further away. Since the required charge is available nearby, there won't be any ground bounce. Larger the bypass capacitor is the more charge it can supply but larger capacitors have large internal inductance which limits the rate at which it can supply said charge. On the other hand, smaller capacitors can supply their charge more quickly thanks to the smaller internal inductance which is required by the fast-switching gates inside ICs. However, smaller capacitors can't store as much charge as larger capacitors. If even faster capacitors are required, planar capacitance can be designed in the PCB. [5]

To achieve the best possible decoupling performance multiple different sizes of bypass capacitors should be used. Larger 100 nF capacitors are usually used for bulk charge and smaller 10 nF to 1 nF capacitors for fast response. When multiple bypass capacitors are used for a single power pin, the smaller capacitors should be placed closest to the power pin since they will be the first of the capacitors to provide charge. With CMOS devices the bypass capacitors should also be equal distance from power and ground pin for optimal performance. [5]

To conclude, according to the traditional approach at least two different sizes of bypass capacitors should be used. One smaller size for quick response and a larger one for bulk storage. Capacitors should also have low internal inductance. Finally, the smallest capacitor should be placed closest to the power pins. [5]

3.4.3 Power system impedance approach

Unlike traditional bypass capacitor approach which focuses on individual ICs, power system approach focuses on creating an impedance curve for the whole power system which is high for DC component and low for all other frequencies. Since the traditional approach focuses on individual ICs, it can lead to unnecessary large number of capacitors used while power system approach attempts to optimize the whole power system so that there is no need to individually decouple each IC. [5]

As previously mentioned, the goal of the power system impedance approach is to achieve ideally infinite impedance for DC and low impedance for other frequencies. Impedance of an ideal capacitor can be calculated with (10)

$$Z = \frac{1}{2\pi fC} \tag{10}$$

where f is the frequency of the signal and C is the capacitors capacitance [5].

It is clear from the equation that as the frequency of the signal increases the impedance of the capacitor decreases which is desired. Unfortunately, real capacitors have internal inductance which affects the capacitors impedance. Impedance of a real capacitor can be calculated using (11)

$$Z = \left|2\pi fL - \frac{1}{2\pi fC}\right| \tag{11}$$

where f is the frequency of the signal and C is the capacitors capacitance, and L is the inductance of the internal inductor [5]. From this equation it is clear that as the frequency of a signal increases the impedance of the capacitor goes down to a minimum at which point the impedance of the internal inductor starts to dominate and the impedance of the whole capacitor starts to increase again. Frequency response of an ideal and real bypass capacitor is visualized in Figure 3.

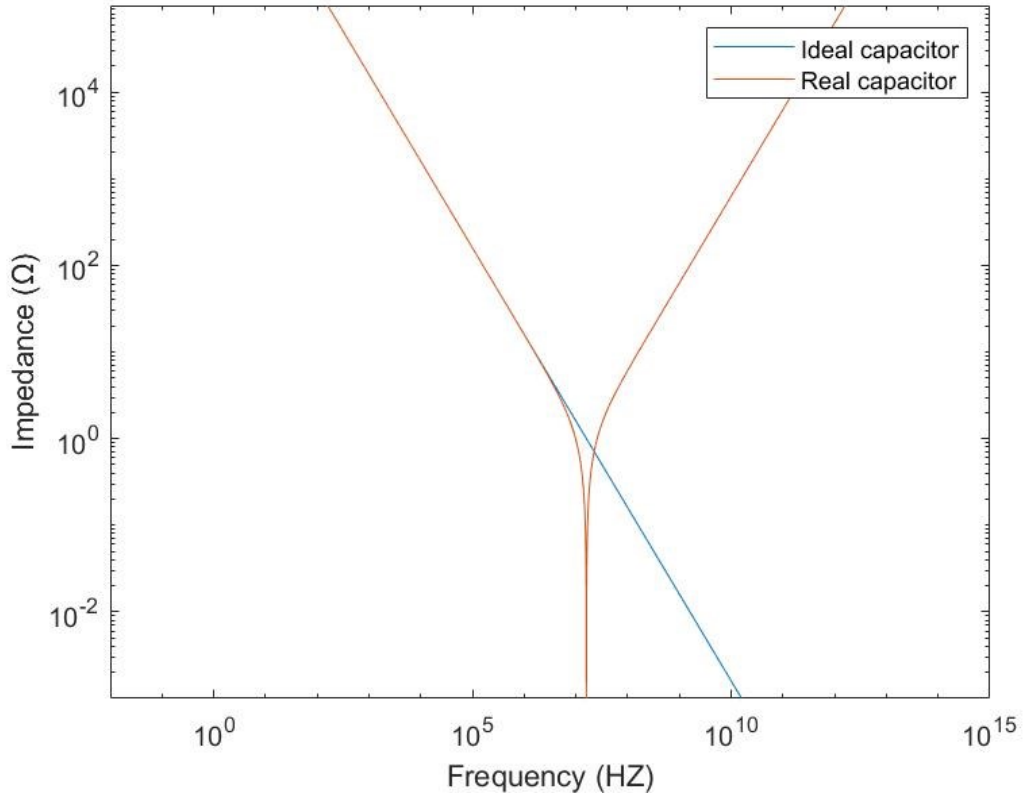


Figure 3. *Frequency response of an ideal and real bypass capacitor. Both capacitors have capacitance of 10nF and the real capacitor has 10nH inductance.*

The minimum point of impedance is called self-resonant frequency at which the impedance of the capacitors internal LC circuit is zero [5]. The self-resonant frequency can be calculated with (12)

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

where L is the capacitors internal inductance and C is the capacitance.

It is clear from Figure 3 that a single bypass capacitor is not enough to provide low impedance at wide range of frequencies. This can be made better by adding multiple identical capacitors in parallel. Parallel connection of capacitors increases their capacitance and decreases inductance. [6] Frequency curve of multiple identical capacitors versus inductance of a single similar capacitor is shown in Figure 4.

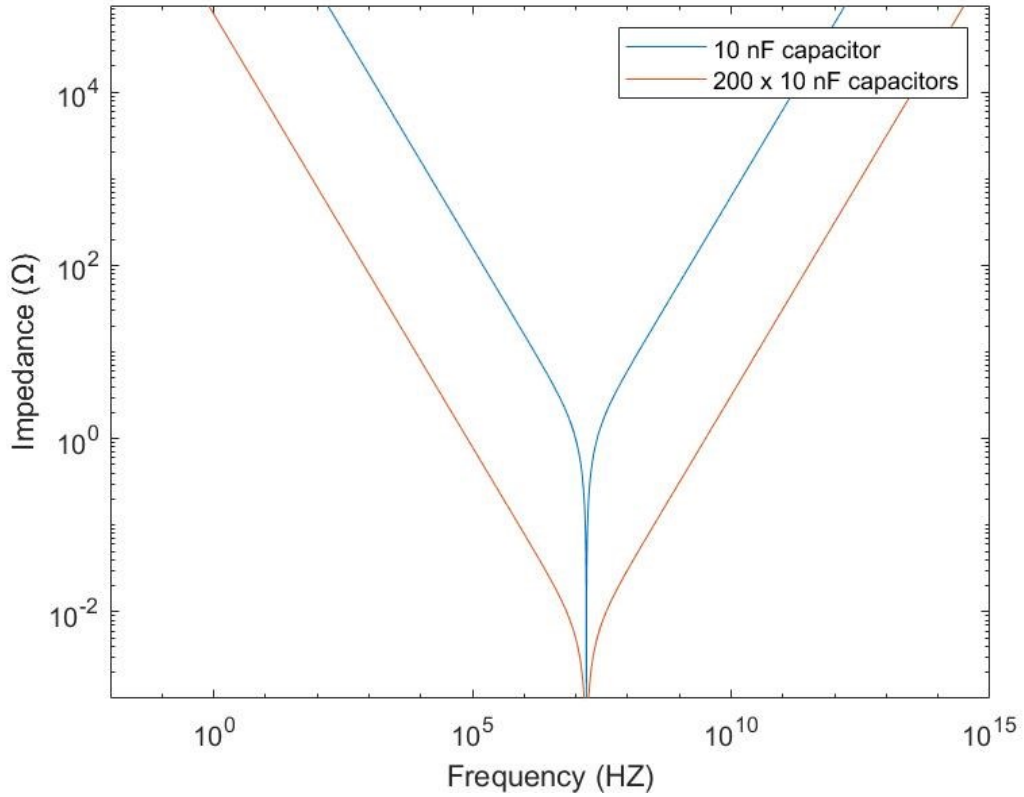


Figure 4. *Frequency response of single 10nF, 10nH capacitor versus frequency response of 200 10nF, 10nH capacitors in parallel.*

Parallel identical capacitors have the same self-resonant point as a single identical capacitor, but the impedance is lower for larger range of frequencies [5]. This is desired as the goal is to achieve low impedance over wide range of frequencies. Frequency response can be improved further by adding different values of capacitors. Different sized capacitors have different capacitance and inductance, so their self-resonant frequencies are also different. Figure 5 visualizes frequency response of the previous parallel capacitors and larger value capacitor's frequency response.

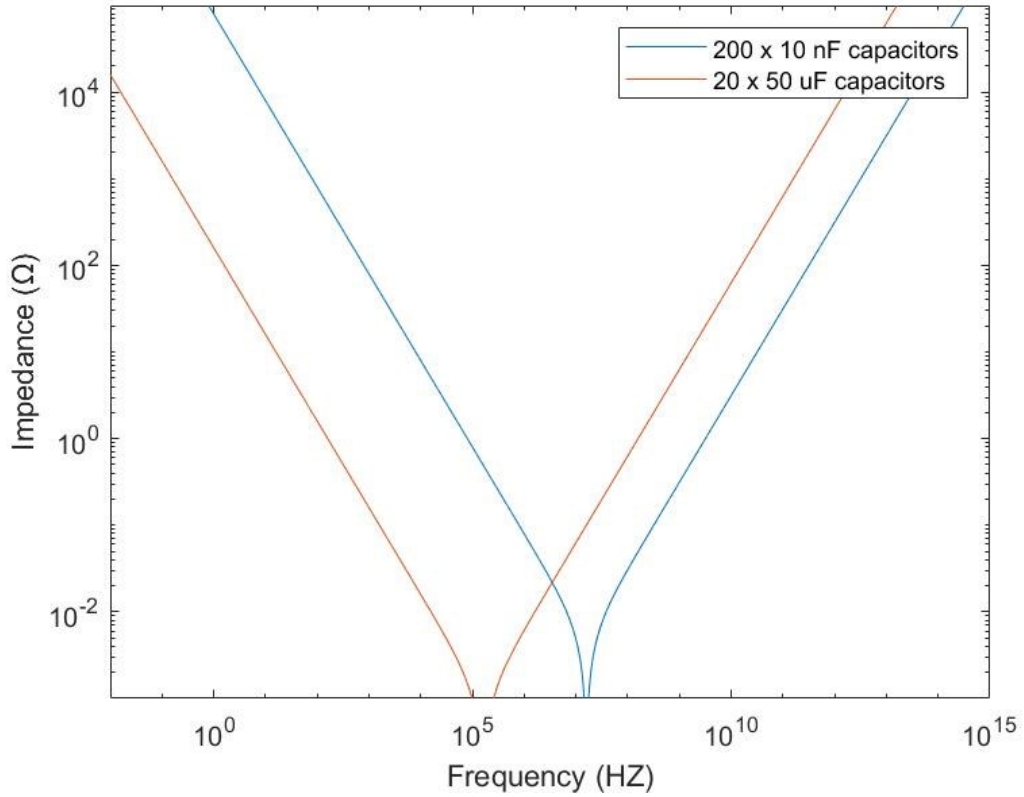


Figure 5. *Frequency response of 200 10nF, 10nH capacitors in parallel and 20 50 μF, 20nH capacitors in parallel*

Since the new capacitors are larger, their self-resonant frequency is lower and thus, they have smaller impedance at lower frequencies. With two different capacitor sizes the Frequency response is starting to be good for lower frequencies but is lacking for higher frequencies. This can be remedied by designing planar capacitance into the PCB. In planar capacitance power and ground planes are designed on top of each other very closely so that they form a capacitor [5]. Advantage of a planar capacitor is that they have very little inductance and can be assumed to have only capacitance [6]. Planar capacitance can be calculated using (13) which is the standard equation parallel-plate capacitors

$$C = \frac{\varepsilon_0 \varepsilon_r (n-1) A}{d} \tag{13}$$

where ε_0 is permittivity of free space, ε_r is relative permittivity of the PCB material, n is number of plates, A is the area of over lapping planes, and d is the distance between planes.

Let's assume that there is 950 pF of planar capacitance and add it to Figure 5. The new frequency-response curve is shown in Figure 6.

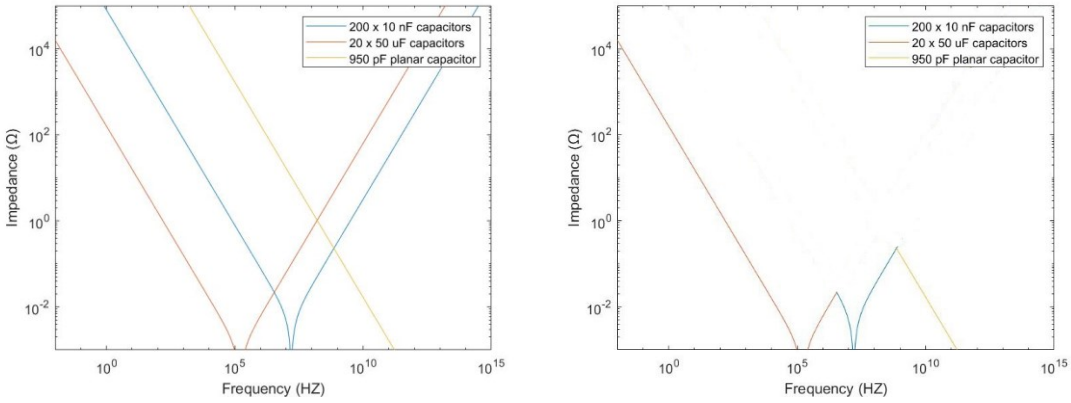


Figure 6. *Frequency response of 200 10nF, 10nH capacitors in parallel and 20 50 µF, 20nH capacitors in parallel and 950 pF planar capacitance. Left figure shows the impedance of each capacitor and right figure shows the combined impedance of all capacitors.*

Now the combination of two capacitor sizes and planar capacitance achieve a low impedance at higher frequencies and high impedance for low frequencies as was the goal. The frequency curve in Figure 6 is not a perfect representation of reality as it is lacking spikes at the high points of the curve. These spikes have infinite impedance and are caused by LC circuit resonance. In reality though, capacitor also have equivalent series resistance (ESR) which limits highs and lows of the impedance curve. [5]

To conclude, according to power system impedance approach capacitors should be carefully selected so that a wide range of self-resonant frequencies can be achieved. Planar capacitance is needed for low impedance at high frequencies and moderate ESR is better than low ESR. Placement of capacitors is not important, but the electrons still need to travel to their target so it beneficial to place at least some capacitors near their target. [5]

3.5 PCB stackup and routing

Stackup is the arrangement of layers in a PCB. These layers can be made of copper for signal and power layers or made of insulating material in between the copper layers. PCB stackup must be defined in an early state of the design since it determines how many layers can be used and what they are used for. Selected stackup depends on multiple things such as circuit density, manufacturers capabilities and signals frequencies. With high-speed signals transmission lines are needed which in turn require a ground layer beneath them. [7] To have a dedicated ground layer usually requires designing a multilayer PCB.

In multilayer PCBs there are more than two layers and the layers are often divided by their usage to power planes or signal layers. Power planes are layers which are fully dedicated for ground or power. Signal layers are layers which are used to route signals. There are multiple different ways to select a stackup. With slow signals most stackups usually work but with higher speed signals stackup can have a major impact on the PCB's performance. Poorly designed stackup can cause reflections and electromagnetic interference. This chapter will focus on four-layer stackups as those are used in the Graniitti PCB.

There are three common four-layer stackups which are shown in Figure 7. In Figure 7 symbol "GND" means ground plane, "PWR" means power plane, "H" means signal layers with mostly horizontal traces and "V" means signal layer with mostly vertical traces. Separating the signal layers by routing direction makes routing more efficient for high-speed designs and reduces the number of vias needed [1]. Power layer can be made of a singular plane or of multiple different areas or wide traces depending on the number of power rails.

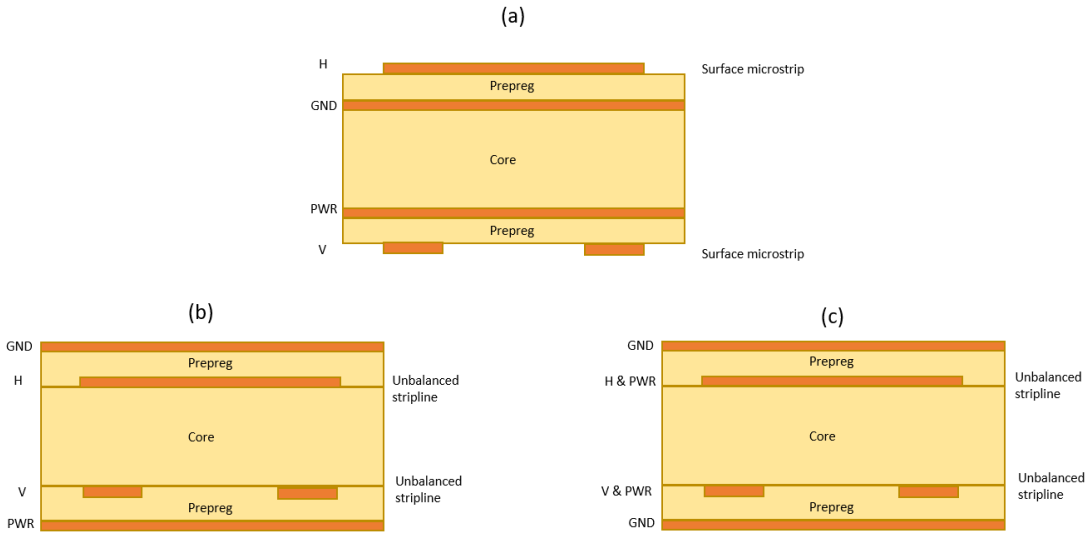


Figure 7. *Four-layer PCB stackup options.*

Figure 7a shows the most common stackup for four-layer designs. Outside layers are used for routing signals and the inner layers for ground and power plane. Having the signal layers on the outside allows easy post fabrication troubleshooting and inspections [7]. Top layer should be used to route all high-speed signals because it is closest to the ground plane and vias can be avoided since most components are usually mounted on the top layer.

Figures 7b and 7c on the other hand show stackups with power and ground planes on the outside. This design shields the inside traces from outside EMI and helps to contain any generated EMI [7]. These stackups are the best when low noise is desired, but post fabrication troubleshooting is much harder and especially with stackup option c there is less room to route signals.

3.5.1 Routing guidelines for signal integrity

As mentioned in previous chapters, the best way to achieve good signal integrity and low EMI is to have optimal return path for every signal. This can be achieved most easily by having a ground plane directly under every signal or at least under every high-speed signal.

It is also beneficial to minimize trace lengths between components by placing functionally similar components close to each other. If traces become longer than their critical length, they should be made to be transmission lines. This is done by designing the trace to have defined impedance through its whole length. Transmission lines should also be used when a signal on a PCB connects to something on the outside of the PCB that also features defined impedance traces.

In addition to previous guidelines, it is beneficial to separate noisy and noise sensitive components from each other. This can be achieved best by placing noisy components such as power converters nearest to connectors and most noise sensitive components such as analog circuits as far as possible from connectors. In this way the amount of common return plane is minimized. [7]

In Chapter 3.2.3 it was shown how to calculate the trace width for controlled impedance lines. For non-impedance-controlled lines such as slower signals and power rails trace width will depend on the amount of current the trace carries. The wider the trace the more current it can carry since it heats up less. The minimum trace width required for carrying a certain current can be calculated using (14).

$$w = \left(\frac{1}{1.4 \cdot h}\right) \cdot \left(\frac{1}{k \cdot \Delta T^{0.421}}\right)^{1.379} \tag{14}$$

Where w is the width of the trace in mils, h is the thickness of the copper in oz/ft^2, I is the current flowing through the trace, ΔT is the maximum allowed rise in temperature above ambient temperature, and k is 0.024 for inner layers and 0.048 for outer layers. [7] Since the trace width is given in mils it can be converted to millimetres by multiplying it with 0.0254mm.

3.5.2 Signal timing and Length matching

Speed of a signal in a PCB trace could be calculated with (8). When the signal speed is known, the propagation time of signal can be easily calculated when the length of the trace is known. This can be useful as some digital interfaces require some signals to be delayed by a certain amount.

More commonly though the time difference between the signals is much more important than the propagation time of a signal. In synchronous systems data signals must align exactly right with clock signal so that they are sampled correctly. If there is large time difference between the signals they might be in incorrect state when sampled or setup and hold times may be violated. Setup time is used to describe the time a signal must be stable for before it is sampled and hold time describes the time signals must be stable for after they are sampled. Violation of setup or hold time can lead to reading erroneous signal states.

From PCB design point of view signal timings can be affected by controlling trace length. Traces can’t be made shorter than the shortest distance between its start and end point, but it can always be longer since in most cases the total length is not important. By making each trace to be of equal length on a PCB it can be ensured that each of the signals reaches its target simultaneously. Matching the signals trace lengths between signals of a bus is called length matching. This can be done most easily with serpentine routing. PCB design tools can automatically adjust the length of a trace so that the designer does not have to manually draw the signal trace to be of certain length.

4. POWER MANAGEMENT

Modern high-performance ICs such as SoCs and FPGAs can require multiple different power rails for the different parts of the IC. The rails may differ in voltage levels or they can have the same voltage but different tolerances. All these power rails also require sequencing and protection from faults. [10]

That is where power managers (PM) come in handy. They are single ICs or a group of ICs which are responsible of the three different power supply cycles: sequence-up, monitoring and sequence-down. In sequence-up state the power supplies are powered up to correct voltages in predefined times. Monitoring state begins when the last power supply has reached its target voltage. In monitoring state, the power supplies are monitored for faults such as over- and undervoltage. In sequence down state, the power supplies are turned off in predefined order which often differs from sequence-up order. [10][11]

4.1 Power rail protection

Power management system must monitor the input voltage for a brownout and each power rail for undervoltage, overvoltage, overcurrent and short-circuit. When a fault is detected all power rails should be turned off. It is not enough to only turn off the faulty power rails as this can cause harmful voltage differences.

The following two chapters will explain different methods for monitoring power rails for undervoltage, overvoltage, overcurrent and short-circuit.

4.1.1 Overcurrent and short-circuit

Overcurrent is a situation in which more current flows than was intended. This can be caused by a short-circuit, underestimating current usage or by other faults. Excessive current can cause overheating which can damage affected components or cause a fire hazard. Short-circuit is a special case of overcurrent in which there is a low resistance path between the power rail and ground.

Current can be measured using a shunt resistor and measuring the voltage drop over it. When the value of the resistor is known, the current can be easily calculated using Ohm’s law. The shunt resistor’s value should be precise to allow accurate measurements and

small enough not to cause noticeable voltage drop over itself. Power converters can also have built-in overcurrent and short-circuit protection.

4.1.2 Overvoltage and undervoltage protection

Overvoltage protection (OVP) and undervoltage protection (UVP) are used to protect circuitry in case power rails voltage goes outside of its designated tolerances. Voltages outside of operating tolerances can cause unwanted behaviour or damage to chips through latch-up. OVP and UVP work by monitoring the voltage of a power rail and shutting it down quickly if it is outside of tolerances thus preventing damage. One cause for an overvoltage or undervoltage can be a malfunctioning power supply. Excess power drawn can also cause a undervoltage if power supply is incorrectly rated or overcurrent protection is not working correctly.

Many power converters have OVP and UVP functionality built in, but it may not be precise enough for microchips with tight tolerances. Precise and fast over- or undervoltage detection circuit can be built by using operational amplifier, voltage reference and resistors. This circuit is presented in Figure 8.

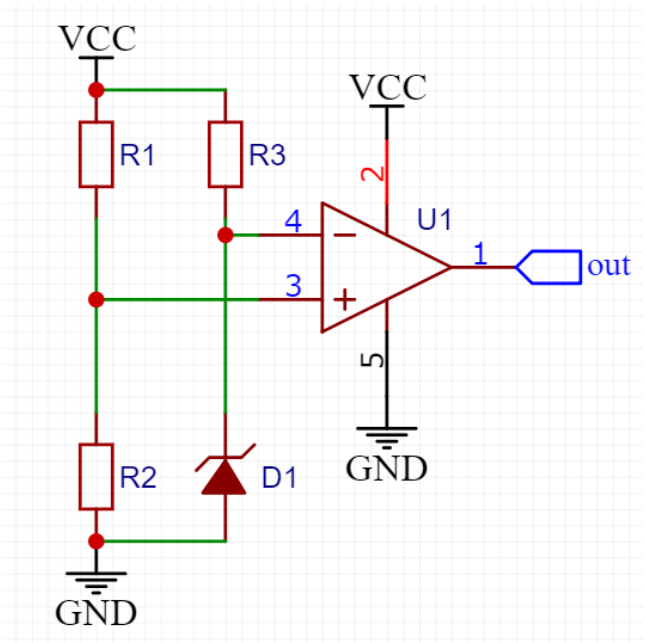


Figure 8. *over- or undervoltage detection using operational amplifier*

D1 Zener diode is used to make a reference voltage to which VCC divided by resistors R1 and R2 is compared. R1 and R2 are used to set the trigger point. In overvoltage detection trigger point is set so that in case of an overvoltage the voltage in non-inverting input of the operational amplifier will be higher than the reference voltage in the inverting

input. This will cause the output to go high when overvoltage is detected. Undervoltage can be detected by changing the reference to the non-inverting pin. In this case the output will go to zero when inverting input is higher and will go high when the voltage is lower than the reference voltage. Using operational amplifiers is precise and fast but will use a lot of space if there are multiple power rails since each rail will need two such circuits.

Another possibility for detecting over- and undervoltage is to use an analog to digital converter (ADC) if a microcontroller is used in the power management system. Since most microcontrollers have built-in ADCs, it will not increase the complexity of the circuit, but ADCs are not as fast or accurate as using operational amplifiers. Often it is not desirable for protection to activate for smallest faults, so with ADCs it is possible to easily set the minimum duration or magnitude for fault before actions are taken. ADCs can also be a bit inaccurate so usually they must be calibrated to achieve the best possible accuracy.

4.2 Power sequencing

Power supply sequencing means the way in which different power supplies are enabled or disabled in order. Power sequencing is used avoid latch-up which can cause permanent damage or more minor faults which can cause unwanted malfunctions. [10][13]

There are three common ways of multi-rail sequencing: sequential start-up, ratiometric start-up and simultaneous start-up. The first and the most common way is the sequential start-up in which power rails are turned on one after the other separated by a delay. The delay is long enough for the previous rail to reach regulation before the next rail is enabled. [12]

The second way is ratiometric start-up in which the power rails are turned on at the same time and they reach their regulation also at the same time. This requires precise control of the rise times of the rails since higher voltage rails must rise faster to reach regulation at the same time as lower voltage rails. [12]

The third option is simultaneous stat-up which minimises instantaneous voltage differences between different voltage domains. The power rails are enabled at the same time, and they have the same rise rate. This means that all voltages rise together, and lover voltage rails reach their target first and higher voltage rails keeps increasing until they reach their target. [12]

Shutdown is often executed in the reverse sequence of the start-up. Shutdown sequences can be used in controlled shutdowns and when power is cut off if there are enough energy reserves to keep the power stable for the duration of the shutdown. In an uncontrolled shutdown it is often best to shut down all rails instantly to avoid damage. A sudden failure of a single power rail would cause unwanted voltage differences inside a chip so fast shutdown would be required. A probe slip can be a common cause of a power rail failure.

4.2.1 Latch-up

Latch-up is a low impedance path between power rails in a metal-oxide-semiconductor field-effect transistor (MOSFET) circuit caused by parasitic NPN and PNP bipolar transistors. This low impedance path causes high currents leading to possible destruction of the circuit as a result of overheating. Latch-ups can be cleared by power cycling the device if no permanent damage has occurred. [14]

In CMOS technology parasitic bipolar transistors form between the N-type metal-oxide-semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) transistor pairs on the substrate. A N-P-N-P structure is formed between source the NMOS, P-substrate, N-well and source of the PMOS. The resulting parasitic circuit, shown in Figure 9, is such that if one of the transistors gets biased, it will also activate the other transistor. This positive feedback will increase the current until the circuit fails. This is similar to a Darlington pair. [14]

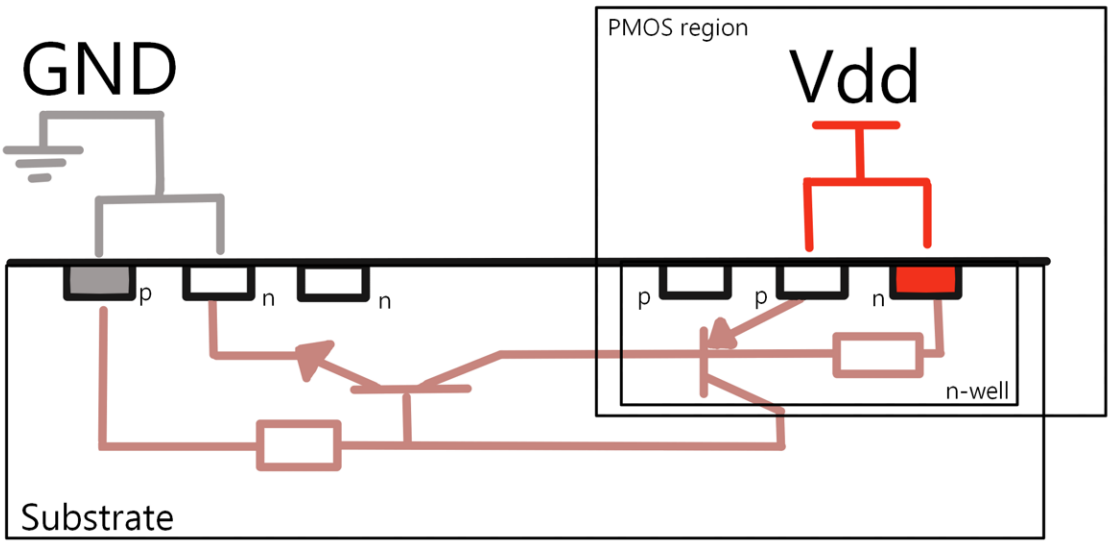


Figure 9. *Parasitic bipolar transistors in CMOS technology.*

A latch-up can form between two different voltage domains such as between the core and the I/O of a chip. Capacitance of the core power rail is often significantly greater than the I/O power rail's leading to different charge times. This can lead to forward bias states in the parasitic transistors causing latch-up. This kind of latch-up can be prevented using correct power supply sequencing. [14]

It is also possible to cause latch-up with input pin overshoot and undershoot. Same goes for over- and undershoots on power rails which can also cause a latch-up. Over- and undershoots can be prevented by utilizing electrostatic discharge (ESD) -networks. The most common ESD-network is called dual-diode ESD network in which the pin is connected to power and ground rail trough diodes. These diodes limit the over- or undershoot to voltage equal to the diodes forward voltage since excess current is sunk by power rails. I/O pins often have built-in dual-diode protection, but it is possible to add additional diodes if higher voltage ESD is to be expected. Power supply overshoots can also be avoided by using power supplies with soft start functionality which slowly increase their voltage. [14]

4.3 Power manager types

Power managers are important, and they should be used when powering complex microchips. For a microprocessor that is in development it is most important for the power management system to be configurable and flexible. Since the processor's requirements might change, it is important to be able to react to changes ideally with just software

change or in worst case by changing some components. This is important so that costly and time-consuming hardware design changes can be avoided. [13] However, there are multiple different ways to achieve the same functionality. The next Chapters 4.3.1 – 4.3.3 will compare different ways to build a power manager to make it easier to select the best option.

4.3.1 Discrete converters

The first option is to use discrete converter ICs. Discrete ICs allow a great amount of flexibility if the requirements change. If the requirements of a single power rail change, it is possible to only modify the affected circuitry. Often it might also be enough just to change some components without the need to modify the layout. [15]

Sequencing on the other hand can get tricky when only using converter ICs. Converter ICs can be sequenced by connecting them in series. Power converters usually have an output signal that indicates whether or not the converters output has reached regulation. Power good output of previous converter can be fed in to the enable of the next converter to enable the converters one after another. Power good outputs can be substituted with converters voltage outputs if the voltages are enough to trigger enable. If timing is required in addition to sequencing, this can be achieved with some passive components though tolerances of the passive components can make precise timing impossible. Shutdown sequencing can also be problematic since shutdown will happen in the same order as start-up when the shutdown should be in the reverse order. This can also be fixed with additional components, but this starts to go against the simplicity of just using converter ICs. [16][13]

Another downside for using only dedicated converters is the lack or poor quality of monitoring features. Converter ICs can often have integrated UVP and OVP protection, but the threshold values are not often tight enough for high-end ICs. Precise UVP and OVP monitoring can be achieved using comparators and resistor divisions, but this approach would require two comparators for each power rails. Another problem can be the way in which individual converters react to faults. Fault will cause a single power rail to shut down, but the others may not. This will cause voltage differences inside the IC being powered which in turn can cause latch-ups. This could also be fixed with additional circuitry which causes all power rails to shut down. [13]

Using only converters is flexible with requirements and easy to implement in simple cases but will become problematic when more advanced protections are desired. The

easiest way to fix this is to add an additional IC which is responsible for controlling the converters.

4.3.2 Discrete converters and MCU

The most flexible way to fix the problems in the previous power management option is to add a microcontroller (MCU) to control the converters. This option will have the same positive attributes as the previous option while fixing the negative aspects.

Instead of connecting the converters to enable each other, the MCU will be connected to the enable pins of each converter. This will allow very precise start-up/shutdown sequencing and the timing and order can also be changed easily with software. And since the sequencing is software configurable the shutdown sequence can be in reverse order of start-up.

The OVP and UVP fault protection problems can be fixed by reading the output voltages of the converters with the analog to digital converter (ADC) of the MCU. This allows the MCU to continuously monitor the output voltages for faults and react to them instantly by shutting down all power rails and preventing damage. MCU allows also monitoring of input voltage for sudden shutdowns. When the input voltage falls the MCU can perform a controlled shutdown if the converters capacitors are rated to provide power for long enough. Most importantly MCUs allow the state of the power management system to be indicated to users via LEDs (light emitting diode) or more advanced interfaces. Also, other features such as power buttons can be easily implemented with MCUs.

Downside of using a MCU is the added complexity of adding an MCU. Though, in most cases this is worth the added protection and flexibility. The MCU will also require its own power which must be independent of the monitored power rails.

4.3.3 Power management with PMIC

If it is desired to reduce complexity and increase fault monitoring capabilities it is possible to use power management integrated circuits (PMIC). These ICs integrate multiple converters, linear regulators, power monitoring features and power rail sequencing into a single package. PMICs can greatly simplify design and decrease the number of components required for power management but that comes with somewhat decreased flexibility. If specification of even a single power rail changes outside of the PMICs

capabilities the whole power management system may need to be redesigned if there is no drop-in replacement with correct specifications available. [15]

There are four kinds of PMICs: externally configurable, software configurable, factory programmed and user programmable. Externally configurable PMICs are similar to discrete converters since their output is set with external components, but they integrate multiple power rails into one IC and usually can have some digital logic integrated. [15]

With software configurable PMICs output voltage and other parameters are set using communication interface instead of passive components. Usually using Inter-Integrated circuit (I^2C) or Power Management Bus (PMBus) interface. Usually, a microcontroller is used to set up the PMIC. Software configurable PMICs do not have non-volatile memory so they must be setup after each start-up/reset. [15]

Factory-programmed PMICs are pre-programmed in factory and their configuration cannot be changed later. Factory-programmed PMICs are usually made for a certain type of microprocessor and are not meant for universal use. [15] Factory-programmed PMICs are a great choice if they exist for the microprocessor in question but in this case, they could not be used.

The last and the most flexible PMIC type is the user programmable PMIC. Similarly to software configurable PMICs almost everything in the user programmable PMICs can be configured with software. However, user programmable PMICs have built in non-volatile memory which allows saving the configuration. These kinds of PMICs can be used with almost any kind of microprocessor since they can be configured to match almost any need. [15]

Overall, PMICs can integrate massive number of features into a single IC while being very flexible and configurable. Since PMICs require an MCU to control them in most cases, the controller can be used to indicate the state and possible faults of the power management system to the user. The largest downside of PMICs is that if the requirements change outside of PMICs capabilities the whole power management system may need to be redesigned.

5. DESIGNING POWER MANAGEMENT FOR BALLAST SOC

From the previously aforementioned power management types the one with discrete converters and an MCU was selected. The main reason for this is the flexibility since this is the first time the Ballast SoC will be manufactured, and because Graniitti PCB is meant for testing the SoC, it is best to be prepared for small changes. Another reason is that using PMIC would also require an MCU and since there is only a need to monitor few different voltages it is easier just to monitor those voltages with an MCU.

5.1 Power management system requirements

Power management system must fulfil the following requirements.

- Provide five different power rails, three for the Ballast SoC and three for the Ethernet. The SoC requires 1.8 V for I/O, 1.8 V for PLL (phase-locked loop) and 0.9 V for core. The Ethernet requires 2.5 V, 1.8 V and 1.0 V. The 1.8 V for Ballast SoC and Ethernet PHY is shared so there are five unique power rails. Additionally, 3.3 V voltage must be generated for the control MCU.
- Power rails must be monitored for UVP and OVP faults and appropriate actions must be taken when fault occurs. Voltage should be with in 90mV of the nominal voltage for each power rail.
- Sequenced start up and shutdown for power rails. For Ballast SoC the I/O voltage should be turned on first, then the core voltage and finally the PLL voltage.
- Power on/off reset.
- Power rails should have soft start. Ramp up time for Ballast SoC power rails must be longer than 10µs.
- LEDs to indicate state and faults.
- Power button to safely turn on/off the Ballast SoC.
- Jumper to disable UVP and OVP protection.

5.2 Selected converters and regulators.

There are two main types of power converters to choose from: a linear regulator or a switching converter. Linear regulators act as variable resistors in which varying resistance is used to turn excess power to heat to maintain a stable output voltage.

Linear regulators are best for applications where either current draw is low or the voltage drop over the regulator is low, since all of the power is dissipated by the regulator. Linear regulators also turn on hard which means that they ramp-up their output voltage rapidly. This can damage some circuits, but it can be prevented with the use of additional soft start circuitry. [17]

Linear regulators also have pros. They require only just a few external components. This makes them easy to use and they are perfect also for applications with little space. Linear regulators are also cheap and most importantly they generate low noise. This makes them perfect for application which require low current and low noise such as analog circuitry like ADCs or PLLs. [17]

Switching converters, more accurately buck converters, are circuits which are used to step down the voltage. They consist of at least a diode, a transistor, an inductor, and a capacitor. Their efficiency is often higher than linear regulators which makes them optimal for cases with higher currents or voltage drops. They also often have soft start capabilities built in which makes it possible to ramp up the output voltage more slowly. Downside of switching converters is their higher noise output but that can be mitigated with filtering components. Because of their attributes switching converters are often used for IO and core power rails since they can have high current demands and their low voltage requires high voltage drop over the converter. [17]

Power converters and regulators are selected in the two following chapters. The chapters will explain the reasoning for each selected component but detailed schematic overview for each converter and regulator is reserved for Chapter 6.

5.2.1 Ballast core, IO and PLL voltages

Ballast SoC requires three power rails: 1.8 V for I/O, 1.8 V for PLL, and 0.9 V for core. Power usage estimate for the I/O is 114 mW and 1890 mW for the core. It is important to note that estimate for the I/O does not include any loads the I/O might drive so in practice it is going to be larger. Since power usage and voltages are known, current draw from each power rail can be calculated. The core draws 2100 mA and the I/O draws at least 63 mA. C2C interface has 18 outputs which all are driving 50 Ω transmission lines.

If all of those outputs are driven high, additional 648 mA of current is drawn from the I/O power rail. Power usage of the PLL rail is not known but it is estimated to be small since it is only driving few PLLs. The technology used in the SoC also limits the ramp-up speed of the power rails to 18 kV/s. To be on the safe side, the ramp-up speed is limited to 1.8 kV/s. All converters or regulators must have adjustable soft start and enable pin to allow power rail sequencing.

The core and the I/O power rails must be able to source large amounts of current, so power converters are the best choice for those power rails. For the core power rail, the converter must be able to source at least three amps of current, ideally a bit more. In addition to these requirements any converter selected must be readily available which is something that can't be taken for granted because of the global chip shortage. For core power rail LM20125MH buck converter was selected. It has an output voltage range from 5.5 V down to 0.8 V and it can deliver up to 5 A on continuous current [18]. The same converter is also selected for the I/O power rail to simplify the bill of materials and make component sourcing easier.

The PLL of the SoC also requires 1.8 V but it must be low noise so the 1.8 V I/O power rail cannot be shared with the PLL. The I/O power rail is noisy since it is generated with a switching converter and is connected to digital logic. The PLL also requires only a small amount of current so linear regulator would be perfect for this application. Analog Devices ADM7155 ultralow noise linear regulator was chosen because of its excellent low noise capabilities. It can also source 600mA of current which is more than required [19]. Its downside is that it requires multiple external components to achieve the low noise. ADM7155 also supports soft start, and it has an enable pin.

5.2.2 Ethernet voltages

The Ethernet PHY that is used with Ballast SoC is DP83867ERGZ. For now, only its power requirements are important. It can be powered either in three-supply or two-supply configuration. In three-supply configuration the PHY requires 2.5 V, 1.8 V, 1.0 V, and I/O power supply which can be 3.3 V, 2.5 V or 1.8 V. In three-supply configuration the 1.8 V power rail must be stable within 25 ms of 2.5 V power supply ramping up. In two-supply configuration the 1.8 V power supply can be left unconnected and only 2.5 V, 1.0 V, and I/O power is required. In this configuration the power supply sequencing is not required but the PHY consumes slightly more power. [20] The Ethernet PHY is used in the two-supply configuration because it is simpler and larger power consumption is not a concern.

Ballast SoCs 1.8 V I/O power rail can be used as the Ethernet PHYs I/O power supply, but 2.5 V and 1.0 V power rails are missing. The PHY consumes 137 mA from the 2.5 V power rail and 108 mA from the 1.0 V power rail [20]. The power consumption is so low that it is best to use voltage regulators to produce the required voltages since they require fewer components than switch mode power supplies. The 2.5 V regulator should also have an enable pin to allow sequencing. There are many equally good power regulators to choose from but in this case the availability of the voltage regulator is the deciding factor. So, for those reasons LD39100PU25RY from STMicroelectronics was selected. It has output voltage of 2.5 V, maximum input voltage range of 1.5 V to 5.5 V, maximum current of 1 A and it has an enable pin [21]. Since there in no need to sequence the Ethernet power supplies individually, the 1.0 V regulator can be just cascaded after the 2.5 V regulator so that they turn on/off together. This means that the enable pins are optional and other requirements are that it must be able to source at least 108 mA of current and dropout voltage lower than 1.5 V. TLV75710PDRVR from Texas Instruments was selected, because it can source 1 A of current and it has maximum voltage drop of 1150 mV [21].

5.3 Power management microcontroller

Requirements for microcontroller are not strict in this case. The microcontroller only must have an ADC and be fast enough to sample the power rails and react to changes in those. All other possible microcontroller features are optional. I have experience with 8-bit AVR ATmega microcontrollers and ST's STM32 32-bit microcontrollers, so one of these options is chosen. STM32 microcontrollers are much more powerful, and they have more peripherals than ATmega microcontrollers so in this case STM32 microcontrollers are chosen. The decision might have been different if low power consumption was important but in this case it was not. In many cases STM32 microcontrollers are even cheaper than ATmegas.

In ST's STM32 line-up there are more than thousand microcontrollers to choose from. Any STM32 microcontroller with an ADC resolution of 12-bit or more would be enough. This application does not require too many pins so a microcontroller with 48 or 64 pins could be chosen. Unfortunately, because of the global chip shortage pretty much all models worth considering were out of stock. Luckily, the university had Bluepill development boards in storage which could be used. Bluepill development boards normally use a STM32F103C8T6 microcontroller, but these Bluepill boards are Chinese copies, and they instead use a CS32F103C8T6 microcontroller which is a copy of the STM32F103C8T6 microcontroller. Those microcontrollers are almost identical, so

programs compiled for STM32F103 work with the CS32F103. One thing that is different between genuine STM32 microcontroller and a clone is the device ID. This can cause problems with programming utilities. For example, STM32CubeIDE can be used to develop and upload STM32 programs. Unfortunately, the programming utility embedded in to the STM32CubeIDE does not recognise the clone chip and thus can't be programmed. Due to the described reason, separate STM32CubeProgrammer utility must be used to program the clone microcontrollers. Features of the CKS32F103 microcontroller are shown in the Table 1.

Table 1. *CKS32F103 Features and peripherals [23]*

ARM 32-bit Cortex™-M3 CPU Core
72 MHz maximum frequency
2.0 to 3.6V power supply
48 pins (37 for I/O)
64 kB Flash
20 kB RAM (Random access memory)
2 x 12-bit ADC (16 channels). Range 0 to 3.6V
7 x timer
3 x UART (Universal asynchronous receiver-transmitter)
2 x SPI (Serial peripheral interface)
2 x I^2C
USB 2.0
7-channel DMA (Direct memory access) controller

The selected microcontroller offers enough speed and enough memory for this relatively simple application. The 12-bit ADC with a resolution of 0.81mV can also be served with the DMA controller which allows the sampling of the power rail voltages independently of the main processor.

5.4 Functionality and program

Power management programs main functionality is to monitor and sequence the power rails. Its secondary functionality is to provide a user interface through which it can be monitored and controlled.

The structure of the program is shown in Figure 10. It visualizes how time critical parts like power rail monitoring is done concurrently with the use of DMA and interrupts. All other cycles that are left after executing time critical parts are used by main loop to execute non-critical functions such as printing the user interface.

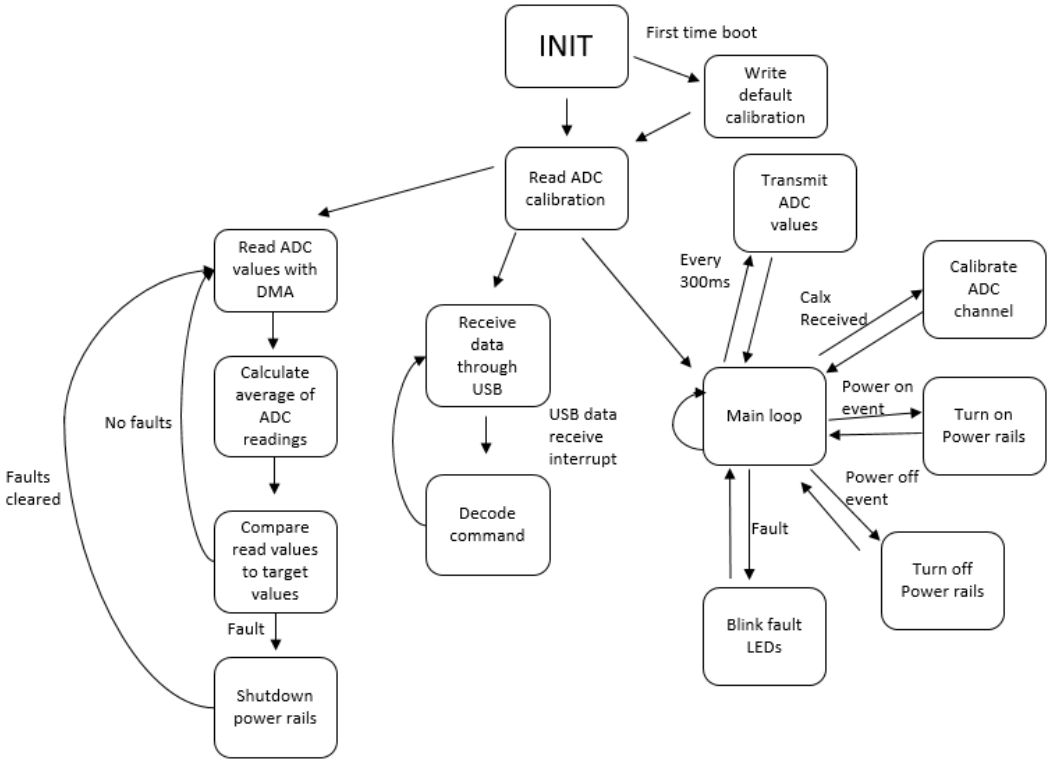


Figure 10. *Structure of the power management program*

Left part of the Figure 10 represent sampling of the power rails. With the help of DMA, it samples the power rails independently of rest of the program. Middle of the figure represent a USB receiver which receives commands from the user. Finally on the right of the figure is main loop of the program. All of the clock cycles that are left over after handling the power rail monitoring is used by the main loop. The main loop is responsible for non-critical functions such as printing the user interface and blinking the LEDs. The following chapter gives a better insight at how the different parts of the program work.

5.4.1 Start-up and shutdown

Start-up sequence is determined by an array in the program which includes delays for each power rail after which each power rail is turned on. The delay is given in

milliseconds. For example, a value 30 in the array means that the power rail corresponding to the index of that value will be turned on 30 ms after start-up is initiated. Each of the power rails are monitored continuously and if they do not reach their target voltage within 50 ms of their start up a shutdown is initiated. If each power rail reaches its target voltage, Ballast's reset signal is released.

There are two different ways to turn off the power rails: power down and shutdown. Power down is controlled and with it the first reset signal is set, and every power rail is turned off in the opposite order of start-up. Power down is initiated by the user via user interface. Shutdown on the other hand is initiated when a fault is detected in the power rails. In shutdown, first the reset is set and immediately after that all power rails are turned off at the same time.

5.4.2 ADC reading and calibration

Power rail monitoring is achieved with ADC and DMA. DMA is a hardware component inside the controller which allows transferring data from memory to memory, memory to peripheral, or peripheral to memory independently of the main processor. This allows the processor to execute other parts of the program while data is transferred. The DMA is used to read 200 samples from one of the ADC channels. When the transfer is completed, an interrupt is issued in which the sampled values are averaged and converted to voltage. After that the active ADC channel is switched, and the next power rail is sampled. If the difference between target and measured values is larger than a given tolerance a shutdown is issued. The sampling of a single ADC channels takes about 1.0 ms. Sampling speed can be increased by lowering the sample count. On the other hand, the systems immunity to quick voltage drops or spikes can be increased by slowing down the ADC or by increasing the sample count.

The ADC can often be slightly inaccurate which is a problem in this case since the power rails should be monitored as accurately as possible. For that reason, it is possible to calibrate each of the ADC channels independently. To calibrate the channels a slope and an offset is needed which can be used to calculate the accurate value of the ADC for any measured value. Calibration requires measuring two known voltages with the ADC. [24] The slope m_m can be calculated using (15).

$$m_m = \frac{Code_2 - Code_1}{V_{IN2} - V_{IN1}} \tag{15}$$

where $Code_2$ is the ADC value when measuring a higher voltage, $Code_1$ is the ADC value when measuring a lower voltage, V_{IN2} is the higher voltage and V_{IN1} is the lower voltage. [1]

Offset b_m can be calculated using (16).

$$b_m = Code_1 - m_m * V_{IN1} \tag{16}$$

where $Code_1$ is the ADC value when measuring a lower voltage, m_m is the slope and V_{IN1} is the lower voltage [24].

When slope and offset are known, an accurate value can be calculated for any input value V_{IN} with (17).

$$V_{IN} = \frac{Code - b_m}{m_m} \tag{17}$$

where $Code$ is an ADC value, b_m is the offset and m_m is the slope. [24]

5.4.3 User interface

A text-based user interface is used to monitor and configure the power manager. This interface could be provided through USB or UART. Using USB, it would be enough to just plug an USB cable to the Bluepill and the microcontroller itself works as a virtual communication (COM) port for any computer attached to it. With UART a separate UART to USB adapter is needed. For the end user, the USB approach would be simpler, so it was selected as the interface for the serial terminal interface.

Including STM32Cube™ USB device library makes it very easy to make USB applications without having to implement complex USB communication myself. The library provides ready-made implementations for multiple different USB classes such as human interface device (HID) class, mass storage class, device firmware upgrade (DFU) class, audio class, and communication device class (CDC) [25]. From those, communication device class is used to realize a virtual COM port. The USB communication device class requires roughly 25 kB of flash memory.

The serial terminal must have the ability to print floating-point numbers. STM32 microcontrollers do not support this by default but it can be enabled with compiler flags. The problem is that enabling floating-point numbers requires roughly 10 kB of flash memory. This becomes a problem since the selected microcontroller does not have enough flash memory for both the USB interface and the floating-point number printing. USB interface is important for simple user interface so for that reason it was decided to write self-made smaller function for floating-point printing.

The self-made floating-point printing function takes the same parameters as the default printf function, but it does have limited functionality. It only supports integers and floating-point numbers as specifiers. The plan is to convert a floating-point number to two integers where the integer part and the fractional parts of the floating-point number are both stored as integers and can be printed easily. The integer part of the floating-point number can be acquired by just casting the floating-point number to an integer. The fractional part is a bit harder to acquire. First the integer part is subtracted from the original floating-point number. This just leaves the fractional parts as a floating-point number. In this case there are three numbers after the decimal point. By multiplying the floating-point number with one thousand, the fractional part is shifted to the integer side of the floating-point number. Now this floating-point number can be casted to an integer and both the integer part and the fractional part are saved as integers. Integer numbers can be easily converted to characters which can be printed through the USB using a ready-made function from STM32Cube™ USB device library. The same library also provides a function for reading the USB communication. This function is called every time the USB interface receives data. The serial terminal transmits every character individually when a key is pressed on a keyboard. This means that the USB receive function is called for each key press individually. For that reason, in the receive function the received characters are stored in a buffer until character code for enter key is received. Once this happens the buffer is passed forward to a function that parses any commands from the buffer.

On start-up the PM transmits a list of supported commands, and calibration and measurement values for each channel. Voltage readings are updated every 300ms. The user interface is visualized in Figure 11.

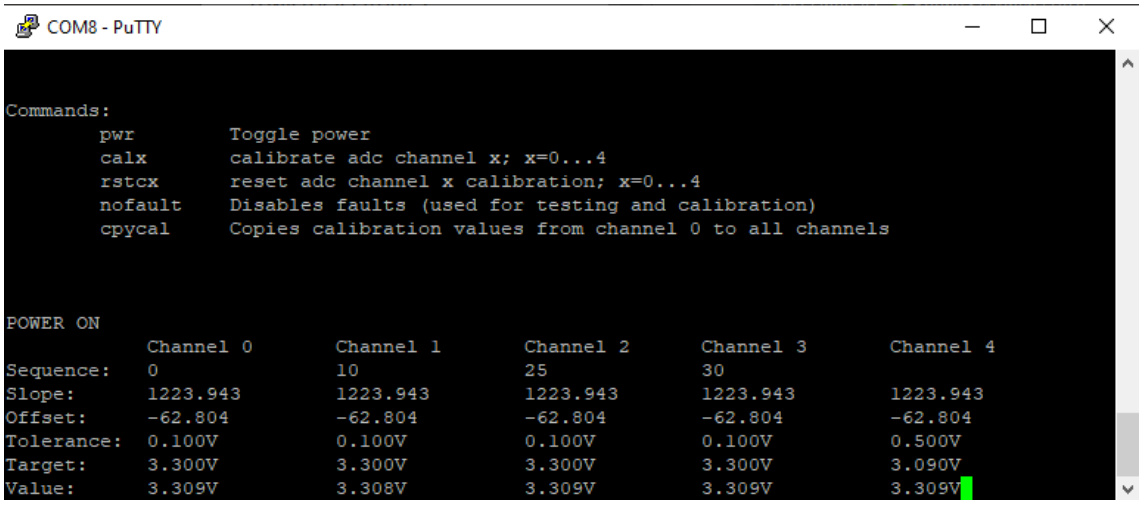


Figure 11. *PM user interface*

The PM supports four different commands which are listed in Table 2.

Table 2. *Commands supported by PM*

Command	Parameter	Functionality
pwr		Toggles power on/off
calx	x: 0…4	Starts calibration subroutine for channel x.
rstcx	x: 0…4	Reset's slope and offset to default values for ADC channel x
nofault		Toggles faults on/off. When faults are off power rails are not shutdown in case of a fault.
cpycal		Calibration values are copied from channel 0 to other channels

The power management microcontroller can also be controlled with a button and two jumpers. The button can be used to turn on or off the power rails. The two jumpers can be used to configure the settings without a user interface. The first jumper can be used to select the no-fault functionality and the other to enable auto-start. With the auto start the PM will enable the power rails automatically after being powered on.

There are two LEDs connected to the PM; green and red. The green LED is used to indicate the state of the power rails. Fully on LED means that the power rails are turned on. Blinking indicates that the power rails are on, but no-fault state is activated. The red LED is used to indicate a fault. In a fault situation the red LED will blink and stay off for one second. The number of blinks will indicate which channel encountered the fault.

5.4.4 Non-volatile memory

Since the ADC channels can be calibrated at runtime there needs to be some way to save the calibration values into non-volatile memory. Often Electronically Erasable Programmable Read-Only Memory (EEPROM) is used. Unfortunately, CKS32F103 does not have EEPROM. This means that the internal flash memory must be used. Difference between Flash and EEPROM is that with EEPROM every byte can be erased individually but with Flash the memory can only erased in sectors or pages.

Unfortunately, datasheets written in English for CKS32F103 are hard to find and the one datasheet found does not mention the structure of the flash memory. STM32CubeProgrammer software indicates that there are 128 pages with 1 kB of space. That should not be true since there should only be 64kB of flash storage, not 128kB. When trying to use the second half of the flash memory it seems to work. At least variables can be written there and read even after power down. Unfortunately, it seems that the second half of the flash memory cannot be erased by page but the whole area must be erased. This makes it inconvenient to use and for that reason only the first 64 pages are used in this application. Reason for the hidden half of the flash memory could be that the same chip is shared between CKS32F103x8 and CKS32F103xB models. The B-model has 128kB of flash memory so maybe the second half of the CKS32F103x8 models flash memory is hidden or partially disabled.

The ADC calibration requires saving two floating-point number for each ADC channel. Since each floating-point number requires four bytes and there are five channels with two variables each, this requires 40 bytes of flash storage to save. Page 63 of the flash memory was selected to be used since it is the last page so there is nothing written there as long as the program is not too large so the controller can be reprogrammed without losing calibration values. Those calibration values are read after each start-up. If those values are not present in the flash memory, default values are written. This should only happen after the first boot-up.

5.5 Power management prototype

The power management system was developed and tested with STM32 Nucleo development board. The Nucleo board is almost identical in performance to the Bluepill so it could be used in prototyping instead of the Bluepill. In addition, a perfboard was used to add connections for buttons, switches, and LEDs. The perfboard was also used to connect all of the ADC channels together so that their values could be easily compared. The test setup is shown in Figure 12. This test setup lacks the converters and

LDOs (low-dropout regulator) to generate the actual power rail voltages, but correct functionality of the controller can be verified without them.

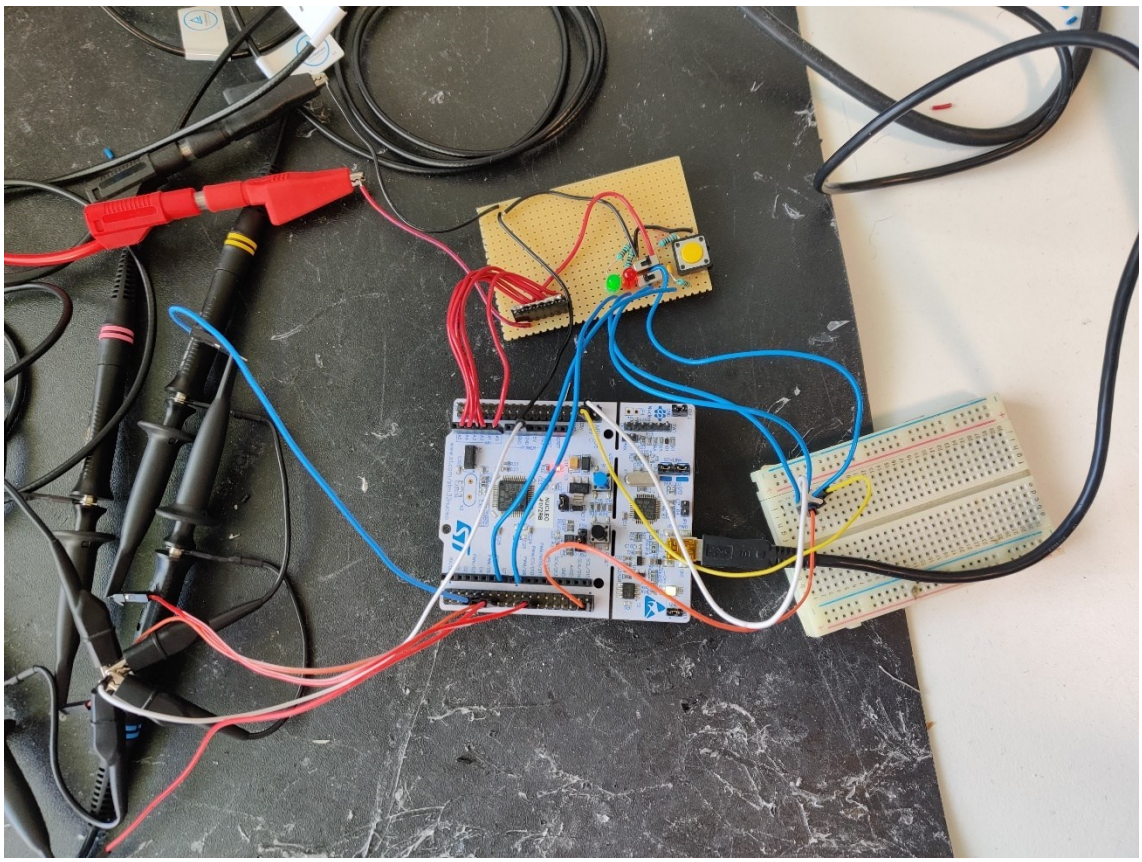


Figure 12. *Power management test setup*

The first test was to measure the accuracy of the ADC channels. A lab power supply was used to feed a voltage to the ADC channels. The voltage was also measured with a multimeter. Before the test all of the ADC channels were calibrated at 0.3 V and at 3.0 V. The voltage range for the test was from 0 V to 3.3 V. The voltage range was divided into thirteen measurement steps with most steps being at lower voltages. The test results are shown in Table 3.

Table 3. *ADC channel accuracy measurements and error*

	Measured voltage (V)					Error (mV)				
Vin (V)	Ch0	Ch1	Ch2	Ch3	Ch4	Ch0	Ch1	Ch2	Ch3	Ch4
0	0,053	0,052	0,053	0,053	0,053	53	52	53	53	53
0,038	0,053	0,052	0,053	0,053	0,053	15	14	15	15	15
0,079	0,08	0,08	0,081	0,081	0,081	1	1	2	2	2
0,104	0,105	0,104	0,105	0,105	0,105	1	0	1	1	1
0,311	0,312	0,312	0,312	0,312	0,312	1	1	1	1	1
0,611	0,61	0,61	0,61	0,611	0,611	-1	-1	-1	0	0
0,91	0,911	0,91	0,911	0,911	0,911	1	0	1	1	1
1,21	1,21	1,209	1,21	1,21	1,21	0	-1	0	0	0
1,507	1,506	1,506	1,506	1,506	1,506	-1	-1	-1	-1	-1
1,811	1,811	1,81	1,811	1,811	1,81	0	-1	0	0	-1
2,108	2,108	2,107	2,108	2,108	2,108	0	-1	0	0	0
2,508	2,509	2,509	2,509	2,509	2,509	1	1	1	1	1
3,01	3,011	3,009	3,011	3,01	3,011	1	-1	1	0	1
3,308	3,307	3,306	3,307	3,308	3,307	-1	-2	-1	0	-1

From Table 3 results it is clear the microcontroller is able to measure the voltages within a few millivolts of the real value. Voltages that are near zero cannot be measured accurately but it does not matter in this application.

The next test was to ensure that the power rail sequencing works correctly. This was done by measuring all of the power rail enable signals with an oscilloscope. In the power manager software, it was set so that power rail 1 is activated at 0 ms, power rail 2 is activated at 10 ms, power rail 3 at 25 ms and power rail 4 is activated at 30 ms after start-up. Screenshot of the oscilloscope measurement is shown in Figure 13. In the figure one division is 10 ms which makes it easy to verify that all power rails are enabled exactly at the correct times. Cursors were also used to verify that the time between the first and last enable is really 30 ms. Cursors show that time was 30.60 ms which is perfect given the measurement accuracy with cursors.

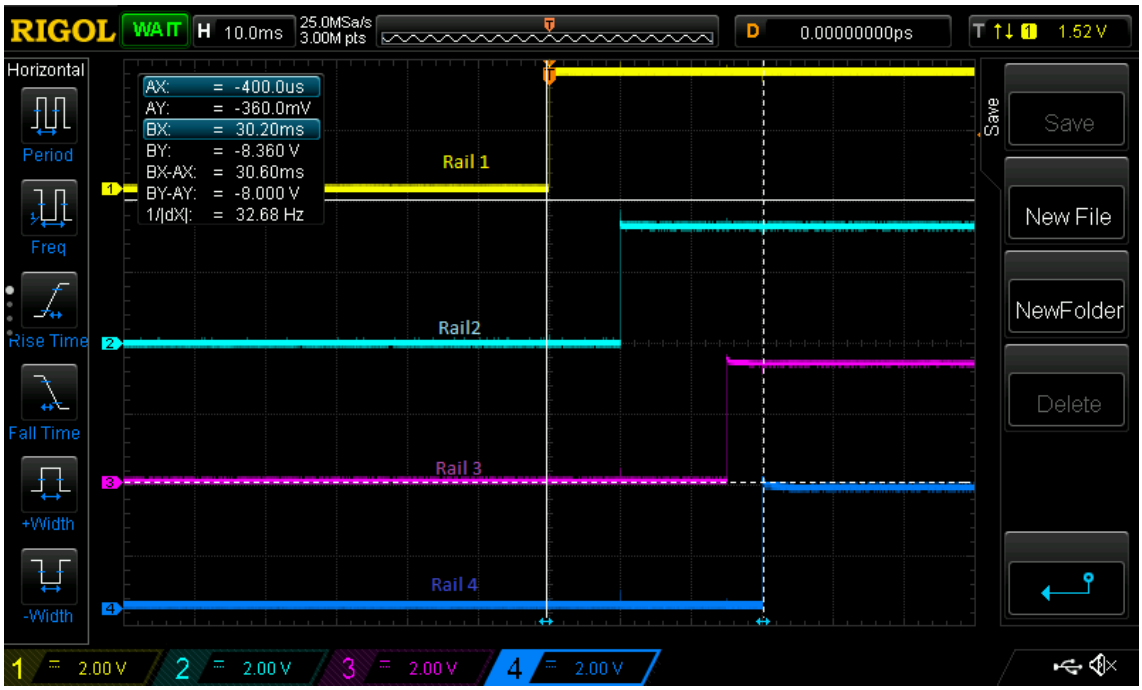


Figure 13. *Power rail start-up sequence*

Next the shutdown sequence was tested using the same method. It is expected that the power rails are tuned off in opposite order of start-up and the delays between the rails are same as in start-up. The shutdown sequence is shown in Figure 14. As expected, the shutdown sequence has the correct order and timings.

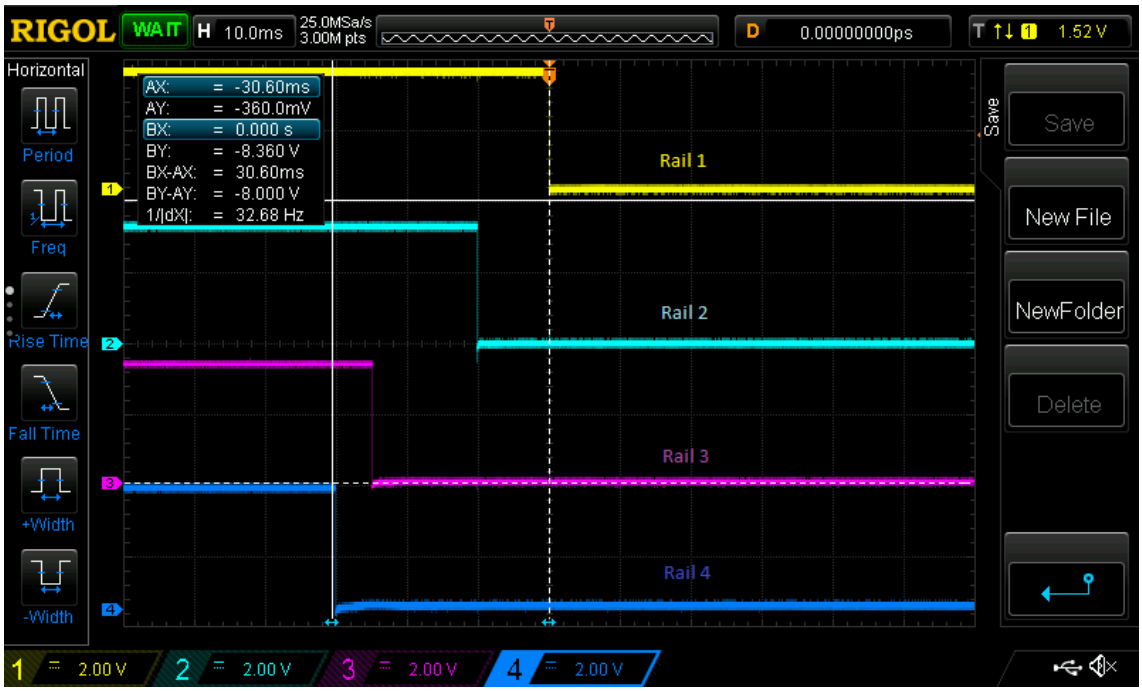


Figure 14. *Power rail shutdown sequence*

During the start-up, each power rail has 50ms to stabilize to their target voltage. If they do not stabilize in the given time a shutdown is initialized. To test this functionality, some kind of way was needed to simulate the power rails with a configurable turn on delay. This could be done using another microcontroller which reads the power rail enable signals and turns on the corresponding output after some delay. The test setup is shown in Figure 15. Another Nucleo development board was used to delay the signals.

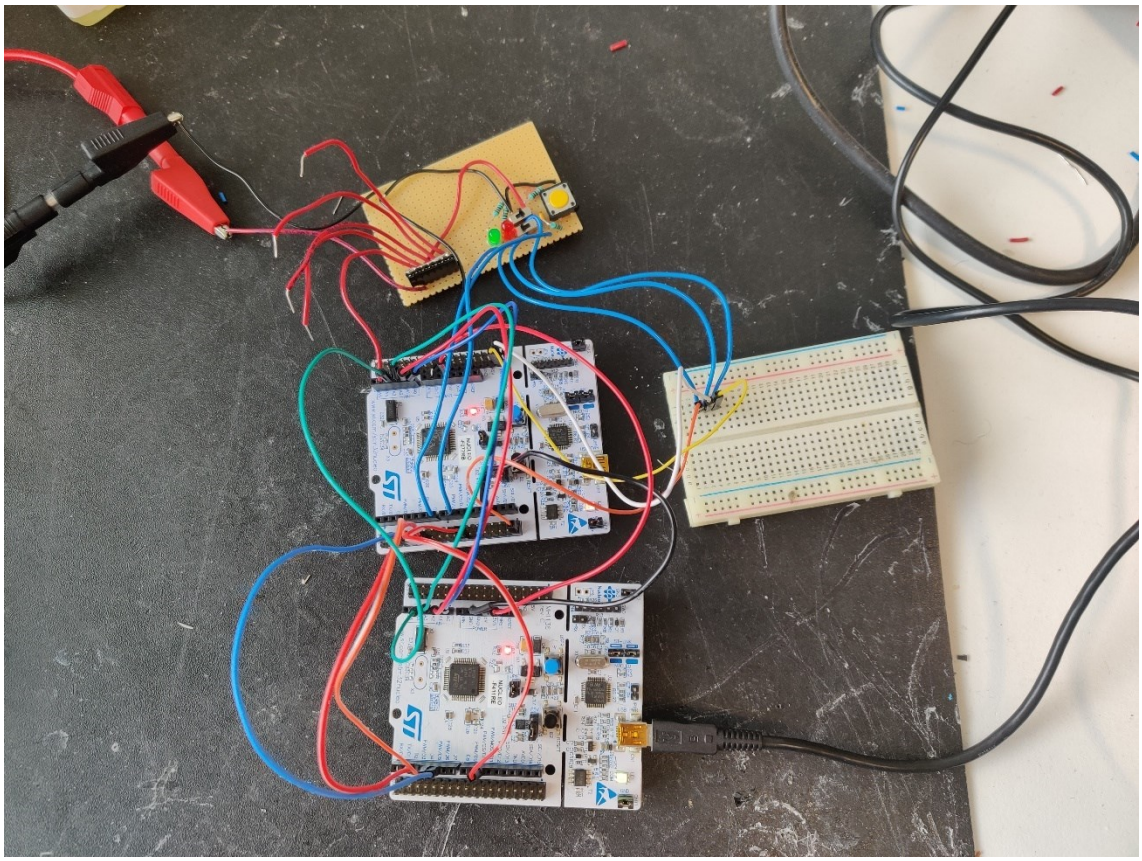


Figure 15. *Test setup for start-up delay testing*

First the delay was set to 30 ms for all rails to test that the start-up sequence works correctly with some delay, which it did. Next each power rail was tested by setting its delay to 50 ms and leaving others delays to 30 ms. During the start-up, the controller correctly noticed that one of the power rails failed to reach its target in 50 ms and all of the rails were shut down and a fault LED started to blink. The blinking pattern correctly identified the right power rail as the cause of the fault. This test was repeated for each power rail. The test was also repeated with delay of 49 ms for the rail under testing. Now the start-up failed in about every other try. With delay 48 ms the star-up succeeded every time. This tells that the time measurement is not perfect. Both microcontrollers used sysTick for time keeping which has resolution of one millisecond. This will explain some of the inaccuracy in the testing. Despite the small inaccuracy the system is accurate

enough for this application and the maximum stabilization time of 50 ms can also be changed if necessary.

These tests give enough confidence that the power management program will work, and it can be used to manage power rails on Graniitti. Even though the test were made on Nucleo board the software itself can be ported on Bluepill with only small changes. The power management system must still be tested once it is on Graniitti, but at least its most important features are verified to work.

6. GRANIITTI SCHEMATIC DESIGN

Eurocircuits was selected to manufacture the test PCBs. Eurocircuits is a European PCB manufacturer which offers both PCB manufacturing and assembly services. Manufacturer's capabilities will affect what kind of a PCB can be designed. Eurocircuits capabilities are looked over in Chapter 7.2.

The first plan was to make this test PCB stackable with the FPGA board. The PCB would be 10 mm above the FPGA board due to the height of the FMC connector. Unfortunately, there is a cooler mounted on FPGA which is more than 10 mm in height. This makes it impossible to mount the PCB on the FPGA board. This leaves two options. Attaching the PCB with FMC cable or making a hole in the PCB where the cooler would be. The hole approach would result into a more complicated PCB design, so it was decided to go with the FMC cable. FMC cable also allows attaching any FPGA board with FMC instead of just the one it was designed for.

The schematic of the Graniitti PCB is divided into seven sheets: SysCtrl, MPC, C2C, Ethernet, DFT, power management controller, and powering. In the schematic the Ballast SoC is divided into nine subcomponents according to the subcomponent's functionality. This allows dividing the schematic into logical sheets and makes it much clearer than having everything on the same sheet. The schematic pages are shown in pieces in the following chapters as its pages are too large to be shown in their entirety. Entire schematic can be found as Appendix A.

Since Graniitti PCB is used for testing it is important that the I/O is easily accessible and testable. In practice this means almost every signal will be attached to a pin header and there is a ground pin near each signal pin. If signals are not brought to a pin header or to some other I/O connecter there should be a test point to allow probing those signals.

6.1 Component selection

Eurocircuits assembly services allows components to be supplied by the assembler, customer or left unassembled. It was decided to let the assembler source the components as this is the most convenient way. This requires checking at schematic design phase that Eurocircuits can actually source the selected components. Luckily Eurocircuits provide an online tool for this purpose.

For common passive components Eurocircuits offers using generic components instead of a specified component. The generic components will have the same attributes as

required by the design but their exact model in not know. Since there is no need to source generic components, Eurocircuits offers them for free.

Most of the components that are going to used are surface-mount devices (SMD) as they take less space than thru-hole components. There are also often wider variety of SMD components than thru-hole components. SMD components which use packages with visible pins are preferred as they are easier to probe that than packages with pins hidden underneath.

6.2 SysCtrl

SysCtrl is the first core in Ballast to boot up and is responsible for booting up other cores, so it requires some additional external components. Schematic page of the SysCtrl subsystem is divided in to two figures. Figure 16 shows most of the connections to SysCtrl subsystem and Figure 17 shows schematic for the SD card. In the schematic SysCtrl subsystem is the component U1:A.

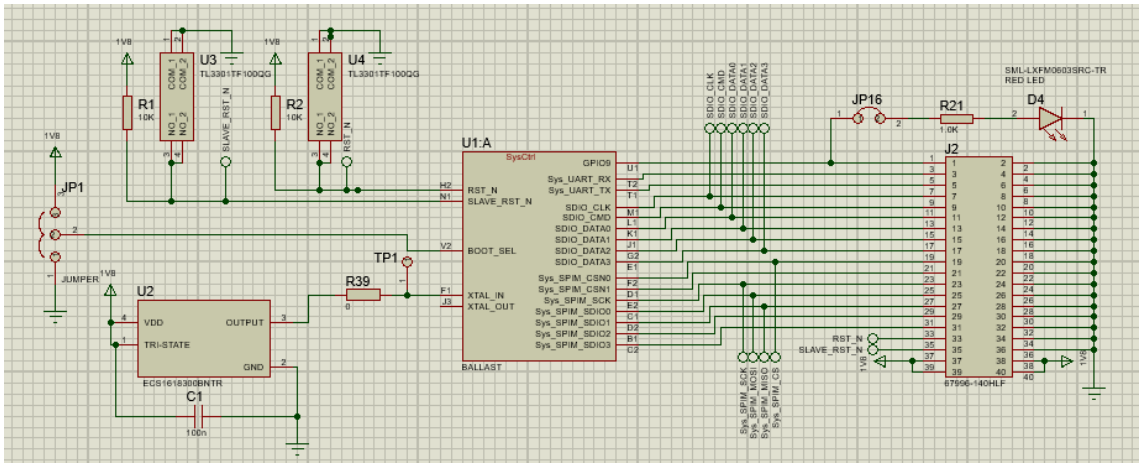


Figure 16. *SysCtrl subsystem schematic*

On the left side of the Figure 16 from top to down the first components are two switches and their pull-up resistors. The switches are connected to reset, and slave reset inputs both of which are active low signals. Next to the oscillator there is a jumper connected to the BOOT_SEL pin. By switching the position of the jumper, the BOOT_SEL can either be connected to ground or to 1.8 V. The last component connected to the left side of the SysCtrl is TG2520SMN 30 MHz oscillator which is used as the systems clock. It was chosen for its high precision and 1.8 V functionality.

On the right side of the SysCtrl there are 16 GPIO pins which are divided into four groups according to their primary functionality. There are SPI, UART, Secure Digital input output (SDIO) and one pin without primary functionality. All of the GPIO and reset signals are

connected to a 40-pin header. The signals are connected to one side of the header while opposite pins are used for ground.

SysCtrl sub system connects to SD card through SDIO and SPI interfaces. Since Ballast SoCs IO operates at 1.8 V and SD cards I/O operates at 3.3 V, those interfaces must be level shifted. Schematic for level shifting SD card interfaces is show in Figure 17.

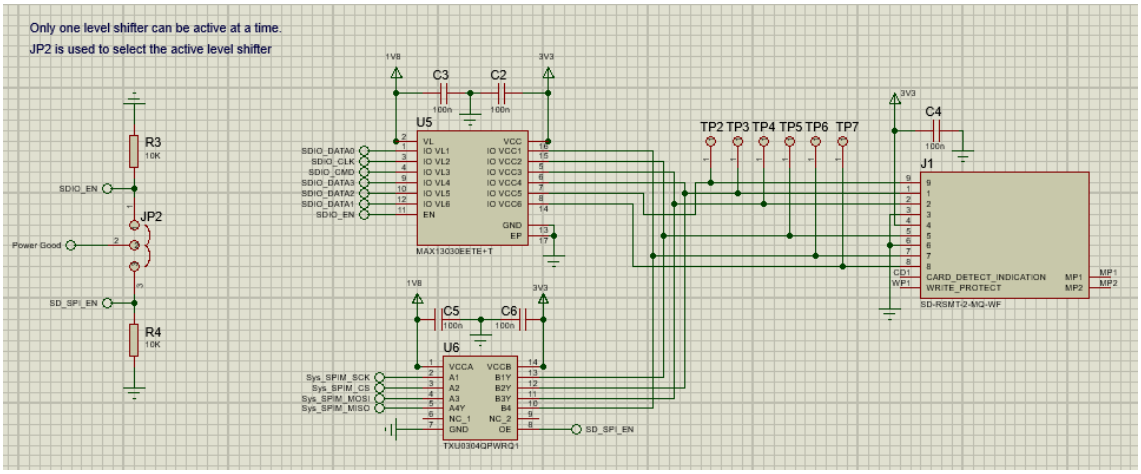


Figure 17. *SysCtrl SD card level shifting schematic*

SDIO signals are bidirectional which is a challenge since most level sifters are unidirectional or they use a signal to control the direction. Luckily there are bidirectional level sifter available for this purpose. There are two options to choose from: TXS0206 from Texas Instruments and MAX13030 from Maxim Integrated. They both have basically the same functionality but TXS0206 is more readily available and cheaper, but it uses 20-bump wafer chip scale package, which is 1.96 mm x 1.56 mm, with 0.4 mm ball pitch [26]. It is so tiny that that it is really difficult to use, and the required PCB technology is at Eurocircuits limits and would be more expensive. MAX13030 is available in similar chip scale package but also in a much more user friendly TQFN (thin quad flat no-lead) package. For that reason, MAX13030 level sifter was selected. In Figure 17 component U5 is the SDIO interfaces level shifter.

SPI signals are unidirectional which makes them easier to level shift. There are three signal which go from the Ballast to the SD card and one signal from the SD card to the Ballast. TXU0304QPWRQ1 level shifter from Texas Instruments was selected since it has four channels with three going in one direction and one going in the opposite direction. SPI and SDIO pins in an SD card are shared which causes problems since both level shifters are trying to drive those signals. In worst case the level shifters can break if the signals are driven into opposite states by the level shifters. For that reason, jumper JP2 is used to select which level shifter is active. Enable signals of both level shifters are pulled down by default which disables them. Jumper is used to select which

enable signal is connected to a Power Good signal. The Power Good signal is driven high when all power rails have reached regulation. This ensure that the level shifters are not enabled before both of their power supplies are present. Finally, there are six test points connected to the SD card signals so that they can be easily probed if necessary.

6.3 MPC

Medium performance core is used mainly for general purpose I/O. There are five interfaces in the MPC: SPIM, UART, CAMIF, I^{2}C and I^{2}S. Figure 18 shows first part of the MPC schematic sheet.

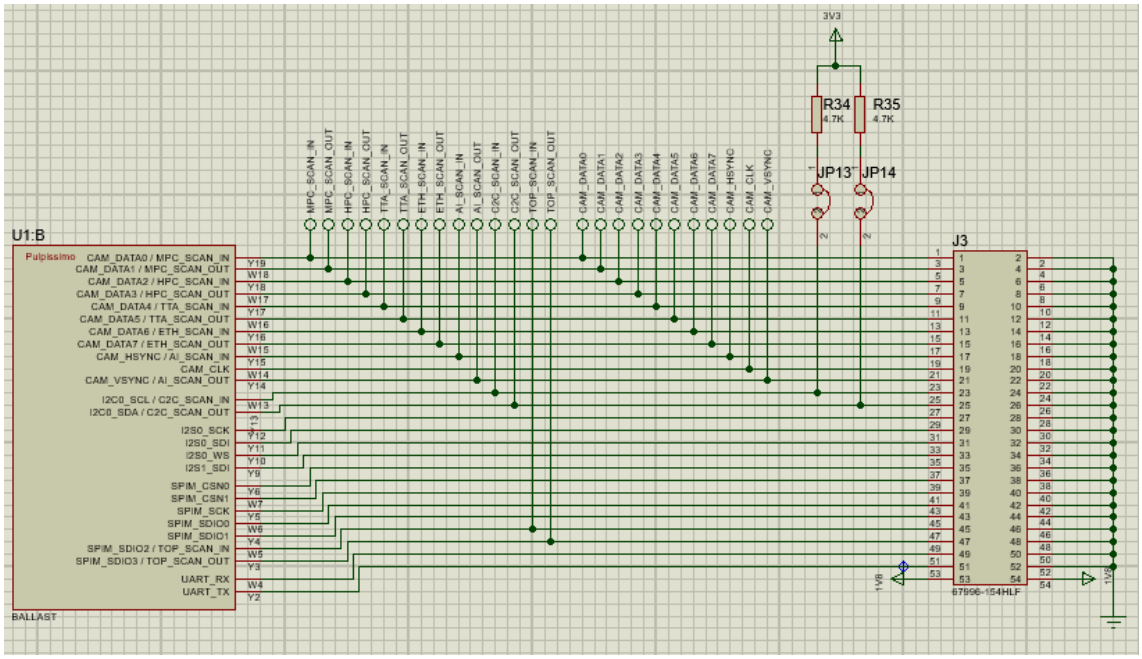


Figure 18. *MPC IO schematic*

Every IO pin of the MPC is connected to a two-row 54-pin header. As in the SysCtrl page the signals are connected to a single side of the pin header and other side of the header is dedicated for ground. In addition to those interfaces there are two 1.8 V pins. I^{2}C interface requires pull up resistors so the I^{2}C pins are pulled up through 4.7 kΩ resistors. The pull-ups are connected to 3.3 V so that the I^{2}C can work with common 3.3 V devices. Because of the large pull up resistors the 3.3 V should not damage the Ballast's 1.8 V I/O. There are also jumpers in series with both pull up resistors so that the pull ups can be disabled if they are not needed. Some of the pins on the MPC can be used for scan testing. These pins are attached to net ports which are connected to the FMC connector on other page of the schematic.

Camera that is going to be used with the camera interface uses 3.3 V I/O voltage. As before this level shifters are needed to translate between 1.8 V and 3.3 V I/O. Figure 19 shows the schematic for camera interface level shifters.

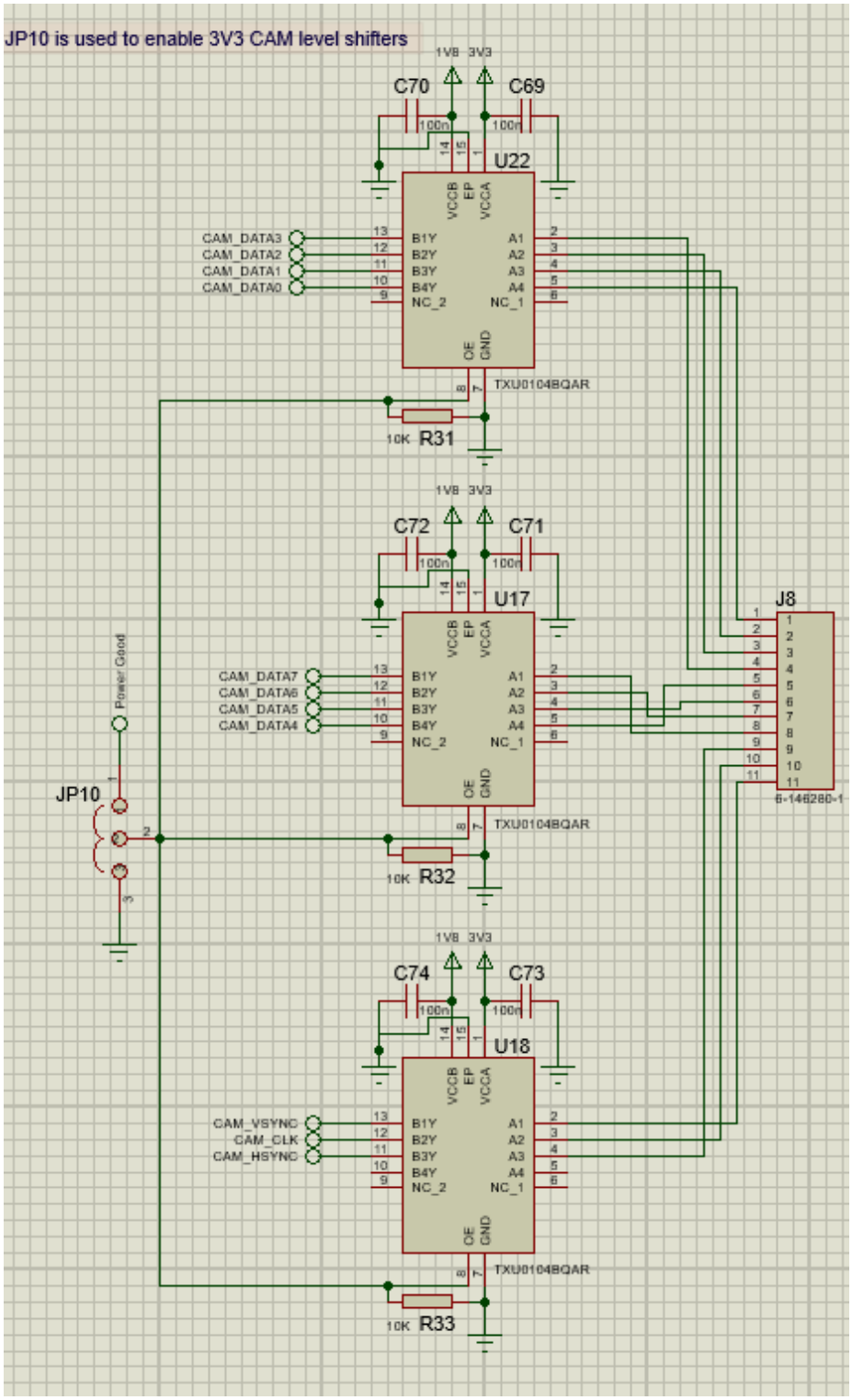


Figure 19. *MPC CAMIF level shifting schematic*

Camera interface signals are unidirectional, so simple unidirectional level shifters are enough. The level shifters can be disabled or activated with the use of jumper JP10. The

enable state of the jumper is connected to the Power Good signal instead of the 3.3 V power rail. This is because the 3.3 V power rail is always enabled but the 1.8 V power rail is not. This means that the level shifters could be enabled when only one of their power supplies is on. This is prevented by using the Power Good signal in the enable jumper. Power Good signal is asserted only after all power rails are enabled. This means that the level shifters are only enabled after all the power rails are enabled even if the jumper is always set to enable.

6.4 Ethernet

The Ethernet sub-module of the Ballast uses reduced gigabit media-independent interface (RGMII). The sub-module requires an external PHY chip to implement the physical layer of the Ethernet. There are three main requirements for the PHY. It must support Gigabit Ethernet, use RGMII interface and use 1.8 V IO. DP83867 PHY from Texas Instruments was selected. Unfortunately, the current global chip shortage caused the PHY to be sold out from everywhere and the earliest estimations for the availability are a year from now. The same availability problems also affect all other compatible PHYs, so another solution is required. Since this PCB is used to test and verify the functionality of the Ballast and not used as a final product, an external PHY can be used.

DP83867ERGZ-R-EVM evaluation board was selected since it uses the same DP83867 PHYs as originally specified and there were few of them still available. The evaluation board integrates all of the required components for the PHY to work so that only the RGMII signals must be connected to it. The evaluation board is made to use 2.5 V IO signals which are incompatible with the Ballasts 1.8 V IO. With the use of external power supplies, it can be made to use the 1.8 V IO. To function it requires the following power rails: AUX_IOVDD_EXT, VDDIO_EXT, VDDA2P5_EXT, VDDA1P8_AB, VDDA1P8_CD and VDDA_1V0_EXT [27]. Power rail VDDIO_EXT is used for IO voltage, and it must be connected to 1.8 V [27]. AUX_IOVDD_EXT is not connected by default so it can be left unconnected [27]. VDDA2P5_EXT must be connected to the 2.5 V power rail and VDDA_1V0_EXT to the 1.0 V power rail [27]. VDDA1P8_AB and VDDA1P8_CD power rails could be connected to the 1.8 V but they are optional, so they won't be connected at all, but they can be connected for additional power saving [27][20]. The evaluation board also requires some changes to its configuration to use the external power rails. Resistors R71, R74 and R81 must be removed. Removing these resistors disconnects the evaluation boards internal power rails from its onboard voltage regulators. Locations R67, R68, R70, R77 and R79 must be populated with 0 Ω resistors. These resistors are used to connect the internal power rails to external power rails [27].

The schematic page for the Ethernet is shown in Figure 20. On the top of the schematic there are connections for the RGMII interface from the Ballast SoC to a pin header. As before, a two-row pin header is used on which one side is used for signals and the other ground. On the bottom of the pin header there are two pins for each power rail. On the bottom of the schematic there are the two voltage regulators which are used to generate the 2.5 V and 1.0 V for the Ethernet PHY. The two regulators are cascaded one after another. This lowers the voltage drop and power loss over the second regulator and enables the second regulator immediately after the first.

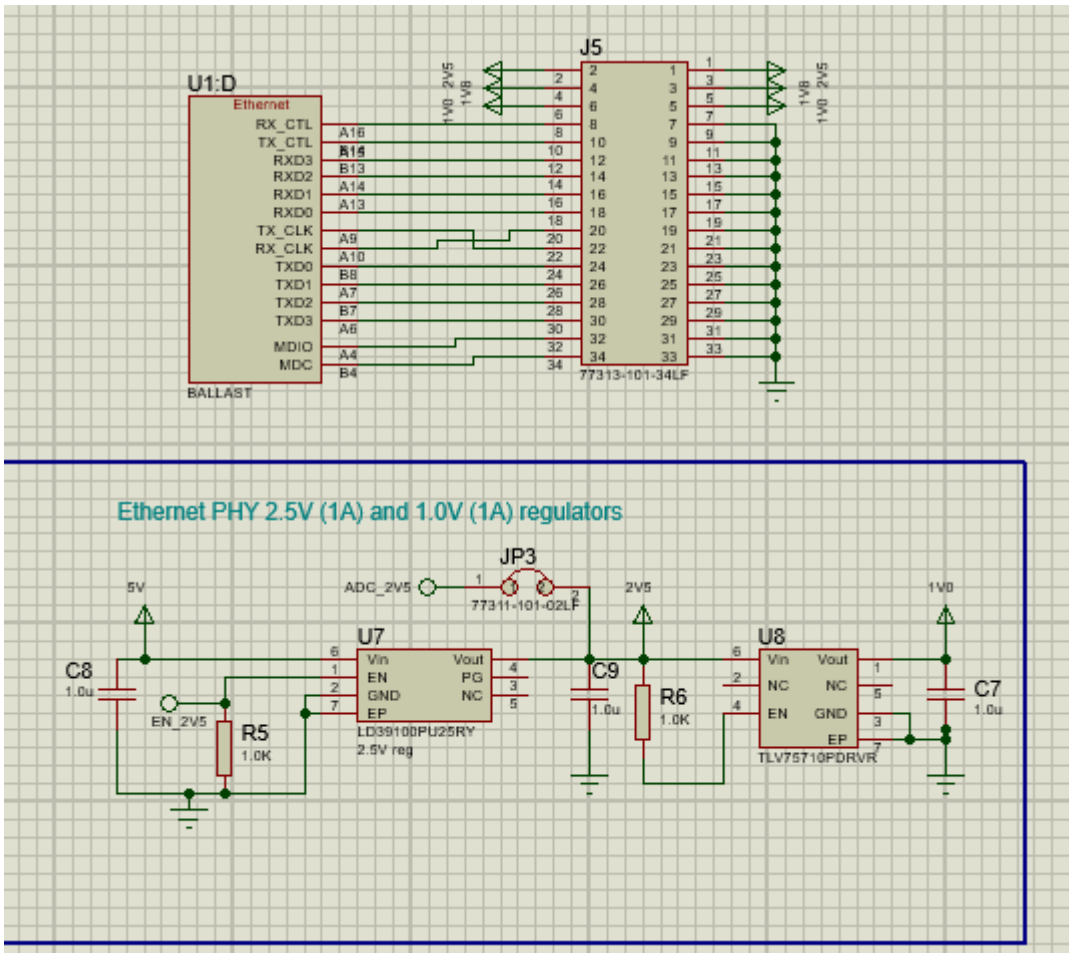


Figure 20. *Ethernet subsystem schematic*

6.5 C2C

Schematic page for C2C is shown in Figure 21 and it consists of C2C subsystem and of the FMC LPC connector. The physical FMC connector has four rows of pins. In the schematic the connector, J4, is made of two parts both of which correspond to two rows of pins. Part A has the pins for rows C and D, and part B has the pins for rows G and H.

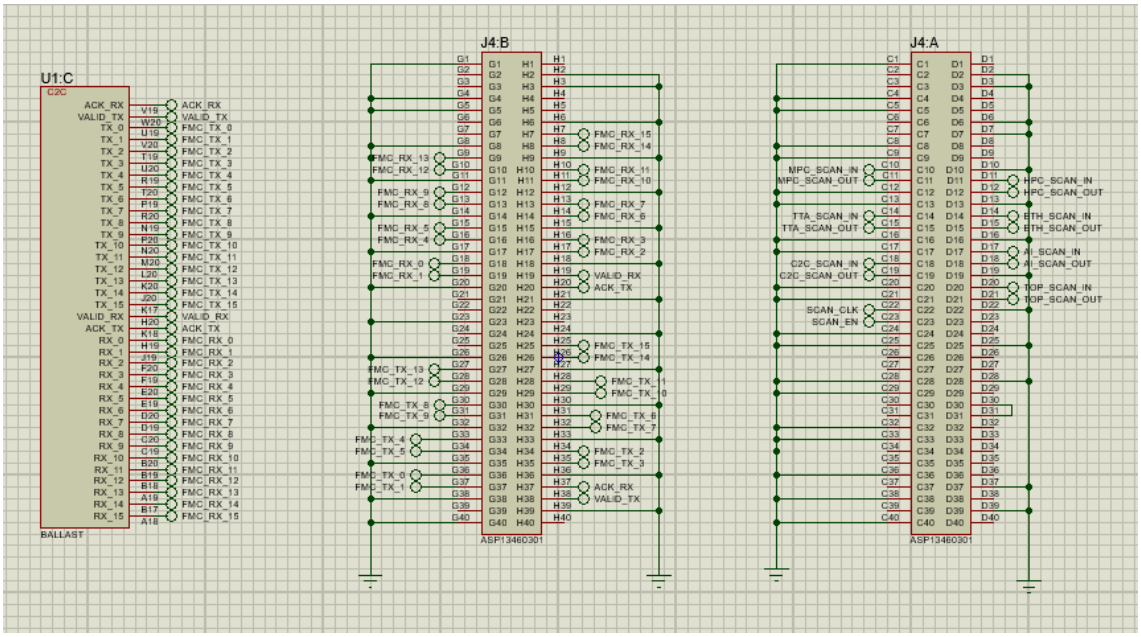


Figure 21. *C2C subsystem schematic*

The FMC connector will be oriented in a way that when the FMC cable is connected to it the cable points away from the PCB. In this orientation the pin rows G and H will be closest to the Ballast, so they were chosen to be used for the C2C signals. Many of the pins in the rows G and H are used for ground and few of the pins have a dedicated purpose but most pins can be freely used as signal pins for the C2C. The pins are populated with C2C signals from the connectors edges towards the middle. This was done to allow maximum amount of room for the signals in layout design phase. The signal ordering for the FMC connector emphasizes layout simplicity over the most visually pleasing signal ordering. For that reason, the signal ordering for TX signals is not as logical as it could be since some signals are not in a numerical order, but this allows the simplest layout design. The ordering of the signals does not affect the functionality since the C2C connects to an FPGA for which the ordering of the pins is not important.

The C and D rows of the FMC connector are used for scan signals. These signals are not high speed so they can be on the other side of the connector. Routing signals to this side of the connector requires using vias and other layers than top layer so it is not optimal for high-speed signals but works well for slower signals like the scan signals.

6.6 Debug

Debug page of the schematic is shown in Figure 22 and it consists of two distinct parts: JTAG and PLL test outputs. PLL test outputs are shown in the bottom of the schematic. They are analog outputs which can be used to output different internal voltages from the

PLL. These outputs do not require any special considerations, so they are simply just connected to an 18-pin two-row pin header. In addition to test outputs, one of the headers pins is connected to the PLLs supply voltage. Rest of the pins in the header are used as ground pins.

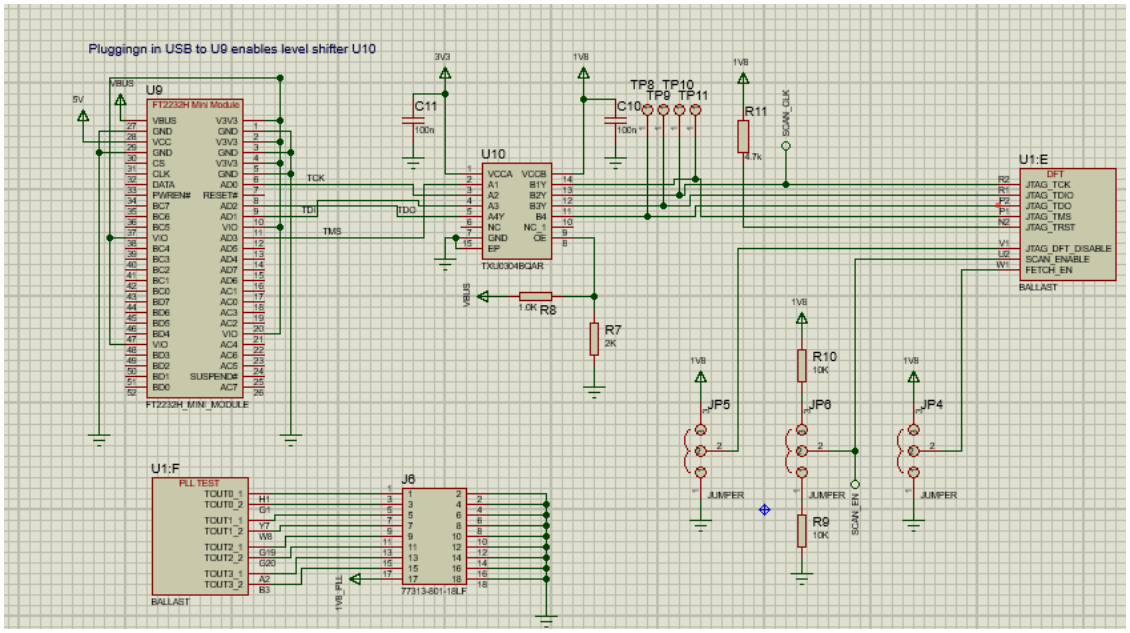


Figure 22. *Debug subsystem schematic*

Top half of the schematic is used for the JTAG. Original goal was to use the FT2232H IC to convert USB to JTAG. Unfortunately, this and other similar chips were all sold out from the manufacturer and distributors because of the global chip shortage. Luckily the FT2232H Mini Module evaluation boards using said FT2232H IC were still available, so it was decided to use those evaluation modules on this PCB. The module is the component U9 in Figure 22. Implementation of the module is easy since the module integrates all the components required for the FT2232H IC to function. The only requirement is to provide power for the module. The module can either be powered from the USB port on the module or externally. It was decided to go with external power. To accomplish this the VCC of the module is connected to 5 V of the PCB. On the module there is a voltage regulator which converts the 5 V to 3.3 V and this 3.3 V is available on the modules V3V3 pins. Finally, the V3V3 pins must be connected to the VIO pins to provide 3.3 V for the chips IO.

The evaluation module uses IO voltage of 3.3 V which is incompatible with the Ballasts 1.8 V IO voltage. This problem can be solved by using a level shifter. The JTAG interface consists of four signals. Three of those go from the module to the Ballast and one goes from Ballast to the module. Since all of the signals are unidirectional, a simple one-way level shifter can be used. TXU0304QPWRQ1 level shifter was selected since it is readily

available, uses easy to use package, and it has four channels of which three work in one direction and one works in opposite direction, so it is a perfect choice for level shifting JTAG signals. In the schematic the level shifter is shown as component U15. It requires only few external components. One bypass capacitor for each power input. Enable signal of the level shifter is connected to two resistors which form a voltage divider. The divider is used to lover the 5 V VBUS to roughly 3.3 V which is used to enable the level shifter. The VBUS is sourced from the USB connector of the FT2232H module so that the level sifter is enabled only when the USB of the FT2232H module is connected. When the level sifter is disabled, its outputs are in high impedance state.

The JTAG signals from the level shifter are connected to the Ballast which is the component U1:E in the schematic. JTAG_TRST signal is pulled up through a resistor and not connected anywhere else as it is optional signal and not used. There is also a test point attached to each of the JTAG signals so that they can accessed if there is something wrong with the level shifter or FT2232H module. The JTAG_TCK signal is shared with SCAN_CLK signal. For that reason, the level shifter is disabled when the JTAG is not used so that the SCAN_CLK can be used to drive the JTAG_TCK signal. The last connections to the JTAG part of the Ballast are three control signals. They are all connected to two position jumpers so that they can be connected to either ground or 1.8 V. Scan enable jumpers features pull-up and pull-down resistors so that its state can be controlled by the jumper or by an external FPGA board.

6.7 Power management

Power management controller's schematic is shown in Figure 23 and it consists of the Bluepill microcontroller development board and few external components. Starting from top left of the schematic there are two jumpers. Those are the two jumpers used to set auto start and fault checking functionalities. Switching the jumper position simply switches whether the GPIO pins connected to jumpers are connected to ground or 3.3 V. Beneath the jumpers there are two LEDs, green and red. The LEDs are connected to the microcontroller through 1 kΩ resistors to limit current. Final components on the left side are the power button and its pull-up resistor and debounce circuitry. The 10 kΩ pull-up resistor is used to pull up one of the microcontrollers GPIO pins to 3.3 V. The button is connected to the same GPIO pin so that when it is pressed the GPIO line is connected to ground through the button. The 1 kΩ resistor and 100 nF capacitor form an RC circuit which filters out button bounce noise. Finally on the left side there are four nets on microcontrollers pins B12 to B15 which are used to enable power rails.

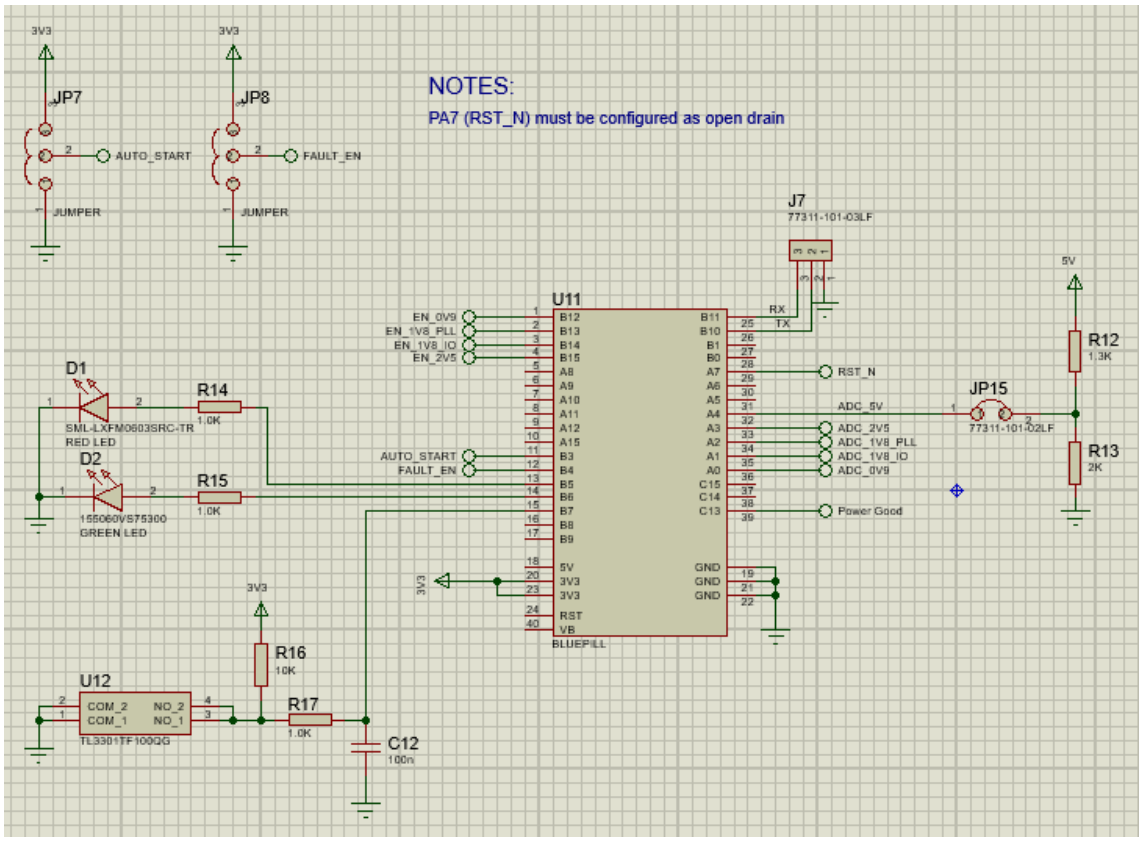


Figure 23. *Power management controller schematic*

Continuing from top right of the schematic there is a three-pin header J7 which could be used for UART but is not used because the USB was selected for serial terminal interface. Beneath that there is connection to reset signal RST_N. The pin A7 to which the reset signal is connected must be configured as open drain output. That is because the Ballast SoC to which it connects to operates with 1.8 V IO voltage and the MCU operates with 3.3 V IO voltage. When the output is configured as open drain, it can only pull that signal down to ground but cannot push it to 3.3 V. The reset signal is pulled up to 1.8 V by an external pull-up resistor in the SysCtrl schematic page. Beneath the reset signal on the right there is a resistor division which is used to lower 5 V input voltage to 3.3 V so that the microcontroller can read it using ADC. Finally, there are four signals which are used to sample the power rails with ADC.

6.8 Powering

The Graniitti PCB is used to generate six different power rails. The schematic design for the Ethernet power rails was explained in Chapter 6.4 as those power rails are only for the external Ethernet PHY and are not used anywhere on the Graniitti PCB. The remaining four power rails are used on Graniitti PCB or to power the Ballast SoC.

The four remaining power rails each offer their own unique design challenges. The 3.3 V power rail must be the last one to turn off. The 0.9 V core and 1.8 V I/O power rails must be able to provide higher current and stable power for fast switching circuitry. And lastly the 1.8 V PLL power rail must be designed to be very low noise. The designs for these four power rails are shown in the following chapters.

6.8.1 3.3 V power rail

3.3 V power rail is used by the power management microcontroller, SD card, and by some level shifters. Because it is used by the power management microcontroller it is important that it is the last power rail to fail when power is disconnected from the Graniitti PCB. This means that there must be some sort of energy storage for the 3.3 V power rail and that power storage must be separated from other power rails. Schematic for 3.3 V power rail is shown in Figure 24.

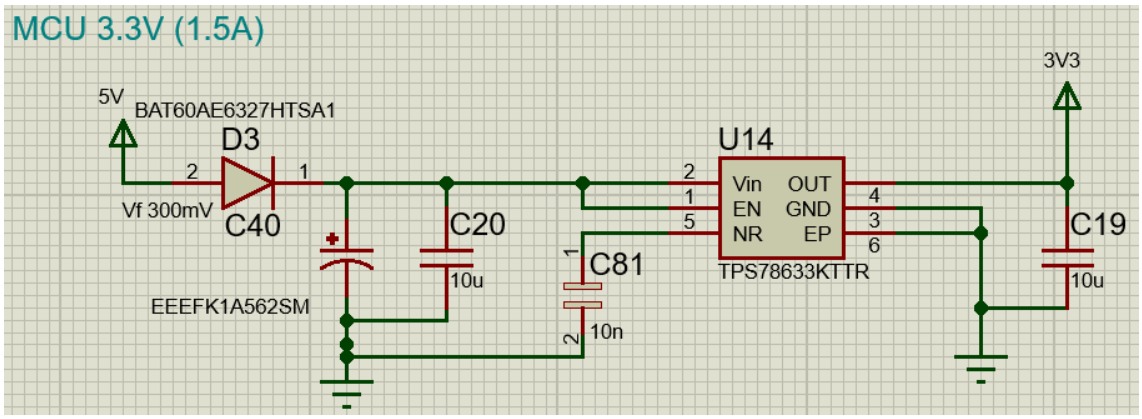


Figure 24. *3.3 V power rail schematic*

Diode D3 is used to separate 3.3 V power rail energy storage from other power rails. A Schottky diode is used because of its lower forward voltage of 300 mV in this case. Low forward voltage is important so that there is the highest possible voltage on the capacitor C40 which is used as the energy storage after the diode. With a 5 V input voltage and a 300 mV forward voltage there is 4.7 V over the C40 capacitor.

A linear regulator can provide stable 3.3 V output as long as its input voltage is higher than its output voltage plus the regulator's dropout voltage. This means that a regulator with the lowest possible dropout voltage must selected. TPS78633KTTR was selected because it has maximum dropout voltage of 390 mV with 1.5 A output current at room temperature [22]. The dropout voltage changes linearly with the output current from few millivolts to 390 mV. This means that the real dropout voltage is much smaller than 390 mV. It is impossible to accurately know the current draw from the 3.3 V power rail but

according to a very rough estimate it should not be higher than 300 mA. To give some headroom let's say that the current draw is 400 mA. Now since the output current and voltage drop of 1.4 V over the regulator is known, a power loss can be calculated. The power loss is 0.56 W at worst case. TPS78633KTTR was basically the only linear regulator is stock with low dropout voltage and good enough power dissipation. TPS78633KTTR requires minimum of 1 µF input and output capacitor [22]. 10 µF capacitors were selected.

Final component that must be selected is the energy storage capacitor C40. The capacitor should be able to keep its voltage high enough for the regulator to keep stable output voltage for 15 ms. The power management microcontroller can react to power faults in a few milliseconds so the 15 ms of stable power was just chosen arbitrarily to be a long enough time. The time t it takes to discharge charge capacitor with a certain current can be calculated with (18).

$$t = C\frac{\Delta V}{I} \tag{18}$$

where C is the capacitance of the capacitor, ΔV is the maximum change in capacitor voltage, and I is the discharge current.

Capacitance C required to provide certain output current for a given time can be calculated from (18) by solving it for C. This gives (19).

$$C = \frac{tI}{\Delta V} \tag{19}$$

In this case the length of time t the capacitor must be able to provide the estimated maximum current $I = 400\ mA$ is 15 ms. With 400 mA output current the dropout voltage for the linear regulator is roughly 100 mV [22]. This means that the minimum input voltage for the linear regulator is 3.4 V which is the dropout voltage added to the output voltage. Maximum input voltage is the 5 V input minus 300 mV forward voltage of the Schottky diode. This means that the usable voltage range of the capacitor is from 4.7 V to 3.4 V. This gives ΔV of 1.3 V. Using aforementioned values in (19) the required capacitance C can be calculated which is $C = 4615\ \mu F$. Closest capacitor value available 4700 μF. But to give some wiggle room a larger capacitor with capacitance of 5600 μF was selected. This was the largest capacitor readily available in the same package as 4700 μF capacitors. This capacitor should be able to provide the required current for 18.2 ms.

6.8.2 Ballast core and IO power rails

As mentioned in Chapter 5.2 same buck converter was selected for both the 1.8 V IO and 0.9 V core power rails. This simplifies bill of materials as there are fewer different components and makes design process simpler since same buck converter design can be used for both power rails by just changing few passive components.

Biggest contributing factors for selecting LM20125MH buck converter were availability, voltage range, output current and package. Minimum output voltage for LM20125MH is 0.8 V, it can output 5 A of current, features HTSSOP-16 package with visible leads and most importantly it is readily available. Schematic for the 1.8 V IO and 0.9 V core power rail buck converters are shown in Figure 25.

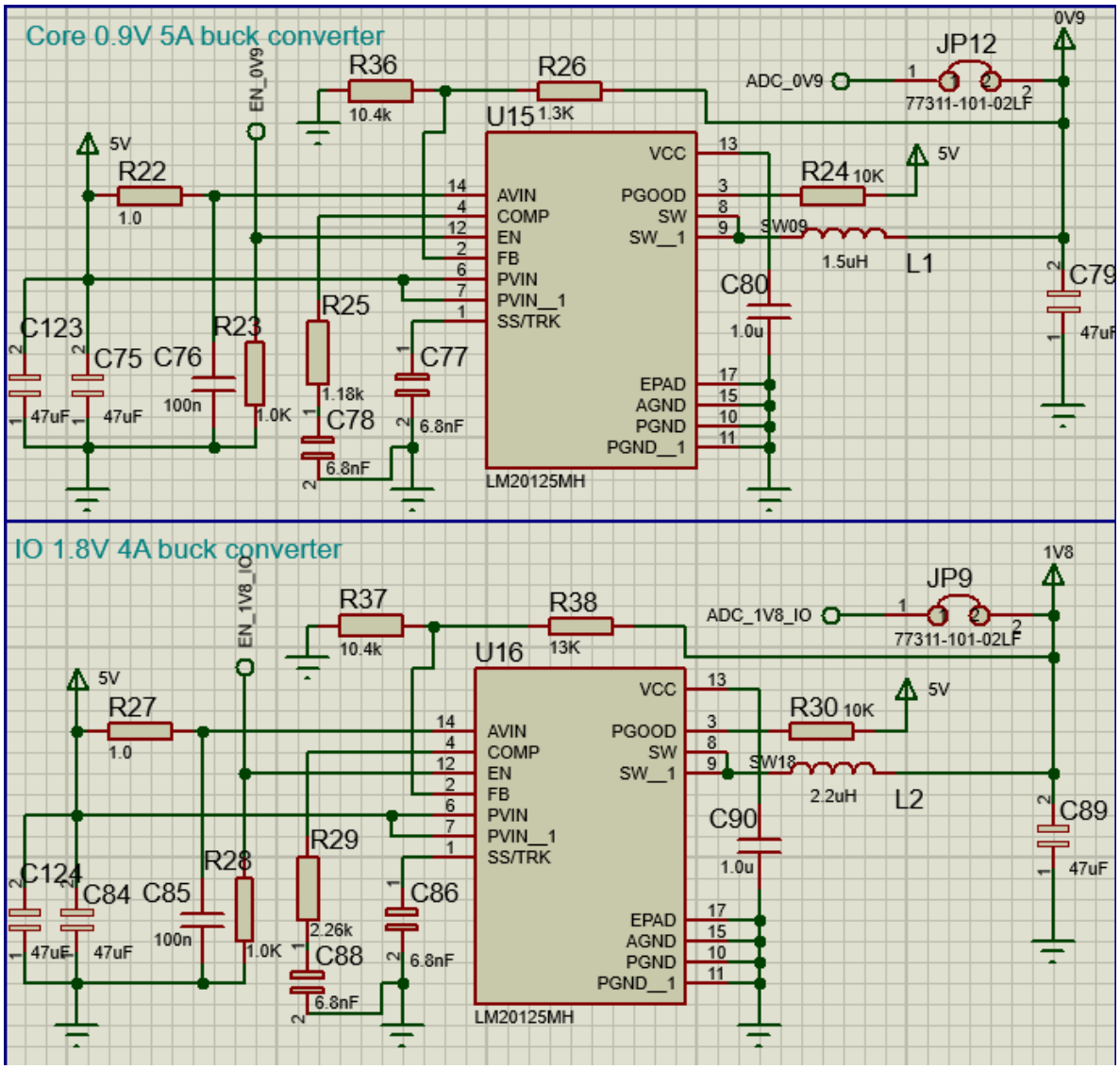


Figure 25. *0.9 V and 1.8 V power rail schematic*

To start selecting the required external components for the buck converters the duty cycle of the converters must be known. The duty cycle D of a converter can be approximated with (20). [18]

$$D = \frac{V_{out}}{V_{in}} \tag{20}$$

where V_{out} is the output voltage and V_{in} is the input voltage of the converter. Using (20) the duty cycles for converters are $D_{0.9V} = 0.18$ and $D_{1.8V} = 0.36$.

First external passive component to select for LM20125MH buck converter is the inductor. The minimum required inductor value L_{min} can be calculated using (21). [18]

$$L_{min} = \frac{(V_{in} - V_{out}) \times D}{\Delta i_L \times f_{sw}} \tag{21}$$

where V_{in} is input voltage, V_{out} is output voltage, D is duty cycle, Δi_L is ripple current, and f_{sw} is switching frequency. LM20125MH operates at fixed switching frequency of 500 kHz and ripple current should be less than 30% of the rated output current [18]. Now minimum inductor sizes can be calculated for both buck converters.

$$L_{min0.9V} = \frac{(5V - 0.9V) \times 0.18}{5A \times 0.3 \times 500\,kHz} = 0.984\ \mu H$$

$$L_{min1.8V} = \frac{(5V - 1.8V) \times 0.36}{4A \times 0.3 \times 500\,kHz} = 1.92\ \mu H$$

Those are the minimum values for the inductors so the selected inductors will be larger in value. For the 0.9 V buck converter a 1.5 µH inductor was selected and for the 1.8 V buck converter 2.2 µH inductor was selected.

Input capacitor is used to limit ripple in input voltage and supply current during on-time of the converter. The datasheet for LM20125MH recommends at least 22 µF ceramic capacitor with X5R or X7R dielectric. These types of capacitors provide better performance over larger temperature range and minimize the DC voltage derating. [18] For both buck converters two 47 µF ceramic capacitors were selected. Bigger capacitors than the recommended minimum were selected so that input voltage ripple is limited even under high current draw. For output capacitor the same 47 µF ceramic capacitor was selected. Ceramic capacitors low ESR reduces output ripple and noise spikes.

Output voltage of the LM20125MH is set using two resistors. This is a basic resistor division setup consisting of two resistors R_{FB1} and R_{FB2}. Where R_{FB1} connects to the output of the converter and feedback voltage is read from between the R_{FB1} and R_{FB2} resistor. R_{FB2} should be between 4.99 kΩ and 49.9 kΩ. When R_{FB2} is selected R_{FB1} can be calculated to achieve wanted output voltage using (22). [18]

$$R_{FB1} = \left(\frac{V_{out}}{0.8} - 1\right) \times R_{FB2} \quad (22)$$

For both 0.9 V and 1.8 V buck converter the R_{FB2} was selected to be 10.4 kΩ. Now R_{FB1} resistor values can be calculated for both converters. For 0.9 V converter R_{FB1} needs to be 1.3 kΩ and for 1.8 V it must be 13.0 kΩ

LM20125MH buck converter provides a pin for loop compensation. This is used to meet static and dynamic requirements while maintaining adequate stability [18]. Loop compensation is done by adding a capacitor and a resistor in series between the compensation pin and ground. The datasheet for LM20125MH provides some pre calculated values for loop compensation but they do not match this application. Calculating those compensation values is a complicated process. Since buck converter theory and optimal design is outside the scope of this thesis, WEBENCH Power Designer online tool by Texas Instrument is used to calculate compensation component values. Compensation values given by the tool are 6.8 nF for the compensation capacitor for both converters and 1.18 kΩ for 0.9 V converters compensation resistor and 2.26 kΩ for 1.8 V converters compensation resistor.

The start-up time of the converters can be set using a single capacitor. The value of the soft start capacitor C_{ss} can be calculated using (23). [18]

$$C_{SS} = \frac{t_{ss} \times I_{ss}}{0.8V} \quad (23)$$

Where t_{ss} is the desired start-up time and I_{ss} is the 5 µA soft start pin current. Solving (23) for 1 ms start-up time gives capacitor C_{ss} size of 6.25 nF. This is close in value to the compensation capacitor so to reduce the amount different components a 6.8 nF capacitor can be used for soft start. This capacitor gives a star-up time of 1.088 ms.

Last external components needed by the buck converters are filtering components to AVIN pin and bypass capacitor to VCC pin. AVIN pin is filtered with a 1 Ω resistor and 100 nF capacitor. A 1 µF capacitor is used to bypass VCC pin. All of those components were selected according to the recommended values.

6.8.3 PLL power rail

Linear regulator chosen for the 1.8 V PLL power rail was ADM7155ARDZ. It is an ultra-low noise linear regulator, so it is ideal for generating power for the PLL because low noise is required for ideal operation. Schematic around ADM7155ARDZ is designed according to recommendations on its datasheet. Schematic for ADM7155ARDZ is shown in Figure 26.

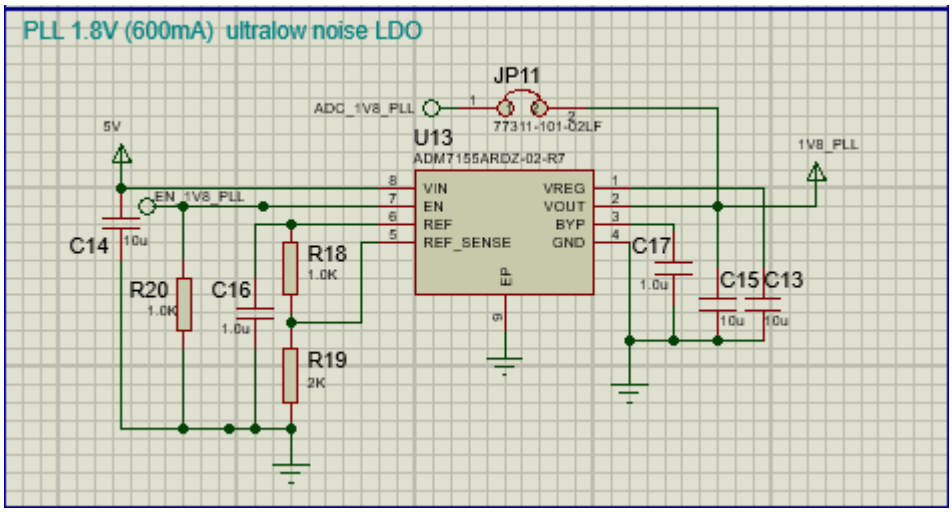


Figure 26. *1.8 V PLL power rail schematic*

Only two things must be configured for this application are the output voltage and soft start time. Output voltage V_{out} can be calculated using (24).

$$V_{out} = 1.2\,V \times (1 + \frac{R_1}{R_2}) \tag{24}$$

where resistors R_1 and R_2 are used to set the output voltage. R_2 must be selected so that it is larger than 1 kΩ to prevent excessive loading of REF pin and it must be smaller than 200 kΩ to minimize errors [19]. Selecting R_2 to be 2 kΩ (23) can be used to calculate value for R_1 so that 1.8 V output voltage is achieved.

$$R_1 = R_2 \times \left(\frac{V_{out}}{1.2\,V} - 1\right) = 2000\,\Omega \times \left(\frac{1.8\,V}{1.2\,V} - 1\right) = 1000\,\Omega$$

Start-up time of the ADM7155ARDZ linear regulator can be configured by a single capacitor attached to the BYP pin. The size of the bypass capacitor C_{BYP} can be calculated using (25) [19].

$$C_{BYP} = \frac{t}{0.0012} \tag{25}$$

where t is the desired start-up time. (25) gives the capacitor size in microfarads. To get a one millisecond start-up time a 0.83 µF bypass capacitor is required. One microfarad capacitors are used multiple times in the schematic so a 1 µF capacitor is used instead 0.83 µF to reduce the number of different components. This capacitor gives start-up time of 1.2 ms.

6.8.4 Power connectors and Ballast decoupling

Final part of the powering page of the schematic is shown in Figure 27 and it is for power input and outputs, connecting power pins of the Ballast, and the bypass capacitors. Left part of the figure is for the Ballasts power connections. Core power pins are connected to the 0.9 V power rail, IO power pins are connected to the 1.8 V power rail, and analog power pins are connected to the 1.8 V PLL power rail.

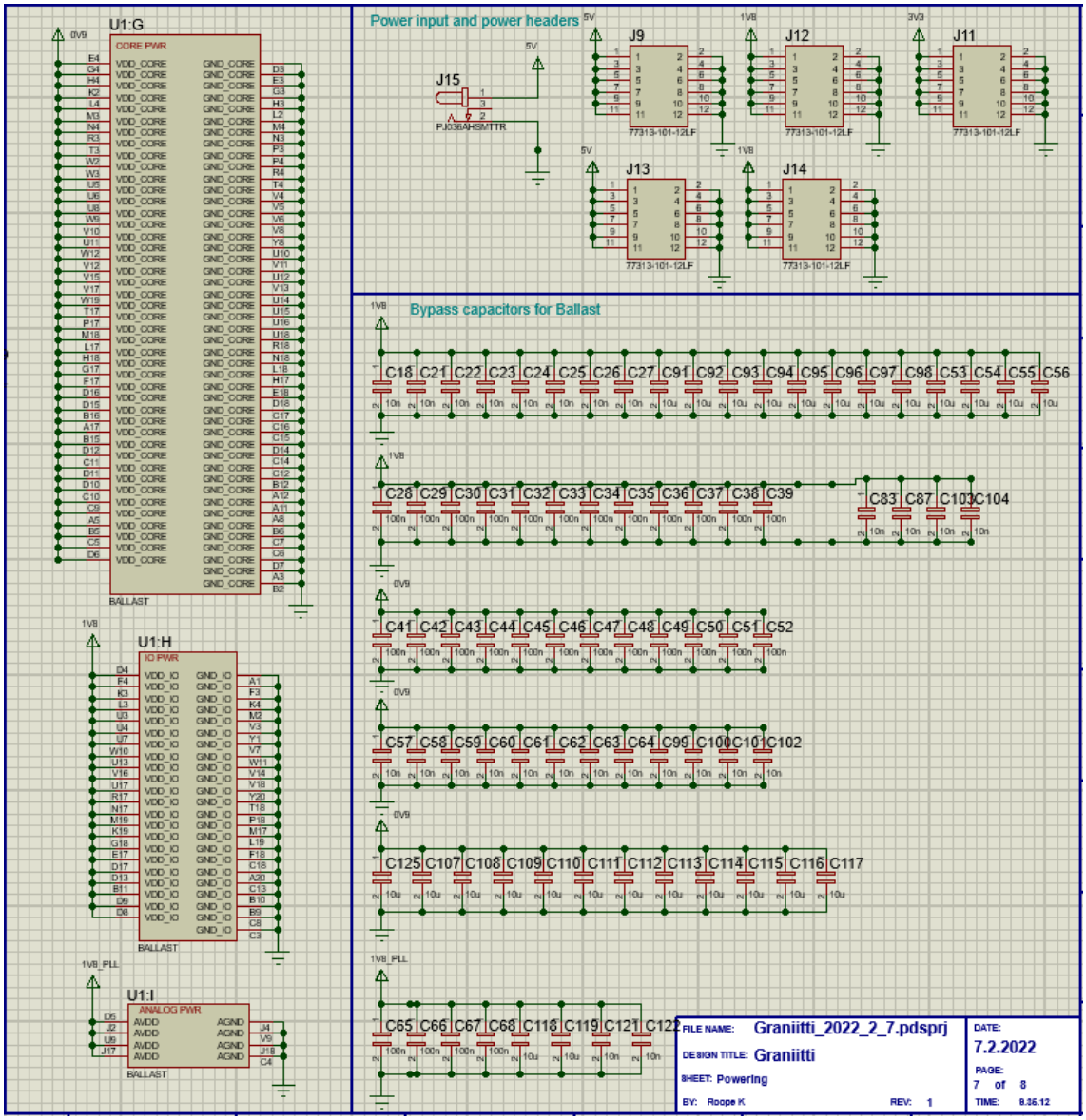


Figure 27. *Graniitti power input and output connectors and Ballast power pins and decoupling.*

Top right of the schematic is for power input and outputs. For a 5 V input a standard 5.5x2.1 mm barrel jack connector is used. There are also five pin headers for the power

output. Two of the headers are for 5 V, two are for 1.8 V, and one header is for 3.3 V. Half of the header's pins are dedicated as ground pins.

Final part of the figure is all of the bypass capacitors for the Ballast. As mentioned in Chapter 3.4, the best bypass capacitor performance can be achieved by using multiple different sized capacitors. Three different capacitor sizes were decided to be used. Those sizes are 10 nF, 100 nF, and 10 µF. 100 nF was selected because it is basically a standard size for bypass capacitor. 10 nF and 10 µF capacitors were selected to give a wider frequency response. 10 nF capacitor gives better high frequency response and 10 µF gives better low frequency response and acts as larger energy storage. A common way to calculate the amount of bypass capacitors is to place one of each capacitor size for each power pin pair. In this case that would result in a such a large number of capacitors that it would be impossible to place all of those close to the power pins. That's why for 0.9 V and 1.8 V power rails twelve of each capacitor is used. For the 1.8 V PLL power rail 100 nF capacitor is placed for each power pin pair and one 10 nF and 10 µF capacitor for the two power pin pairs.

7. GRANIITTI LAYOUT DESIGN

For this application, a four-layer PCB was selected. This allows using one of the internal layers as a ground plane and the other internal layer as power plane while leaving top and bottom layers as signal layers which leads to simpler PCB design. Having the signal traces on the outer layers makes it also easier to debug and make some small changes to the finished PCBs, if necessary. Top layer of the PCB will also be the only layer suitable for defined impedance tracking as only it has a solid ground plane beneath it.

Eurocircuits provide multiple different pools for PCB manufacturing for different applications. There is a standard pool which is good for most applications. There are pools for more defined applications such as defined impedance pool, RF pool, IMS pool, and SEMI-FLEX pool. With the Graniitti PCB the choice is between the standard and defined impedance pool. The defined impedance pool uses different stackup and materials to provide accurately defined impedance for the select traces. Standard pool PCBs can also be used for defined impedance traces, but because of the materials used the impedance of the traces cannot be calculated as accurately. Stackup of standard and defined impedance pool PCBs are shown in Figure 28.

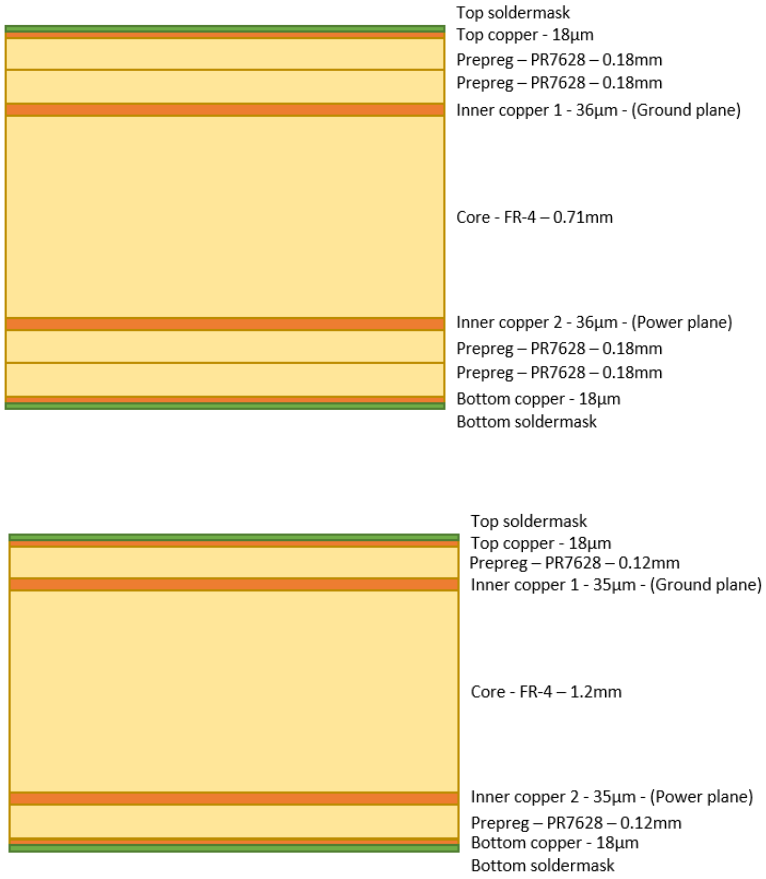


Figure 28. *Standard and defined impedance pool PCB stackups*

Other difference than the material used for the core and prepreg is the stackup. The standard pool uses a stackup with thicker prepreg between outer layers and thinner cores while the impedance pool minimises the distance between outer layers while increasing the thickness of the core.

For standard pool PCBs, Eurocircuits offer two options for the core and prepreg material: NP155F and R1755. Unfortunately, the designer cannot select the material since it is chosen at Eurocircuits discretion. Both of those materials are also used as prepregs with tight weave known as the 7628 weave. For R1755 material the dielectric constant is only available for the laminate, so it is assumed that the dielectric constant of the prepreg is the same. Defined impedance pool uses IS400 material for core and prepreg with tighter 2116 weave. Dielectric constants for the three material options are shown in Table 4.

Table 4. *Dielectric constants for NP155F, R1755, and IS400 FR-4 materials in core and prepreg form*

NP155F (Standard pool)		R1755 (Standard pool)		IS400 (Impedance pool)	
Core	Prepreg (7628)	Core	Prepreg (7628)	Core	Prepreg (2116)
4.3 [28]	4.55 [28]	4.6 [29]	4.6 [29]	4.48 [30]	4.3 [30]

Since the stackups of the PCB options are known the required trace widths for controlled impedance traces can be calculated using (4). The target impedance for the controlled impedance lines is 50 Ω. Let's first calculate the trace width for controlled impedance traces when using the standard pool PCB stackup. Since the material for the standard pool PCB is selected by Eurocircuits and the dielectric constant is only known for NP155F so let's use it when calculating trace width using (4). In this case the isolation height is 0.36 mm, dielectric constant is 4.55, and trace height is 0.018 mm.

$$w = 7.475 \times 0.36\ \text{mm} \times e^{(-50\Omega\sqrt{4.55+1.41})/87} - 1.25 \times\ 0.018\ \text{mm}$$

$$w = 0.639\ mm$$

And the trace width for 50 Ω controlled impedance tracking for the defined impedance pool PCBs is calculated with the same equation. This time the isolation height is 0.12 mm, dielectric constant is 4.3, and trace height is 0.036 mm.

$$w = 7.475 \times 0.12\ \text{mm} \times e^{(-50\Omega\sqrt{4.3+1.41})/87} - 1.25 \times\ 0.036\ \text{mm}$$

$$w = 0.182\ mm$$

Eurocircuits also provides an impedance calculator for calculating the impedance of a trace for defined impedance pool PCBs. The impedance calculator gives the same trace width of 0.182 mm.

The same trace impedance can be achieved using much thinner traces with defined impedance pool PCBs. This is the defining reason why the defined impedance pool PCB stackup was selected because the pitch of the FMC connectors pins is 1 mm. Those would be nearly impossible to route with 0.639 mm traces but easy with 0.182 mm traces. Of course, even with the defined impedance pool the trace impedance will never be exactly 50 Ω. There will always be variance in the impedance caused by the tolerances of the manufacturing process and variables that were not considered in the calculations. In Eurocircuits' experience the real impedance of a PCB is within ±10% of the calculated values [31].

7.1 Manufacturer's capabilities

Eurocircuits' manufacturing capabilities are listed in Table 5. Eurocircuits divides PCBs into classes based on how manufacturable they are. Smaller the minimum size in Table 5 is the harder it is to manufacture which increases price. For that reason, PCBs should not be designed to use the smallest tolerances if possible.

Table 5. *Eurocircuits' capabilities [31]*

Min track width	0.250 mm - 0.090 mm
Min track to track distance	0.25 0mm - 0.090 mm
Min track to pad distance	0.250 mm - 0.090 mm
Min pad to pad distance	0.250 mm - 0.090 mm
Min annular ring	0.200 mm - 0.100 mm
Min inner layer pad isolation	0.275 mm - 0.200 mm
Min plated trough hole size	0.50 mm - 0.10 mm
Min non plated trough hole size	0.60 mm – 0.20 mm
Drill hole to drill hole min distance	0.25 mm
Min copper to board edge distance	Outer layer: 0.25 mm Inner layer: 0.40 mm

These values can be inserted into PCB design programs design rule checking (DRC). The design program prevents from designing a PCB that would break the DRC.

7.2 Layout overview

Goal for The Graniitti PCBs layout is to design a PCB that is ideal for sample testing The Ballast SoCs. This can be achieved by making all signals easily available for the user. The Graniitti PCB is a multilayer PCB with four layers. Top layer is used for mounting most components and routing most signals. Inner layer one, which is directly under top layer, is a dedicated ground layer. Inner layer two is used for multiple power planes. And finally bottom layer is used for routing some signals and bypass capacitors for the Ballast are also placed on the bottom layer. Figure 29 shows the layout of the Graniitti PCB from the top.

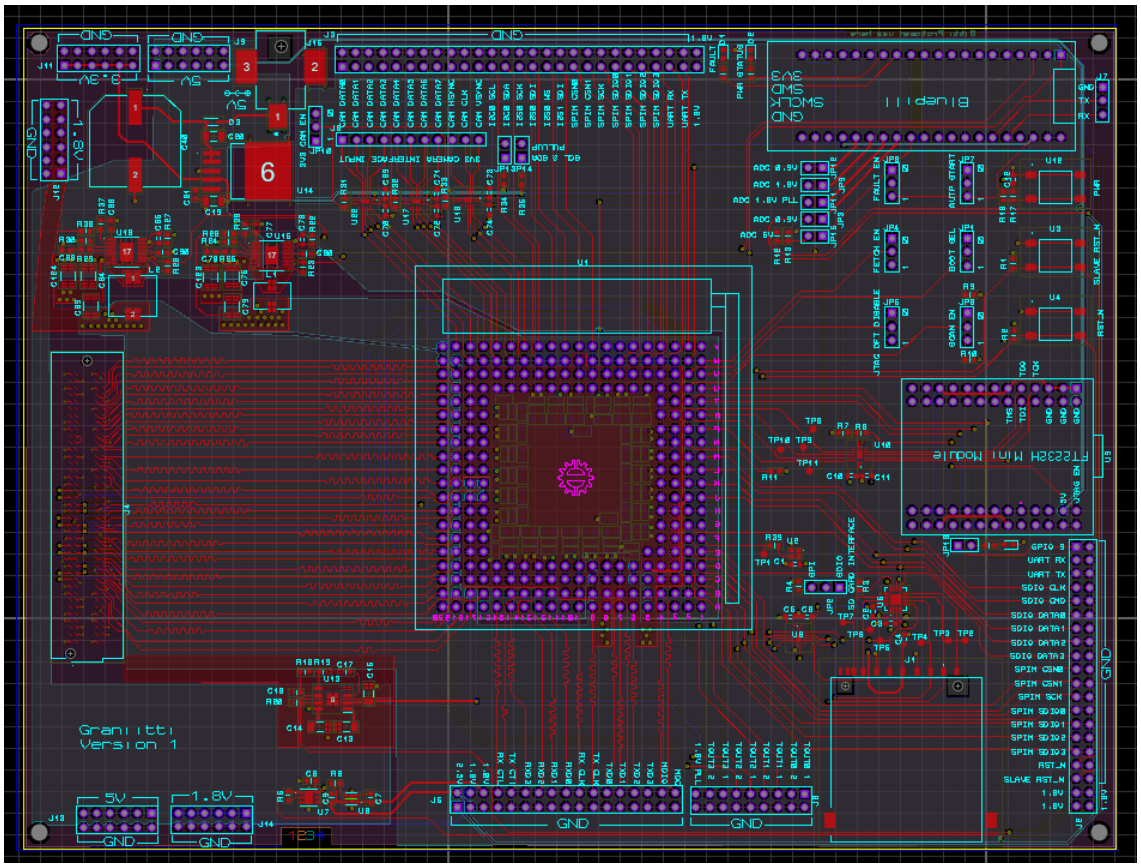


Figure 29. *Graniitti PCB layout*

Centre on the layout design is the ZIF socket for mounting the Ballast SoCs. The Ballast has IO pins on all of its sides so the SoC is mounted on the centre so that all of those signals can be routed easily. As is standard with PCB design, all IO connectors are placed on the edge of the PCB for easy access.

7.3 Top layer layout

As previously noted, the top layer is used to place most components and route most traces. Biggest factor for deciding the top layer layout is the ZIF socket in the centre of the layout. From there IO connectors are placed on the edge of the board so that they are on the side of the PCB that is closest to the pin from which the signal originates. Top layer layout is shown in Figure 30. Traces on the top layer are mostly routed from middle of the board towards edges. This means that traces on top and bottom of the board are routed vertically and on the left and right of the board traces are routed horizontally. On the bottom layer traces are routed in opposite direction. This makes it easy to cross multiple traces.

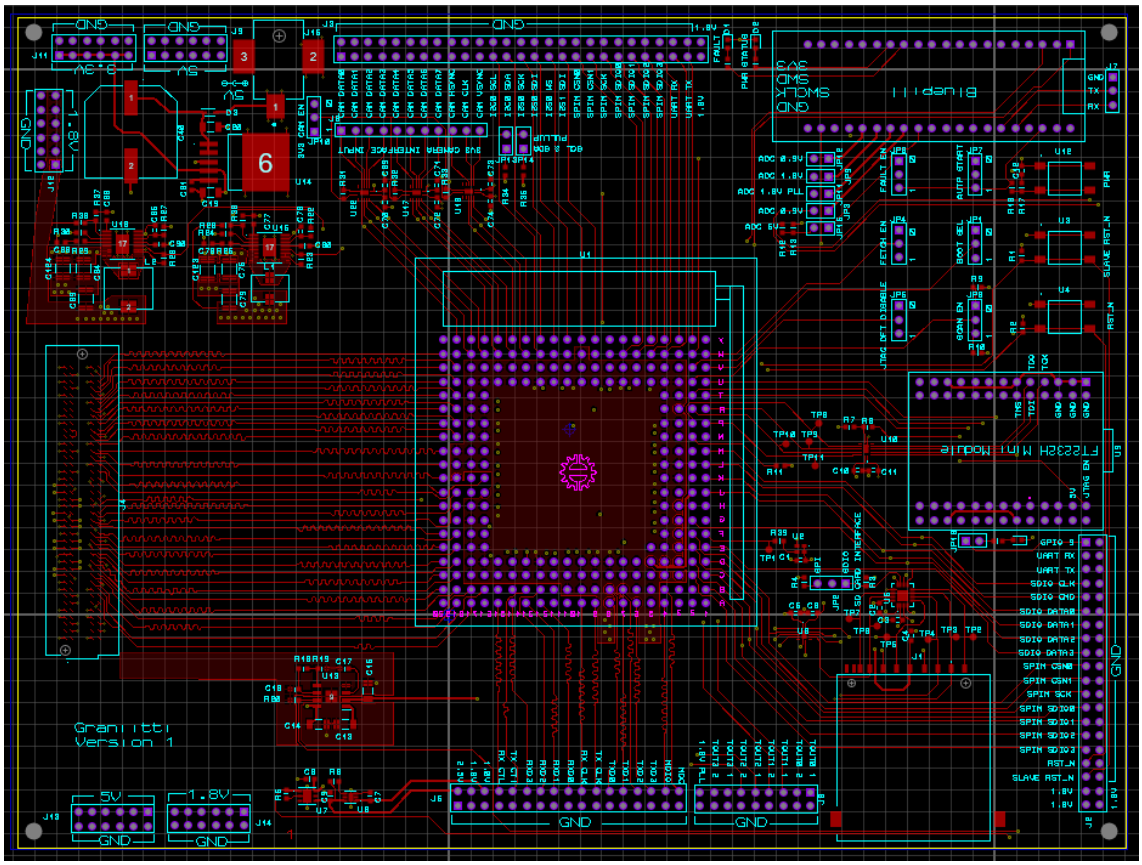


Figure 30. *Graniiti top layer layout*

Right bottom part of the layout is used for SysCtrl subsystems I/O. There is an SD card socket and two level shifters for its I/O interfaces and a jumper to select the active interface. Layout also includes a 40-pin header to which every signal from SysCtrl subsystem is connected to. The design also includes an LED which can be disconnected with a jumper and finally a clock source. The clock source can be disconnected by removing a 0 Ω resistor so an external clock source can be utilized.

Middle right of the PCB is used for the FT2232H USB to JTAG module and a level shifter. This also includes test points on the JTAG signals between the Ballast and the level sifter so that those signals can be easily probed, or the level shifter bypassed. The JTAG module can also be removed and an external JTAG module can be used. For the JTAG signal pins are marked on the silk screen. Pins JTAG EN and 5 V must be also connected together so that level shifter is activated when using external JTAG module.

Top right of the PCB is used mostly for the PCBs user interface and for the Bluepill microcontroller module. Reset and power buttons are placed closest to the edge of the board followed by jumpers further away from the edge. Six of the jumpers that are used to configure settings are spaced further away so that there is enough room to use them easily. Five additional jumpers are used to connect the power rails to the

microcontroller's ADC. These jumpers are mounted close to each other as they are meant to be removed only when assembling the PCBs. The Bluepill microcontroller is mounted near edge of the PCB so that its USB connector can be easily accessed.

Top middle part of the PCB is used for medium performance cores I/O. Each I/O signal is routed to a pin header on the edge of PCB. There are also jumpers for removing pull-up resistors from I^2C lines. CAMIF interfaces also features additional pin header as a 3.3 V input. This pin header is placed close to the other pin header so that the same names on the silk screen can be used for both of the pin headers. Level shifters for the CAMIF are placed close to the 3.3 V pin header. Finally, a jumper is placed next to the 3.3 V pin header which is used to enable the level shifters.

Top left part of the PCB is used for power input and power conversion. 0.9 V and 1.8 V power converters are mounted near the boards power input so that the switching noise from those converters is kept away from rest of the board where there are some noise sensitive parts. A 3.3 V linear regulator is also kept there as it is not noise sensitive and it is logical to keep most power rail components in one place. Edge of the PCB in this area is used for the single power input and multiple different power outputs.

Left middle part of the PCB is used for C2C. There is only one component which is the FMC LPC connector used to connect an external FPGA board. FMC signals should have either 50 Ω impedance for the single ended signals or 100 Ω impedance for the differential signals. In this case only the single ended signals are used. The 50 Ω impedance can be achieved by using the trace width of 0.182 mm. Also, only the top layer is suitable for controlled impedance traces as only it has a full ground plane beneath it. Another layout design consideration with C2C interface is the propagation delays between its signals. Since there are eighteen signals in parallel in both directions it is important that trace lengths are matched between signals. This ensures that all signals are latched correctly, and timing requirements are maintained. PCB design software provides automatic tools to match trace lengths together by using serpentine routing. There is also a ground area beneath the C2C signals on the top layer. This was added later on as the Eurocircuits' automatic checking tools indicated that the copper plating thickness may not be uniform in that area. If there are more copper in some area of the PCB than in others, this may lead to uneven copper thickness. Adding the copper area near the C2C signals made the copper thickness for those signals more even.

Bottom left part of the PCB is used for generating 1.8 V PLL power rail and the Ethernet power rails. 1.8 V PLL power rail linear regulator is placed to the bottom left part so that it is far away from the switching noise generated by the buck converters. 2.5 V and 1.0

V Ethernet power regulators are also placed near so that they are close to the Ethernet IO connector. Ethernet power rails are only used for the external Ethernet PHY and not used anywhere on the Graniitti PCB. Bottom left part of the PCB also has some power headers as there was extra space that was not otherwise utilized.

Bottom middle part of the layout is used for the Ethernet and PLL test outputs. Normally layout design for Ethernet can be divided into two parts: RGMII and connection from Ethernet PHY to RJ45-port. Both of those interfaces have their own requirements that must be considered in the layout design. Since an external PHY is used, only the RGMII signals from the Ballast to the PHY are routed on the Graniitti PCB.

RGMII requires all of the signals to have 50Ω impedance. Same trace width of 0.182 mm can be used as with C2C. In addition to defined impedance, all signals must also be length matched. RGMII standard requires TXC and RXC signals to have a delay of 1.5 to 2.0ns [33]. This is required to ensure that stable data signals are sampled during falling and rising edges. This delay can be made by making the clock traces longer. Luckily the used DP83867PHY supports configurable delay for TXC and RXC signals so there is no need to add additional delay to clock traces [20]. As with highspeed signals, RGMII signals are routed on a single layer and any unnecessary vias or stubs are avoided [33]. The RGMII signals are routed directly from the Ballast to a pin header on a single layer as 50 Ω defined impedance traces with length matching.

Finally, there is a pin header for the PLL test signals. These signals come from each side of the Ballast SoC so for that reason, all of them could not be routed on the top layer.

7.4 Inner layer layouts

The two inner layers are used for ground and power. Inner layer 1, which is under the top layer, is a dedicated ground layer. This makes it possible to route the defined impedance traces on the top layer and a solid plane also increases signal integrity as there are no split planes under any of the top layer traces. Inner layer 1 is show in Figure 31.

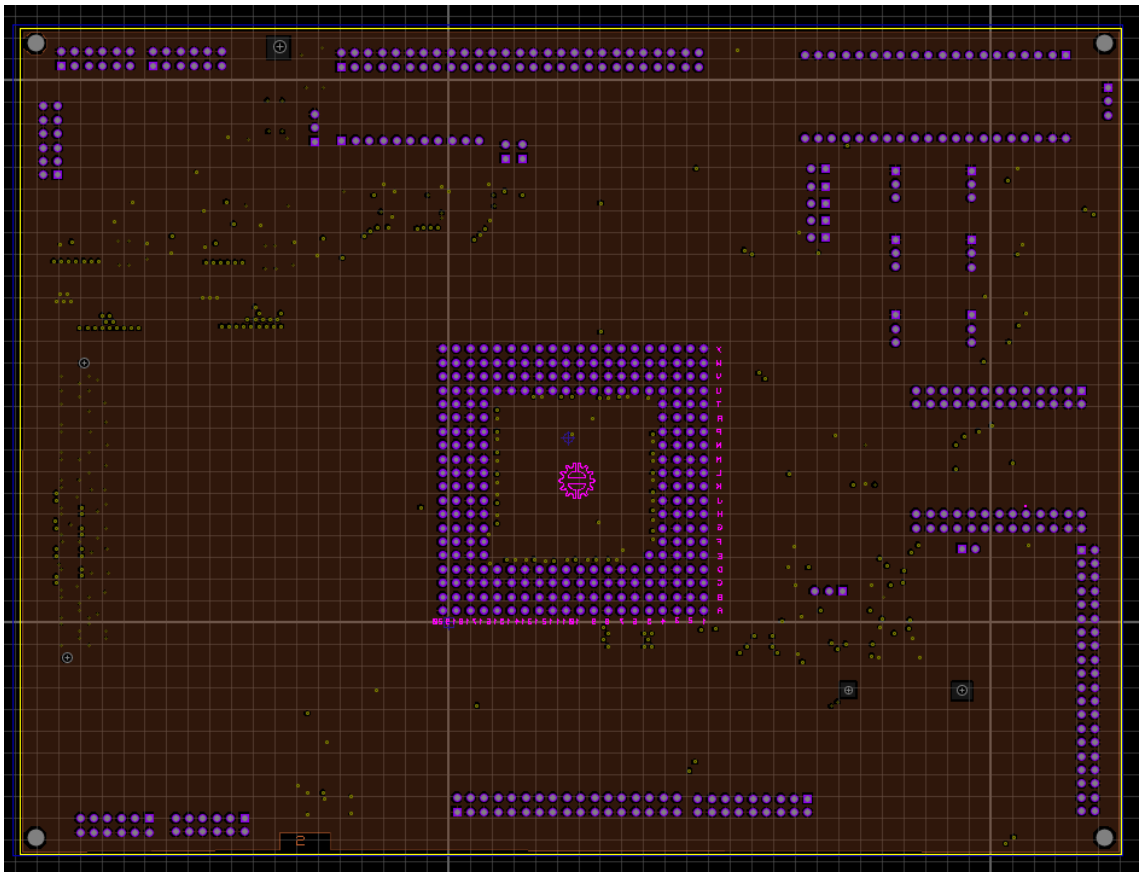


Figure 31. *Graniitti inner layer 1 layout*

Inner layer 2 is used for multiple power planes. There are three different power planes: 5 V, 1.8 V, and 0.9 V. The goal was to have large copper areas for each plane to maximize capacitance between power planes and ground plane. Larger planes also reduce the changes of routing the signals over split planes. Figure 32 shows the inner layer 2.

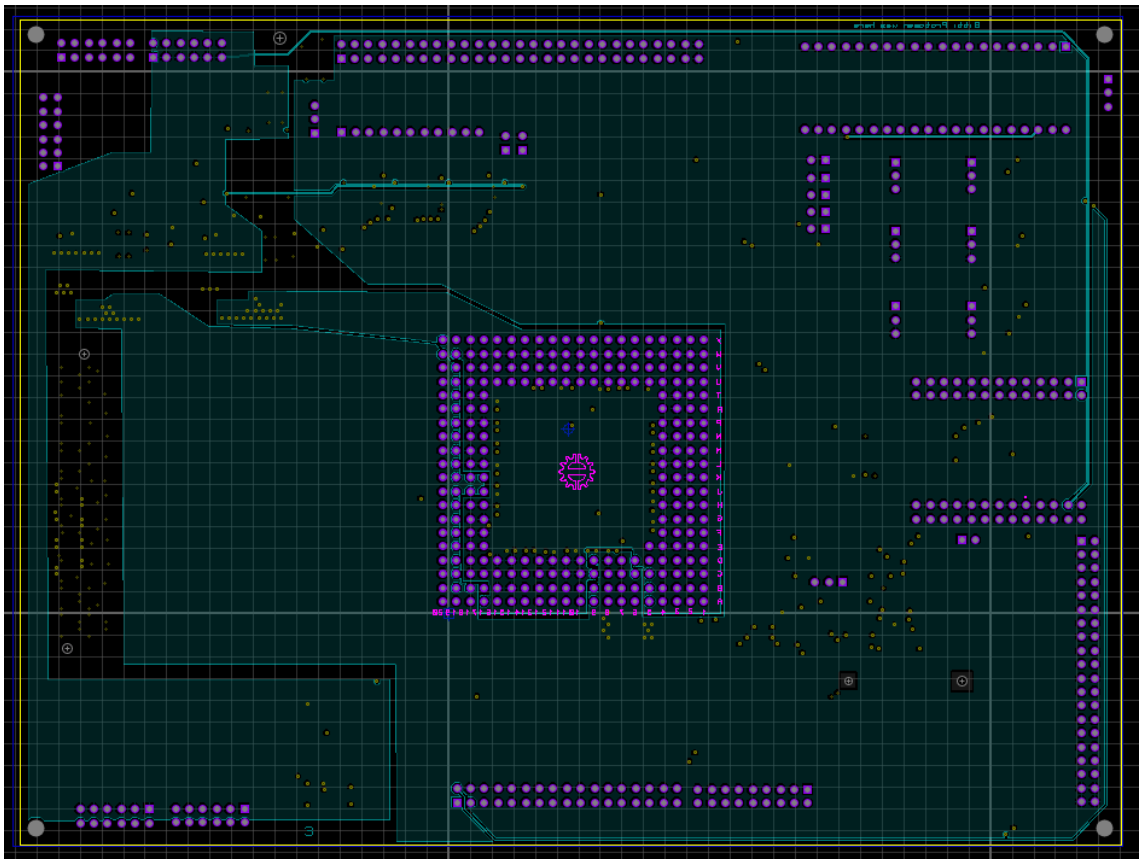


Figure 32. *Graniitti inner layer 2 layout*

Plane on the left part of the layout is for 5 V. It connects the power converters and regulators to the 5 V input. The biggest power plane is for the 1.8 V I/O voltage. It covers largest possible area so that signals that are routed on the bottom layer have to cross as few planes as possible. 1.8 V power plane partially goes under the Ballast SoC where it connects to a copper area on the top layer which connects to the I/O power pins of the Ballast.

Planar capacitances for 1.8 V I/O and 0.9 V power rails can be calculated using (13). There are ground planes on both of the sides of the power planes so the capacitances between each ground plane and power plane have to calculated separately. Area of the 1.8 V I/O power plane is 0.0189 m^2. The distance between the power plane and ground plane on layer 1 is 1.2 mm and dielectric constant is 4.48. The distance between the power plane and ground plane on bottom layer is 0.12 mm and dielectric constant is 4.3. The capacitances for the 1.8 V I/O power plane are

$$C_{L2toL1} = \frac{\varepsilon_0 \varepsilon_r (n-1) A}{d} = \frac{8.854\times10^{-12}\ \mathrm{Fm^{-1}} \times 4.48 \times (2-1) \times 0.0189 m^2}{0.0012 m} = 624.7\ \mathrm{pF}$$

$$C_{L2toB} = \frac{\varepsilon_0 \varepsilon_r (n-1) A}{d} = \frac{8.854\times10^{-12}\ \mathrm{Fm^{-1}} \times 4.3 \times (2-1) \times 0.0189 m^2}{0.00012 m} = 5996.4\ \mathrm{pF}$$

The total planar capacitance for the 1.8 V I/O plane is

$C_{1.8V\ I/O} = C_{L2toL1} + C_{L2toB} = 6621.1\ pF$

Area of the 0.9 V power plane is 0.00186 m^2. The distance between the power plane and ground plane on layer 1 is 1.2 mm and dielectric constant is 4.48. The distance between the power plane and ground plane on bottom layer is 0.12 mm and dielectric constant is 4.3. The capacitances for the 0.9 V I/O power plane are

$C_{L2toL1} = \frac{\varepsilon_0 \varepsilon_r (n-1) A}{d} = \frac{8.854\times10^{-12}\ \mathrm{Fm^{-1}}\times4.48\times(2-1)\times0.00186 m^2}{0.0012 m}$ = 61.5 pF

$C_{L2toB} = \frac{\varepsilon_0 \varepsilon_r (n-1) A}{d} = \frac{8.854\times10^{-12}\ \mathrm{Fm^{-1}}\times4.3\times(2-1)\times0.00186 m^2}{0.00012 m}$ = 590.1 pF

The total planar capacitance for the 0.9 V plane is

$C_{0.9\,V} = C_{L2toL1} + C_{L2toB} = 651.6\ pF$

7.5 Bottom layer layout

Bottom layer of the Graniitti PCB is used mostly for the Ballast SoCs bypass capacitors and for routing some signals that could not be routed on the top layer. The layout of the bottom layer is shown in Figure 33.

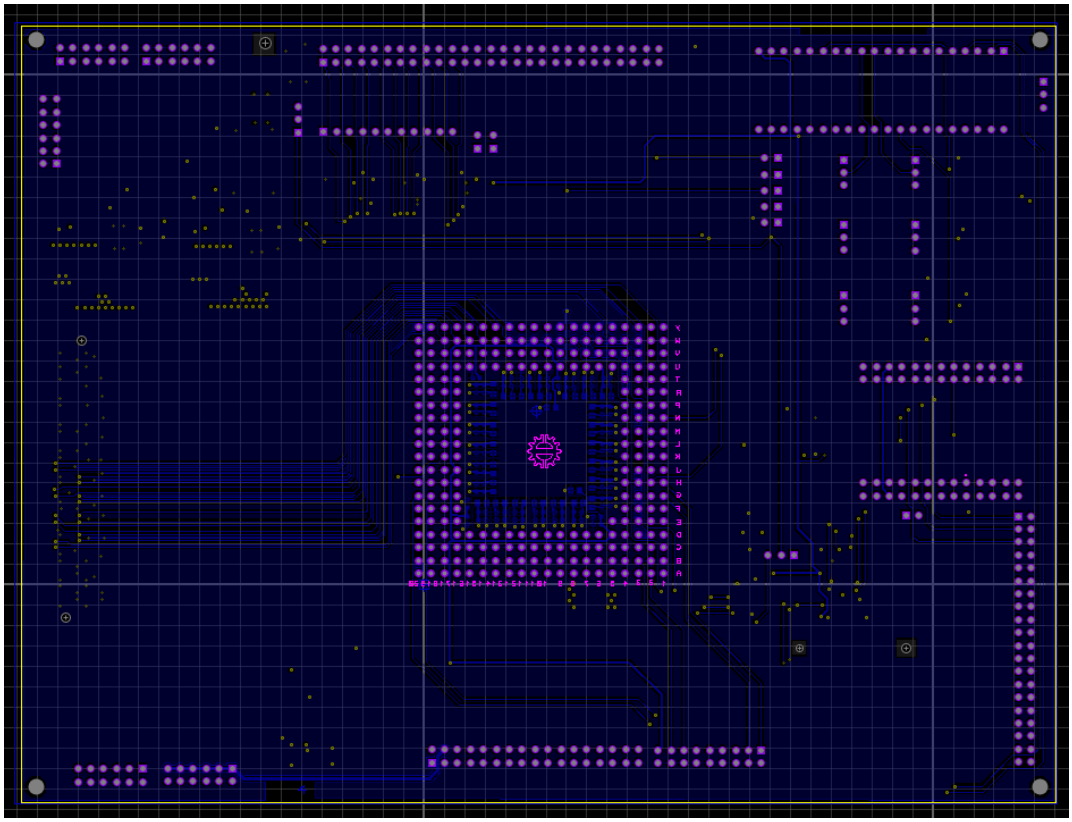


Figure 33. *Graniitti bottom layer layout*

The traces on the bottom layer are mostly routed in the opposite direction as the traces on the top layer. The traces on the top and bottom of the layer go from side to side and

traces on the sides go from top to bottom. This makes it easy to route traces that must cross each other. Exception to this rule are scan-signals that go from the Ballast to the FCM connector. They are routed fully on the bottom layer because they cannot be routed on the top layer as the C2C signals take too much space on the top layer.

Finally, there are the bypass capacitors for the ballast SoC. Those are placed in the middle of the PCB. Most of the Ballast SoCs power pins are on the two inside pin circles of the component. For that reason, the bypass capacitors are placed on the inside of the SoCs pin circles so that they are as close as possible to the power pins. The bypass capacitors are divided into a group of three capacitors. The groups consist of a 10 nF, 100 nF, and a 10 uF capacitor. Within a capacitor group the capacitor are ordered so that the 10 nF capacitor is closest to the power pins and the 10 uF capacitor is furthest.

Finally, there is a ground plane on the bottom layer. The plan was not to have a ground plane there, but it was added later on. Eurocircuits' analysis tools indicated that there would be uneven copper thickness on the bottom layer since some areas have more copper and some less. This was fixed by adding the ground plane so that there is an even copper thickness everywhere on the bottom layer.

8. PCB ASSEMBLY AND TESTING

As mentioned before the Graniitti PCBs were ordered from Eurocircuits and they are manufactured using Eurocircuits' defined impedance pool. The assembly of the PCBs was also bought from Eurocircuits. In this process the components are placed and soldered on to the bare PCBs. The manufacturing and assembly process of the PCBs takes two weeks. Some components are not assembled in the factory but are soldered by hand after the PCBs have been received.

Components that need to be soldered by hand include the ZIF socket for the Ballast SoC and the pin headers for the Bluepill microcontroller and FT2232 module. The lead time for the ZIF sockets is so long that the PCB assembly would have had to wait for it for an unreasonably long time so, it was decided to hand solder the sockets. The pin headers for Bluepill and FT22332 were chosen to be hand soldered as it was not possible to make a single component in schematic that would map into two different components in layout. So, it was easiest to just hand solder those four pin headers. Fully assembled Graniitti PCB is shown in Figure 34.

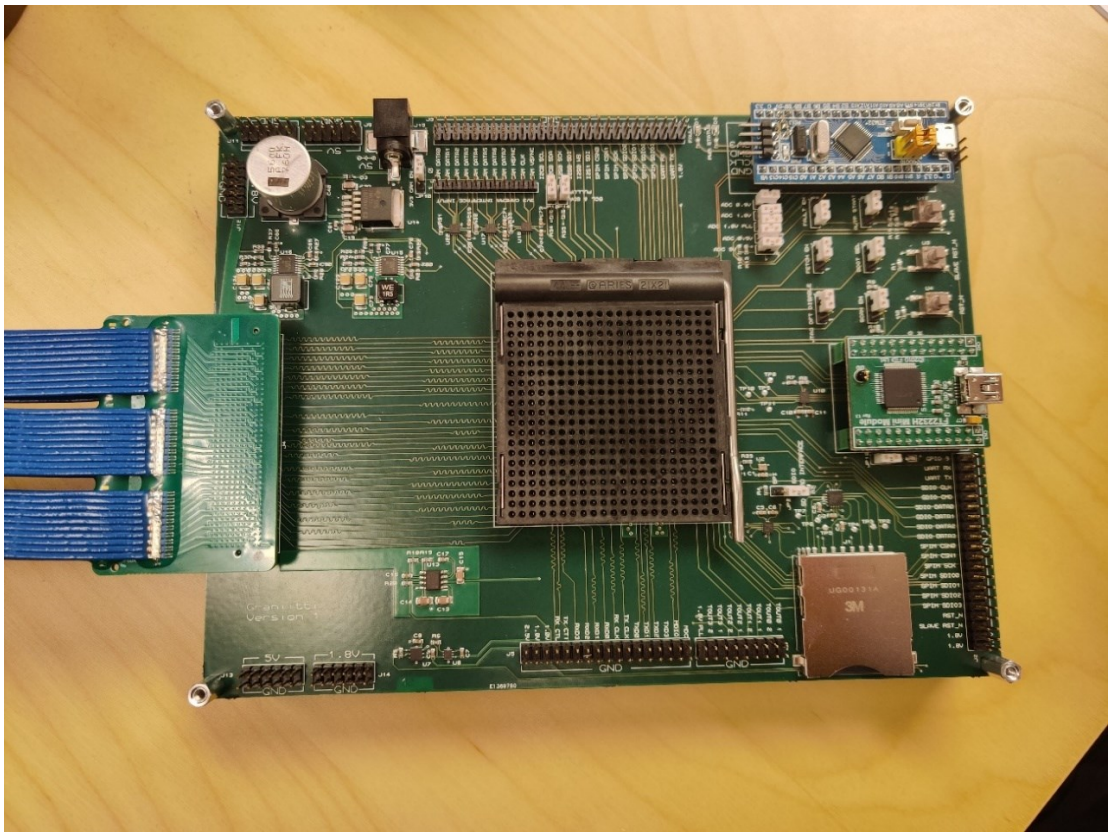


Figure 34. *Fully assembled Graniitti PCB*

8.1 Assembly and testing

The PCBs were received roughly three weeks after their production started. When the PCBs arrived from the factory, they were first visually checked that all components that were supposed to be assembled were assembled on the PCB. One fault was found which was caused by a design error. During the design, a small error was made when selecting LED D2. The selected LED was meant to be mounted on its side instead of on its bottom like most LEDs. The LED still works correctly but it does look a bit out of place on its side. Close up of the LED is shown in Figure 35.

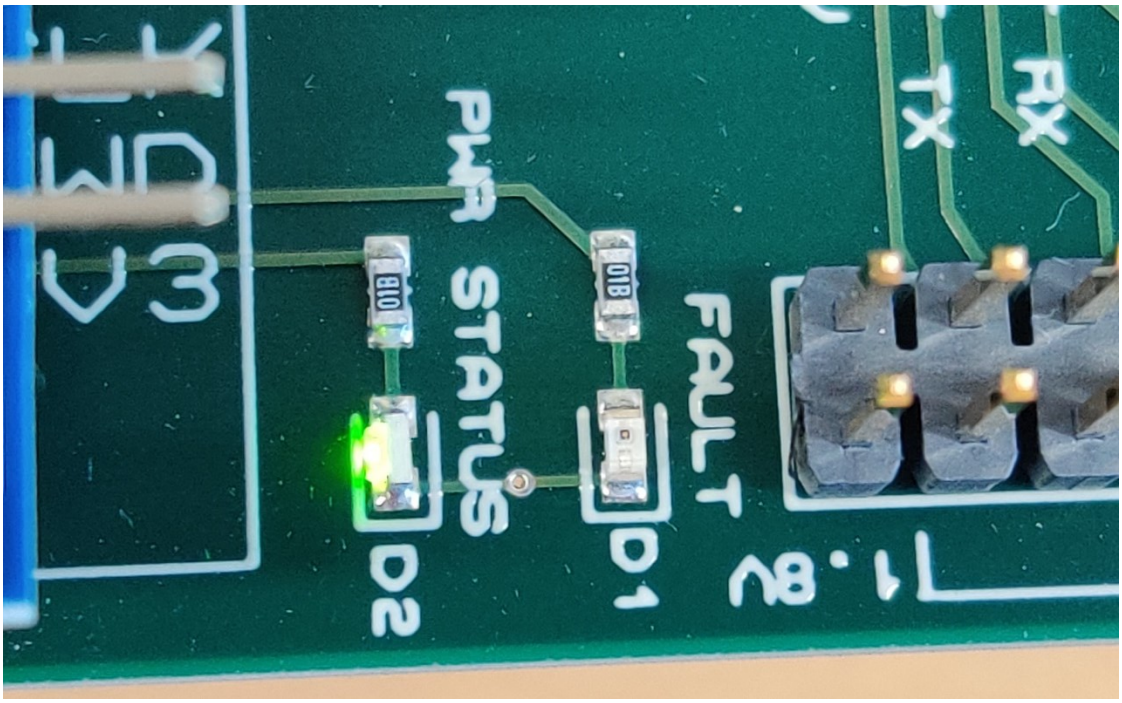


Figure 35. *LED D2 mounted on its side*

Next the power rails were checked for short circuits. Since there were no obvious design or manufacturing faults the board could be powered for the first time. For the first time powering the board was powered from a lab power supply with current limit set to low. This prevents any unknown faults from drawing too much current and causing damage to the board or to the components. After the successful first powering the power rails were measured. As it was supposed to be, only the 3.3 V power rail was enabled, and all other power rails were disabled by default.

Since the 3.3 V functioned correctly the Bluepill microcontroller could be attached next, but the microcontroller required some modifications before it could be used. The Bluepill is powered directly from the Graniitti PCB's 3.3 V power rail. This means that it cannot be powered from other sources at the same time. It can be connected to a computer through an USB cable which carries 5 V power. This 5 V power is stepped down on the board by a 3.3 V LDO. There can be a small voltage difference between the Graniitti PCB's and the Bluepill boards 3.3 V power rails which can lead to a destruction of either LDO. To prevent this the LDO from every Bluepill was removed. This prevents the Bluepill from being powered through the USB cable and it is only powered by the Graniitti PCB. Once the Bluepills were modified they could be attached to the Graniitti PCBs with their pin headers. Next, the Bluepill were programmed. This was done using a ST-LINK/V2 programmer and STM32CubeIDE software. After this, the Bluepill ADC inputs were calibrated. This is done by powering the Graniitti board with 5 V input voltage and attaching a USB cable from computer to the Bluepill on the Graniitti PCB. Computer will

assign a COM port number randomly for the Bluepill so device manager must be used to find out the assigned port number. Once the port number is known a serial terminal program such as PuTTY can be used to connect to it. The Bluepill supports multiple baud rates so pretty much any speed can be selected. A common option is 115200 bit/s. Removing jumper JP12 makes it possible to feed outside voltage to the Bluepill for calibration. Variable power supply is attached to one of the pins in jumper JP12. First a 500 mV voltage is fed to the Bluepill and serial terminal is used to tell the voltage of the input signal. Then the input voltage was increased to 3000 mV and once again the serial terminal is used to tell the voltage of the input signal. After the microcontroller calibration, further tests could be conducted.

For the first full power-up, current limited lab power supply was used, and the state of the power rails was monitored with the serial terminal. During and after the power up there were no faults, and the power rails reached their target voltages according to the serial terminal. Next, the power rail voltages were also measured with a multimeter. Multimeter confirmed that the power rails reached their target voltages accurately and that the microcontroller also reads the voltages with a few millivolts' accuracy. Since the power rails and voltage monitoring worked, the next test was to see if the fault monitoring works correctly. This was done by shorting each power rail to ground and seeing if the fault LED starts to blink and all power rails are shutdown. All power rails were tested individually and the Bluepill microcontroller identified and responded correctly to a fault every time. Since at this point it was known that the power rails and their monitoring works correctly, further test could be conducted.

Further tests included the testing of power sequencing, level shifters, and the clock. Power sequencing was tested by measuring sequenced power rails with an oscilloscope and seeing if the sequencing matches the one set in software. At this point on bug was identified. Power rail sequence did not match the sequence indicated in the serial terminal. This was caused by the sequencing values being printed in the opposite order. This was fixed quickly and then the power rail sequencing matched the one indicated by the serial terminal. Level shifters were tested by powering the board up and feeding a signal to a level shifter and measuring an output signal from the other side. Most level shifter are unidirectional, so it was enough to test them one way. The level shifter for SDIO interface is bidirectional so for that all the signals had to be measured both ways. Finally, the 30 MHz clock oscillators frequency was measured with an oscilloscope, and it was correct. These tests were enough to conclude that the Graniitti PCBs work correctly.

The only thing missing from the Graniitti PCBs at this point were the ZIF sockets. After a few weeks of waiting the ZIF sockets arrived. The Ballast SoC has pins in a 20 by 20 array with only four outer most circles having pins. The ZIF socket that arrived had an array of 21 by 21 holes. The socket is shown in Figure 36.

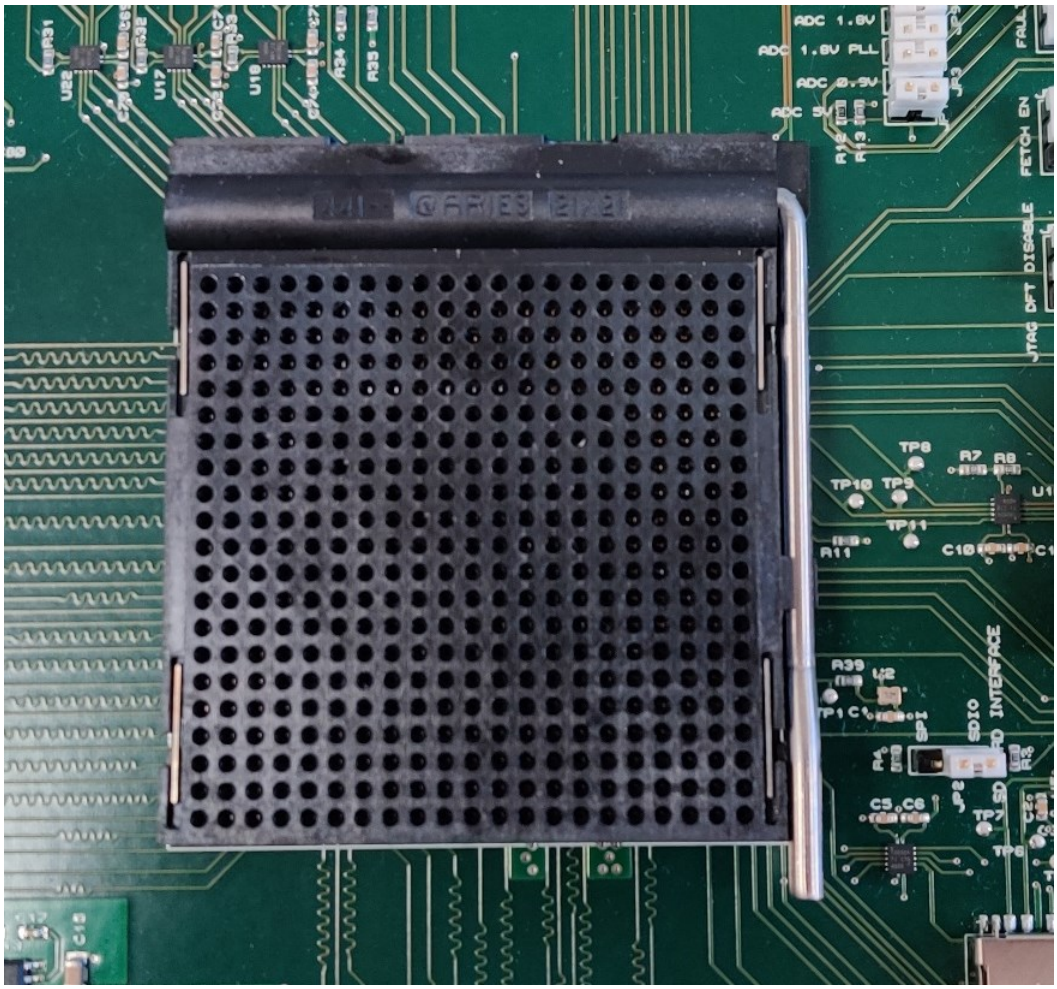


Figure 36. *Close-up of the ZIF socket*

Even though there are too many holes in the socket, only the correct holes are populated by pins so it can be used, but there is a chance that the Ballast SoC can be inserted incorrectly into the socket. This can be prevented by plugging some of the extra holes. At first only one ZIF socket was soldered into one of the boards. If the PCB and the SoC both work correctly, rest of the sockets can be soldered. Lead time for a new PCB is much shorter than for a socket so it is best to only use those sockets if the PCBs work correctly.

Ballast SoCs arrived roughly two months after the ZIF sockets. Before the SoCs could be mounted on the Graniitti PCBs some checks had to made. The point of these tests was to make sure that there were no clear manufacturing errors in the Ballast SoCs. The first test was to make sure that there are no short circuits in the power rails of Ballast.

This was done by checking the continuity of between ground and power pins with a multimeter. There was no short circuit between the I/O and the PLL power rails and ground but when measuring between core power and ground the multimeter beeped to indicate a short circuit. This would have been catastrophic as a short circuit in the core power would prevent the chip from working. Thankfully this was just a user error since the multimeter beeps for any value under 100 Ω. There was roughly 30 Ω resistance between the core power and ground. Since there were no short circuits in the power rails the final check to do was to verify the orientation of the chip inside the package. This was done by finding two pins that are connected together on a one side of the package but not on the other sides. Those two pins were connected together only on the correct side of the package so the ship inside the package should be mounted in correct orientation. After the Graniitti PCB and Ballast SoC had been individually verified the last step was to finally attach the Ballast to the Graniitti. Ballast mounted on Graniitti is shown in Figure 37.

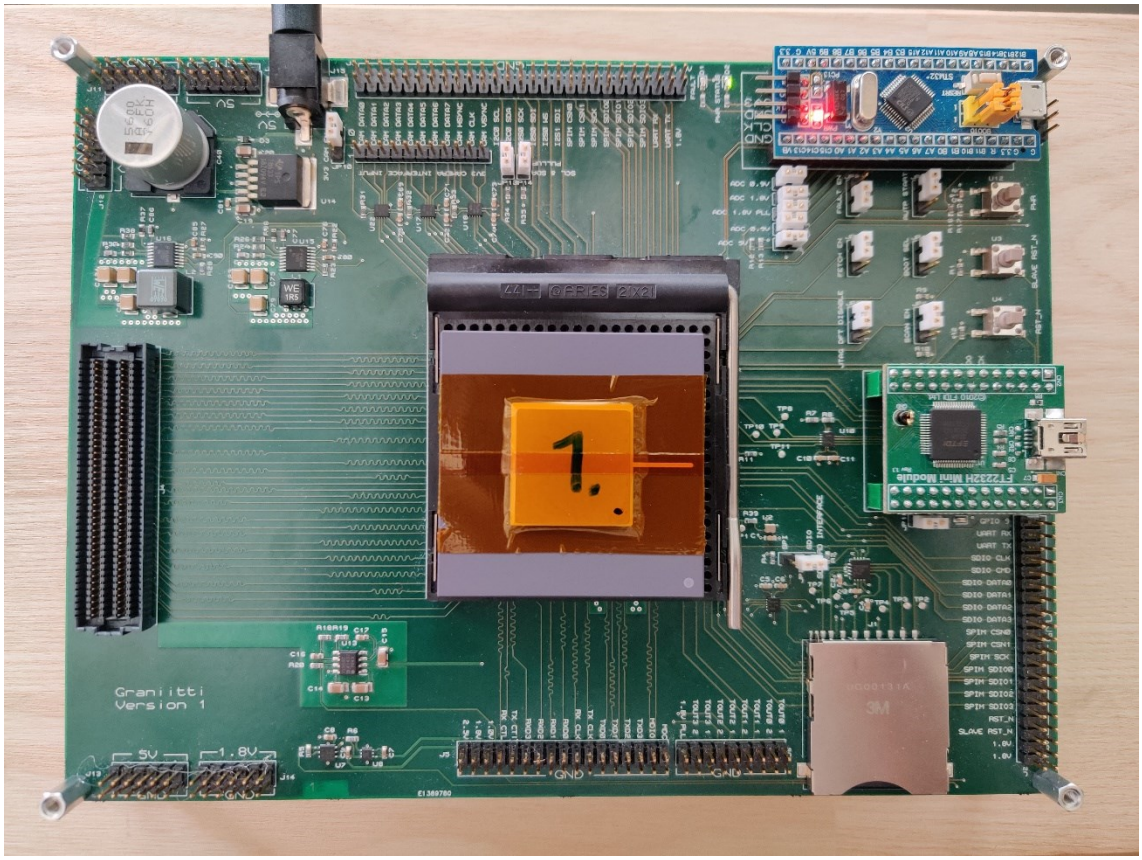


Figure 37. *Ballast SoC mouted on Graniitti PCB*

The corner pins of Ballast have standoffs so that the package doesn't go fully into the socket. This was a surprise, but the pins still go in enough to contact the socket. Once the Ballast was mounted it was time to turn on the power for the first time with Ballast.

The green LED on Graniitti turned on indicating that the power rails had been powered on successfully.

Ballast SoC testing on the Graniitti PCB has identified on0e flaw in the design. For some the Ballast SoC does not read the boot correctly from the SD card when using the SDIO interface. The SDIO signals looked correct when they were probed using an oscilloscope. When the CMD signal of the SDIO interface was probed the Ballast suddenly booted correctly from the SD card. The CMD signal could be probed from either side of the SD card interfaces level shifter and the Ballast would still boot correctly. Since the probe of the oscilloscope fixes the problem, it is impossible to measure the incorrect SDIO signals and find the reason for the incorrect operation with the tools available for testing. The oscilloscopes probe introduces 13 pF of capacitance to the circuit that is probed. That means that the CMD line requires a small capacitive load to function correctly. The SDIO boot problem could be fixed by adding a small capacitor to CMD signals. The capacitance of the added capacitor depends on which Graniitti PCB was used, but most commonly a 6.8 pF capacitor was enough to fix the problem. The root cause for the SDIO boot problems stays uncertain since according to the level shifter and SD card documentation the SDIO should not need any additional capacitance.

With the SDIO boot working the Ballast SoC testing can be continued further. Ballast testing is a long process and might bring out more unnoticed faults with Graniitti but during the thesis, no other faults have been found.

8.2 Component sourcing problems

The global chip shortage was the biggest cause of problems during this project. This resulted into having to change some components multiple times and for some components even their replacement options were totally unavailable.

Since the design process took such a long time for the Graniitti PCB, many components that had been specified in the schematic design phase had totally run out when the layout design phase had been reached. This in turn meant that a lot of time had to be spent looking for new components that full filled the set requirements and were readily enough available so that they would still be available when the PCB is assembled. In some worst cases some component had to be changed even during and after the layout design phase.

Some components that were changed multiple times were the level shifters and buck converters. Level shifters were chosen in an early state of the schematic design but the ones in a package that were preferred to be used had run out. The same level shifters

were available in a smaller less user-friendly package but they were readily available so those were chosen. For buck converters the situation was awful. Almost everything had run out and the current consumption information of the Ballast SoC was only available late in the design process. This meant that the buck converters were selected just before the manufacturing from the few options that were available.

More advanced ICs were affected the most severely by the chip shortage. The Ethernet PHY, microcontroller, and the USB to JTAG chip had been completely sold out everywhere. For most advanced IC's the approximate factory lead time was almost a year so alternative options were needed. For the microcontroller some different models came back in stock and sold out, but at the time of the design none of them fulfilled all of the requirements. So, for those reason the easiest option was to use those Chinese copies of the Bluepill boards. For the Ethernet PHYs the first plan was to buy them into storage after the severity of the chip shortage was noticed. Unfortunately, the summer holiday season disturbed those plans. After the holiday season most of the PHYs had already run out. Some component resellers still had stock and it was decided to by those ICs at fifteen times their original price. The seller cancelled the transaction and doubled the price of the PHY's. Decision to not partake in that extortion was made and thus those PHYs were not bought. The only option left was to use external Ethernet evaluation modules. The final IC that caused problems was the JTAG to USB IC. Since the IC had been specified in the preliminary documentation for Graniitti PCB, the IC could not be easily replaced with some other IC. So, a ready-made module with the specified IC was used.

The last component that was problematic to acquire was the ZIF socket for the Ballast SoC. The Ballast SoC uses a 20x20 socket with 257 pins. This kind of a socket is rarely used and there are only a few manufactures for such sockets. Because it is such a speciality item it was not stocked by any reputable component distributor. One manufacturer that could be found that manufactures suitable ZIF sockets was Aries Electronics. The factory lead time for those sockets would have been 15 working days which is good because at the time of ordering there was a hurry to get those sockets. Unfortunately, Aries Electronics only offers Free On Board shipping. This means that it is the buyers' responsibility to arrange the sea freight shipping. It would have been such a hassle to arrange shipping from USA to Finland that it was decided to buy those socket from alternative seller. Lead time from reputable component distributors was from 6 to 18 weeks so an alternative seller was needed. A Hongkong based distributor was found that promised to have the required sockets in stock and for a cheaper price. Unfortunately, this seller turned out to be a scammer so new alternative seller had to be

found. A Canadian component distributor Future Electronics was selected as they promised to provide those sockets in a few weeks directly from the manufacturer.

The arrival for the ZIF sockets took longer than estimated. So, some alternative options for attaching the Ballast SoC to the Graniitti PCB was thought of. One option would have been to buy standard PGA sockets instead of the ZIF PGA sockets. Unfortunately, these are also used so rarely used that they are not stocked by any component distributor and have long lead times. The final option would have been to build a socket for the Ballast SoC from multiple female pin headers. This would have been a bad option as it would have required a large force to insert the SoC into the socket and possibly cause damage to the SoC's pins. Luckily the ZIF sockets arrived before the Ballast SoCs so that the Graniitti PCBs were ready to be used for testing when the SoCs arrived.

8.3 Testing conclusion and possible changes

From testing and user feedback it became clear that the power management system could be still improved. It fulfilled all its requirements, but it could be improved further. Most importantly it should be able to measure the currents of each power rail. In addition, it should be able to enable or disable individual power rails and change sequencing from the serial terminal. This extended serial terminal functionality can be added by changing the power management microcontrollers software, but the current measurement would require changes to the hardware.

In addition to the power management the SDIO interface could be improved. With better tools like an active oscilloscope probe the SDIO signals could be measured without loading the signals with a passive probes' higher capacitance. Even if the root cause would not be found it could be mitigated by adding capacitors directly on to the PCB. Another option would be to use a different level shifter.

Overall, the Graniitti PCB fulfilled its purpose and made it possible to test the Ballast SoCs. It could be improved by adding the aforementioned changes to the power management but as the most desirable change, current measurement, would require changes to the PCB, it was decided not to do those at this point.

9. CONCLUSION

From the start to testing the Ballast on Graniitti this project lasted year and a half. For the first half a year clear requirements and pinout for the Ballast were not available so Graniitti could only be tentatively designed. Another major hurdle was the global chip shortage. Because of the long design process pretty much each selected IC had to be changed as they would be sold out during the long design phase. This could have been mitigated by buying the required components into storage, but the severity of the chip shortage was not forecasted accordingly. And even buying components in to storage would have not prevented all problems as the power consumption of the Ballast was known very late into the design process, so the used power converters had to be selected from a very limited selection of available converters.

Despite these issues Graniitti PCB was completed on time before the Ballast SoCs. The testing made it clear that the Graniitti PCB could still be improved. Mainly the Graniitti PCBs design could have also been improved by implementing a more advanced power management and fixing the unknown root cause for the SDIO issues. Apart from a few possible changes the Graniitti PCBs work correctly, and they can be used for their intended purpose of testing the Ballast SoCs. So far, the basic functionality of the Ballast SoC on the Graniitti PCB has been verified.

SOURCES

[1] Altera, High Speed Mezzanine Card (HSMC) Specification, 2009. Available: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ds/hsmc_spec.pdf. Accessed (20.3.2021)

[2] ANSI/VITA 57.1-2008, standard for FPGA Mezzanine Card (FMC), 2008, Paid access.

[3] Xiling, ZCU104 Evaluation Board User Guide, 2018. Available: https://www.xilinx.com/content/dam/xilinx/support/documentation/boards_and_kits/zcu104/ug1267-zcu104-eval-bd.pdf. Accessed (25.3.2021)

[4] A. Bahl, High-Speed PCB Design Guide, 2020. Available: https://s3vi.ndc.nasa.gov/ssri-kb/static/resources/High-Speed%20PCB%20Design%20Guide.pdf. Accessed (5.2.2022)

[5] Brooks D. Signal Integrity Issues and Printed Circuit Board Design. 1st edition, Pearson Publishing, 2003, 403 p.

[6] Brooks D. PCB currents: how they flow, how they react. 1st edition. Pearson Publishing, 2013. 400 p.

[7] Mitzner K. Complete PCB design using OrCad capture and layout. Elsevier Science & Technology, 2007. 529 p.

[8] O'Hara M. EMC at component and PCB level. 1st edition. Oxford; Newnes; 1998. 205 p.

[9] Zhang H, Krooswyk S, Ou Z-YJ. High speed digital design: design of high speed interconnects and signaling. First edition. Waltham, MA: Elsevier; 2015. 268 p.

[10] Schweber B. PMICs and Power-Rail Sequencing: Critical to Reliable System Performance. Available: https://www.mouser.fi/applications/pmics-power-rail-sequencing/. Accessed (15.11.2021)

[11] Enger N. Power Supply Sequencing Simplified, 2016. Available : https://www.analog.com/en/technical-articles/power-supply-sequencing-simplified.html. Accessed (15.11.2021)

[12] Miron R. Managing power sequencing, 2019. Available : https://www.newelectronics.co.uk/content/features/managing-power-sequencing. Accessed (15.11.2021)

[13] Singh S, Simple power-rail sequencing solutions for complex multi-rail systems, 2016. Available: https://www.ti.com/lit/wp/slyy101/slyy101.pdf?ts=1614687668694&ref_url=https%253A%252F%252Fwww.google.com%252F. Accessed (15.11.2021)

[14] Volman S. Latchup. Johm Wiley & Sons, Ltd. 2007. 445 p.

[15] Texas Instruments, How to Design Flexible Processor Power Systems Using PMICs, 2015. Available:

https://www.ti.com/lit/an/slda039b/slda039b.pdf?ts=1610639004108&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS65218D0. Accessed (15.11.2021)

[16] Espritu J. Complex Power-Supply Sequencing Made Easy, 2014. Available : https://www.analog.com/en/analog-dialogue/articles/complex-power-supply-sequencing.html. Accessed (16.11.2021)

[17] Falin F, Pham L. Tips for successful power-up of today's high-performance FPGAs, 2005. Available: https://www.ti.com/lit/an/slyt079/slyt079.pdf?ts=1622018188435. Accessed (16.11.2021)

[18] Texas Instruments, LM20125 datasheet, 2007. Available: https://www.ti.com/lit/ds/symlink/lm20125.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&ts=1652078016759&ref_url=https%253A%252F%252Fwww.mouser.fi%252F, Accessed (20.4.2022)

[19] Analog Devices, AMD7155 datasheet, 2014. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ADM7155.pdf. Accessed (20.4.2022)

[20] Texas Instruments, DP8367E datasheet, 2015. Available : https://www.ti.com/lit/ds/symlink/dp83867e.pdf?ts=1631002772852. Accessed (30.4.2022)

[21] Texas Instruments, TLV757P datasheet, 2017. Available: https://www.ti.com/lit/ds/symlink/tlv757p.pdf?HQS=dis-mous-null-mousermode-dsf-pf-null-wwe&DCM=yes&ref_url=https%3A%2F%2Fwww.mouser.fr%2F&distId=26. Accessed (25.6.2022)

[22] Texas Instruments, TPS786 datasheet, 2002, Available: https://www.ti.com/general/docs/suppproductinfo.tsp?distId=26&gotoUrl=http%3A%2F%2Fwww.ti.com%2Flit%2Fgpn%2Ftps786. Accessed (25.6.2022)

[23] CKS32F103 datasheet. Available: http://wtechk.com/CKS32F103.pdf. Accessed (10.1.2022)

[24] Li D. Understanding and Calibrating the Offset and Gain for ADC Systems. Available: https://training.ti.com/sites/default/files/docs/adcs-understanding-and-calibrating-the-offset-and-gain-for-adc-systems-presentation-quiz.pdf. Accessed (25.6.2022)

[25] STMicroelectronics, STM32Cube™ USB device library user manual, 2014. Available: https://www.st.com/resource/en/user_manual/um1734-stm32cube-usb-device-library-stmicroelectronics.pdf. Accessed (25.6.2022)

[26] Texas Instruments, TXS0206-29 Datasheet, 2009. Available: https://www.ti.com/lit/ds/symlink/txs0206-29.pdf?ts=1629456902129&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTXS0206-29. Accessed (25.6.2022)

[27] Texas Instruments, DP83867ERGZ EVM User's Guide, 2015. Available : https://www.ti.com/lit/ug/snlu190/snlu190.pdf?ts=1629803364346. Accessed (25.3.2022)

[28] Technolam, NP-155F datasheet, 2019. Available: https://www.technolam.de/fileadmin/user_upload/pdf/produkt_datenblaetter/np/NP-155FTL_NP-155FR_NP-155FB.pdf. Accessed (25.5.2022)

[29] Panasonic Corporation, R1775M datasheet, 2015. Available http://www.eurocircuits.com/wp-content/uploads/R1755M-emscatalog_1511_hiperm.pdf. Accessed (25.5.2022)

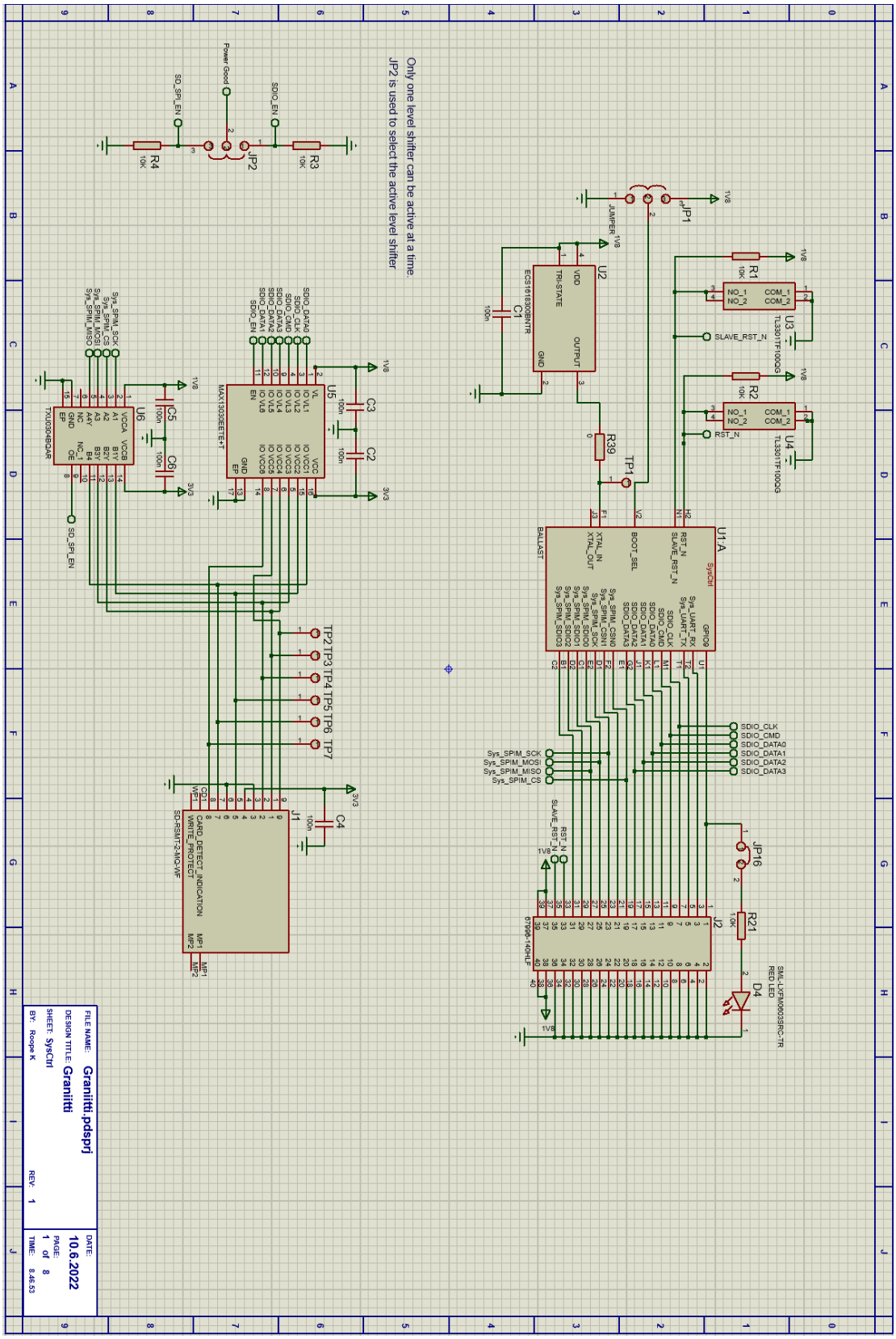
[30] Isola, IS400 datasheet, 2018. Available : https://tspcb.pl/web/uploads/files/materials/Isola_IS400__Dk_Df_Tables.pdf. Accessed (25.5.2022)

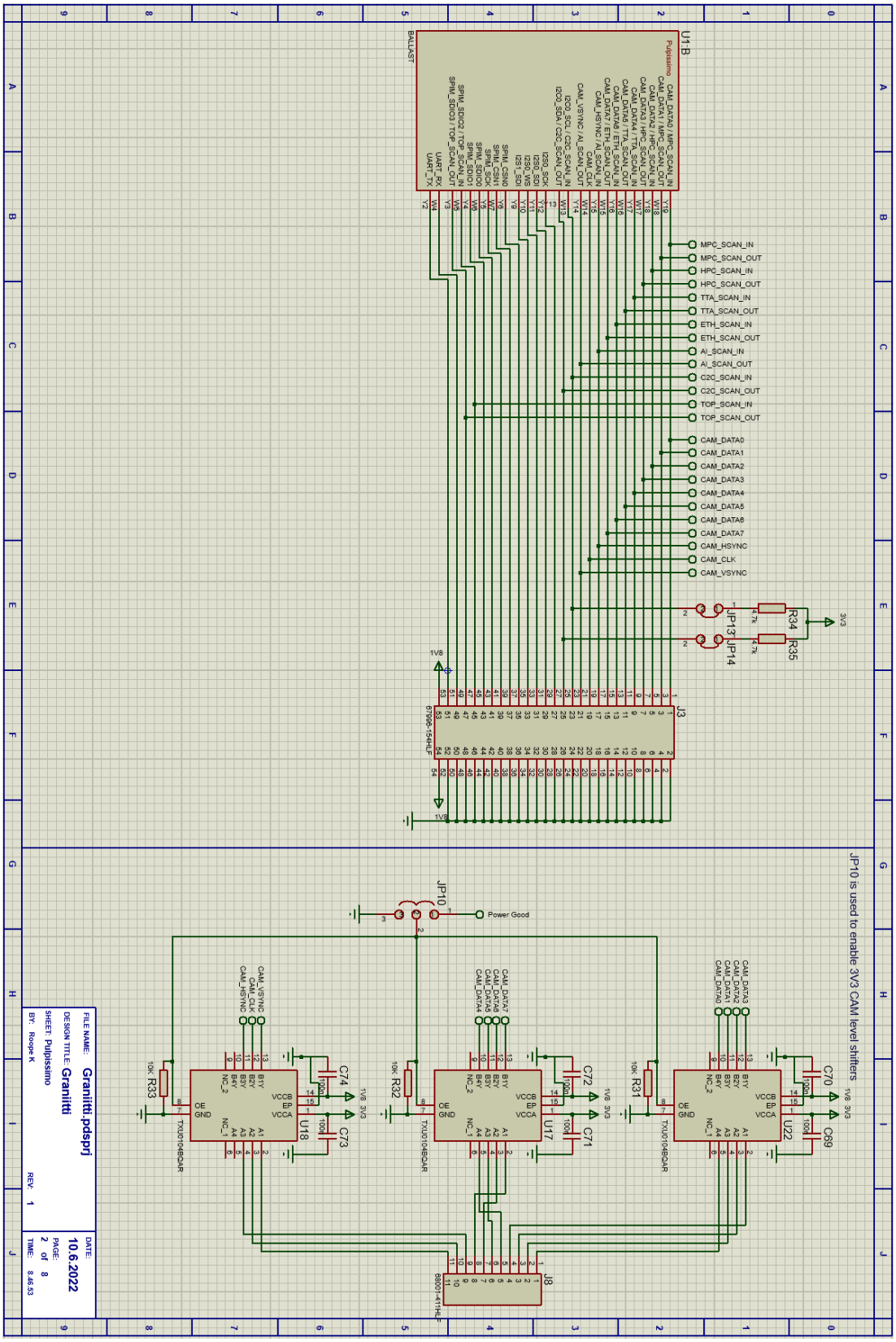
[31] Smith K. Defined Impedance Calculators, 2019, Available: https://www.eurocircuits.com/blog/defined-impedance-calculators/. Accessed (22.4.2022)

[32] Eurocircuits, PCB design classifications. Available : https://www.eurocircuits.com/pcb-design-guidelines-classification/ Accessed (22.4.2022)

[33] Harris M. Gigabit Ethernet 101: Basics to Implementation, 2020. Available: https://resources.altium.com/p/gigabit-ethernet-101-basics-implementation. Accessed (25.6.2022)

APPENDIX A: SCHEMATIC

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Pulpissimo
BALLAST
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MPC_SCAN_OUT
HPC_SCAN_IN
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TTA_SCAN_OUT
ETH_SCAN_IN
ETH_SCAN_OUT
AI_SCAN_IN
AI_SCAN_OUT
C2C_SCAN_IN
C2C_SCAN_OUT
TOP_SCAN_IN
TOP_SCAN_OUT
CAM_DATA0
CAM_DATA1
CAM_DATA2
CAM_DATA3
CAM_DATA4
CAM_DATA5
CAM_DATA6
CAM_DATA7
CAM_HSYNC
CAM_CLK
CAM_VSYNC
JP13
JP14
R34
R35
4.7k
3V3
1V8
J3
87996-1544HLF
JP10
Power Good
JP10 is used to enable 3V3 CAM level shifters
R33
R32
R31
10K
U18
U17
U22
TXU0104BQAR
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C73
C72
C71
C70
C69
100n
1V8 3V3
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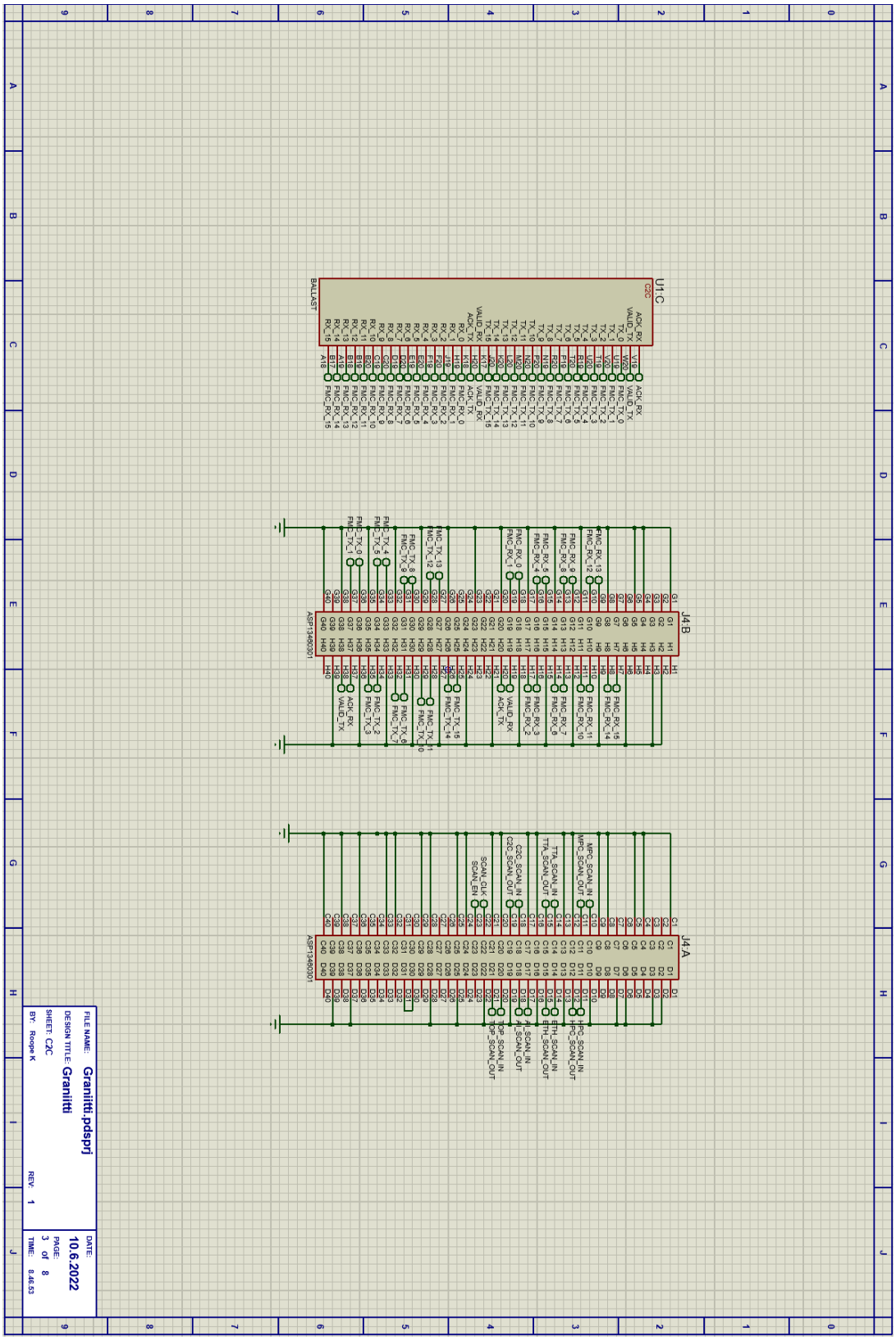
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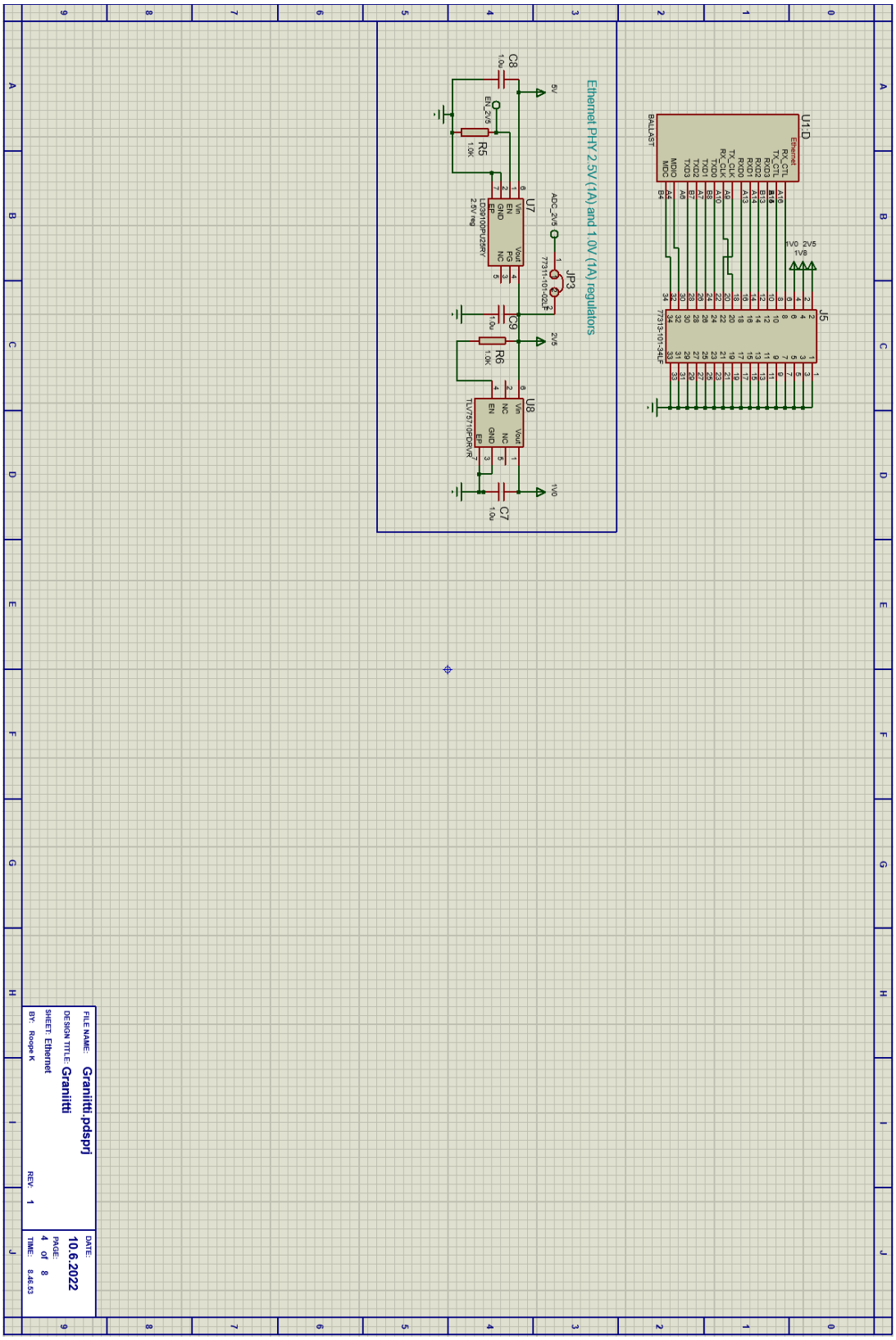
Ethernet PHY 2.5V (1A) and 1.0V (1A) regulators
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Ethernet
BALLAST
J5
JP3
U7
U8
R5
R6
C8
C9
C7
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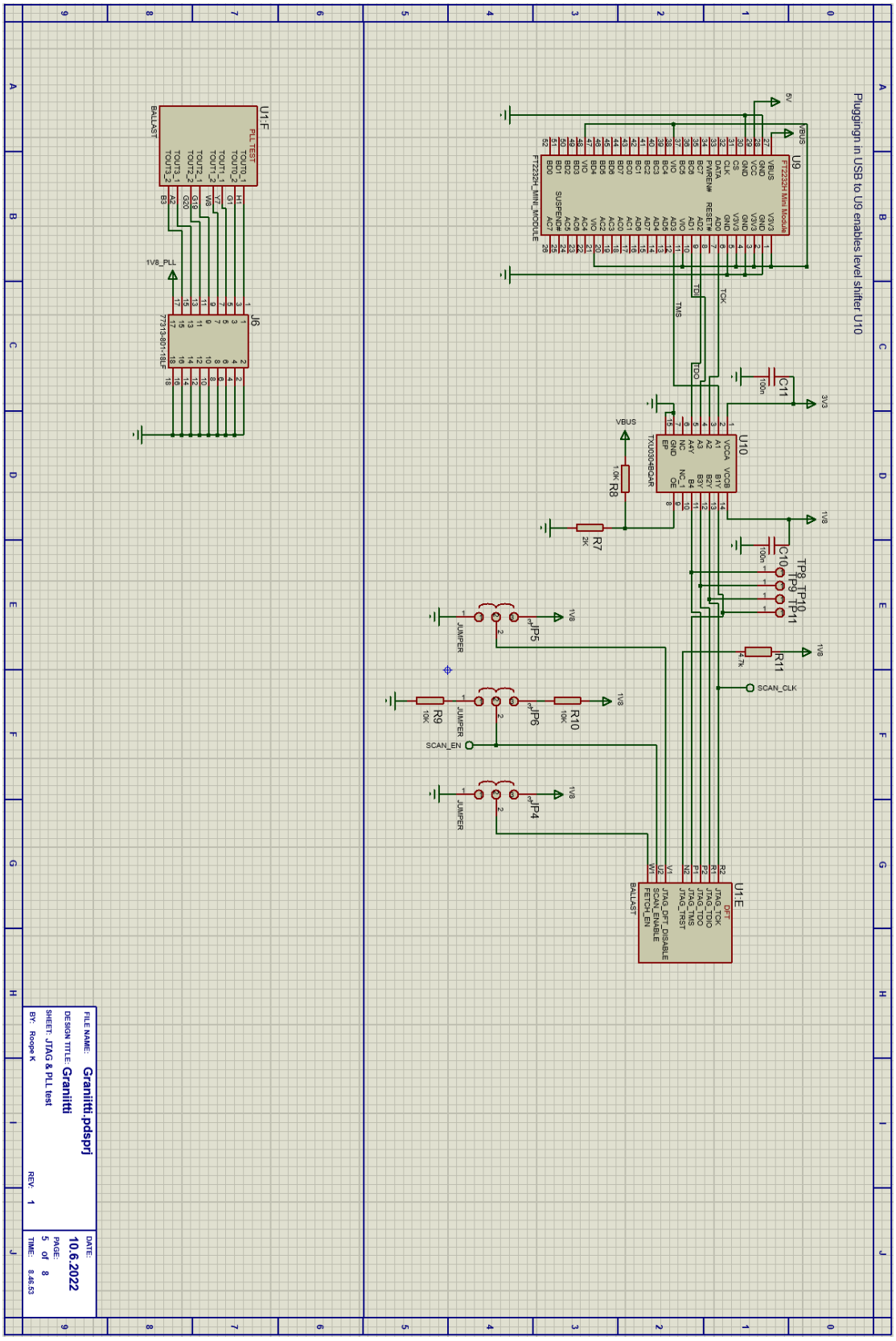
Pluggingin USB to U9 enables level shifter U10
U9
FT2232H Mini Module
FT2232H_MINI_MODULE
U10
TXU0304RGAR
U1:E
DFT
BALLAST
U1:F
PLL TEST
BALLAST
J6
77313-801-18LF
JP4
JP5
JP6
JUMPER
R7
2K
R8
1.0K
R9
10K
R10
10K
R11
4.7K
C10
100n
C11
100n
TP8
TP9
TP10
TP11
SCAN_CLK
SCAN_EN
TCK
TDI
TDO
TMS
1V8_PLL
VBUS
3V3
1V8
5V
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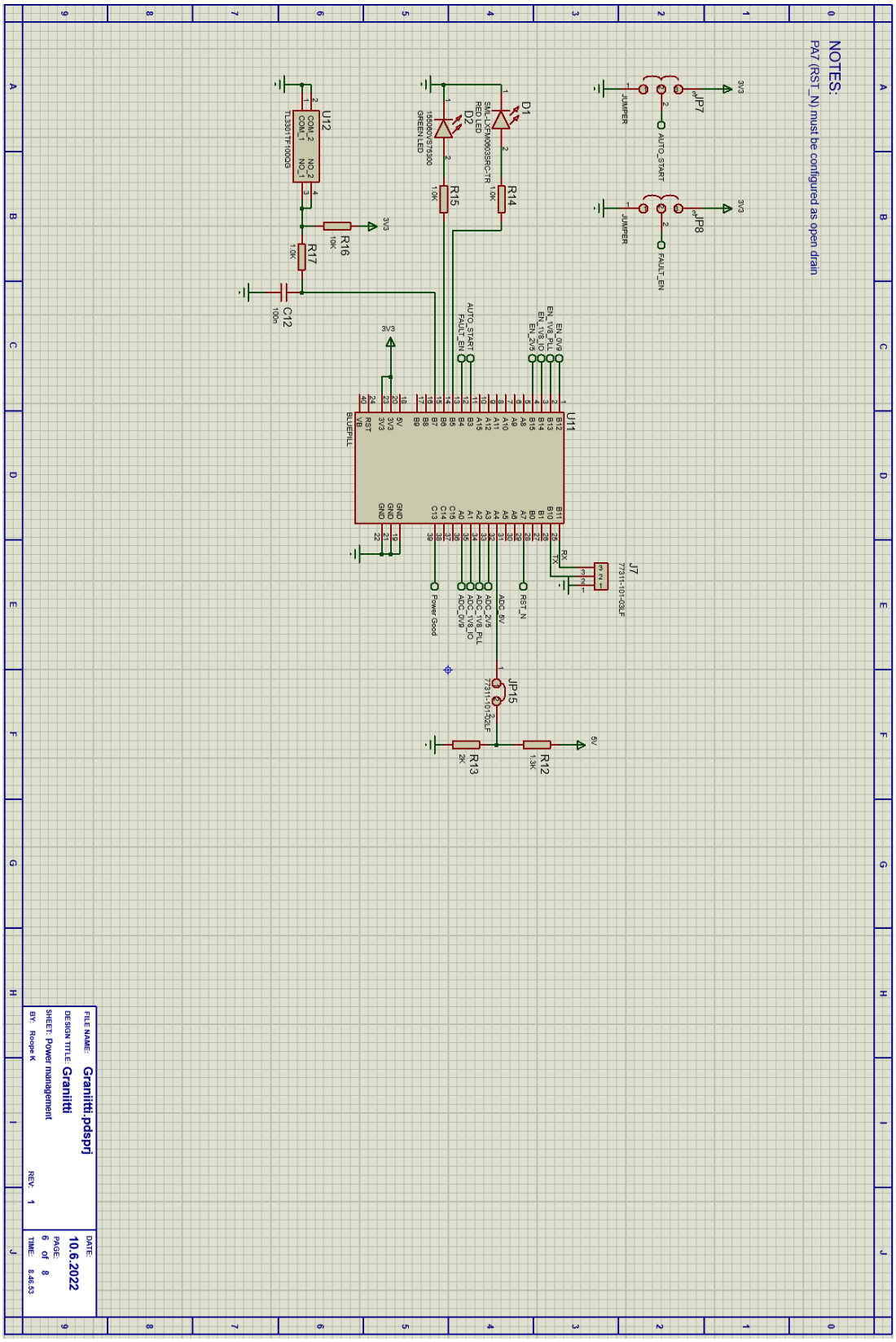
TIME: 8.46.53


NOTES:
PA7 (RST_N) must be configured as open drain
JP7
JUMPER
AUTO_START
JP8
JUMPER
FAULT_EN
D1
SML-LXR0603SRC-TR
RED_LED
D2
156060VS75300
GREEN_LED
R15
10K
R14
10K
U12
TLS301TF100QG
R16
10K
R17
1.0K
C12
100n
U11
BLUEPILL
AUTO_START
FAULT_EN
EN_0V9
EN_1V8_PLL
EN_1V8_IO
EN_2V5
Power Good
ADC_5V
ADC_2V5
ADC_1V8_PLL
ADC_1V8_IO
ADC_0V9
RST_N
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1.3K
3V3
5V
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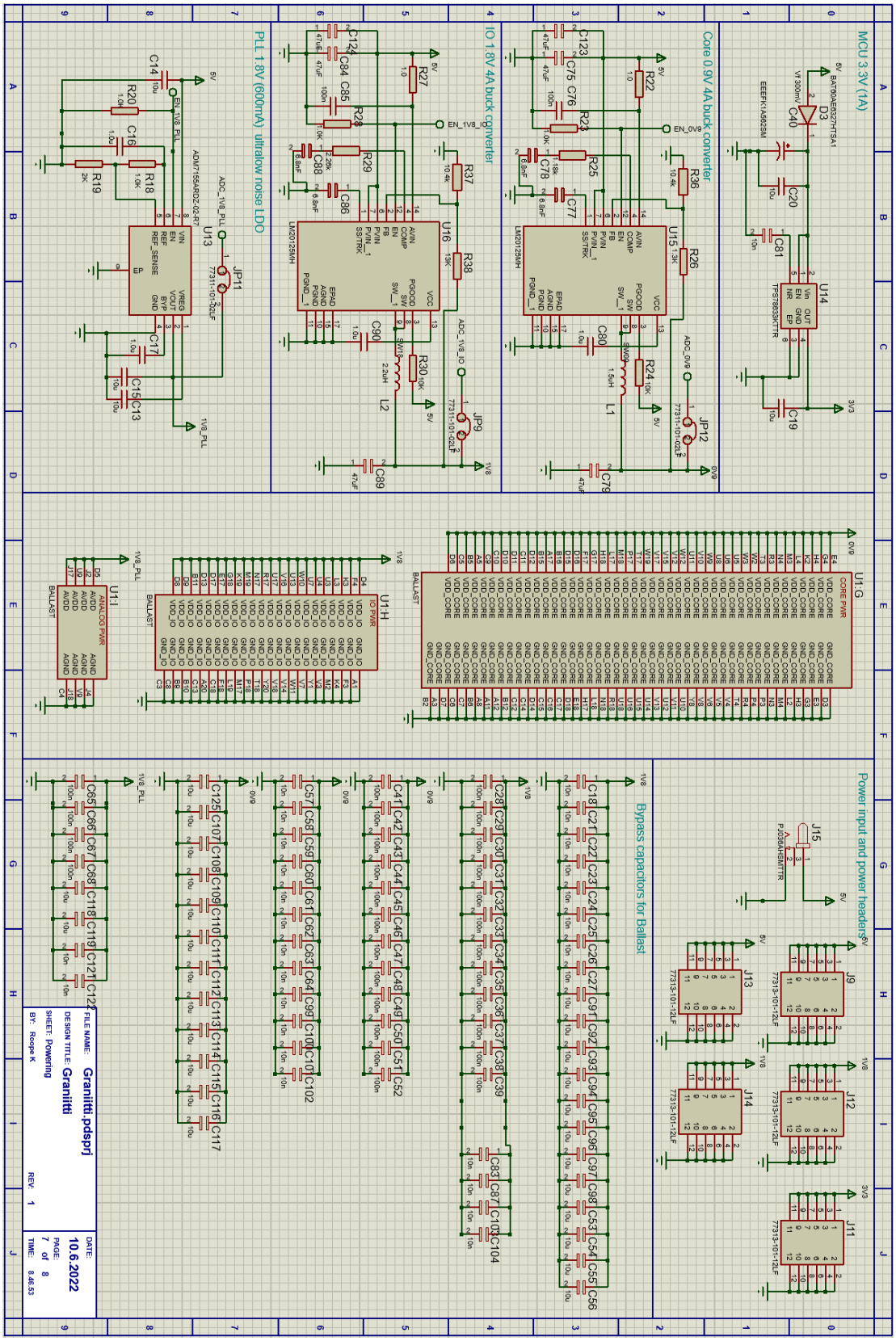
MCU 3.3V (1A)
Core 0.9V 4A buck converter
IO 1.8V 4A buck converter
PLL 1.8V (600mA) ultralow noise LDO
Power input and power headers
Bypass capacitors for Ballast
Granittti.pdsprj
10.6.2022
Graniittti
Powering
Roope K
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