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Electro-Photonic Transmitter Front-Ends for High-Speed Fiber-Optic Communication

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Abstract

This thesis addresses basic scientific research in the field of transmitter front-end circuits for electro-optical data communication. First, the theoretical fundamentals are presented and analyzed. Based on the theoretical considerations, conceptual circuit designs are studied. Finally, in order to prove the described concepts, the circuits were experimentally characterized and subsequently compared to other works in the literature.

The analysis covers key theoretical aspects regarding transmitter front-end circuits. It starts from the basic physical effects inside a transistor and ends with the design of high-swing modulator drivers. Furthermore, it comprises the fundamentals of optical modulators as well as the integration of the electrical driver with the modulator.

The concept of a basic monolithically integrated transmitter consisting of a Mach-Zehnder modulator (MZM) and an electrical driver is presented in Section 3.1. The circuit reaches a bit-error-free (10^{-10}) data rate of 37 Gb/s, which is a record among other monolithically integrated transmitters reported in the literature. It was shown that by employing a high-swing driver, high extinction ratios (ER) can be achieved (namely 8.4 dB at 25 Gb/s and 7.6 dB at 35 Gb/s) while using short-length phase shifters (2 mm of length). It was therefore proved that one of the main drawbacks of the MZM-based transmitters, namely their large chip area, can be mitigated by using high-swing drivers, however without sacrificing the ER.

In Section 3.2, an improved modulator driver design was investigated, the focus of the study being the linearity. In addition to a high peak-to-peak differential output voltage swing of 7.2 $V_{pp,d}$, the driver achieves record-low total harmonic distortion (THD) values of 1% (at 1 GHz, for the output swing of 6.5 $V_{pp,d}$) and 1.7% (at 1 GHz, for the output swing of 7 $V_{pp,d}$). Moreover, the driver reaches a bandwidth of 61.2 GHz and shows a high power efficiency

when relating its DC power consumption to its output voltage swing. The achievement of a high linearity and bandwidth without an increased power consumption is due to the fact that the bias currents of the emitter-follower (EF) stages are provided by means of resistors instead of the conventional current sources. The two approaches were first analyzed mathematically and subsequently compared by means of circuit simulations. It was shown that the proposed approach for the realization of the EFs – i.e. by means of resistors – allows a reduction of the DC power consumption by 19% compared to the current-source approach for an equivalent performance in terms of linearity and bandwidth.

Finally, Section 3.3 studies a modulator driver concept suitable for higher-order modulation formats, namely the 8-level pulse amplitude modulation (PAM-8). The circuit was realized as a 3-bit digital-to-analog converter (DAC), thus being able to yield 8-level output signals. Moreover, the circuit is able to function as a PAM-4 driver as well, thanks to the tunable tail currents of the DAC core. It achieves a symbol rate of 50 Gbaud, which corresponds to a bit rate of 150 Gb/s for the PAM-8 modulation and 100 Gb/s for PAM-4. The study showed that a modulator driver can be realized that is able to switch between different modulation formats (namely PAM-8 and PAM-4), without requiring extra power or additional circuit parts. Moreover, the use of on-chip single-to-differential converters (SDCs) targets the relaxation of the requirements on the stages that precede the driver. Finally, relating its DC power consumption (590 mW, including the SDCs) to its output voltage swing (4 $V_{pp,d}$), the driver shows one of the highest power efficiencies among PAM modulator drivers in the literature.

Zusammenfassung

Diese Arbeit umfasst Grundlagenforschung im Bereich von Transmitter-Front-End-Schaltungen für die elektro-optische Datenübertragung. Als Erstes werden die theoretischen Grundlagen dargestellt und analysiert. Darauf basierend werden konzeptionelle Schaltungsentwürfe untersucht. Um die beschriebenen Konzepte zu überprüfen, wurden die Schaltungen experimentell charakterisiert und anschließend mit anderen Arbeiten aus der Literatur verglichen.

Die Analyse beinhaltet theoretische Schlüsselaspekte bezüglich Transmitter-Front-End-Schaltungen. Sie umfasst die grundlegenden, physikalischen Effekte innerhalb eines Transistors bis hin zum Entwurf von Modulatortreibern mit hohen Spannungshüben am Ausgang. Sie beinhaltet zudem die Grundlagen von optischen Modulatoren sowie die Integration des elektrischen Treibers mit dem Modulator.

Das Konzept eines grundlegenden, monolithisch integrierten Transmitters bestehend aus einem Mach-Zehnder Modulator (MZM) und einem elektrischen Treiber ist im Abschnitt 3.1 vorgestellt. Die Schaltung erreicht eine bitfehlerfreie (10^{-10}) Datenrate von 37 Gb/s, was ein Rekord unter den monolithisch integrierten Transmittern in der Literatur darstellt. Es wurde gezeigt, dass die Verwendung eines Treibers mit hohem Ausgangsspannungshub den Einsatz von kurzen Phasenschiebern (2 mm) ermöglicht, während hohe Extinktionsverhältnisse (ER) erreicht werden können (nämlich 8.4 dB bei 25 Gb/s und 7.6 dB bei 35 Gb/s). Es wurde demzufolge bewiesen, dass einer der Hauptnachteile von MZM-basierten Transmittern, nämlich ihre große Chipfläche, durch den Einsatz von Treibern mit hohen Ausgangsspannungshüben beachtlich verringert werden kann, ohne dabei das ER zu beeinträchtigen.

Im Abschnitt 3.2 wurde das Konzept eines verbesserten Modulatortreibers

untersucht, wobei der Schwerpunkt auf einer hohen Linearität lag. Zusätzlich zu einem hohen Spitze-Spitze-Wert der differentiellen Ausgangsspannung von 7.2 $V_{pp,d}$ zeigt der Treiber einen niedrigen Rekordwert für die gesamte harmonische Verzerrung (THD): 1% bei 1 GHz für den Ausgangshub von 6.5 $V_{pp,d}$ und 1.7% für 7 $V_{pp,d}$. Außerdem erzielt der Treiber eine hohe Bandbreite von 61.2 GHz und weist eine hohe Effizienz auf, wenn der DC-Leistungsverbrauch auf den Ausgangsspannungshub bezogen wird. Die hohe Linearität und Bandbreite wurde erzielt, ohne dass ein erhöhter Leistungsverbrauch notwendig war. Das ist darauf zurückzuführen, dass die Biasströme für die Emitterfolger-Stufen der Schaltung anhand von Widerständen anstatt von Stromspiegeln bereitgestellt werden. Die zwei Ansätze wurden zuerst mathematisch analysiert und anschließnd durch Schaltungssimulationen verglichen. Es wurde gezeigt, dass der neue Ansatz zur Realisierung der Emitterfolger-Stufen – d.h. anhand von Widerständen – eine Verminderung des Leistungsverbrauchs um 19% im Vergleich zum herkömmlichen Ansatz mit Stromspiegeln ermöglicht. Diese Verringerung des Leistungsverbrauchs setzt keine Verschlechterung der Linearität oder Bandbreite voraus.

Letztlich wurde im Abschnitt 3.3 das Konzept eines Modulatortreibers erforscht, das für Modulationsverfahren höherer Ordnung geeignet ist, und zwar für die achtstufige Pulsamplitudenmodulation (PAM-8). Die Schaltung wurde als 3-Bit Digital-Analog-Umsetzer (DAC) realisiert und kann achtstufige Ausgangssignale ausgeben. Zudem kann die Schaltung aufgrund der einstellbaren Fußpunktströme des DAC-Kerns auch als ein PAM-4-Treiber fungieren. Es wurde eine Symbolrate von 50 Gbaud erreicht, was einer Bitrate von 150 Gb/s für die PAM-8-Modulation und 100 Gb/s für die PAM-4-Modulation entspricht. Die Untersuchung hat gezeigt, dass ein Modulatortreiber realisiert werden kann, der zwischen verschiedenen Modulationsverfahren (nämlich PAM-8 and PAM-4) umschalten kann, ohne dass mehr Leistungsverbrauch oder zusätzliche Schaltungsteile notwendig sind. Zudem erlaubt die Verwendung von on-chip Eintakt-Gegentakt-Umsetzern die Vereinfachung der Anforderungen für die Vorstufen. Letztlich zeigt das Verhältnis zwischen DC-Leistungsverbrauch (590 mW, einschließlich der Eintakt-Gegentakt-Umsetzer) und Ausgangsspannungshub (4 $V_{pp,d}$), dass die Schaltung zu den energieeffizientesten PAM-Modulatortreibern in der Literatur zählt.

Note on the Use of IEEE Material from Own Publications

The contents of section 1.2 of chapter 1, section 2.6 of chapter 2 as well as chapter 3 are largely based on published IEEE papers where I was the first author. The papers were published during my doctoral research work at Technische Universität Dresden. All these papers are referenced accordingly. A list of these publications is available at the end of the thesis, in the section called ”Own Publications”. When citing the figures and tables from the own publications, a special symbol (†) was used in order to distinguish them from other citations in the thesis. Finally, a footnote at the beginning of each chapter or section mentioned above was introduced, which specifies the own publication on which the respective chapter or section is based.

Contents

1 Introduction

1.1 Electro-Optical Communication

In the last decades, the data volume in the worldwide networks has been growing sharply, and this trend is currently accelerating with the development of the Internet of Things and other big data applications. Therefore, there is a high motivation for research on faster, low-loss and high-reliable channels of communication.

Attempts to use light as a data carrier date back to the 19th century, however it is only in the 1970s that low-loss transmission through optical fibers has been achieved. Thus, in 1970, light transmission with a loss of less than 20 dB/km was demonstrated. In 1975, this figure was improved to 4 dB/km and in 1979 to 0.2 dB/km [Raz03], which allows reliable data transmission over an optical medium.

At the present day, the optical fibers, as communication medium, offer a series of advantages compared to the traditional copper cables. First, they show a higher bandwidth as well as lower losses, thus being suitable for high-speed data transmission over long distances [Raz03]. Second, they are not susceptible to electromagnetic interference. Third, they are lighter, thinner and have lower production costs. Finally, they provide a higher degree of security, since they cannot be intercepted by means of tapping.

A key part in the realization of electro-optical transmission is the conversion of electrical data into optical data. This implies the modulation of an optical carrier signal by an electrical data signal. This can be done either directly, by modulating the laser source with an electrical signal, or indirectly, by means of optical modulators, which in turn modulate the laser. The Mach-Zehnder optical modulators (MZM) are one of the most popular modulator types used in electro-optical transmitters, since they provide high speed, wide

optical spectra and low thermal sensitivity [XLX+14]. The input of these modulators is the light coming from a continuously emitting laser source. The modulation is realized by means of phase shifting of the light waves in the two modulator arms. This phase shift occurs as a result of the applied voltage provided by an electrical driver. Subsequently, the light waves are being recombined, thus realizing a logical "1" if the recombination is constructive, or a logical "0" if the recombination is destructive. A more detailed insight into the functioning of an MZM is provided in Section 2.5.

There are several integration methods for realizing electro-photonic communication systems. The most straightforward way is to fabricate all components separately (and in different materials) and subsequently assemble them. While no special manufacturing techniques are required, this method implies several fabrication processes as well as long interconnections between the electrical and optical components. Another method of integration is the hybrid one, which makes use of silicon (Si) photonic technologies, where the optical components are fabricated on a Si substrate. Such technologies (also known as photonic integrated circuit technologies, or PIC) offer advantages in terms of high-yield, volume and low-cost manufacturing, as well as higher integration capabilities. Nevertheless, the electrical and optical components are realized separately and their integration require additional fabrication steps as well as long interconnections. A particularly promising way of fabricating electro-photonic communication systems is the monolithic integration of electronic and photonic components on the same Si chip (with the exception of laser diodes, which up to this date could not be successfully integrated on a Si chip). Several such technologies have been presented in the literature [KLB+15] [ASG+12]. Also known as electro-photonic integrated circuit (EPIC) technologies, this way of integration shows two main advantages in comparison to the hybrid integration. First, the interconnections between the optical and the electrical components are reduced to a minimum length, thus enabling high-speed performance [PLL+16]. Second, it offers a good approach to decreasing manufacturing costs as well as to enable mass production [ASG+12], since the chips are produced in one single fabrication process.

For the purpose of increasing the data volume that can be transmitted via

the telecommunication networks, several modulation formats have been investigated. In recent times, coherent transmission techniques became particularly attractive [NWY+20], since they use both amplitude and phase modulation and thus multiply the number of bits that can be sent within one symbol. By means of such modulation schemes (called quadrature amplitude modulation, or QAM), systems with data rates as high as 400 Gb/s are being realized [Miy16]. However, such systems, as well as the modulation format itself, pose very high requirements on the integrated electric drivers of the electro-optical assemblies. The modulator drivers are therefore expected to have a high bandwidth for high-speed operation, a high linearity to avoid harmonic distortions, a high output voltage swing for an efficient driving of the optical modulator, and finally a low power consumption. Fulfilling all these requirements simultaneously represents a considerable challenge for the driver design.

1.2 Scientific Context and Open Challenges[1]

This section presents an overview of the state of the art in the field of MZM-based electro-optical transmitters and of electrical modulator drivers in particular. We present the latest and most relevant designs reported in the literature, as well as their performance and trade-offs.

1.2.1 MZM-Based Electro-Optical Transmitters

Several designs of MZM-based electro-optical transmitters have been reported in the scientific literature, realized either by means of monolithic integration (excluding the laser) or by hybrid integration techniques (i.e. wire bonding or flip-chip). In [RLP+16] and [PRL+16], transmitters realized in a co-integrated electro-photonic technology were presented. The designs reached high extinction ratios (ER) of 13 dB and 11 dB, respectively, and symbol rates of 28 Gbaud and 32 Gbaud, respectively. Since the electrical drivers provided only a limited peak-to-peak differential output swing (4 $V_{pp,d}$ and

1 **Copyright Note**: Section 1.2 of Chapter 1 is largely based on the descriptions of the state of the art from the IEEE publications [GBK+22]† and [GKB+22]†, in which I was the first author.

3.5 $V_{pp,d}$, respectively), phase shifters with a length of 6.05 mm each had to be employed in order to ensure the high ERs. This led to a significant chip area. The power consumption was considerable as well (2 W and 1.8 W, respectively). Another transmitter making use of monolithic integration of the optical and electrical components was presented in [XGP+15]. The transmitter employed a CMOS driver and consumed a much less amount of DC power, namely 270 mW. The circuit was also more compact than the previously mentioned designs, since the MZM's phase shifters were only 3 mm long. Nevertheless, the short phase shifter length as well as the limited driver output swing (2.2 $V_{pp,d}$) led to a lower ER (6.3 dB). The transmitter achieved a symbol rate of 28 Gbaud. In [YSM+18], a design using hybrid integration, namely the flip-chip technique, was shown. The circuit achieved a high symbol rate of 50 Gbaud and a good ER of 8 dB, while employing 4-mm long phase shifters and consuming 553 mW of DC power. Other transmitters using hybrid integration methods were presented in [TMR+16] (integration by means of flip-chip) and [BRG+20] (integration by means of wire bonding). These circuits achieved high symbol rates (56 Gbaud and 53 Gbaud, respectively) and featured a low power consumption (300 mW and 386 mW, respectively). However, due to the limited output voltage swing of the electrical drivers (1.6 $V_{pp,d}$ and 2 $V_{pp,d}$, respectively) and because of the short phase shifter lengths (3.15 mm and 3.45 mm, respectively), the circuits achieved low ERs (2.5 dB and 4.5 dB, respectively). A design employing wire bonding was presented in [LQL+20]. The transmitter achieved a high ER of 9.6 dB with a compact MZM design featuring 3-mm long phase shifters. The circuit had nevertheless a limited symbol rate (25 Gbaud) and consumed a high amount of DC power (1.34 W).

An open research topic in the field of electro-optical transmitters that was not thoroughly investigated in the literature is the realization of compact monolithically integrated assemblies capable of reaching high symbol rates and high ERs. Nevertheless, the compactness and speed are one of the main advantages of the monolithic integration compared to its hybrid counterpart, since the assemblies are supposed to be realized on the same Si chip, without long interconnections between the electrical and optical components that limit the data rate and without extra bond wires or flip-chip bumps, which

require additional floorplanning for the chip layout.

1.2.2 MZM Drivers

Next, an overview of the latest MZM driver designs reported in the literature is presented. The focus is on circuits with high output voltage swing, but also high bandwidth and high linearity, since these are the main requirements for future coherent electro-optical communication systems. For the purpose of maximizing the ER that can be achieved at the MZM output, a high-swing driver employing the breakdown voltage doubler topology was proposed in [AML+20]. The circuit reached a high output voltage swing of 6 $V_{pp,d}$, however it had a limited bandwidth of only 40 GHz as well as a high power consumption of 1 W. Moreover, it showed an average linearity, with a total harmonic distortion (THD) of 3.6% measured at 1 GHz and for the full output swing. A high voltage swing was also achieved in [RJA+19], namely 4.9 $V_{pp,d}$, by using the cascode topology in the output stage. The circuit also showed a high bandwidth of 86.8 GHz. However, this was achieved by means of inductive peaking, which considerably increases the circuit layout size. At 10 GHz and for 2.5 $V_{pp,d}$ output swing, the driver showed a THD of 5%, which indicates a low linearity. The power consumption of the circuit was 1.2 W, which is considerable. In [ZSV17], a driver with lower power consumption was presented, namely 820 mW, while reaching a comparable output voltage swing (4.8 $V_{pp,d}$). However, the bandwidth was limited to 57.5 GHz. The driver employed a MOS-HBT cascode topology. Its THD at 10 GHz and for 2.5 $V_{pp,d}$ output swing was 2.5%. A driver using the distributed amplifier topology was shown in [BHSV17]. It achieved a high bandwidth of 70 GHz, a high linearity (THD was 2% at 4 GHz for 4.5 $V_{pp,d}$ output swing) as well as a high differential gain of 20 dB. Nevertheless, it showed a high power consumption of 1.1 W. The design shown in [RGA+17] made use of the distributed amplifier topology as well and reached a high bandwidth of 90 GHz. The circuit had a limited output voltage swing, namely 4 $V_{pp,d}$, as well as a low linearity (the THD was 5% at 1 GHz for 3 $V_{pp,d}$ output swing). A very high bandwidth of 110 GHz was achieved in [NWY+20] by means of a bandwidth doubler topology using a 2:1 analog multiplexer. However, the

design had a very low output voltage swing (1.5 $V_{pp,d}$), which makes the use of long-length phase shifters unavoidable in order to reach a high ER at the MZM output. Moreover, the circuit had an average linearity, with a THD of 3% at 1 GHz for the full output swing, while the power consumption was considerable (990 mW). In order to minimize the power consumption, the designs presented in [NNT+17] and [JNO+20] employed the stacked current mode architecture as well as an open-drain topology. Thus, the circuits showed a power consumption of only 180 mW and 225 mW, respectively. Nevertheless, the designs had limited output voltage swings (2 $V_{pp,d}$ and 1.5 $V_{pp,d}$, respectively), bandwidths of 56 GHz and 48 GHz, respectively, and THD values of 3.8% and 2.2%, respectively, at 1 GHz and for the maximum output voltage swings. In [NBNM13] and [WNY+14], two highly linear drivers were presented with THDs as low as 1.2% and 1.1%, respectively, at 1 GHz and for the full output swing. Both circuits used a cascode topology with resistive emitter degeneration. Nevertheless, the designs showed very low bandwidths (37.8 GHz and 22 GHz, respectively) as well as low output voltage swings (3 $V_{pp,d}$ each).

As it can be seen, the modulator driver designs reported in the literature show either a high bandwidth, a high output voltage swing or a high linearity. An unresolved challenge is the optimization of the driver design with the purpose of maximizing all these parameters at the same time, while keeping the power consumption as low as possible. Moreover, the output voltage swing of the driver is of particular importance, since for MZM-based assemblies a high-swing driver allows the use of short-length phase shifters without sacrificing the modulator's ER, thus being an essential feature for compact electro-optical transmitters.

1.3 Objectives and Structure of the Thesis

In this thesis, we address the basic scientific research in the field of circuits and systems for electro-optical communication networks, with focus on MZM-based electro-optical transmitters. We describe the underlying theory, we establish the concepts for our work, and finally we prove these concepts by means of chip implementations and their experimental verification.

The first circuit concept that we propose is a monolithically integrated electro-optical transmitter front-end consisting of an MZM and an electrical driver. The design targets the realization in an EPIC-type technology of a compact and high-speed electro-photonic assembly by employing a short-length MZM, however without sacrificing the ER. This was achieved by co-integrating the MZM with a high-swing electrical driver, which uses the breakdown voltage doubler topology [MH04] and thus overcomes the physical limitations of the output transistors regarding the maximum allowed output voltage swing.

Second, a similar driver architecture is investigated and subsequently enhanced. Thus, the concept of an MZM driver design is presented, which simultaneously achieves a high output voltage swing, a high linearity as well as a high bandwidth. Moreover, the driver has a low power consumption thanks to a new implementation approach for its emitter-follower stages, where the bias currents are provided by resistors instead of traditionally used current sources.

Finally, in order to increase the amount of data that can be sent for a given bandwidth, we study the concept of a non-linear DAC-based modulator driver design capable of yielding PAM-8 output signals. Furthermore, depending on the given requirements, the circuit can operate as a PAM-4 driver as well. This switching capability between two modulation formats does not come at the expense of additional power consumption or circuit complexity.

The thesis is structured as follows. Chapter 2 introduces the basic theoretical concepts of the electrical and optical design of MZM-based transmitters, with focus on the transmitter front-ends. Chapter 3 presents the proposed chip implementations, which are based on the theory described in Chapter 2. The successful experimental characterization of these circuits proves the concepts introduced in Chapter 2. Finally, Chapter 4 draws up the conclusion of the thesis and offers an outlook on the future research work.

2 Theory and Fundamentals of Electro-Optical Transmitters

In this chapter, an overview of the basic theoretical concepts for the design of electro-photonic transmitters is outlined. First, a general view over the electro-optical communication systems is provided including a short presentation of the building blocks on the transmitter and the receiver side. Next, the design of electrical modulator drivers is addressed. We first describe the working principles of bipolar transistors, since they are the basic active components of all circuits that are going to be presented in this thesis. Afterwards, the common-emitter stage is described. Subsequently, the cascode amplifier is presented as an enhancement of the common-emitter stage. Next, the breakdown voltage doubler architecture is explained, since this topology was mainly preferred for the chip implementation of the modulator drivers presented in this thesis. Finally, the fundamentals of Mach-Zehnder optical modulators are presented and explained. The chapter is concluded by a description of two ways of implementing MZM-based electro-optical transmitters, namely the segmented and the traveling-wave topology.

2.1 Electro-Optical Communication Systems

A basic electro-optical communication system consists of three elements: a transmitter, where electrical data is modulated and converted to optical data; an optical fiber, which serves as a medium for the transfer of data; and a receiver, where optical data is converted back to electrical data. The basic diagram of such a system is shown in Fig. 2.1. On the transmitter side, there are two approaches for converting electrical signals to optical signals. The first approach is the direct modulation, where a laser diode is used to convert the

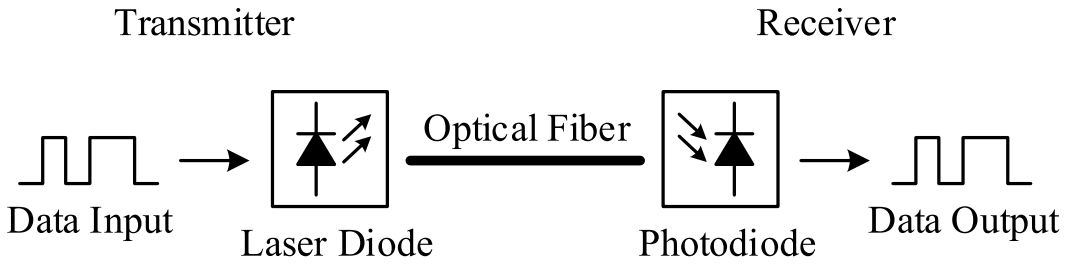
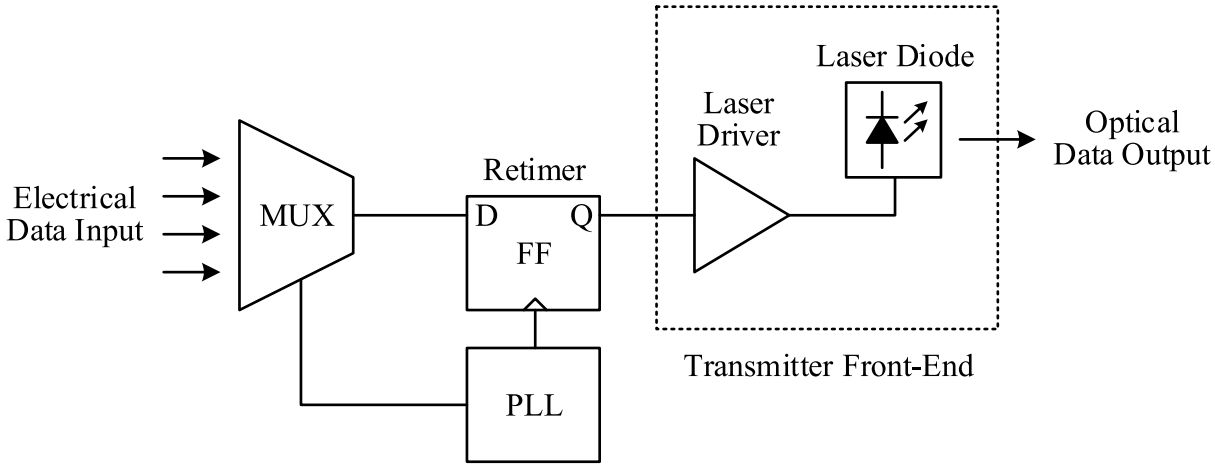


Figure 2.1: Basic electro-optical communication system.

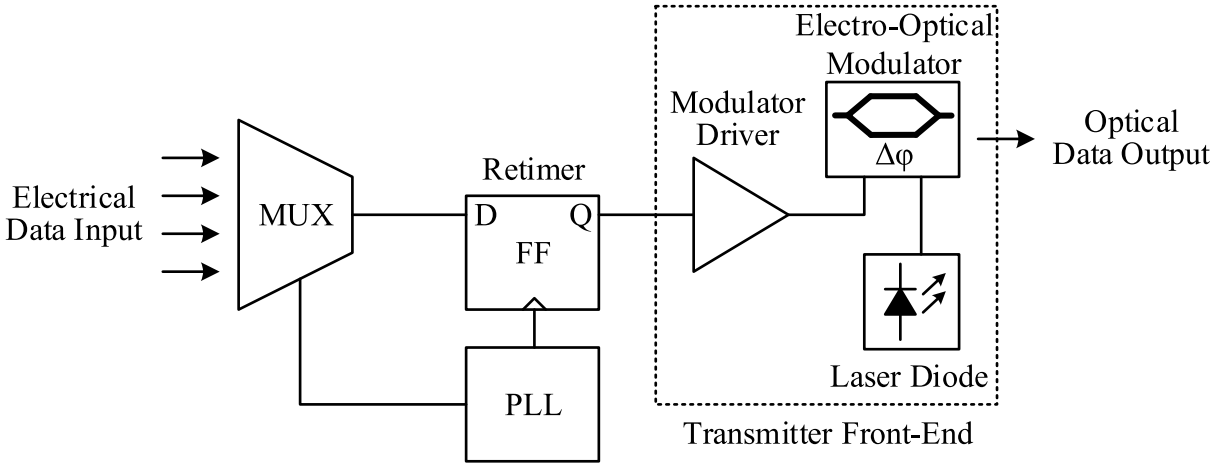
electrical pulses (in form of electric current) coming from a laser driver into optical pulses. Thus, the laser diode outputs a light signal with an intensity that depends on the current provided by the laser driver. The second approach is the indirect modulation. Here, a continuous emitting laser source is used in combination with an optical modulator. The continuous light wave coming from the laser diode is provided to the modulator, which outputs it with different intensities, depending on the voltage that is applied to the modulators' electrodes by an electrical driver. For both approaches, the signal transmitted over the optical fiber is a digital waveform with several amplitude levels and phase shifts, depending on the chosen modulation scheme.

When transmitting data over large distances, several challenges appear, mainly due to chromatic dispersion and non-linear effects within the optical fibers [Agr18]. Therefore, special circuitry is required both on the transmitter side as well as on the receiver side in order to ensure reliable data transfer.

Fig. 2.2 depicts the basic block diagram of a transmitter of an optical communication system for direct (a) and indirect (b) modulation, respectively [Raz03]. First, the electrical data coming from multiple users via several parallel channels has to be converted into a single data stream. This process of parallel-to-serial conversion is done by means of a multiplexer (MUX). A MUX requires a certain number of clock frequencies with very precise phase alignment. A plain oscillator would not suffice to this task, since it is prone to process variations, jitter, temperature and aging. Therefore, a phase-locked loop (PLL) is employed, which offers a stable and synchronized output by means of a feedback loop. As the MUX usually shows jitter and intersymbol interference, a re-timer flip-flop (FF) is also employed which ensures a clean MUX output [Raz03].



(a)



(b)

Figure 2.2: Transmitter block diagram of an electro-optical communication system for (a) direct modulation and (b) indirect modulation.

The front-end of the transmitter is constituted either by a laser driver and a laser diode, in case of direct modulation (Fig. 2.2 (a)), or by a modulator driver, an optical modulator and a laser, in case of indirect modulation (Fig. 2.2 (b)). The purpose of the transmitter front-end is to amplify the electrical data coming from the MUX and to convert it into optical data with a sufficient output optical power in order to be transmitted over a certain dis-

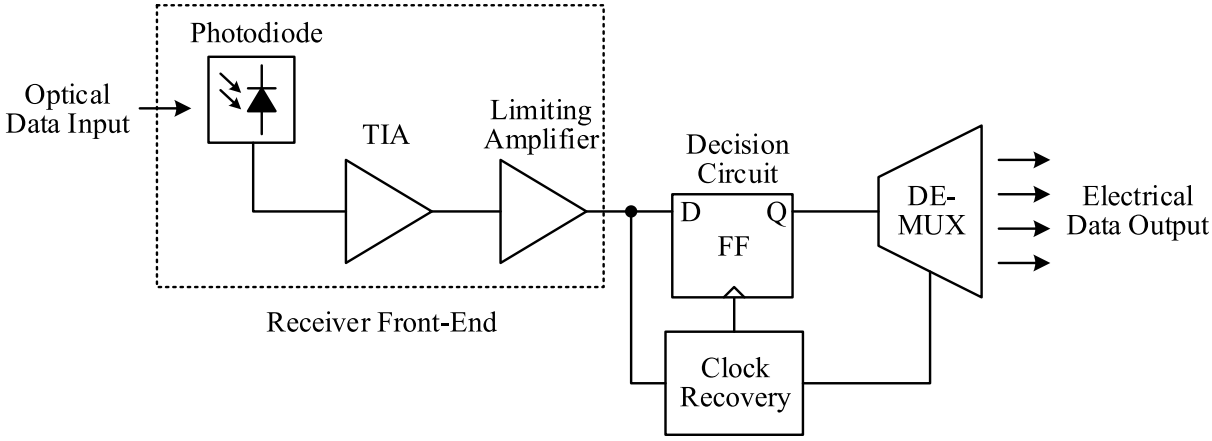


Figure 2.3: Receiver block diagram of an electro-optical communication system.

tance. In the case of direct modulation, the laser driver has to provide a certain amount of output current to the laser diode, depending on the current-voltage characteristics of the laser. This represents a challenge since the maximum collector current that a transistor is able to switch at high frequencies is related to its size. Thus, for high laser currents, large transistor sizes with high parasitic capacitances are required, which restrict the achievable bandwidth. On the other hand, if indirect modulation is used, a modulator driver has to provide a sufficiently high output voltage swing in order to efficiently drive the optical modulator. This poses a challenge to the driver design, since the maximum output voltage swing is restricted by the technology-given breakdown voltage of the transistors.

In Fig. 2.3, the block diagram of a receiver for optical communication systems is illustrated [Raz03]. The incoming optical signal from the transmitter is converted into electrical signal by means of a photodiode. The photodiode output current is then converted into voltage by means of a transimpedance amplifier (TIA). Since the light wave arriving at the receiver is considerably attenuated, the photodiode usually outputs a low current. Therefore, a high amplification and a high signal-to-noise ratio (SNR) are among the main requirements of the TIA. A limiting amplifier further amplifies the TIA's output. Next, a flip-flop cell is employed in order to cancel the noise in the signal and to ensure a clean waveform, where the digital levels are clearly distinguish-

able. For this reason, this flip-flop cell is called a decision circuit [Raz03]. In order to generate the clock for the components of the receiver, a clock recovery cell is employed. This circuit recovers the frequency of the transmitter's PLL based on the received bit stream. Finally, a demultiplexer (DEMUX) is used at the output of the receiver in order to restore the initial electrical channels that were merged by the transmitter's MUX.

2.2 Bipolar Junction Transistor

The transistor is the basic active component of any amplifier circuit. A bipolar junction transistor (BJT) can be regarded as a voltage controlled current source, since it outputs a current depending on its input voltage. Usually, bipolar transistors are used for high-frequency applications and for circuits requiring a high-current-driving capability. In comparison, the field-effect transistors (FET) are preferred for low-power applications and for circuits that require a high input impedance [SS16].

Fig. 2.4 shows the basic structure of an *npn*-type bipolar transistor [SS16]. It consists of three regions that are differently doped. The emitter and the collector region are doped with electrons (*n*-type doping), while the base region is doped with holes (*p*-type doping). The three regions correspond to the three terminals of a BJT: the base (B), the emitter (E) and the collector (C). When

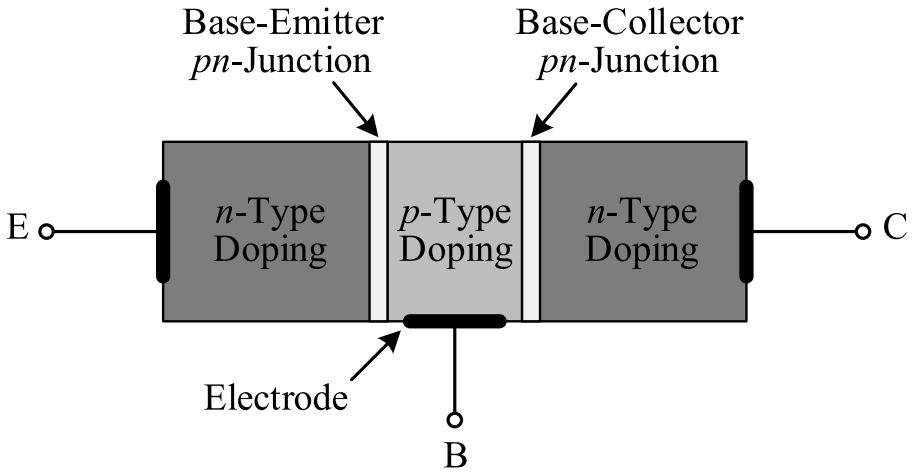


Figure 2.4: Basic structure of an *npn* bipolar transistor.

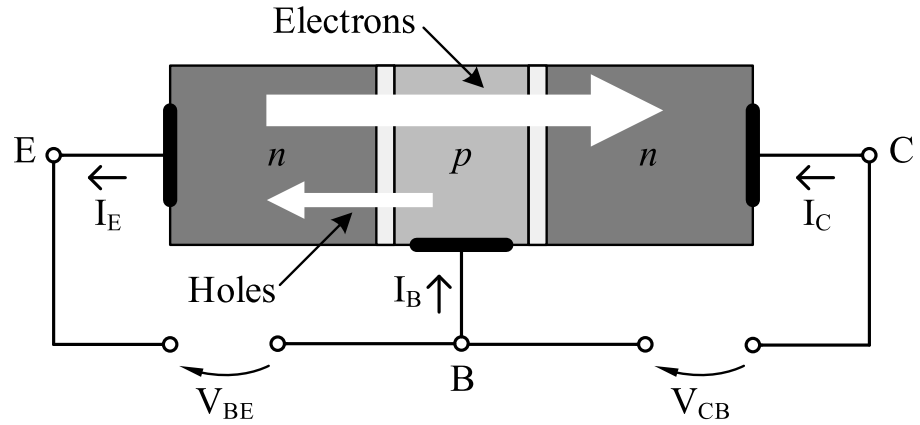


Figure 2.5: Working principle of an *npn* bipolar transistor.

a voltage V_{BE} is applied over the base and the emitter of the BJT (Fig. 2.5), the base-emitter *pn*-junction becomes forward biased and starts conducting a current (the emitter current I_E): the holes from the base region are injected into the emitter, while the electrons from the emitter region are injected into the base. We also assume a positive voltage V_{CB} applied over the collector and the base of the BJT. Since the emitter is much highly doped than the base, the electron current largely dominates the hole current [SS16]. Next, the electrons injected from the emitter into the base diffuse throughout the base in the direction of the collector due to the concentration gradient. Since the base is only lightly doped, only a few electrons are lost by recombination [SS16]. As the voltage potential at the collector of the transistor V_C is higher than the potential V_B at the transistor's base, the electrons injected into the base diffuse further into the collector region, thus forming the transistor's collector current I_C.

The collector current I_C, which constitutes the transistor's output current, can be expressed in terms of the base-emitter voltage V_{BE} (which can be seen as the transistor's input voltage) by means of the following equation [SS16]:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{2.1}$$

where I_S is the saturation current of the transistor and V_T the thermal voltage, defined as:

$$V_T = \frac{kT}{q} \tag{2.2}$$

where k is the Boltzmann constant, T the absolute temperature and q the elementary charge of an electron.

The base current I_B is proportional to $e^{\frac{V_{BE}}{V_T}}$ as well [SS16] and can thus be expressed in terms of the collector current I_C by means of the following equation:

$$I_B = \frac{I_C}{B_i} \tag{2.3}$$

Therefore, the parameter $B_i = I_C/I_B$ is considered to be the current gain of the bipolar transistor [SS16].

Based on equation (2.1), the I_C-V_{BE} relation of a BJT can be represented graphically as in Fig. 2.6. As it can be seen, the collector current I_C starts rising exponentially after a certain threshold voltage $V_{BE,0}$. This behavior is similar to the current-voltage characteristic of a diode.

Ideally, the collector current I_C does not change with the collector-emitter voltage V_{CE}, since the transistor is supposed to be an ideal current source. Nevertheless, due to the Early effect, I_C does show a slight linear increase with V_{CE} for a certain base current V_B. Fig. 2.7 shows the dependence of I_C on V_{CE} for different I_B currents. The two main operating regions of the transistor,

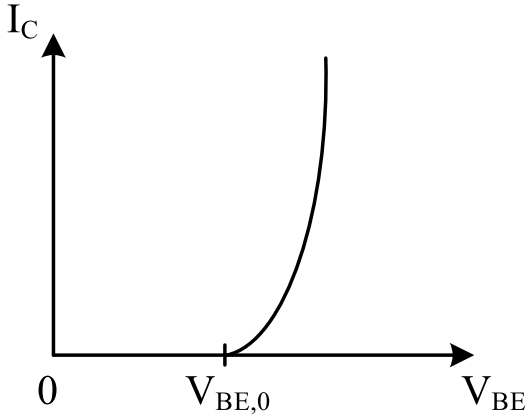


Figure 2.6: I_C dependence on V_{BE} for an *npn*-type BJT.

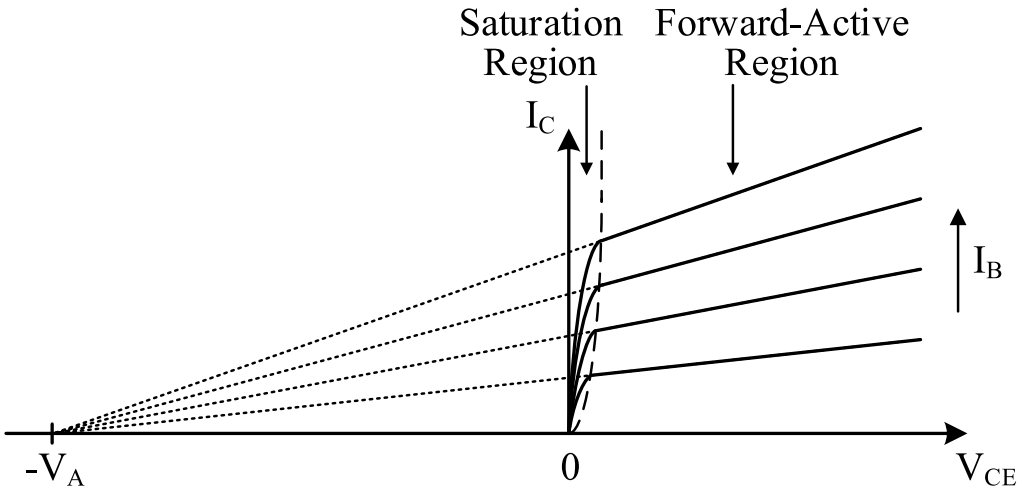


Figure 2.7: I_C dependence on V_{CE} for different I_B. *npn*-type BJT.

namely the saturation and the forward-active region are also highlighted.

The linear increase of I_C with V_{CE} due to the Early effect can be expressed by inserting a factor $(1+\frac{V_{CE}}{V_A})$ in equation (2.1), where V_A is the Early voltage (as depicted in Fig. 2.7) [SS16]. Thus, equation (2.1) becomes:

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \left(1 + \frac{V_{CE}}{V_A}\right) \tag{2.4}$$

Small-signal wise, the slope of the i_C-v_{CE} function (in the forward-active region) can be regarded as the small-signal output resistance r_o of the bipolar transistor and is calculated using the following formula [SS16]:

$$r_o = \left(\frac{\delta i_C}{\delta v_{CE}}\bigg|_{v_{BE}=constant}\right)^{-1} \tag{2.5}$$

Based on the knowledge acquired so far and taking into account the main parasitic effects, the equivalent small-signal model of an *npn*-type bipolar transistor in the forward-active region can be drawn (Fig. 2.8). It consists of the input resistance r_π (between the base and the emitter), the capacitance C_π of the base-emitter *pn*-junction, the capacitance C_μ of the base-collector *pn*-junction, the transconductance g_m, the output resistance r_o – expressed in equation (2.5) – and the substrate capacitance C_S (between collector and sub-

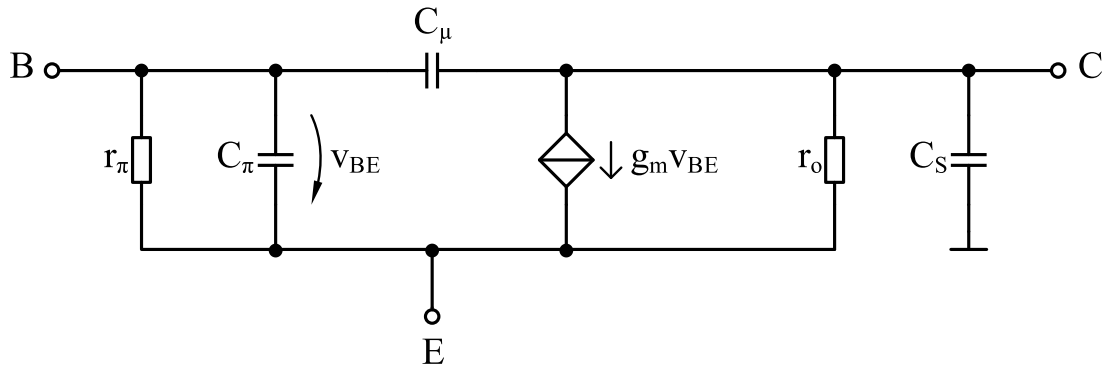


Figure 2.8: Small-signal equivalent circuit model of an *npn*-type BJT in forward-active region.

strate). All these parameters are small-signal parameters and are dependent on the chosen operating point (OP) of the transistor.

The input resistance r_π is defined as the ratio between the small-signal base-emitter voltage v_{BE} and emitter current i_B [SS16]:

$$r_\pi = \frac{v_{BE}}{i_B} \tag{2.6}$$

The transconductance g_m gives the relationship between the transistor's small-signal output current i_C and voltage v_{BE}, which can be regarded as the transistor's input voltage. The transconductance is calculated by the following equation [SS16]:

$$g_m = \left.\frac{\delta i_C}{\delta v_{BE}}\right|_{OP} \tag{2.7}$$

An important metric of the high-frequency performance of a transistor is the transit frequency f_T. This is the frequency where the current gain of the transistor equals 1. The transit frequency is given by the two dominant parasitic capacitances of the transistor's small-signal model, namely C_π and C_μ. The formula for the calculation of f_T is [TS02]:

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{2.8}$$

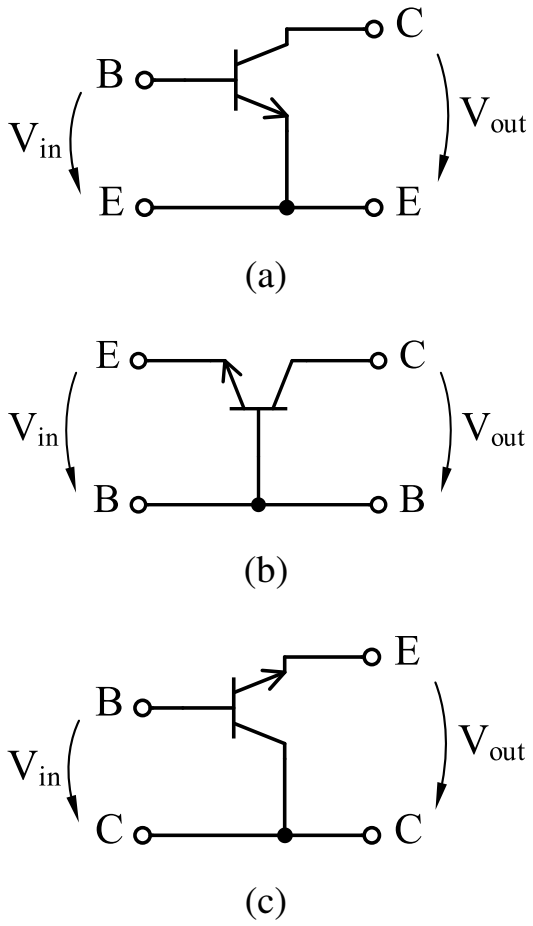


Figure 2.9: Basic amplifier topologies: (a) common emitter, (b) common base, (c) common collector.

2.3 Basic Amplifiers

There are three possibilities to realize an amplifier circuit by means of a transistor. Depending on which of the transistor terminals are connected to ground or supply voltage (or any other DC bias voltage), three basic amplifier topologies can be realized: the common-emitter, the common-base or the common-collector amplifier, as shown in Fig. 2.9 [Ell07]. Thus, the terminal connected to ground or supply voltage is common to both the input and output of the circuit. These amplifier topologies have different characteristics, therefore the choice which topology to use depends on the system requirements. In the following three subsections, an analysis of the basic amplifiers is done in order to investigate their characteristics.

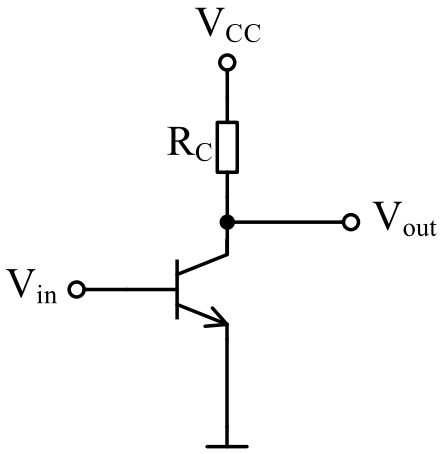


Figure 2.10: Common-emitter circuit.

2.3.1 Common-Emitter Amplifier

The common-emitter circuit is shown in Fig. 2.10. The emitter terminal is connected to ground and is common to both the input and the output of the circuit. The collector resistance R_C is connected to the supply voltage V_{CC}. The transistor's collector terminal represents the output of the circuit.

The large-signal behavior of a common-emitter amplifier is illustrated in Fig. 2.11 (a). The output voltage V_{out} remains constant and equals the supply voltage V_{CC} as long as no collector current I_C is flowing through the transistor. Once the threshold voltage $V_{in} = V_{BE} = V_{BE,0}$ is reached, the transistor starts conducting and its output voltage becomes:

$$V_{out} = V_{CC} - R_C I_C \tag{2.9}$$

In order to characterize the small-signal behavior of the circuit, a linear operation is assumed around the chosen OP for very low input voltage amplitudes (Fig. 2.11 (a)). The resulting input and output voltages are shown in Fig. 2.11 (b) and (c), respectively.

Next, the choice of the OP of the common-emitter amplifier is described [Ell07]. Fig. 2.12 illustrates several OPs based on the transistor's I_C-V_{CE} diagram. Since $V_{out} = V_{CE}$ and given the equation (2.9), the resistor R_C determines the slope of the operating line. $V_{CE,min}$ represents the minimum collector-emitter voltage for which the transistor still operates in the forward-

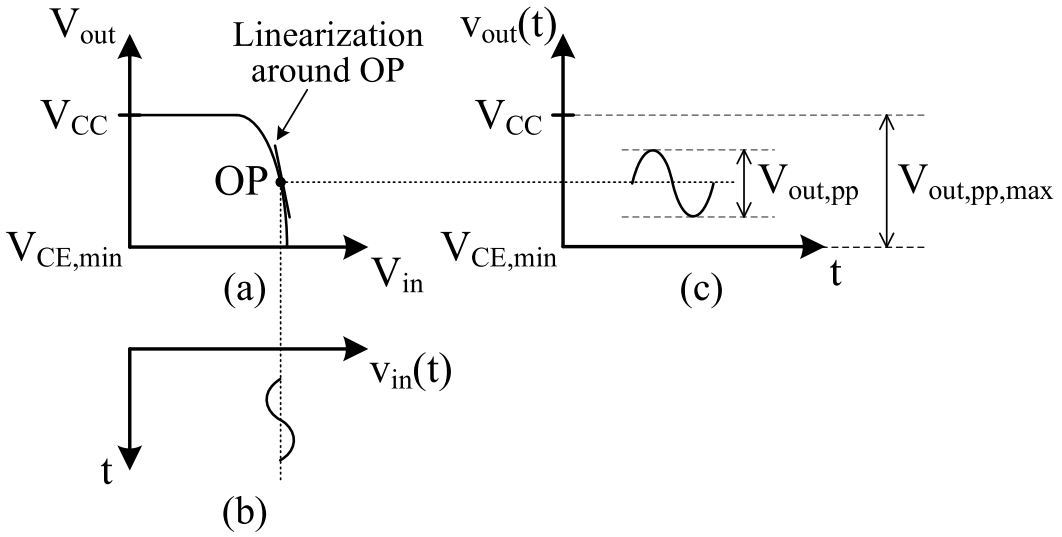


Figure 2.11: Large-signal behavior of the common-emitter amplifier and the small-signal linearization around the operating point.

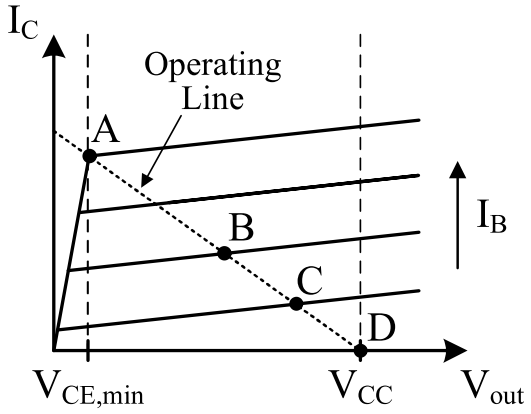


Figure 2.12: Choice of the operating point for the common-emitter amplifier.

active region (for the depicted operating line). The highest amplification is reached in point *A*, which yields the highest amount of collector current. Nevertheless, a symmetrical drive of the transistor is not possible, since the OP is close to $V_{CE,min}$. In order to guarantee a linear operation with a minimal amount of distortions, the transistor needs to be operated in point *B*. However, this OP implies a high dissipation of DC power. Point *C* is suitable for low-noise applications: the shot noise, which is dominant in bipolar transistors, increases with I_C; however, for a too low I_C the BJT behaves as a passive RC network, showing a high thermal noise. Therefore, the choice of this OP rep-

resents an optimum I_C targeting the lowest amount of noise. Finally, point D is used for applications requiring a high power efficiency, since the collector current at this OP is close to 0.

Next, we shall analyze the small-signal behavior of the common-emitter amplifier. To this end, the inverse hybrid parameters of the circuit are used [TS02]:

$$\begin{aligned} i_{in} &= g_{11} v_{in} + g_{12} i_{out} \\ v_{out} &= g_{21} v_{in} + g_{22} i_{out} \end{aligned} \tag{2.10}$$

Based on the inverse hybrid parameters, the following small-signal parameters of the circuit are defined:

$$g_{21} = a_v = \left. \frac{v_{out}}{v_{in}} \right|_{i_{out}=0} \tag{2.11}$$

as the small-signal voltage gain of the circuit,

$$g_{22} = r_{out} = \left. \frac{v_{out}}{i_{out}} \right|_{v_{in}=0} \tag{2.12}$$

as the small-signal output resistance of the circuit, and

$$g_{11} = r_{in}^{-1} = \left. \frac{i_{in}}{v_{in}} \right|_{i_{out}=0} \tag{2.13}$$

as the small-signal input conductance of the circuit. Next, we shall derive these parameters based on the small-signal equivalent circuit model depicted in Fig. 2.13. The Early effect is neglected, since it is assumed that the tran-

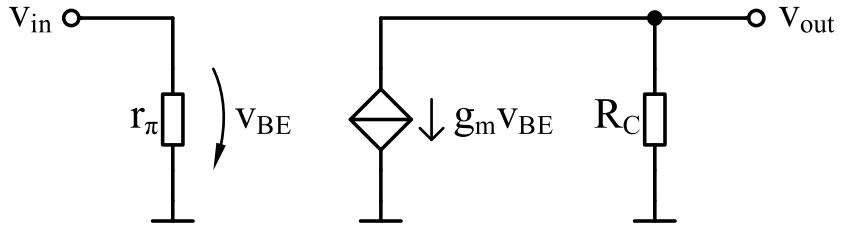


Figure 2.13: Small-signal equivalent circuit of the common-emitter amplifier.

sistor's output resistance described by equation (2.5) is much greater than the collector resistance R_C.

First, we shall calculate the the small-signal voltage gain a_v, as defined in equation (2.11). To begin with, we express the output voltage v_{out} as:

$$v_{out} = -g_m v_{BE} R_C \tag{2.14}$$

With $v_{in} = v_{BE}$ and by inserting equation (2.14) in equation (2.11), we obtain the following relation for the small-signal voltage gain:

$$\begin{aligned} a_v &= \frac{-g_m v_{in} R_C}{v_{in}} \\ &= -g_m R_C \end{aligned} \tag{2.15}$$

Next, we investigate the small-signal output resistance of the common-emitter amplifier. Since the condition for calculating the output resistance is $v_{in} = 0$ (as defined in equation (2.12)) and therefore $v_{BE} = v_{in} = 0$, the output resistance equals the collector resistance R_C.

Finally, the small-signal input resistance of the common-emitter amplifier equals the base-emitter small-signal resistance r_π, as it can be seen in Fig. 2.13.

2.3.2 Common-Base Amplifier

The common-base amplifier is shown in Fig. 2.14. For this amplifier topology, the base is shared between the input and output of the circuit and is connected to ground (or to a DC bias voltage). The equivalent small-signal circuit model is shown in Fig. 2.15.

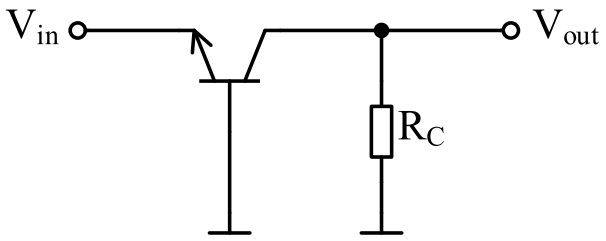


Figure 2.14: Common-base circuit.

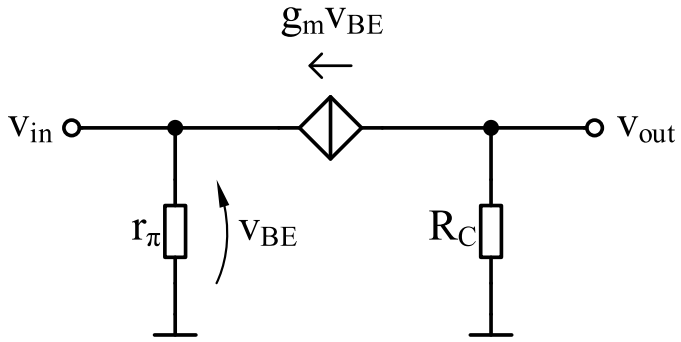


Figure 2.15: Small-signal equivalent circuit of the common-base amplifier.

We shall first calculate the small-signal voltage gain of the circuit. Similarly to the common-emitter amplifier, we express the output voltage as:

$$v_{out} = -g_m v_{BE} R_C \tag{2.16}$$

considering that $v_{in} = -v_{BE}$, we insert equation (2.16) in equation (2.11) and we obtain the following formula for the small-signal voltage gain of the common-base amplifier:

$$\begin{aligned} a_v &= \frac{-g_m v_{BE} R_C}{-v_{BE}} \\ &= g_m R_C \end{aligned} \tag{2.17}$$

The calculated gain is similar to the gain of the common-emitter amplifier, except that it has a positive sign. This is of great importance for the bandwidth of the circuit, since the Miller effect is considerably reduced, as it will be explained in Subsection 2.3.6.

Next, we investigate the amplifier's small-signal output resistance. As for the common-emitter amplifier, the condition for calculating the output resistance is the shorted input ($v_{in} = 0$, equation (2.12)). With $v_{BE} = -v_{in} = 0$ and therefore $g_m v_{BE} = 0$, the output resistance equals the collector resistance R_C.

Finally, we calculate the small-signal input resistance, as defined in equation (2.13). We first express the input current as:

$$\begin{aligned} i_{in} &= -\frac{v_{BE}}{r_\pi} - g_m v_{BE} \\ &= v_{in}\left(g_m + \frac{1}{r_\pi}\right) \\ &= v_{in}\frac{1+g_m r_\pi}{r_\pi} \end{aligned} \tag{2.18}$$

assuming that $g_m r_\pi \gg 1$ and inserting equation (2.18) in equation (2.13), we obtain the following small-signal input resistance:

$$r_{in} = \frac{1}{g_m} \tag{2.19}$$

Thus, contrary to the common-emitter amplifier, the small-signal input resistance of the common-base circuit is low-ohmic.

2.3.3 Common-Collector Stage

The schematic of the common-collector circuit is depicted in Fig. 2.16. Analogously to the common-emitter and common-base amplifiers, the collector terminal of the common-collector stage is connected to a constant supply voltage (or to any other DC bias voltage). The small-signal equivalent circuit model is illustrated in Fig. 2.17.

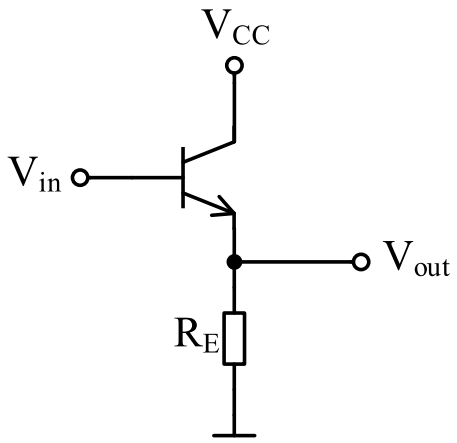


Figure 2.16: Common-collector circuit.

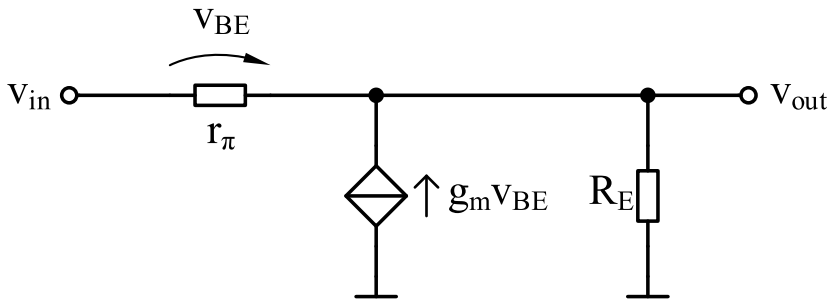


Figure 2.17: Small-signal equivalent circuit of the common-collector stage.

We begin our analysis by calculating the small-signal voltage gain of the circuit. First, we express the output voltage as:

$$\begin{aligned} v_{out} &= R_E \left(g_m v_{BE} + \frac{v_{BE}}{r_\pi} \right) \\ &= R_E v_{BE} \left(g_m + \frac{1}{r_\pi} \right) \\ &= R_E v_{BE} \frac{1 + g_m r_\pi}{r_\pi} \end{aligned} \tag{2.20}$$

assuming that $g_m r_\pi \gg 1$, equation (2.20) becomes:

$$v_{out} = g_m v_{BE} R_E \tag{2.21}$$

Next, we express the input voltage as:

$$v_{in} = v_{BE} + v_{out} \tag{2.22}$$

Inserting equation (2.21) in equation (2.22), we obtain:

$$\begin{aligned} v_{in} &= v_{BE} + g_m v_{BE} R_E \\ &= v_{BE}(1 + g_m R_E) \end{aligned} \tag{2.23}$$

Inserting equations (2.21) and (2.23) in equation (2.11), we obtain the following formula for the small-signal voltage gain:

$$\begin{aligned} a_v &= \frac{g_m v_{BE} R_E}{v_{BE}(1+g_m R_E)} \\ &= \frac{g_m R_E}{1+g_m R_E} \end{aligned} \tag{2.24}$$

Assuming that $g_m R_E \gg 1$, we conclude from equation (2.24) that the small-signal voltage gain of the common-collector circuit is approximately 1, meaning that this topology has no voltage gain. Since the voltage at the emitter of the transistor (i.e. the output of the circuit) is almost equal to the voltage at the base (i.e. the input), the common-collector circuit is also known as emitter follower (EF).

Further, we calculate the small-signal output resistance. With the condition that $v_{in} = 0$ (equation (2.12)), it results that $v_{out} = -v_{BE}$. Next, we define the output current as:

$$\begin{aligned} i_{out} &= -g_m v_{BE} - \frac{v_{BE}}{r_\pi} + \frac{v_{out}}{R_E} \\ &= g_m v_{out} + \frac{v_{out}}{r_\pi} + \frac{v_{out}}{R_E} \\ &= v_{out}\left(g_m + \frac{1}{r_\pi} + \frac{1}{R_E}\right) \\ &= g_m v_{out}\left(1 + \frac{1}{g_m r_\pi} + \frac{1}{g_m R_E}\right) \end{aligned} \tag{2.25}$$

Inserting equation (2.25) in equation (2.12) and assuming that $g_m r_\pi \gg 1$ and $g_m R_E \gg 1$, we obtain the following small-signal output resistance of the common-collector stage:

$$\begin{aligned} r_{out} &= \frac{v_{out}}{g_m v_{out}} \\ &= \frac{1}{g_m} \end{aligned} \tag{2.26}$$

which indicates a low-ohmic output.

Next, we calculate the small-signal input resistance of the common-collector

circuit. The input current can be expressed as:

$$i_{in} = \frac{v_{BE}}{r_\pi} \tag{2.27}$$

Inserting equations (2.27) and (2.23) in equation (2.13), we obtain the following expression for the small-signal input resistance:

$$\begin{aligned} r_{in} &= v_{BE}(1 + g_m R_E)\frac{r_\pi}{v_{BE}} \\ &= r_\pi(1 + g_m R_E) \\ &\approx g_m r_\pi R_E \end{aligned} \tag{2.28}$$

which indicates a high-ohmic input.

2.3.4 Comparison of the Basic Amplifier Topologies

All the above calculated parameters of the basic amplifier topologies are summarized in Table 2.1. For a comprehensive overview of the characteristics of the three topologies, a qualitative comparison is done in Table 2.2 [Ell07].

Table 2.1: Quantitative Comparison Between Basic Amplifier Topologies

	Common-Emitter	Common-Base	Common-Collector
Voltage Gain	$-g_m R_C$	$g_m R_C$	≤ 1
Output Resistance	R_C	R_C	$\frac{1}{g_m}$
Input Resistance	r_π	$\frac{1}{g_m}$	$g_m r_\pi R_E$

Table 2.2: Qualitative Comparison Between Basic Amplifier Topologies

	Common-Emitter	Common-Base	Common-Collector
Voltage Gain	High	High	≤ 1
Output Impedance	High	High	Low
Input Impedance	High	Low	High
Current Gain	High	≤ 1	High
Bandwidth	Average	High	High

2.3.5 Common-Emitter with Current-Type Negative Feedback

From all the basic amplifier topologies presented in the previous three subsections, the common-emitter stage is one of the most widely used in the realization of modulator or laser driver circuits, thanks to its high input and output impedance and its high voltage gain (Table 2.2). In this section, we shall focus on the enhancement of its performance.

As equation (2.15) shows, the voltage gain of the common-emitter amplifier depends on the transistor's transconductance g_m, which depends on the transistor's OP and is a source of non-linearity. In order to make the circuit linear, a resistor R_E can be added at the emitter of the transistor. This resistor is therefore called emitter-degeneration resistor and it realizes a current-type negative feedback. The resulting common-emitter amplifier is shown in Fig. 2.18. Fig. 2.19 shows the equivalent small-signal circuit model.

In order to calculate the new voltage gain $a_{v,e}$, we start from the input voltage v_{in}:

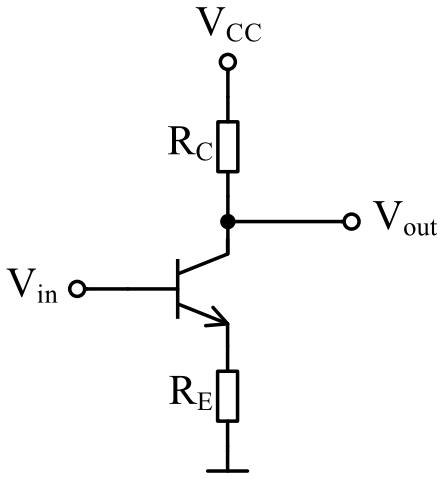


Figure 2.18: Common-emitter amplifier with emitter-degeneration resistor.

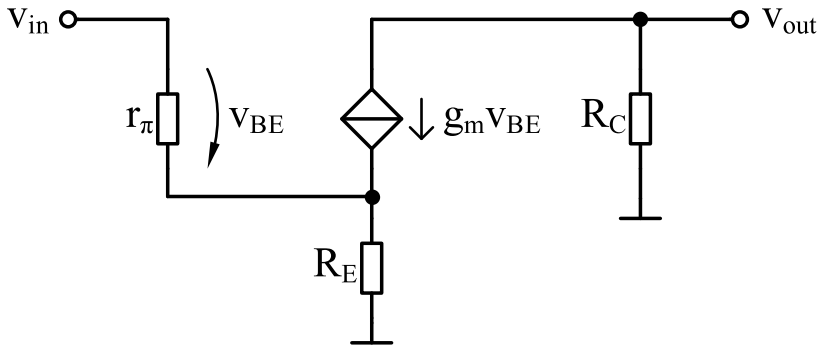


Figure 2.19: Equivalent small-signal circuit model of the common-emitter with emitter-degeneration.

$$\begin{aligned} v_{in} &= v_{BE} + v_{R_E} \\ &= i_B r_\pi + (i_B + i_C) R_E \end{aligned} \tag{2.29}$$

With $i_B = \frac{i_C}{b_i}$ and $r_\pi = \frac{b_i}{g_m}$, equation (2.29) becomes:

$$\begin{aligned} v_{in} &= \frac{i_C}{b_i}\frac{b_i}{g_m} + \left(\frac{i_C}{b_i} + i_C\right) R_E \\ &= \frac{i_C}{g_m} + i_C \left(\frac{b_i + 1}{b_i}\right) R_E \end{aligned} \tag{2.30}$$

With $\frac{b_i+1}{b_i} \approx 1$, equation (2.30) becomes:

$$v_{in} = i_C \left(\frac{1}{g_m} + R_E \right) \tag{2.31}$$

With the output voltage

$$v_{out} = -i_C R_C \tag{2.32}$$

the voltage gain of the common-emitter amplifier with resistive emitter degeneration is calculated as:

$$\begin{aligned} a_{v,e} &= \frac{v_{out}}{v_{in}} \\ &= \frac{-i_C R_C}{i_C \left(\frac{1}{g_m} + R_E \right)} \\ &= -\frac{g_m R_C}{1 + g_m R_E} \end{aligned} \tag{2.33}$$

Compared to the small-signal voltage gain of the common-emitter amplifier in equation (2.15), the gain of the amplifier with emitter degeneration resistor is reduced by the factor $(1 + g_m R_E)$. However, as equation (2.33) shows, the gain $a_{v,e}$ is less dependent on the transistor's parameter g_m. Thus, if a sufficiently large resistor R_E is chosen, the gain of the common-emitter amplifier with resistive emitter-degeneration is approximately $a_{v,e} \approx -\frac{R_C}{R_E}$, which is constant and therefore indicates a linear behavior of the amplifier.

Besides linearity, applying current-type negative feedback to the common-emitter amplifier further increases the input impedance of the circuit as well as its bandwidth [SS16]. Moreover, by minimizing the dependence of the voltage gain on the transistor's small-signal parameters, the circuit is less sensitive to temperature and process variations.

2.3.6 Cascode Amplifier

In order to increase the small-signal output resistance, the voltage gain as well as the bandwidth of a common-emitter circuit, two basic amplifier stages can be cascaded, namely a common-emitter and a common-base stage. Such a

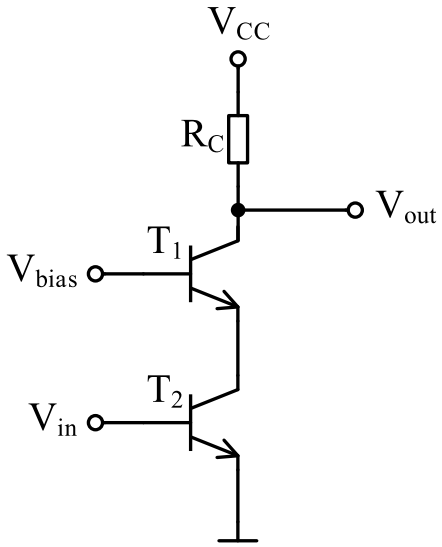


Figure 2.20: Cascode amplifier.

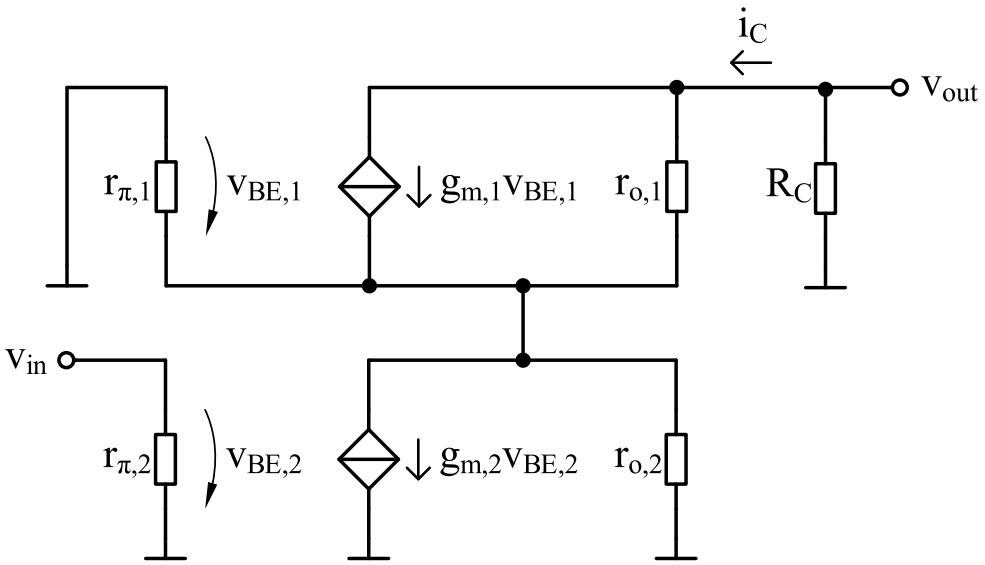


Figure 2.21: Equivalent small-signal circuit model of the cascode amplifier.

circuit is called cascode amplifier and is shown in Fig. 2.20. The equivalent small-signal circuit is shown in Fig. 2.21.

To begin with, we shall explain the Miller effect. This effect is illustrated in Fig. 2.22. It manifests itself when a capacitor C_f is fed back from the output to the input of an inverted amplifier. As a consequence of the Miller effect, the capacitor will be seen at the input of the amplifier magnified by the factor

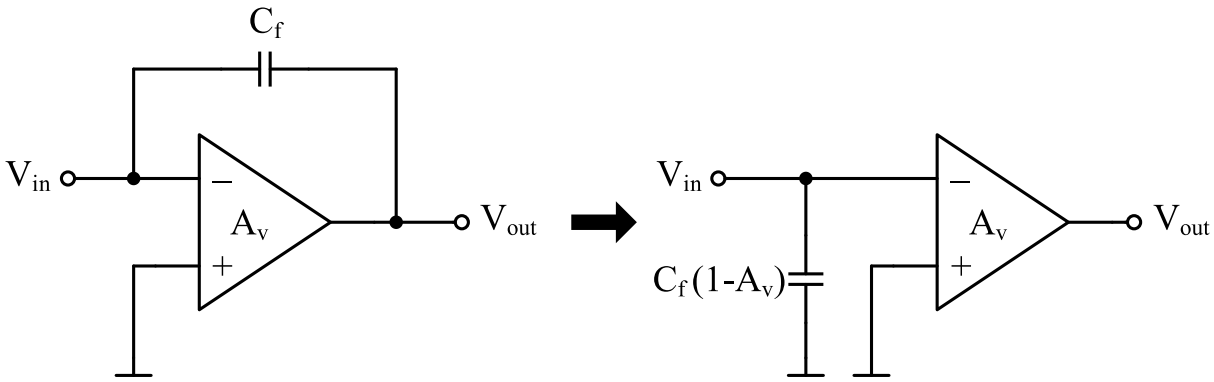


Figure 2.22: The Miller effect.

$(1-A_v)$, where A_v is the voltage gain of the amplifier. For the common-emitter stage, the capacitance which is fed back from the output to the input of the circuit is represented by the transistor's base-collector capacitance C_μ (Fig. 2.8). As the small-signal voltage gain of the common-emitter stage is high and negative (equation (2.15)), the Miller capacitance that is created at the input is considerable, thus lowering the overall bandwidth of the circuit.

In a cascode amplifier, the common-emitter stage (T_2 in Fig. 2.20) is followed by a common-base stage (T_1) in order to neutralize the Miller-effect (since the latter stage shows a high, but positive voltage gain, thus having a low parasitic Miller capacitance). Since the common-base stage acts as a load for the common-emitter stage, the common-emitter's voltage gain $a_{v,2}$ can be expressed as:

$$a_{v,2} = -g_{m,2} r_{\pi,1} \tag{2.34}$$

where $r_{\pi,1}$ is the small-signal input resistance of the common-base stage. With $r_{\pi,1} = \frac{b_{i,1}}{g_{m,1}}$ and considering the fact that the common-base circuit has a low current gain ($b_i \leq 1$), equation (2.34) becomes:

$$\begin{aligned} a_{v,2} &= -g_{m,2} \frac{b_{i,1}}{g_{m,1}} \\ &\approx -g_{m,2} \frac{1}{g_{m,1}} \end{aligned} \tag{2.35}$$

Assuming that the two transistors T_1 and T_2 have equal geometries and are

biased under similar conditions, we consider that $g_{m,1} = g_{m,2}$. Thus, equation (2.35) yields that $a_{v,2} \approx -1$. Therefore, we conclude that the common-emitter stage of a cascode amplifier does not generate a considerable parasitic Miller capacitance at the input.

The small-signal voltage gain of the common-base stage is given by the following formula:

$$a_{v,1} = g_{m,1} r_{out,c} \tag{2.36}$$

where $r_{out,c}$ is the small-signal output resistance of the cascode amplifier. Thus, in order to determine the overall voltage gain $a_{v,c} = a_{v,1} a_{v,2}$ of the cascode stage, we first need to calculate its output resistance. To begin with, we omit the load resistor R_C. Based on the small-signal equivalent circuit in Fig. 2.21, we write:

$$r'_{out,c} = \left. \frac{v_{out}}{i_C} \right|_{v_{in}=0} \tag{2.37}$$

where i_C is the small-signal collector current of T_1 and T_2. The output voltage v_{out} of the cascode amplifier can be expressed as:

$$v_{out} = v_{o,1} + v_{o,2} \tag{2.38}$$

where $v_{o,1}$ and $v_{o,2}$ are the voltages over the output resistances $r_{o,1}$ and $r_{o,2}$ of the common-base and common-emitter stages, respectively. Since $v_{BE,2} = v_{in} = 0$ and subsequently the current $g_{m,2} v_{BE,2} = 0$, voltage $v_{o,2}$ is calculated as follows:

$$v_{o,2} = i_C r_{o,2} \tag{2.39}$$

Voltage $v_{o,1}$ is calculated as follows:

$$v_{o,1} = (i_C - g_{m,1} v_{BE,1}) r_{o,1} \tag{2.40}$$

With $v_{BE,1} = -v_{o,2}$ and considering equation (2.39), equation (2.40) becomes:

$$v_{o,1} = (i_C + g_{m,1} i_C r_{o,2}) r_{o,1} \tag{2.41}$$

Thus, the output voltage of the cascode stage becomes:

$$\begin{aligned} v_{out} &= v_{o,1} + v_{o,2} \\ &= (i_C + g_{m,1} i_C r_{o,2}) r_{o,1} + i_C r_{o,2} \\ &= i_C (r_{o,1} + r_{o,2} + g_{m,1} r_{o,1} r_{o,2}) \end{aligned} \tag{2.42}$$

Inserting equation (2.42) in equation (2.37) we obtain the expression for the small-signal output resistance of the cascode amplifier (while omitting R_C):

$$r'_{out,c} = r_{o,1} + r_{o,2} + g_{m,1} r_{o,1} r_{o,2} \tag{2.43}$$

Under the assumption of equal transistors T_1 and T_2 biased under equal conditions, equation (2.43) becomes:

$$\begin{aligned} r'_{out,c} &= 2r_o + g_m r_o^2 \\ &\approx g_m r_o^2 \end{aligned} \tag{2.44}$$

Inserting the newly calculated $r'_{out,c}$ in equation (2.36) and while still omitting R_C, we obtain:

$$a'_{v,1} = g_m^2 r_o^2 \tag{2.45}$$

which results in a total small-signal voltage gain of the cascode amplifier $a'_{v,1}$ (without resistor R_C) of:

$$\begin{aligned} a'_{v,c} &= a_{v,1} a'_{v,2} \\ &= -g_m^2 r_o^2 \end{aligned} \tag{2.46}$$

Both equations (2.44) and (2.46) indicate a very high small-signal output resistance and voltage gain of the cascode amplifier compared to the common-emitter stage. Nevertheless, the total output resistance of the cascode amplifier is also influenced by the load resistor R_C:

$$r_{out,c} = r'_{out,c} \parallel R_C \tag{2.47}$$

Therefore, in order to take full advantage of the cascode amplifier's high output resistance and voltage gain, it is reasonable to choose a high-impedance load.

2.3.7 Differential Amplifier

The amplifiers presented so far are single-ended, having one input and one output. Therefore, they amplify not only the main signal, but also unwanted spurious signals. By placing two amplifiers symmetrically, it is possible to drive them in a differential manner, thus amplifying only the difference between two input signals of opposite phases (differential signals), while suppressing the unwanted common-mode signals. Such a circuit is called differential amplifier and is illustrated in Fig. 2.23. It consists of two common-emitter stages sharing the emitter terminal, and a current source which yields the tail current I_{CC}. The purpose of the current source is to provide the bias current for transistors T_1 and T_2 and to keep the sum of the two collector currents $I_{C,1}$ and $I_{C,2}$ constant.

We begin the analysis of the circuit from equation (2.1):

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{2.48}$$

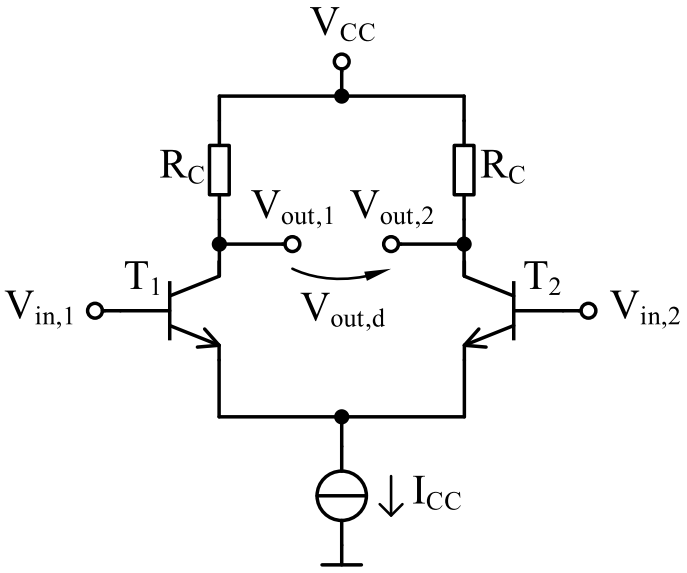


Figure 2.23: Differential amplifier.

Assuming that $I_C \gg I_B$, the tail current I_{CC} is defined as:

$$I_{CC} = I_{C,1} + I_{C,2} \tag{2.49}$$

Next, we define the output differential current $I_{out,d}$ as:

$$I_{out,d} = I_{C,1} - I_{C,2} \tag{2.50}$$

Finally, we define the input differential voltage $V_{in,d}$ as:

$$\begin{aligned} V_{in,d} &= V_{in,1} - V_{in,2} \\ &= V_{BE,1} - V_{BE,2} \end{aligned} \tag{2.51}$$

From the following two relations:

$$I_{C,1} - I_{C,2} = I_S \left(e^{\frac{V_{BE,1}}{V_T}} - e^{\frac{V_{BE,2}}{V_T}} \right) \tag{2.52}$$

and

$$I_{C,1} + I_{C,2} = I_S \left(e^{\frac{V_{BE,1}}{V_T}} + e^{\frac{V_{BE,2}}{V_T}} \right) \tag{2.53}$$

we get the ratio:

$$\frac{I_{C,1} - I_{C,2}}{I_{C,1} + I_{C,2}} = \frac{e^{\frac{V_{BE,1}}{V_T}} - e^{\frac{V_{BE,2}}{V_T}}}{e^{\frac{V_{BE,1}}{V_T}} + e^{\frac{V_{BE,2}}{V_T}}} \tag{2.54}$$

By applying the following definition of the hyperbolic tangent function:

$$\tanh(x) = \frac{e^x - e^{-x}}{e^x + e^{-x}} \tag{2.55}$$

and after several calculations, equation (2.54) becomes:

$$\begin{aligned} \frac{I_{C,1} - I_{C,2}}{I_{C,1} + I_{C,2}} &= \tanh \left(\frac{V_{BE,1} - V_{BE,2}}{2V_T} \right) \Leftrightarrow \\ \Leftrightarrow I_{out,d} &= I_{CC} \tanh \left(\frac{V_{in,d}}{2V_T} \right) \end{aligned} \tag{2.56}$$

Considering equations (2.49), (2.50) and (2.56), the collector currents $I_{C,1}$ and $I_{C,2}$ can be expressed as:

$$\begin{aligned} I_{C,1} &= \frac{I_{CC} + I_{out,d}}{2} \\ &= \frac{I_{CC}}{2}\left(1 + \tanh\frac{V_{in,d}}{2V_T}\right) \end{aligned} \tag{2.57}$$

and

$$\begin{aligned} I_{C,2} &= \frac{I_{CC} - I_{out,d}}{2} \\ &= \frac{I_{CC}}{2}\left(1 - \tanh\frac{V_{in,d}}{2V_T}\right) \end{aligned} \tag{2.58}$$

Based on equations (2.56), (2.57) and (2.58), diagram 2.24 can be drawn, which illustrates the dependence of the two collector currents $I_{C,1}$ and $I_{C,2}$ as well as of the output differential current $I_{out,d}$ on the input differential voltage $V_{in,d}$. Thus, a differential amplifier switches almost all the tail current I_{CC} between the two transistors T_1 and T_2, provided that the input differential voltage is sufficiently high. However, for small $V_{in,d}$, the differential amplifier shows a linear behavior, the transfer function being approximately:

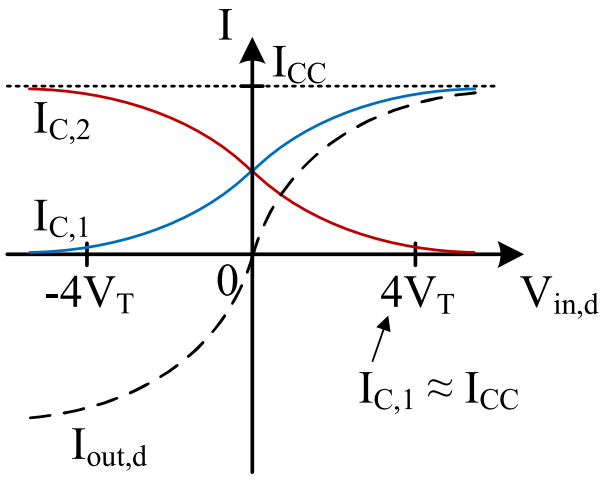


Figure 2.24: Transfer characteristics of the differential amplifier.

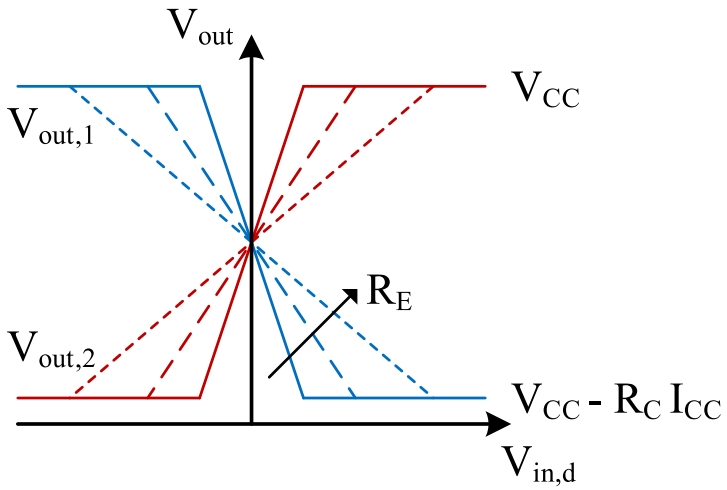


Figure 2.25: Conceptual representation of the linearization of a differential amplifier by means of emitter-degeneration resistors R_E.

$$I_{out,d} = I_{CC}\left(\frac{V_{in,d}}{2V_T}\right) \tag{2.59}$$

In order to increase the linear operation range of the differential amplifier, the resistive emitter degeneration technique is employed, which was described in Section 2.3.5. Nevertheless, as for the common-emitter stage with current-type negative feedback, the voltage gain of the circuit is reduced. Fig. 2.25 shows the effect of the emitter-degeneration resistors R_E on the transfer characteristics of the differential amplifier. As it can be seen, a higher R_E means a higher linear operation range, however the gain of the differential amplifier is decreased. Therefore, in case that both a high output voltage swing and a high linearity are required, the tail current of the circuit has to be increased, which considerably increases the power consumption.

2.4 High-Swing Amplifier

Based on the basic amplifier topologies presented in the previous section, more complex circuit architectures can be realized, with enhanced functions and parameters. One very important parameter for amplifier circuits is the maximum achievable output voltage swing.

Mach-Zehnder modulators are widely employed in the front-ends of electro-optical communication systems. Such modulators require high voltage swings in order to efficiently convert the electrical data into optical data. Nevertheless, the maximum output voltage swing that can be provided by an amplifier circuit is limited by the collector-emitter breakdown voltage (BV_{CE}) of the output bipolar transistors, or the drain-source breakdown voltage (BV_{DS}) of the field-effect transistors. This voltage is given by the technology specifications and represents a major design constraint. Therefore, special circuit topologies need to be investigated in order to overcome this limitation.

2.4.1 Physics of the Transistor Breakdown Process

In this subsection, we provide a brief description of the breakdown process in a bipolar transistor. For a better visualization, this process is illustrated in Fig. 2.26. We assume a V_{CE} voltage applied over the collector and emitter of the transistor, where the collector potential V_C is higher than the emitter potential V_E. The base of the transistor is initially left open, the base current I_B being thus equal to 0.

The base-collector *pn*-junction is reversed biased and shows a reverse saturation current. This current is caused by the minority charge carriers in the *n*-doped collector and *p*-doped base region, respectively, which cross the *pn*-junction. Holes are therefore injected from the collector region into the

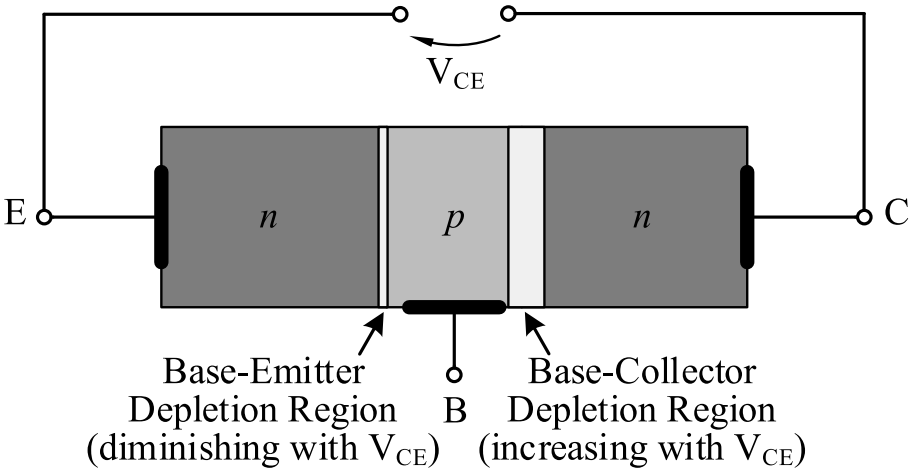


Figure 2.26: Physics of the breakdown process in the *npn* transistor.

base, and drift further towards the base-emitter *pn*-junction. In turn, electrons are injected from the emitter region into the base, and move further towards the base-collector junction. As the V_{CE} voltage increases, a chain reaction occurs: more holes arrive at the base-emitter junction, thus making it narrower [MH07]. A narrower base-emitter junction means a lower barrier for the electrons in the emitter, so that more electrons are injected into the base and afterwards into the base-collector junction, which keeps widening [MH07]. The increase of V_{CE} causes the increase of the electric field in the depletion region of the base-collector junction. Therefore, the drift velocity of the electrons in this region increases, and their collision with atoms produces more electron-hole pairs, which further speeds up the chain event. This phenomenon is called avalanche breakdown [SS16]. When $V_{CE} = BV_{CE}$, the current through the transistor rises exponentially and the transistor enters into breakdown.

So far, we have regarded the case where the base of the bipolar transistor is left open. If a certain impedance is available at the transistor's base, some of the holes injected from the base-collector junction into the base will be prevented from arriving at the base-emitter region, being absorbed by the base terminal instead. Therefore, the transistor breakdown will occur at a higher V_{CE}. The following relationship can be established between various BV_{CE} depending on the impedance seen at the base of the transistor [TS02]:

$$BV_{CE,\,open\ base} < BV_{CE,\,base\ impedance} < BV_{CE,\,shorted\ base} \tag{2.60}$$

2.4.2 Circuit Concept

A way to overcome the limitation imposed by the breakdown voltage of the transistors and increase the maximum achievable voltage swing at the output of a driver circuit is to use a cascaded transistor structure. Nevertheless, a basic cascode amplifier, as presented in Section 2.3.6, would not be sufficient to accomplish the task of increasing the output voltage swing. Fig. 2.27 (a) illustrates a basic cascode amplifier. The upper transistor T_1' is a common-base circuit and its base is connected to a constant DC bias voltage. Be-

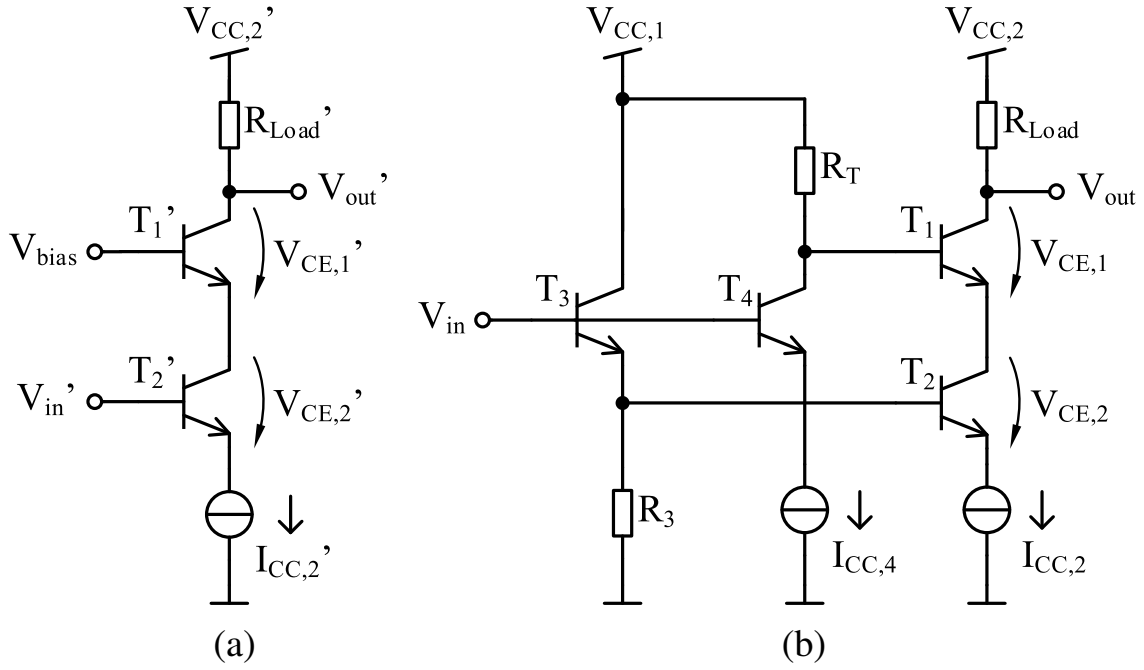


Figure 2.27: (a) Basic cascode amplifier; (b) Breakdown Voltage Doubler [GBK+18a]†. ©[2018] IEEE

cause of this, and due to the fact that the transistor's base-emitter voltage V_{BE} varies logarithmically with the transistor's collector current I_C (as shown in Fig. 2.6), the voltage $V'_{BE,1}$ of transistor T'_1 and thus the voltage at the emitter of T'_1 change only slightly. Therefore, the collector-emitter voltage $V'_{CE,2}$ of transistor T'_2 remains largely constant during the whole operation of the driver. This means that almost the whole output voltage swing of the driver falls over the upper transistor T'_1, which can go into breakdown in the case of a too large swing.

In order to distribute equally the output voltage swing between the two cascaded transistors, the base of T'_1 should vary in a synchronized manner with the base of T'_2. This is done by adding a common-emitter circuit T_4 (Fig. 2.27 (b)) with the load resistor R_T that drives the base of the upper transistor T_1 [MH07]. Both the common-emitter circuit T_4 and the base of transistor T_2 are connected to the input V_{in} of the circuit (transistor T_2 is connected via the common-collector stage T_3). By this means, the bases of the two cascaded transistors T_1 and T_2 are driven in a synchronized manner and the output voltage swing is divided equally between them, with $V_{CE,1} = V_{CE,2}$

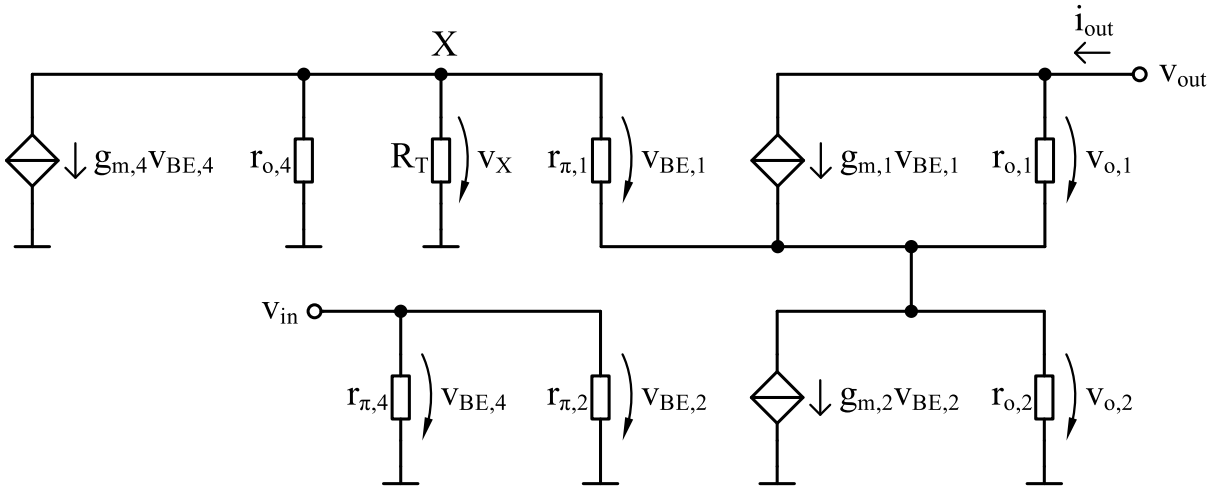


Figure 2.28: Equivalent small-signal circuit model of the breakdown voltage doubler topology.

during the whole operation of the driver. This circuit topology is called breakdown voltage doubler [MH07], since it doubles the maximum achievable output voltage swing of the circuit by driving the two output transistors close to their BV_{CE}, however without exceeding it.

2.4.3 Circuit Analysis

In this subsection, the small-signal circuit behavior of the breakdown voltage doubler topology is studied. The equivalent small-signal model of this topology is shown in Fig. 2.28 (without load resistors). The emitter-follower stage represented by transistor T_3 was neglected, since it does not affect the small-signal behavior of the circuit.

First, we calculate the small-signal gain $a_{v,BVD}$:

$$a_{v,BVD} = \left.\frac{v_{out}}{v_{in}}\right|_{i_{out}=0} \tag{2.61}$$

The small-signal output voltage v_{out} can be defined as follows:

$$\begin{aligned} v_{out} &= v_{o,1} + v_{o,2} \\ &= -g_{m,1}v_{BE,1}r_{o,1} - g_{m,2}v_{BE,2}r_{o,2} \end{aligned} \tag{2.62}$$

Next, we define voltage v_X between node X an ground as:

$$v_X = v_{BE,1} + v_{o,2} \tag{2.63}$$

Assuming the collector current of transistor T_4 much larger than the base current of transistor T_1, voltage v_X can also be expressed as:

$$v_X = -g_{m,4} v_{BE,4} (r_{o,4} \parallel R_T) \tag{2.64}$$

Inserting equation (2.64) in equation (2.63) and assuming that $r_{o,4} \gg R_T$, we obtain:

$$-g_{m,4} v_{BE,4} R_T = v_{BE,1} + v_{o,2} \tag{2.65}$$

Considering voltage $v_{o,2}$ as expressed in equation (2.62) and the fact that $v_{BE,4} = v_{BE,2} = v_{in}$, equation (2.65) becomes:

$$-g_{m,4} v_{in} R_T = v_{BE,1} - g_{m,2} v_{in} r_{o,2} \tag{2.66}$$

Therefore, voltage $v_{BE,1}$ can be expressed as:

$$v_{BE,1} = v_{in}(g_{m,2} r_{o,2} - g_{m,4} R_T) \tag{2.67}$$

Inserting equation (2.67) in equation (2.62), we obtain:

$$\begin{aligned} v_{out} &= -g_{m,1} r_{o,1} (g_{m,2} r_{o,2} - g_{m,4} R_T) v_{in} - g_{m,2} r_{o,2} v_{in} \\ &= v_{in}(-g_{m,1} g_{m,2} r_{o,1} r_{o,2} + g_{m,1} g_{m,4} r_{o,1} R_T - g_{m,2} r_{o,2}) \\ &= v_{in}(g_{m,2} r_{o,2}(-g_{m,1} r_{o,1} - 1) + g_{m,1} g_{m,4} r_{o,1} R_T) \\ &\approx v_{in}(-g_{m,1} g_{m,2} r_{o,1} r_{o,2} + g_{m,1} g_{m,4} r_{o,1} R_T) \end{aligned} \tag{2.68}$$

Therefore, the small-signal voltage gain of the breakdown voltage doubler topology is expressed as follows:

$$\begin{aligned} a_{v,BVD} &= \left.\frac{v_{out}}{v_{in}}\right|_{i_{out}=0} \\ &= -g_{m,1}g_{m,2}r_{o,1}r_{o,2} + g_{m,1}g_{m,4}r_{o,1}R_T \end{aligned} \tag{2.69}$$

Next, the small-signal output resistance $r_{out,BVD}$ of the circuit is calculated, which is defined as follows:

$$r_{out,BVD} = \left.\frac{v_{out}}{i_{out}}\right|_{v_{in}=0} \tag{2.70}$$

The small-signal output current is defined as:

$$\begin{aligned} i_{out} &= g_{m,1}v_{BE,1} + \frac{v_{o,1}}{r_{o,1}} \\ &\approx g_{m,2}v_{BE,2} + \frac{v_{o,2}}{r_{o,2}} \end{aligned} \tag{2.71}$$

Since the condition assumed for the calculation of the output resistance is $v_{in} = 0$, and as $v_{BE,2} = v_{in}$, from equation (2.71) it results that:

$$\begin{aligned} i_{out} &= \frac{v_{o,2}}{r_{o,2}} \Leftrightarrow \\ \Leftrightarrow v_{o,2} &= r_{o,2}i_{out} \end{aligned} \tag{2.72}$$

Since $v_{BE,4} = v_{in} = 0$ and considering that $r_{o,4} \gg R_T$, voltage v_X is defined as:

$$v_X = -R_T\frac{v_{BE,1}}{r_{\pi,1}} \tag{2.73}$$

From equations 2.73, 2.72 and knowing that $v_X = v_{BE,1} + v_{o,2}$, it results:

$$\begin{aligned} -R_T\frac{v_{BE,1}}{r_{\pi,1}} &= v_{BE,1} + r_{o,2}i_{out} \Leftrightarrow \\ \Leftrightarrow v_{BE,1} &= -r_{o,2}\frac{r_{\pi,1}}{r_{\pi,1}+R_T}i_{out} \end{aligned} \tag{2.74}$$

With $v_{out} = v_{o,1} + v_{o,2}$ and considering equation (2.72), we obtain:

$$\begin{aligned} v_{o,1} &= v_{out} - v_{o,2} \\ &= v_{out} - r_{o,2} i_{out} \end{aligned} \tag{2.75}$$

Inserting equations 2.74 and 2.75 in equation (2.71), we obtain the following expression for the small-signal output current:

$$\begin{aligned} i_{out} &= -g_{m,1} r_{o,2} \frac{r_{\pi,1}}{r_{\pi,1} + R_T} i_{out} + \frac{v_{out} - r_{o,2} i_{out}}{r_{o,1}} \Leftrightarrow \\ \Leftrightarrow i_{out} &\left(1 + g_{m,1} r_{o,2} \frac{r_{\pi,1}}{r_{\pi,1} + R_T} + \frac{r_{o,2}}{r_{o,1}} \right) = \frac{1}{r_{o,1}} v_{out} \end{aligned} \tag{2.76}$$

From equation (2.76), the small-signal output resistance of the breakdown voltage doubler topology is calculated as follows:

$$\begin{aligned} r_{out,BVD} &= \left. \frac{v_{out}}{i_{out}} \right|_{v_{in}=0} \\ &= r_{o,1} + r_{o,2} + g_{m,1} r_{o,1} r_{o,2} \frac{r_{\pi,1}}{r_{\pi,1} + R_T} \\ &\approx g_{m,1} r_{o,1} r_{o,2} \frac{r_{\pi,1}}{r_{\pi,1} + R_T} \end{aligned} \tag{2.77}$$

The investigation of the small-signal behavior of the breakdown voltage doubler showed that this topology has a similar (though slightly lower) small-signal voltage gain and output resistance compared to the basic cascode amplifier (equations 2.46 and 2.44, respectively). Nevertheless, the main difference between the two topologies concerns their large-signal behavior, as the breakdown voltage doubler is able to divide equally the output voltage swing between the two cascaded transistors, thus avoiding that they exceed their collector-emitter breakdown voltages.

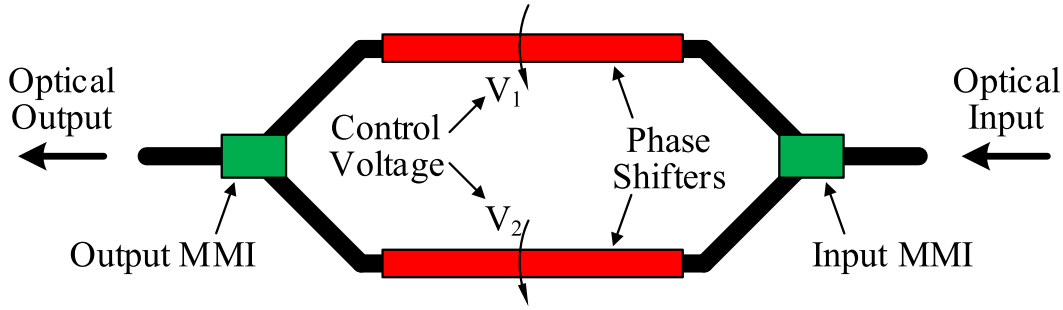


Figure 2.29: Basic MZM schematic.

2.5 Mach-Zehnder Modulator

In order to convert electrical data into optical data and transmit it via an optical fiber, either a laser diode or an electro-optical modulator in combination with a laser are required, for direct or indirect modulation, respectively. Nevertheless, for high-speed applications above 20 GHz, as well as for applications requiring a high spectral purity, the indirect modulation proved to be superior to the direct one [LMY04] [TGM+16]. There are several modulator types available, such as the electro-absorption modulator, the ring-resonator modulator and the Mach-Zehnder modulator. The electro-absorption and ring-resonator modulators are compact, have small load capacitances and require low driving voltages, however they are sensitive to process and temperature variations [QXH+16]. In comparison, MZMs, despite their large size and high driving voltage, show a high optical bandwidth, low chirp effect as well as a high thermal stability, making them reliable components for the front-ends of the electro-optical transmitters [RLP+16] [QXH+16].

Fig. 2.29 shows the basic schematic of an MZM. The modulator consists of two arms. The light of a continuous emitting laser source is fed at the modulator's optical input and subsequently divided into the two arms by means of a multi-mode interference coupler (MMI). In the output MMI coupler, the recombination of the two optical waveforms occurs. If the waveforms are in phase (i.e. if the phase shift between them is 0°), they recombine constructively, resulting in a high-intensity optical signal. This corresponds to the "1" state of a digital signal. On the contrary, if the waveforms have opposite phases (i.e. a phase shift of 180°), they recombine destructively, yielding a

low-intensity optical signal which corresponds to the ”0” state of a digital signal. The ratio between the optical power of the high-intensity waveform (P_1) and low-intensity waveform (P_0) is called extinction ratio (ER) and is usually expressed in decibel (dB) [Säc05]:

$$ER = 10\text{dB}\left(\frac{P_1}{P_0}\right) \tag{2.78}$$

The phase shift in an MZM is realized by means of phase shifters. These optical components use the electro-optic effect in order to change the phase delay of a waveform [Säc05]. Due to this effect, the refractive index of certain materials changes when an electric field is applied to them. Such materials include lithium niobate ($LiNbO_3$), gallium arsenide (GaAs), indium phosphide (InP), silicon (Si) and polymers [LMY04]. For long-distance communications, where high ERs are required, $LiNbO_3$ and InP MZMs are usually employed [QXH+16]. Nevertheless, for short- and medium-range applications such as data centers or intra-data-center communications, where low power, low cost, high speed and high integration capability are required, Si MZMs are particularly attractive, since they allow energy-efficient modulation, high bandwidth, low-cost and high-yield production as well as the possibility of full electro-optical integration on the same chip [QXH+16] [DCS+15].

The phase shifter of a Si MZM consists of a *pn*-junction. For an efficient operation, the junction must remain in the reverse bias region. The change in the refractive index of the *pn*-junction determines the phase shift of the optical waveform, depending on the voltage that is applied to the *p*- and *n*-doped region, respectively. The depletion region of the junction presents a parasitic capacitance, which, together with the series resistance of the phase shifter, represents a limitation for the bandwidth of the circuit [RLP+16].

MZMs require a certain voltage applied to their electrodes in order to produce a phase shift. This voltage is provided by a modulator driver. The relation between the driver voltage and the MZM's optical output power is given by the following formula [DCS+15]:

$$P_{out} = \frac{P_{in}}{2}\left[1+\cos\left(\pi\frac{V_{drv}}{V_\pi}\right)\right]e^{-\alpha L} \tag{2.79}$$

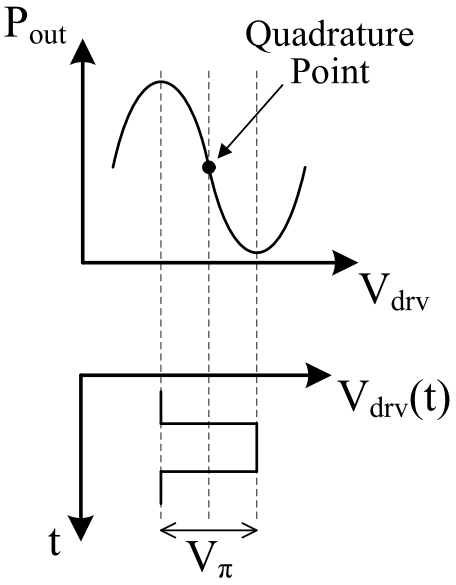


Figure 2.30: Modulation curve of an MZM.

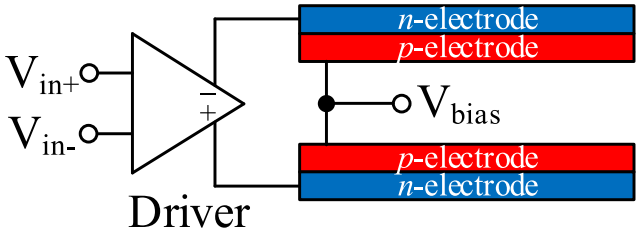


Figure 2.31: Differential push-pull driving scheme of the MZM.

where P_{out} is the MZM's output optical power, P_{in} the input power provided by the laser source to the MZM, V_{drv} the voltage provided by the driver, V_π the voltage required to produce a 180° phase shift between the two MZM arms, α the insertion loss factor (in dB/m) and L the length of the phase shifters. Thus, for $V_{drv} = nV_\pi$ with $n = 0,2,4,...$ the MZM outputs the maximum optical power, while for $V_{drv} = nV_\pi$ with $n = 1,3,5,...$ the MZM's output reaches the minimum intensity. Equation (2.79) is conceptually illustrated in Fig. 2.30.

The easiest way to drive an MZM is the single-ended driving scheme, where an RF signal is driving one of the two MZM arms, thus shifting its phase compared to the second arm. Nevertheless, a more efficient way of driving an MZM is the differential push-pull driving scheme depicted in Fig. 2.31, where both modulator arms are driven simultaneously by a differential RF

signal [QXH+16]. Such a driving scheme presents two important advantages compared to its single-ended counterpart. First, a much higher ER can be achieved with the same voltage swing of the driver. This is because the driver only needs to provide $V_{drv} = V_\pi/2$ to the modulator arms, since it drives them with opposite phases [Säc05] [QXH+16]. Second, the optical chirp effect is reduced to a minimum [Säc05]. For this driving scheme and for non-return-to-zero (NRZ) modulation, the operating point of the modulator must be set in the middle of the switching curve, also called the quadrature point [Säc05], as depicted in Fig. 2.30. Furthermore, changing the operating point allows other modulation formats such as phase modulation or quadrature-amplitude modulation (the latter requiring at least two MZMs).

The V_π of an MZM is inversely proportional to the length L of its phase shifters and is given by the constant product $V_\pi L$, also known as modulation efficiency [RLP+16]. Long-length phase shifters represent a serious limitation for the bandwidth of the modulator, pose a challenge for the matching of the propagation delays in the phase shifter's waveguides and its electrodes, and also increase considerably the overall chip size. Therefore, a key requirement of modulator drivers is a high output voltage swing, in order to allow the use of MZMs with low phase shifter lengths without sacrificing the ER of the modulator. To this end, the driver topology presented in Section 2.4 is of particular importance, since it overcomes the limitations imposed by the breakdown voltage of the transistor and enables high output voltage swings.

2.6 Concepts of MZM-Based Transmitter Front-Ends[1]

After having studied the fundamentals of electrical driver designs and of MZMs, we shall now investigate the ways of integrating the electrical and optical components with the purpose of realizing electro-optical transmitter front-ends. In this section, we shall speak about the two most commonly employed topologies for MZM-based electro-optical transmitters, namely the

1 **Copyright Note**: Section 2.6 of Chapter 2 is largely based on the IEEE publication [GBK+18b]†, in which I was the first author. The figures are specifically referenced.

segmented and the traveling-wave topology (Fig. 2.32 and 2.33, respectively).

2.6.1 Segmented Transmitter Front-End Topology

One approach of integrating the electrical driver and the MZM is the segmented topology. The block diagram is shown in Fig. 2.32. This approach uses several driver segments, which drive simultaneously the same number of phase shifter segments of the MZM. The main advantage of this topology is that the full output voltage swing of the driver is applied along the entire length of the phase shifters of the MZM, without being attenuated. For this topology, the phase shifter can simply be modeled as a capacitor (the MZM load capacitance) in series with a resistor [RLP+16]. Therefore, the modulator load does not reduce the output impedance of the driver, whose output voltage swing remains unaltered.

Nevertheless, a large number of segments increases the power consumption of the transmitter. In addition to this, special care has to be given to the matching of the propagation delays between the optical and electrical signal that drives the phase shifters. One technique for matching the propagation delays is shown in Fig. 2.32, where meandered transmission lines ensure the same delay between the RF signal and the optical waveform [RLP+16]. Other techniques employ active delay circuits [QXH+16], which however increase the power consumption.

Thus, there are a series of trade-offs when designing electro-optical transmitters based on the segmented topology. These trade-offs concern the bandwidth, the ER and the DC power consumption. As explained in the previous section, the ER is given by the MZM's modulation efficiency, i.e. by its V_π and its phase shifter length L. A long phase shifter segment implies a high load capacitance C_{load}, which loads the electrical driver and limits the achievable data rate. In order to improve the speed, the segment length can be decreased (thus decreasing C_{load}), while the number of segments is increased. However, this results in a higher DC power consumption, as each phase shifter segment needs to be driven by a separate driver cell. Finally, a short segment length (meaning a low C_{load}) and a low number of segments result in a short overall length L of the phase shifter, which in turn increases the MZM's V_π (since the

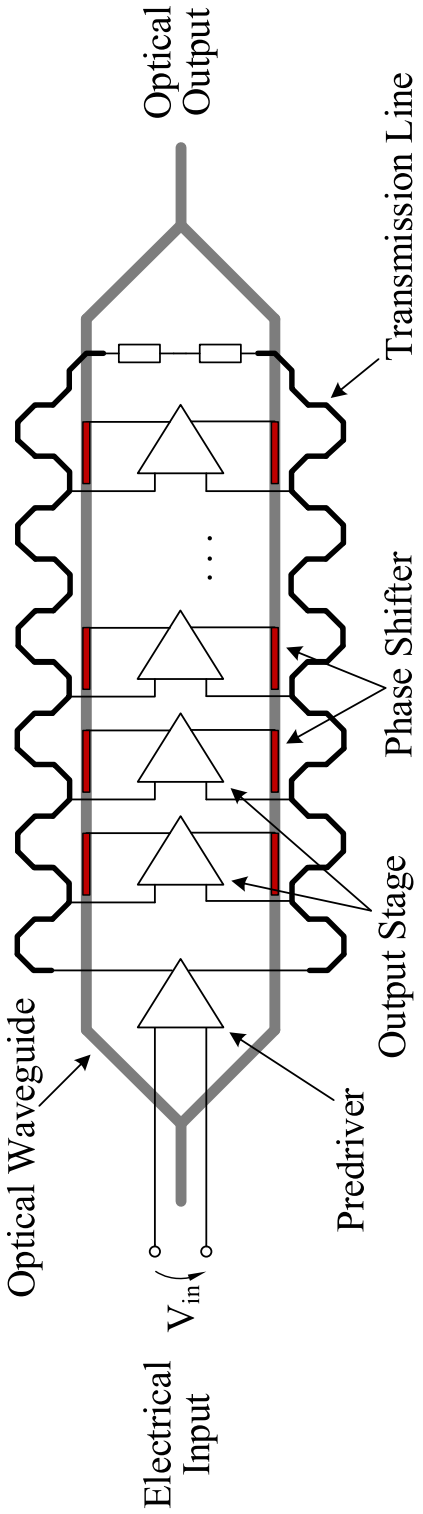


Figure 2.32: Segmented MZM-based transmitter front-end [GBK+18b]†. ©[2018] IEEE

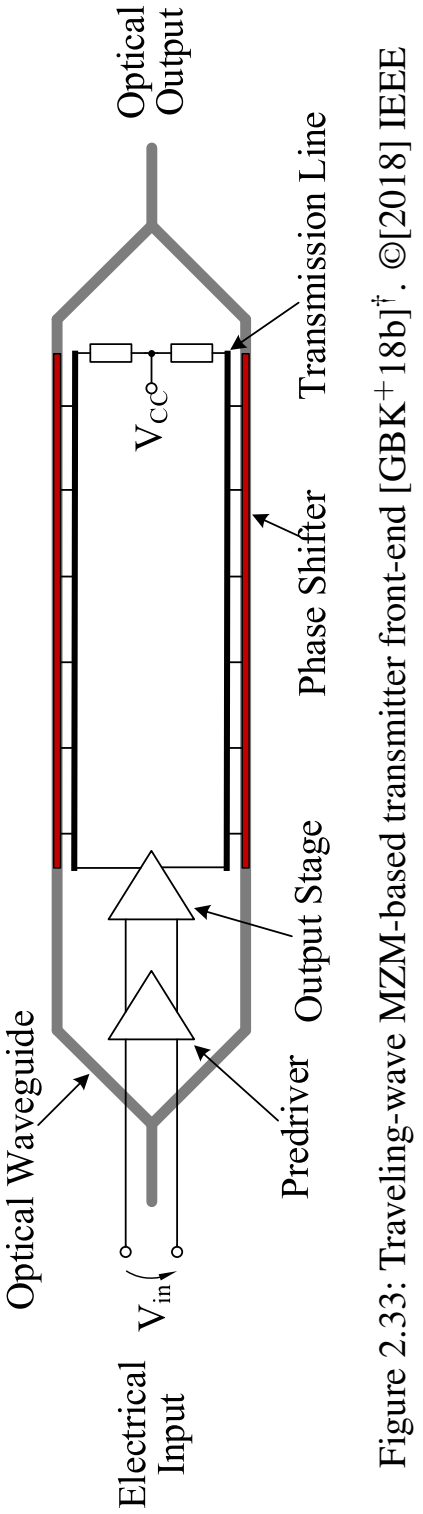


Figure 2.33: Traveling-wave MZM-based transmitter front-end [GBK+18b]†. ©[2018] IEEE

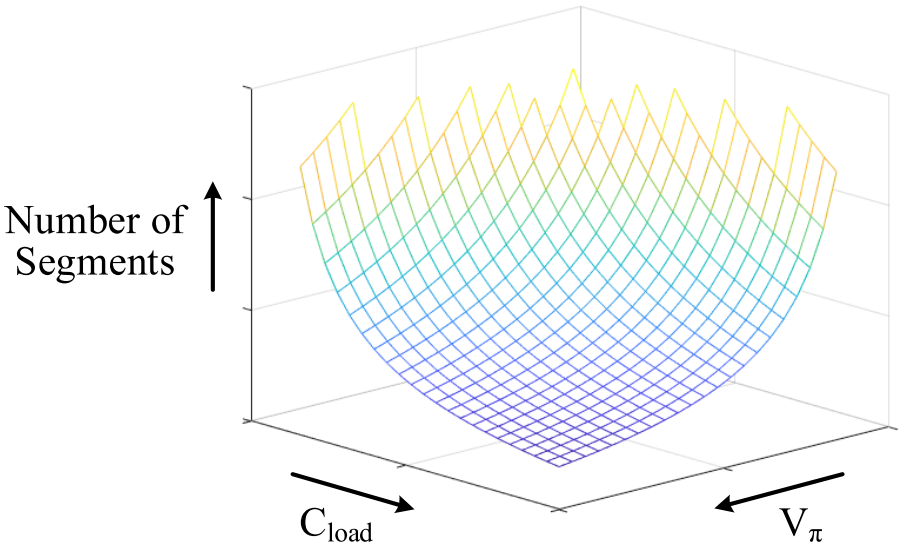


Figure 2.34: Trade-offs for the design of segmented MZM-based transmitter front-ends, conceptual representation.

$V_\pi L$ product is constant), thus imposing high requirements on the design of the electrical driver. These trade-offs are conceptually illustrated in Fig. 2.34 for a typical EPIC process [PRL+16].

2.6.2 Traveling-Wave Front-End Topology

The traveling-wave transmitter topology is depicted in Fig. 2.33. Its implementation is less complex than the segmented one, since it only requires a single driver cell. The driver is connected to the electrodes of the MZM's phase shifters by means of transmission lines (TL), hence the name of the topology. One of the main disadvantages of this topology compared to its segmented counterpart is the fact that the signal is attenuated as it propagates along the TL due to the TL's ohmic resistance. This effect is accentuated at high frequencies, where the TL's resistance increases because of the skin effect.

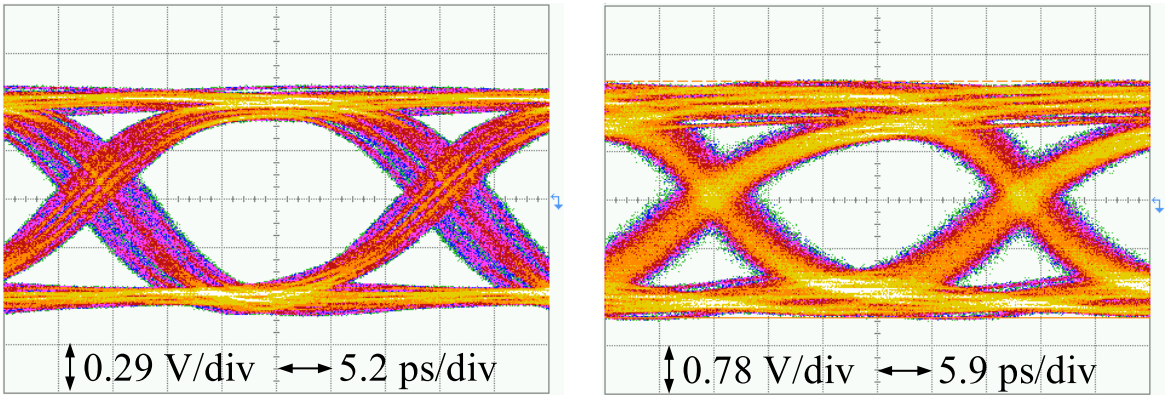
Due to the use of TLs, the *pn*-junction capacitance of the phase shifters does not directly load the electrical driver, since it is canceled by the TLs' inductance. Nevertheless, the phase shifters' capacitance does load the TLs, decreasing their characteristic impedance. This has a negative effect on the

driver, since it requires a higher tail current in order to yield the same output voltage swing as in the case of unloaded TLs. However, the loading of the TLs by the phase shifters' capacitance has a positive effect with regard to the velocity matching between the optical and electrical path: the propagation delay in the TLs is increased and can thus be easily matched to the delay in the phase shifters, without needing special layout or circuit techniques [QXH+16].

2.6.3 Comparison Study between Segmented and Traveling-Wave Topologies

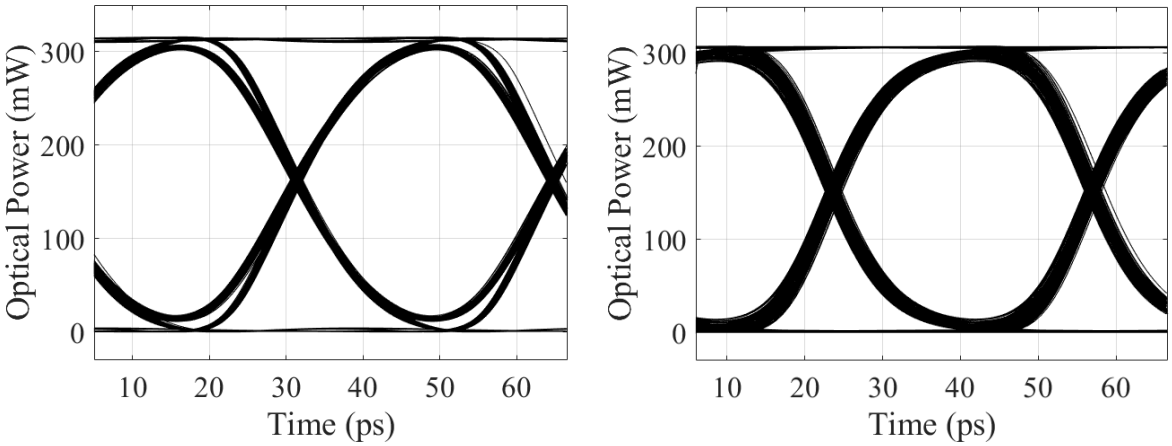
Next, a case study is presented in order to compare the segmented and traveling-wave topologies. To this end, two electro-optical transmitters where designed consisting of an MZM and an electrical driver. For the driver, the breakdown voltage doubler architecture was employed in order to maximize the ER and relax the requirements regarding the phase shifter length. For the traveling-wave topology, an open-collector driver was used, the output resistance being represented by the TLs' impedance and their termination resistors. For the segmented topology, a driver with 70-Ω collector resistors for the output transistors was used; additionally, inductors were employed at the driver output in order to enhance its speed. Both drivers were able to provide a differential peak-to-peak output swing of 7.6 $V_{pp,d}$. As the maximum ER was targeted, this voltage swing required phase shifters with a total length of 3.6 mm for both topologies [PRL+16]. For the segmented topology, a number of 10 segments was chosen in order to limit the length of each segment and thus its load capacitance, and on the other hand to limit the overall power consumption of the transmitter.

The above design concepts were proved by means of electrical measurements and electro-optical simulations. Fig. 2.35 shows the measured single-ended eye diagrams at 30 Gb/s of both electrical drivers. In the case of the driver for the segmented topology (Fig. 2.35 (a)), the full output voltage swing could not be reached during measurements since the 50-Ω impedance of the sampling oscilloscope reduced the driver gain. For the open-collector driver of the traveling-wave topology (Fig. 2.35 (b)), the 50-Ω impedance of the



(a) (b)

Figure 2.35: Measured electrical eye diagrams at 30 Gb/s of the MZM drivers for (a) the segmented topology and (b) the traveling-wave topology [GBK$^+$18b]†. ©[2018] IEEE



(a) (b)

Figure 2.36: Simulated optical eye diagrams at 30 Gb/s of (a) the segmented transmitter and (b) the traveling-wave transmitter [GBK$^+$18b]†. ©[2018] IEEE

oscilloscope served as termination resistor, while the output common-mode voltage was provided by means of bias tees.

Fig. 2.36 (a) and (b) show the simulated output optical eye diagrams at 30 Gb/s for the segmented and traveling-wave transmitter, respectively. Both MZMs provide similar optical eye diagrams with ERs of 14 dB each. Thus, both transmitters were able to achieve high ERs at high data rates, while

showing clean eye diagrams with low rise and fall times and low jitter. However, the 10 driver segments of the segmented topology consume a total DC power of 6.4 W, while the power consumption of the driver for the traveling-wave topology is 1.5 W.

This case study showed that for data rates above 30 Gb/s and for systems requiring high ERs, the traveling-wave topology is much more suitable in terms of energy efficiency. This insight was considered for the implementation of the electro-photonic co-integrated transmitter that will be presented in Section 3.1.

3 Conceptual Circuit Implementations[1]

This chapter comprises the proof of the theoretical concepts and considerations presented in the previous chapter. To this end, several circuits relating to basic electro-optical transmitter front-ends have been designed. All circuits were subsequently fabricated and experimentally measured in order to verify their functionality.

In Section 3.1, a monolithically integrated electro-optical transmitter assembly is presented, which consists of an MZM and an electrical driver. The circuit was realized in a 250-nm BiCMOS EPIC technology. The circuit is able to reach a data rate of 37 Gb/s, which is, up to this date, the highest data rate among monolithically integrated electro-optical transmitters in the literature. By using a high-swing electrical driver, a compact MZM assembly with 2-mm long phase shifters could be realized, while not sacrificing the ER. Thus, the driver reaches an ER of 8.4 dB at 25 Gb/s, 7.6 dB at 35 Gb/s and 6.1 dB at 37 Gb/s. The design particularity of the driver is the open-collector topology, which allows to increase the data rate and in the same time to reduce the power consumption. The realized transmitter thus proves that compact and high-speed MZM-based transmitters can be realized while still achieving a high ER and a good power efficiency.

Section 3.2 presents the design of an enhanced electrical driver for MZMs, realized in a 130 nm SiGe BiCMOS technology. Compared to the driver described in the previous section, this design is linear, thus allowing the use of higher-order modulation formats, for example PAM or QAM. The driver achieves peak-to-peak differential output swings above 6.5 $V_{pp,d}$, which en-

1 **Copyright Note**: Major parts (text, figures and tables) of Chapter 3 are taken from IEEE publications where I was the first author. Thus, sections 3.1, 3.2 and 3.3 are to a large extent taken from [GBK+22]†, [GKB+22]† and [GKB+21]†, respectively. The figures and tables are specifically referenced.

ables the use of short-length MZMs without sacrificing their ER. By means of an open-collector topology as well as by implementing the emitter-follower stages with emitter resistors instead of current mirrors, the power consumption was reduced by 19% without losing bandwidth or linearity. The circuit achieves a bandwidth above 60 GHz, allowing NRZ data rates up to 72 Gb/s and PAM-4 data rates up to 90 Gb/s. At 1 GHz, the driver has a THD of 1% for 6.5 $V_{pp,d}$ output swing and 1.7% for 7 $V_{pp,d}$, which are the highest linearity and output voltage swing reported in the literature for modulator drivers with bandwidths higher than 40 GHz.

Finally, Section 3.3 shows the design of a PAM-8/PAM-4 modulator driver realized as a 3-bit digital-to-analog converter (DAC). The circuit was realized in a 130 nm SiGe BiCMOS technology. It consists of two stages, namely a single-ended to differential converter (SDC) and an output stage, which represents the DAC core. The circuit has an output voltage swing of 4 $V_{pp,d}$ and consumes 590 mW of DC power. The driver is able to yield both PAM-8 and PAM-4 output signals at data rates up to 50 Gbaud, which corresponds to 150 Gb/s and 100 Gb/s, respectively. This tuning capability of the modulation format does not imply a penalty in power consumption or an increase of the circuit complexity.

3.1 A Monolithically Integrated Electro-Optical Transmitter in a Si Photonics 250-nm BiCMOS Technology

3.1.1 Introduction

In this section we present the design and measurement of a monolithically integrated electro-optical transmitter consisting of an MZM and an electrical driver. The design aims at overcoming the limitation imposed by the technology-dependent electro-optical modulation efficiency by using a high-swing modulator driver. With an output voltage swing of 7.6 $V_{pp,d}$, short phase shifters of 2 mm could be employed while still reaching an ER of 7.6 dB at 35 Gb/s. Moreover, by employing an open-collector topology for the elec-

trical driver, the DC power consumption of the transmitter was reduced down to 1440 mW, while a maximum, bit-error-free (10^{-10}) data rate of 37 Gb/s was reached.

The transmitter was realized in a Si photonics 250-nm BiCMOS technology with an f_T/f_{max} of around 190 GHz. Such electro-photonic technologies allow the monolithic integration of the optical and electrical components on the same chip. This type of integration offers a series of advantages. On the one hand, the electrical driver can be placed close to the modulator, thus mitigating the interconnection losses. On the other hand, high-yield and low-cost fabrication is possible, since the additional manufacturing steps of integrating separate electrical and optical structures onto one die (e.g. via wire bonding or flip-chip) are not required anymore.

3.1.2 Circuit Design

The block diagram of the monolithically integrated electro-optical transmitter is shown in Fig. 3.1. The optical input is provided by a continuous wave laser source with a wavelength of 1550 nm. The light coming from the laser is coupled into the circuit by means of a grating coupler. The light wave is then split between the two arms of the MZM by means of an MMI coupler. The light modulation is realized by changing the phase of the light signals in the two MZM arms and by recombining them in the output MMI coupler. If the two signals are in phase, the output light wave resulting through recombination will have a high intensity, thus realizing the logical ”1” of a digital waveform. However, if the signals are in opposite phases, they will recombine destructively, resulting in a low intensity output light wave which corresponds to the digital ”0”. This phase modulation is done by means of the phase shifters of the two MZM arms. The phase shifters are driven by the voltage provided by the electrical driver. The driver and the modulator are connected by means of transmission lines (TL), which are terminated by two resistors R_{end} matching the loaded TL impedance. The resistors are connected to the supply voltage V_{CC} = 6.4 V. The MZM is driven in a differential push-pull mode [QXH+16].

Fig. 3.2 shows the photograph of the realized electro-optical subassembly. The following three subsections provide a detailed description of the imple-

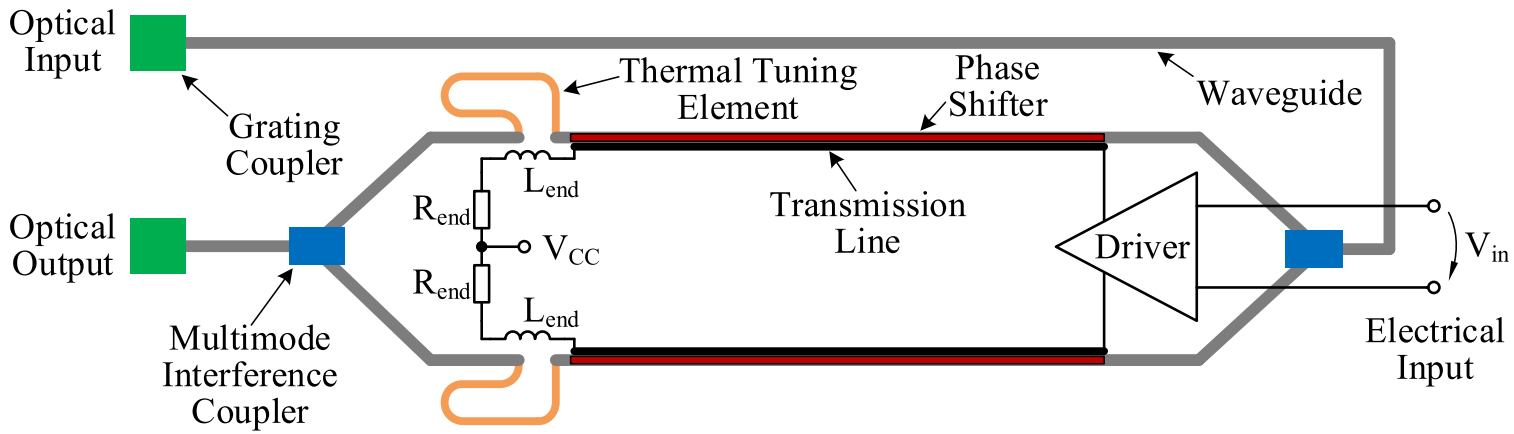


Figure 3.1: Block diagram of the monolithically integrated electro-optical transmitter consisting of an MZM and an electrical driver [GBK+22]†. ©[2022] IEEE

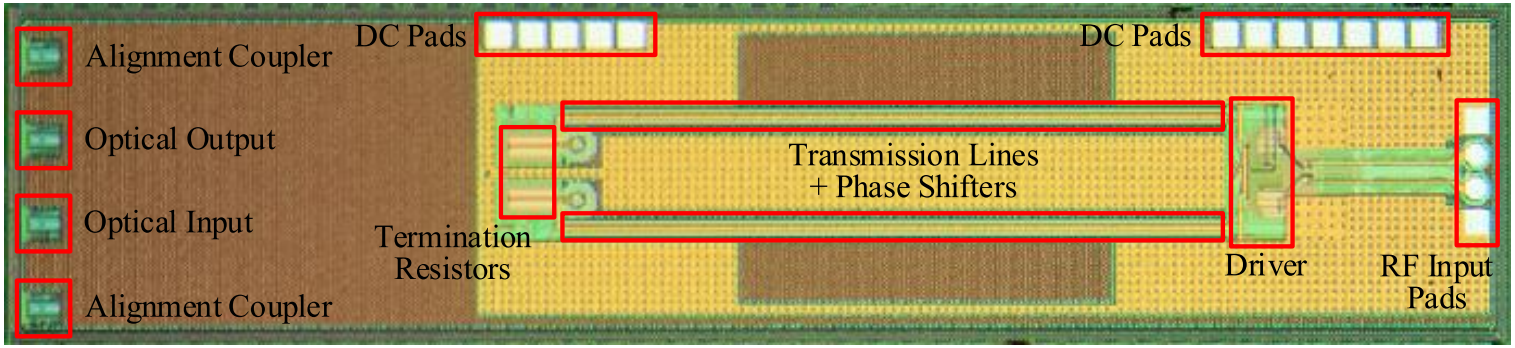


Figure 3.2: Chip micrograph. Size: 4.5×1 mm^2 [GBK+22]†. ©[2022] IEEE

mentation of the MZM and the electrical driver.

MZM Design

The phase shifters used in the proposed transmitter have the *p-n* junction in the middle of the waveguide. The cross section as well as the doping profile are shown in [PZG+15] (Fig. 7 (b), moderate *p*-doping). For the chosen reverse bias voltage over the *p-n* junction, namely 2.5 V, the phase shifters have an electro-optical modulation efficiency of $V_\pi L$ = 1.5 Vcm [PZG+15]. The reverse bias voltage was chosen by targeting a minimal depletion capacitance of the phase shifters' *p-n* junction and thus a maximum data rate. Nevertheless, this choice was conditioned by the high voltage swing of the driver, since a forward bias operation of the *p-n* junction should be avoided.

Thanks to the high output voltage swing of the electrical driver, the length of the phase shifters could be reduced down to 2 mm, which is in accordance with the design target of a compact and high-speed transmitter. Considering the aforementioned eletro-optical modulation efficiency, this phase shifter length corresponds to a V_π of 7.5 V. If optimization for better ER is needed, the output swing of the driver can be reduced by reducing its tunable tail current. Based on equation (2.79), the transfer function of the MZM with V_π = 7.5 V can be represented as in Fig. 3.3 (the maximum output optical power was normalized to 1).

Since the MZM is driven in a differential push-pull manner and the modulation format is on-off keying (OOK), the operating point must be set in the quadrature point [QXH+16] (as shown in Fig. 3.3). To this end, one of the MZM arms must be shifted by 90° with regard to the other arm. This is done by means of a thermal tuning element (Fig. 3.1). Such an element consists of a narrow metal layer on top of a waveguide. By applying a DC voltage on the metal, its temperature rises and generates a phase shift in the waveguide. The power dissipated by the thermal element in order to reach a 90° phase shift is 10 mW.

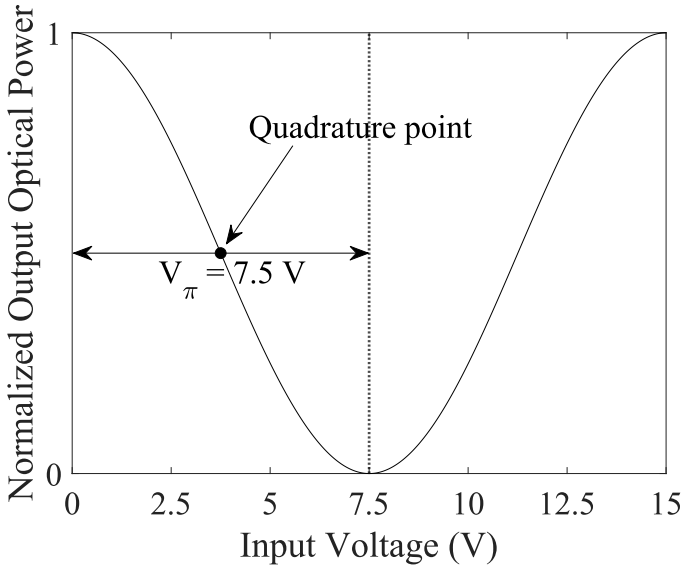


Figure 3.3: Transfer function of the MZM for V_π = 7.5 V [GBK+22]†. ©[2022] IEEE

Transmission Line Design

The TLs connecting the MZM's phase shifters and the electrical driver were modeled segmentally, every segment having a length equal to a small fraction of the signal wavelength [XM07]. The loaded TL model is shown in Fig. 3.4. Each segment is described by a series of lumped elements: L_u, C_u and R_u are the inductance, capacitance and resistance of a TL segment per unit of length, respectively. C_{load} represents the depletion capacitance of the phase shifter's *p-n* junction, which acts as a load for the TL.

The characteristic impedance Z_0 of the TL is an important metric for the electro-optical integration, since it determines the output voltage swing of the driver and subsequently the modulator's ER. The characteristic impedance is directly impacted by the depletion capacitance of the phase shifter's *p-n*

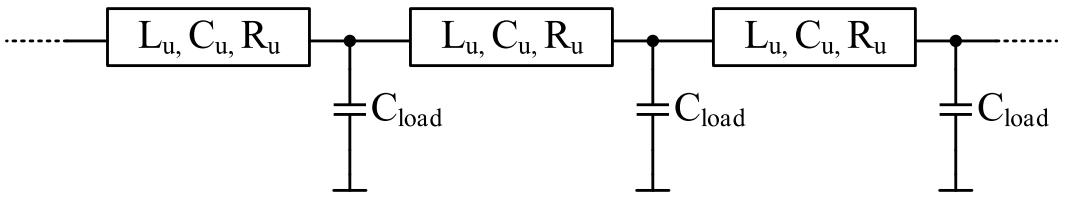


Figure 3.4: Loaded TL model [GBK+22]†. ©[2022] IEEE

junction. Therefore, for the electrical driver design, the loaded TL impedance needs to be taken into account. The two equations for calculating the unloaded ($Z_{0,unloaded}$) and loaded ($Z_{0,loaded}$) impedance of the TL are [DCS+15]:

$$Z_{0,unloaded} = \sqrt{\frac{L_u}{C_u}} \tag{3.1}$$

$$Z_{0,loaded} = \sqrt{\frac{L_u}{C_u + C_{load}}} \tag{3.2}$$

Another important aspect for the electro-optical integration is the velocity matching between the electrical signal in the TL and the optical signal in the phase shifter, since mismatches cause high rise and fall times, which reduce the vertical opening of the optical eye [TGM+16]. The propagation delay t_{op} in the optical path can be calculated by means of the following formula [RLP+16]:

$$t_{op} = L\frac{n_g}{c} \tag{3.3}$$

where L is the optical waveguide length, n_g the refractive group index of the waveguide and c the speed of light in vacuum. With an n_g = 3.6 for the given technology [RLP+16], the propagation delay in the phase shifters was calculated to be t_{op} = 12 ps/mm.

In the electrical path, the propagation delay t_{el} for the loaded and unloaded TL is given by the following equations [DCS+15]:

$$t_{el,unloaded} = \sqrt{L_u C_u} \tag{3.4}$$

$$t_{el,loaded} = \sqrt{L_u(C_u + C_{load})} \tag{3.5}$$

where $t_{el,unloaded}$ and $t_{el,loaded}$ are the propagation delays for the unloaded and loaded TL, respectively. Thus, by changing the TL geometry, matching between the propagation delays in the optical and electrical paths can be achieved.

Fig. 3.5 shows the conceptual 2D cross-sectional profile of the TL. The phase shifter's *n*-electrode is connected to the TL's signal line, while the *p*-

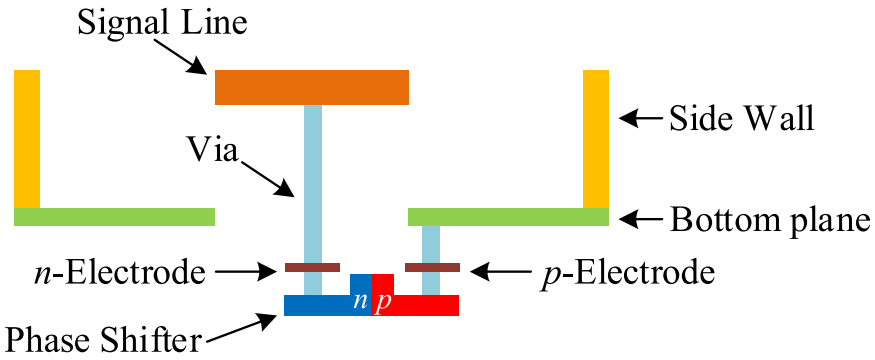


Figure 3.5: Conceptual 2D cross-sectional profile of the TL [GBK+22]†. ©[2022] IEEE

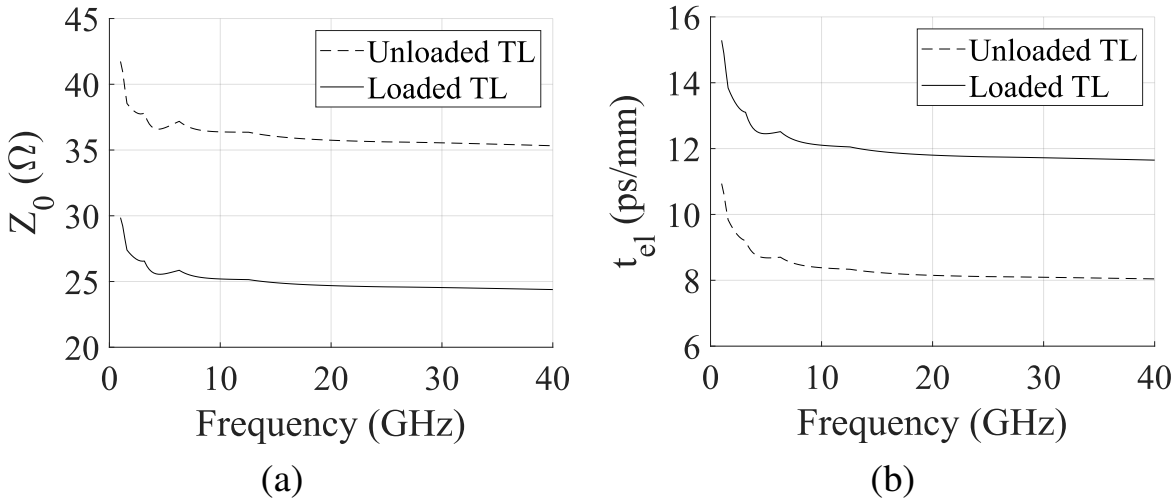


Figure 3.6: Calculated characteristic impedance Z_0 and propagation delay t_{el} of the TL, based on the electromagnetic simulation results [GBK+22]†. ©[2022] IEEE

electrode is connected via the TL's bottom plane and side walls to the chip pad providing the reverse bias voltage.

The TL was modeled and simulated by means of an electromagnetic simulation software. By applying the simulated L_u and C_u in equations (3.1), (3.2), (3.4) and (3.5), the characteristic impedance and propagation delay for the unloaded and loaded TL were calculated (Fig. 3.6). The TLs' termination resistors R_{end} (Fig. 3.1) were chosen according to the results in Fig. 3.6 (a), in order to ensure matching with the loaded TL impedance. Additionally, a pair of inductors L_{end} was employed in order to cancel the parasitic capacitances

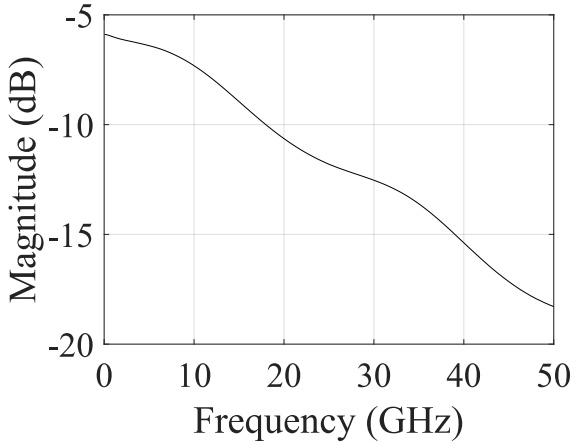


Figure 3.7: S_{21} parameter of loaded TL (post-layout simulation) [GBK+22]†. ©[2022] IEEE

introduced by R_{end}. These resistors have considerable dimensions since they need to sustain the high output current of the electrical driver, therefore showing a non-negligible parasitic capacitance. Furthermore, as it can be seen in Fig. 3.6 (b), the propagation delay in the loaded TL matches the one in the optical path, which was calculated according to equation (3.3).

Fig. 3.7 shows the simulated (post-layout) S_{21} parameter of the loaded, full-length (2 mm) TL, including the termination resistors R_{end} and inductors L_{end}. This part of the circuit has a 3-dB bandwidth of 15 GHz, which decreases the vertical eye opening of the MZM's optical output signal as well as its ER at higher frequencies.

Electrical Driver Design

The electrical driver consists of two stages, namely a predriver and an output stage, which are illustrated in Fig. 3.8 and 3.9, respectively. The driver operates under switching conditions. For the purpose of maximizing the output voltage swing without exceeding the collector-emitter breakdown voltage of the output transistor pairs T_5-T_6 and T_7-T_8, a breakdown voltage doubler architecture was employed [MH07]. Such a topology allows for the output voltage swing to be equally distributed between the cascaded transistors $T_{5/6}$ and $T_{7/8}$, since the bases of the upper transistors T_7 and T_8 are coupled to the input of the output stage by means of common emitter circuits (T_9 and T_{10}).

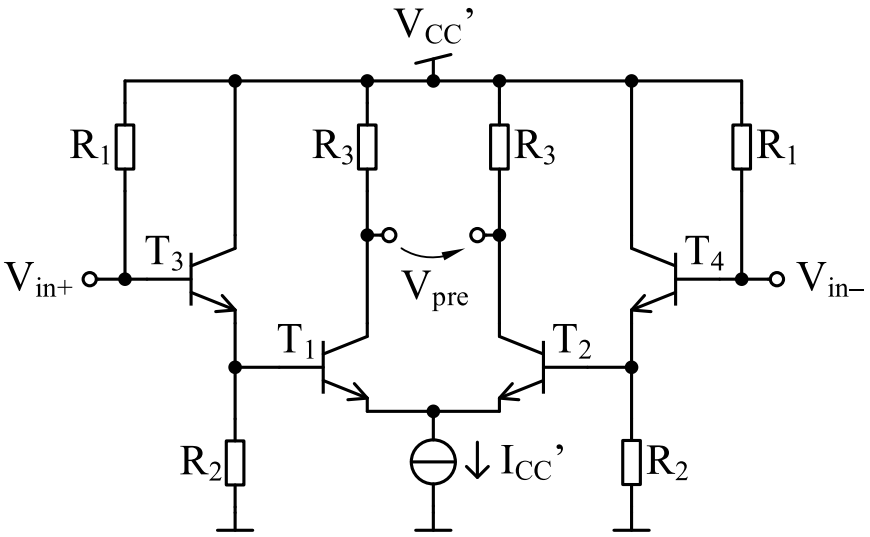


Figure 3.8: Circuit schematic of the predriver stage of the electrical driver [GBK+22]†. ©[2022] IEEE

Compared to the monolithically integrated transmitters shown in [RLP+16] and [PRL+16], the driver of the proposed transmitter employs an open-collector topology for the output stage, for the purpose of maximizing the data rate and minimizing the power consumption. An additional pair of collector resistors for the transistors $T_{7/8}$ would require a two-times higher tail current $I_{CC,2}$ in order to ensure the same output voltage swing, since in this case, the tail current would be divided between the collector resistors and R_{end}. This would not only increase considerably the power consumption, but the maximum achievable data rate would also be reduced, since larger transistors with larger parasitic capacitances and thus higher rise and fall times would be required in order to sustain the higher $I_{CC,2}$.

In order to prove this design concept, a comparison study was done between the proposed driver design (realized as an open collector) and the same driver implemented conventionally, by using collector resistors for the transistors $T_{7/8}$. For the conventional approach, the transistors were redimensioned according to the larger tail current $I_{CC,2}$. Fig. 3.10 shows the simulated output waveforms of the two electrical drivers at 37 Gb/s. The simulations included the loaded TLs as well as the TL termination resistors. The conventional driver has higher rise and fall times and thus achieves a smaller output voltage swing at 37 Gb/s than its open-collector counterpart. Furthermore, by using a

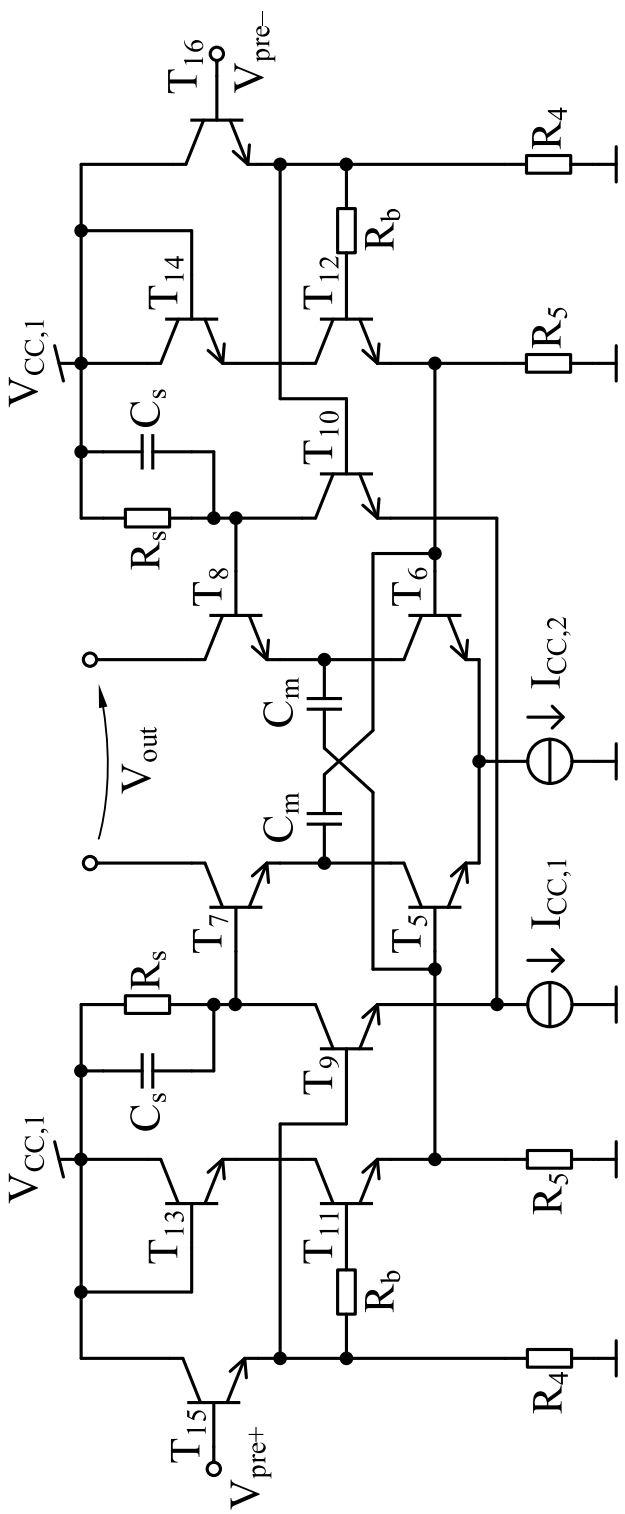


Figure 3.9: Circuit schematic of the output stage of the electrical driver [GBK+22]†. ©[2022] IEEE

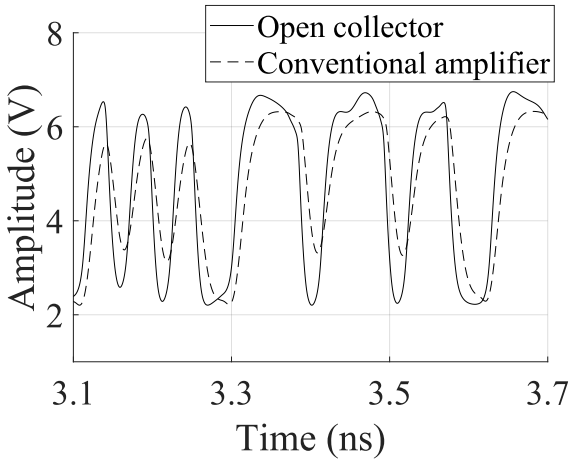


Figure 3.10: Driver output waveform at 37 Gb/s (pre-layout simulation). Solid line: driver implemented as open collector; dashed line: conventional driver with collector resistors [GBK+22]†. ©[2022] IEEE

two-times lower tail current, the open-collector driver has a 37% lower power consumption compared to the driver using collector resistors.

3.1.3 Experimental Characterization

Experimental measurements were performed in order to study the functionality of the circuit and to prove the previously presented design concepts. The measurement setup is shown in Fig. 3.11. The electrical input signal was a 2^7-1 pseudo-random bit sequence (PRBS) with an amplitude of 600 mV_{pp} provided by a bit pattern generator (BPG). According to simulation results, longer bit sequences are not expected to have a high impact on the optical output eye diagram in terms of ER, horizontal or vertical eye opening. The optical input signal was provided by a 1550-nm distributed feedback (DFB) laser source with an optical output power of 10 dBm. A polarization controller was used in order to minimize the optical losses when coupling light into the modulator. The losses in the optical fibers and the polarization controller amount to 1.5 dB, while the losses in the transmitter amount to 16.5 dB, where 8.5 dB are the optical losses in the MZM and 8 dB the total – input and output – coupling losses (measured by means of the alignment grating cou-

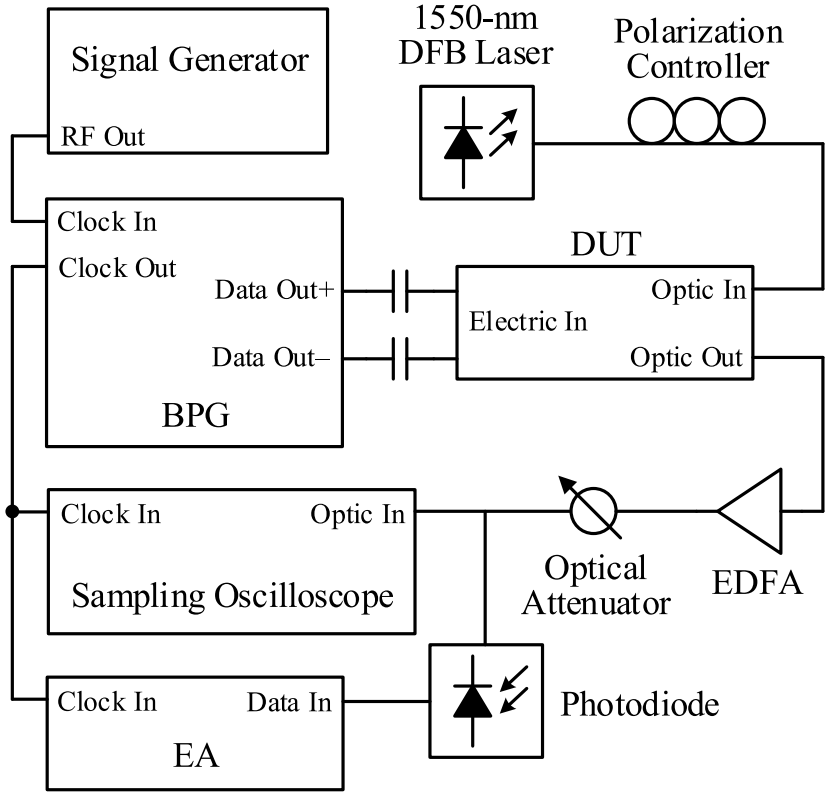


Figure 3.11: Experimental measurement setup [GBK+22]†. ©[2022] IEEE

plers shown in Fig. 3.2, which are connected by a waveguide). In order to compensate these losses, an erbium-doped fiber amplifier (EDFA) was employed at the optical output of the circuit. Since the signal-to-noise ratio of the EDFA deteriorates at low amplifications, the optical signal was amplified up to 10 dBm. Subsequently, in order not to exceed the maximum allowed input power of the oscilloscope, the optical signal was attenuated down to 1.2 dBm by means of a variable optical attenuator. The sampling oscilloscope is equipped with a >30-GHz optical module which is capable of measuring optical eye diagrams. In order to measure the bit error rate (BER), the optical signal was converted into electrical signal by means of a photodiode and fed into an error analyzer (EA).

The light was coupled in and out of the circuit by means of a 4-channel V-groove fiber array which was packaged with the chip (Fig. 3.12). The channel configuration is shown in Fig. 3.2: the inner two channels are the input and output of the MZM, while the outer channels served for alignment dur-

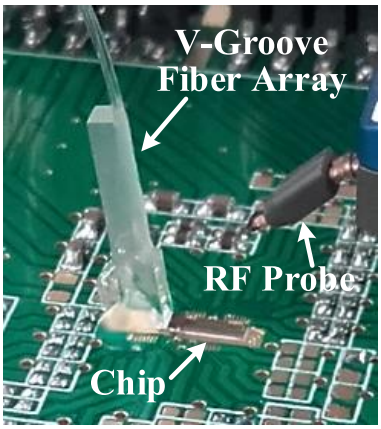


Figure 3.12: Packaged V-groove fiber array and electro-photonic chip [GBK+22]†. ©[2022] IEEE

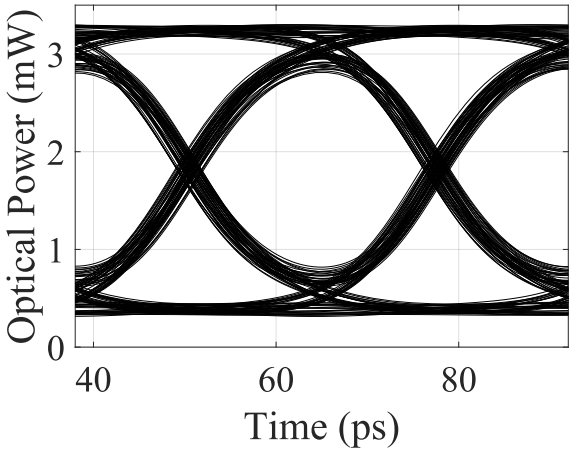


Figure 3.13: Simulated optical eye diagram at 37 Gb/s (post-layout simulation) [GBK+22]†. ©[2022] IEEE

ing the packaging process. On the electrical side, the chip was contacted by means of an RF probe.

Fig. 3.13 shows the simulated (post-layout) optical eye diagram at 37 Gb/s for an electrical input signal with an amplitude of 600 mV_{pp}. The ER of the simulated optical eye is 7.4 dB. Fig. 3.14 (a)–(d) show the measured optical eye diagrams. The ER was measured by means of the oscilloscope's measurement function. At 35 Gb/s, the proposed transmitter achieves an ER of 7.6 dB. The circuit shows an open eye diagram up to 37 Gb/s, however the ER is reduced to 6.1 dB. At lower data rates, the ER increases, reaching 8.4 dB at

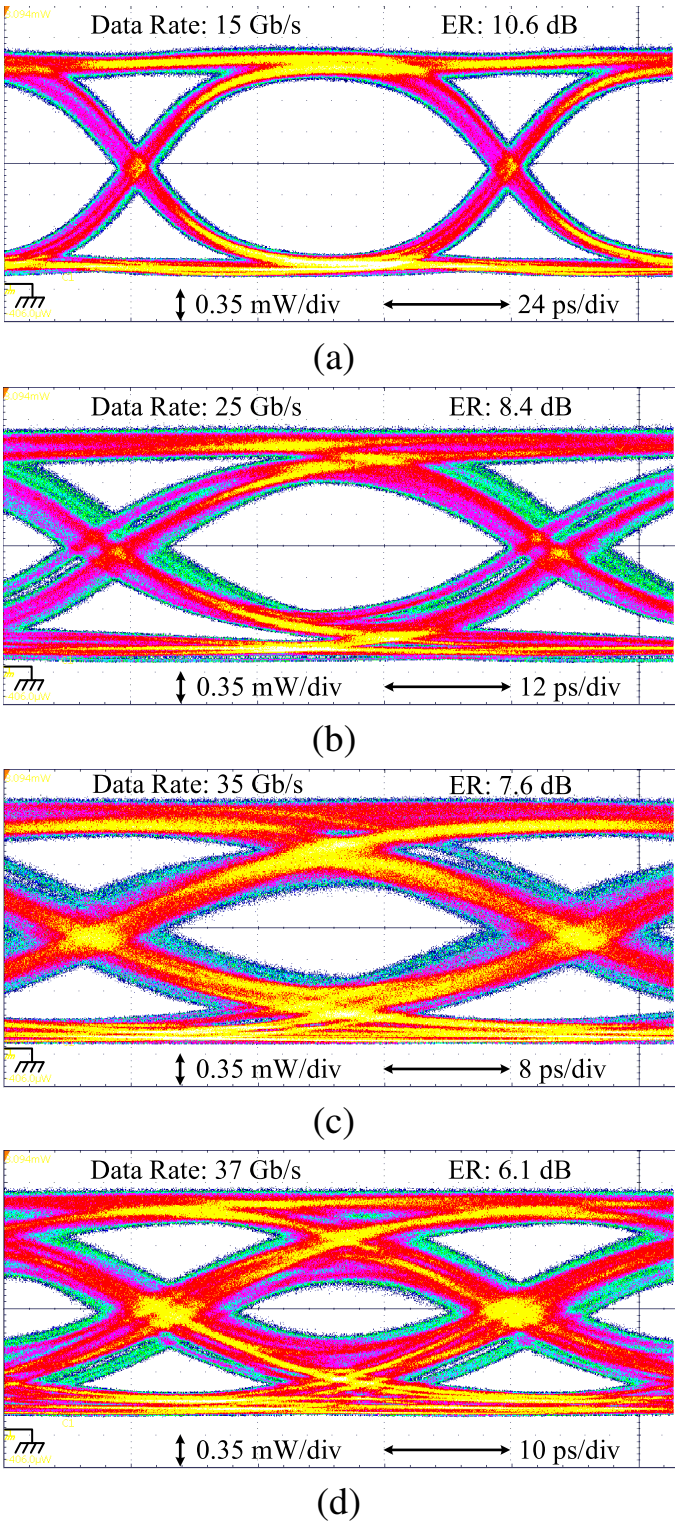


Figure 3.14: Measured optical eye diagrams at (a) 15 Gb/s, (b) 25 Gb/s, (c) 35 Gb/s and (d) 37 Gb/s [GBK+22]†. ©[2022] IEEE

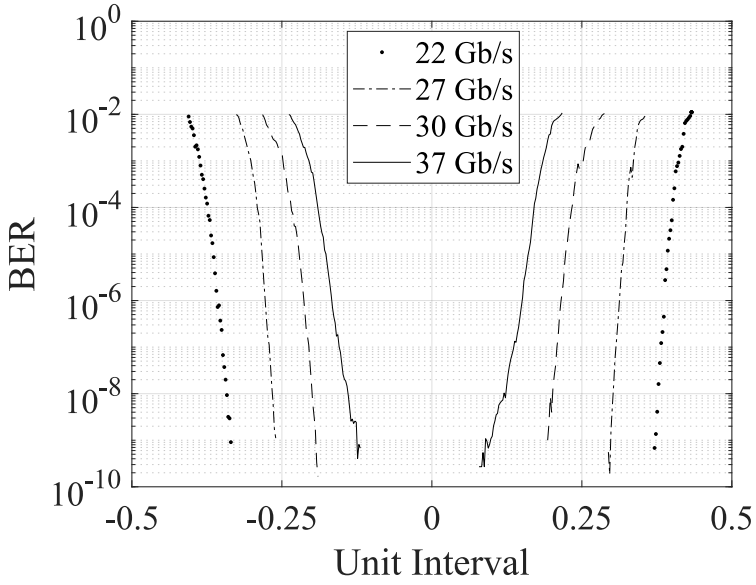


Figure 3.15: BER at different data rates [GBK+22]†. ©[2022] IEEE

25 Gb/s and 10.6 dB at 15 Gb/s. There are several reasons for the reduction of the ER at higher data rates. First, the propagation velocity mismatch between the optical path (phase shifters) and the electrical path (TLs) has a higher impact on the vertical opening of the optical eye. Next, the ohmic resistance of the TLs rises at higher frequencies due to the skin effect, thus reducing the voltage swing over the phase shifters. Finally, the rise and fall times of the driver as well as the MZM's limited bandwidth result in the vertical closing of the electro-optical eye and thus in the reduction of the ER. The intersymbol interference (ISI) seen at data rates of 25 Gb/s and above is partly caused by reflections due to impedance mismatches between the open-collector stage, the loaded TL impedance and the TLs' termination resistors. The use of a conventional driver with collector resistors for the output transistors would improve the impedance matching and help mitigate the ISI, however such a topology presents the disadvantages described in Subsection 3.1.2.

The BER measurement results at different data rates are shown in Fig. 3.15. The circuit is bit error free (10^{-10}) up to 37 Gb/s.

The further increase of the data rate can be the object of future research work. To this end, shorter phase shifter lengths can be taken into consideration. A significant drop in the ER should not be expected, since the driver is

able to provide a sufficiently high output voltage swing for the given electro-optical modulation efficiency. Moreover, this design improvement towards higher data rates does not imply the increase of the power dissipation of the circuit.

The total DC power consumption of the transmitter is 1440 mW. During measurements, no significant impact on the transmitter performance due to heat dissipation was noticed, one reason for this being the symmetry of the design. Moreover, the Si MZMs as well as the traveling-wave topology are known to have a high thermal stability [QXH+16].

3.1.4 Achievements of the Basic Scientific Research

In this section, the concept of a monolithically integrated electro-optical transmitter was presented. The circuit consists of a Si photonics MZM and a BiCMOS electrical driver which were implemented in a co-integrated electro-photonic technology. The study showed that bit-error-free (10^{-10}) data rates up to 37 Gb/s can be reached by a monolithically integrated transmitter, which is a record among transmitters with this type of integration reported in the literature. By implementing the electrical driver as a breakdown voltage doubler architecture in order to overcome the physical limitations regarding the breakdown voltage of the transistors and to increase the output swing, we proved that a compact MZM assembly can be realized without sacrificing the ER. Thus, with a 7.6-$V_{pp,d}$ differential swing of the driver, short-length phase shifters of 2 mm of length could be employed, while reaching ERs of 8.4 dB at 25 Gb/s and 7.6 dB at 35 Gb/s. Moreover, the open-collector design approach for the output stage of the electrical driver allowed to reduce the DC power consumption, while achieving a higher data rate compared to a conventional driver with collector resistors for the output transistors.

Table 3.1 summarizes the performance of different state-of-the-art MZM-based electro-optical transmitters and compares them with the design presented in this section. The circuits shown in [TMR+16] and [BRG+20] achieve higher symbol rates and have a lower power consumption, however they have significantly lower voltage swings and ERs. The design shown in [YSM+18] was realized in a small-node CMOS technology and has a high

symbol rate and a low power consumption. However, it uses two-times longer phase shifters while achieving a comparable ER, and the electro-optical integration was done in an additional manufacturing step, as flip-chip. The designs presented in [PRL+16] and [RLP+16] are monolithically integrated and have higher ERs, however they use three times longer phase shifters, have lower symbol rates and consume a much higher amount of DC power. The design shown in [XGP+15] uses monolithic integration as well and has a lower power consumption, however it is inferior in terms of symbol rate and ER.

From Table 3.1 it can be concluded that the design presented in this section achieves the highest symbol rate among monolithically integrated electro-optical transmitters in the literature. Moreover, the circuit achieves a high ER while using short-length phase shifters compared to the designs listed in Table 3.1, thus showing that one of the main disadvantages of MZM-based transmitters, namely their large chip footprint, can be mitigated by employing a high-swing electrical driver.

Table 3.1: Performance Summary and Comparison of MZM-Based Electro-Optical Transmitters [GBK+22]†.

	Symbol Rate (Gbaud)	ER (dB)	Phase Shifter Length (mm)	Driver Voltage Swing ($V_{pp,d}$)	$V_\pi L$ (Vcm)	DC Power (mW)	Wavelength (nm)	Electro-Optical Integration	Technology
[TMR+16]	56	2.5	3.15	1.6	2.5	300	1310	Flip-Chip	55 nm BiCMOS
[BRG+20]	53	4.5	3.45	2	2.2	386	1550	Wire Bonding	55 nm BiCMOS
[YSM+18]	50	8	4	4 (V_{pp})	2.5	553	1550	Flip-Chip	28 nm CMOS
[PRL+16]	32	11	6.05	3.5	2.7	1800	-	Monolithic	250 nm BiCMOS
[XGP+15]	28	6.3	3	2.2	1.5	270	1300	Monolithic	90 nm CMOS
[RLP+16]	28	13	6.05	4	2.9	2000	1550	Monolithic	250 nm BiCMOS
This Work	37 35	6.1 7.6	2	7.6	1.5	1440	1550	Monolithic	250 nm BiCMOS

3.2 A Linear, High-Swing and Power-Efficient Modulator Driver in a 130-nm SiGe BiCMOS Technology

3.2.1 Introduction

In this section, we present the concept of an enhanced MZM driver design, which in addition to the high-swing characteristic of the driver presented in the previous section, shows a high linearity, achieves a higher speed and consumes less power.

The driver employs a breakdown voltage doubler architecture in order to achieve the high-swing requirement. Emitter degeneration resistors were used in order to linearize the driver. By using an open-collector topology for the driver output stage, the extra power that would have been dissipated in the collector resistors of the output transistors was saved. Furthermore, by providing the bias currents of the emitter followers by means of resistors instead of current sources, the power consumption could be decreased by 19%, while not sacrificing the bandwidth or the linearity of the circuit. With a maximum output voltage swing of 7.2 $V_{pp,d}$, a bandwidth of 61.2 GHz, a THD of 1% (at 1 GHz for 6.5 $V_{pp,d}$ output swing) and a power consumption of 670 mW, the driver reached all the intended design targets. The circuit was designed in a 130-nm SiGe BiCMOS technology with an f_T/f_{max} of around 350/450 GHz.

3.2.2 Circuit Design

Circuit Concept

The conceptual circuit topology is shown in Fig. 3.16. As a breakdown voltage doubler, the circuit divides the output voltage swing between the transistors T_1 and T_2, thus avoiding that their BV_{CE} is exceeded. In order to have an equal voltage drop over the output transistors (i.e. $V_{CE,1} = V_{CE,2}$), several circuit parameters have to be tuned. For example, changing the supply voltage V_{CC} will shift one V_{CE} up and the other one down, whereas tuning the resistor R_T will increase one V_{CE} and decrease the other one. Fig. 3.17 (a)–(d) sum-

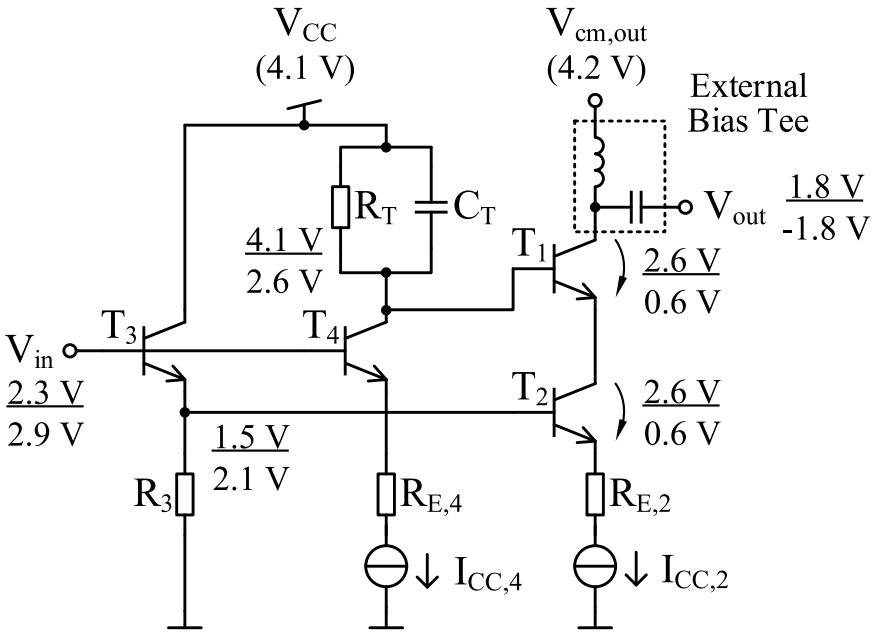


Figure 3.16: Conceptual implementation of the driver topology [GKB+22]†. ©[2022] IEEE

marize the influence of different circuit parameters that were used to align the two collector-emitter voltages during the design process.

The DC bias of the circuit (Fig. 3.16) as well as the value of resistor R_T were carefully chosen so that $V_{CE,1} = V_{CE,2}$. For the purpose of having a linear operation, an emitter degeneration resistor $R_{E,2}$ was employed. A more detailed description of the linearization of the driver is presented in the next subsection.

As it can be seen in Fig. 3.16, the driver was designed as an open-collector. When connected to an optical modulator, the load is represented by the impedance of the TLs connecting the driver with the modulator's electrodes, as well as by the TLs' termination resistors. As it was explained in Section 3.1, the open-collector topology enables both a higher speed and a lower power consumption of the circuit.

Having two cascaded output transistors T_1 and T_2 coupled to the input means that there are two distinct paths from the input to the output of the circuit. The first path goes from V_{in} to the base of T_4, then from T_4's collector to T_1's base, and finally to T_1's collector (V_{out}). The second path goes from V_{in} to the base of T_3, then from T_3's emitter to T_2's base, then from T_2's collector

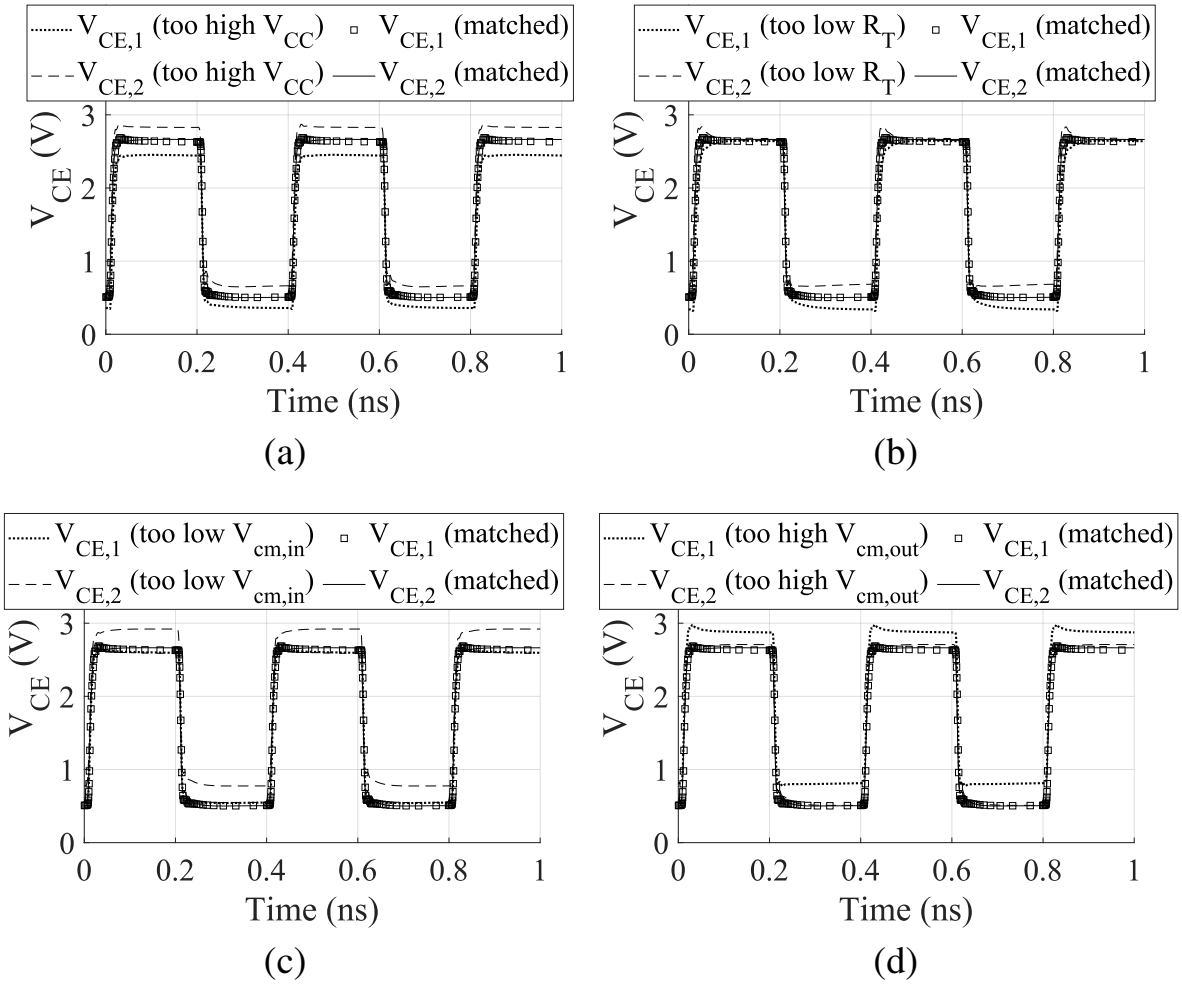


Figure 3.17: Variation of $V_{CE,1}$ and $V_{CE,2}$ with (a) supply voltage V_{CC}, (b) resistor R_T, (c) input common mode voltage $V_{cm,in}$ and (d) output common mode voltage $V_{cm,out}$ (transient simulations) [GKB+22]†. ©[2022] IEEE

up to T_1's emitter, and finally to T_1's collector. The two paths have different time delays, which must be matched in order to have an output signal with low rise and fall times and without distortions. As the first path (via T_4) is faster than the second one [MH07], a compensation capacitor C_T was placed in parallel with resistor R_T in order to match the delays in the two paths. Furthermore, capacitor C_T impacts the distribution of the output voltage swing between transistors T_1 and T_2. Fig. 3.18 (a) and (b) illustrate this effect for a too low and a too high C_T, respectively.

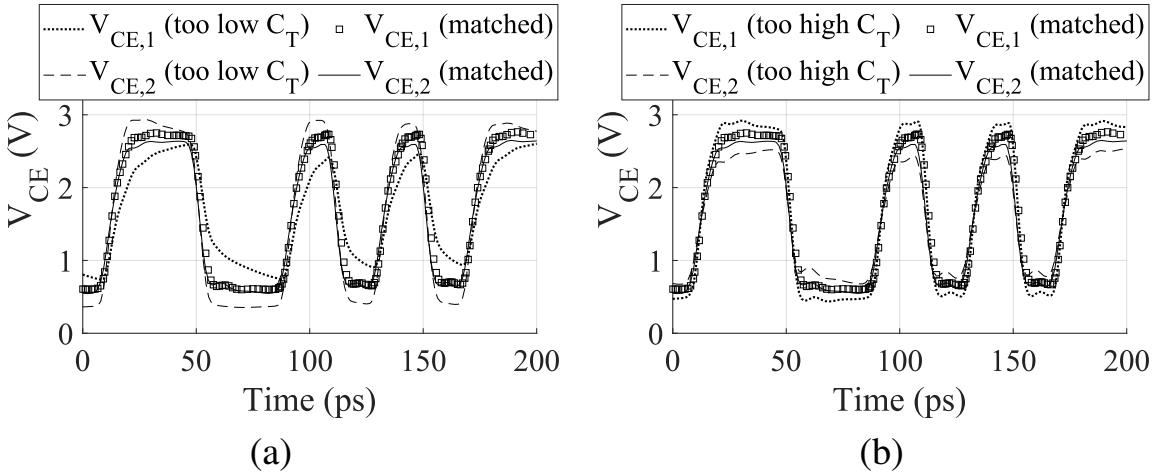


Figure 3.18: Influence of C_T on $V_{CE,1}$ and $V_{CE,2}$ (transient simulations at 50 Gb/s) [GKB+22]†. ©[2022] IEEE

Circuit Realization

The diagram of the circuit is shown in Fig. 3.19. The driver was realized as a fully differential architecture. It consists of the stages shown in Fig. 3.16 plus an additional EF stage at the input, used as buffer. The input common mode voltage $V_{cm,in}$ is fed externally. Resistors $R_1 = 50\ \Omega$ provide input matching.

EF Implementation – Mathematical Analysis

Compared to the previously published breakdown voltage doubler drivers presented in [MH07], [KSE11] and [AML+20], the proposed driver employs resistors (R_6 and R_3) instead of current sources in order to provide the bias currents for the EF stages T_6/T_6' and T_3/T_3'. As it will be shown, this approach offers a higher bandwidth and linearity for the same power consumption compared to the current-source approach. However, we first make a mathematical analysis of the two implementation approaches of the EFs, in order to prove that the proposed approach shows no impairment in the large-signal performance in terms of rise and fall times compared to the conventional approach that uses current-sources.

The two EF realization approaches are illustrated in Fig. 3.20, where C_L represents the capacitive load of the EF. We begin our analysis by expressing the emitter current I_E of transistor T_x:

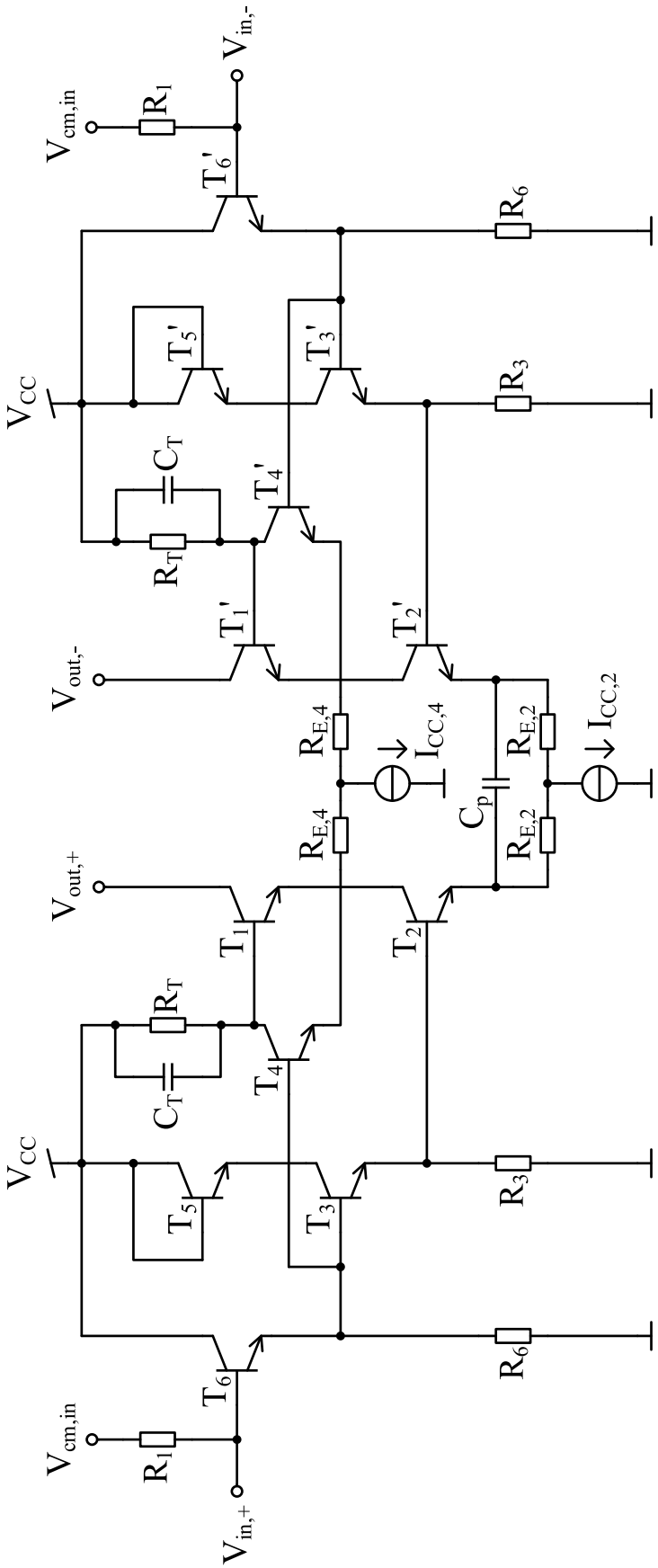


Figure 3.19: Circuit diagram [GKB+22]†. ©[2022] IEEE

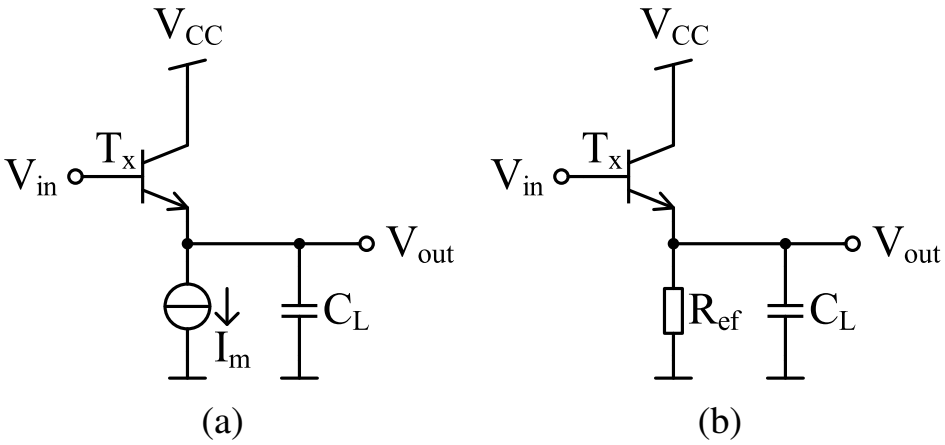


Figure 3.20: EF implementation with the bias current provided by (a) a current source and (b) a resistor [GKB+22]†. ©[2022] IEEE

$$\begin{aligned} I_E(t) &= I_S \exp\left(\frac{V_{BE}(t)}{V_T}\right) \\ &= I_S \exp\left(\frac{V_{in}(t) - V_{out}(t)}{V_T}\right) \end{aligned} \tag{3.6}$$

Next, we express the same emitter current I_E for the current-source approach case (Fig. 3.20 (a)):

$$I_E(t) = I_m + C_L \frac{dV_{out}(t)}{dt} \tag{3.7}$$

Inserting equation (3.6) in (3.7), we obtain the following relation:

$$I_S \exp\left(\frac{V_{in}(t) - V_{out}(t)}{V_T}\right) = I_m + C_L \frac{dV_{out}(t)}{dt} \tag{3.8}$$

By applying the following two derivation rules:

$$\frac{de^x}{dx} = e^x \tag{3.9}$$

and

$$\frac{df[g(x)]}{dx} = \frac{dg(x)}{dx}\frac{df[g(x)]}{dx} \tag{3.10}$$

and by differentiating equation (3.8) with respect to time t, we obtain:

$$\frac{I_S}{V_T}\left(\frac{dV_{in}(t)}{dt}-\frac{dV_{out}(t)}{dt}\right)\exp\left(\frac{V_{in}(t)-V_{out}(t)}{V_T}\right)=C_L\frac{d^2V_{out}(t)}{dt^2} \tag{3.11}$$

Considering equation (3.7), equation (3.11) becomes:

$$\begin{aligned}&\frac{1}{V_T}\left(\frac{dV_{in}(t)}{dt}-\frac{dV_{out}(t)}{dt}\right)\left(I_m+C_L\frac{dV_{out}(t)}{dt}\right)=C_L\frac{d^2V_{out}(t)}{dt^2}\Leftrightarrow\\&\Leftrightarrow\frac{d^2V_{out}(t)}{dt^2}=\frac{I_m}{C_LV_T}\frac{dV_{in}(t)}{dt}+\frac{1}{V_T}\frac{dV_{in}(t)}{dt}\frac{dV_{out}(t)}{dt}-\\&-\frac{1}{V_T}\left(\frac{dV_{out}(t)}{dt}\right)^2-\frac{I_m}{C_LV_T}\frac{dV_{out}(t)}{dt}\end{aligned} \tag{3.12}$$

Analogously, the emitter current for the resistor approach case (Fig. 3.20 (b)) is defined by the following relation:

$$I_E(t)=\frac{V_{out}(t)}{R_{ef}}+C_L\frac{dV_{out}(t)}{dt} \tag{3.13}$$

Inserting equation (3.6) in (3.13), we obtain the following relation:

$$I_S\exp\left(\frac{V_{in}(t)-V_{out}(t)}{V_T}\right)=\frac{V_{out}(t)}{R_{ef}}+C_L\frac{dV_{out}(t)}{dt} \tag{3.14}$$

By differentiating equation (3.14) with respect to time t, we obtain:

$$\frac{I_S}{V_T}\left(\frac{dV_{in}(t)}{dt}-\frac{dV_{out}(t)}{dt}\right)\exp\left(\frac{V_{in}(t)-V_{out}(t)}{V_T}\right)=\frac{1}{R_{ef}}\frac{dV_{out}(t)}{dt}+C_L\frac{d^2V_{out}(t)}{dt^2} \tag{3.15}$$

Considering equation (3.13), equation (3.15) becomes:

$$\frac{1}{V_T}\left(\frac{dV_{in}(t)}{dt}-\frac{dV_{out}(t)}{dt}\right)\left(\frac{V_{out}(t)}{R_{ef}}+C_L\frac{dV_{out}(t)}{dt}\right)=$$

$$=\frac{1}{R_{ef}}\frac{dV_{out}(t)}{dt}+C_L\frac{d^2V_{out}(t)}{dt^2}\Leftrightarrow$$

$$\Leftrightarrow\frac{d^2V_{out}(t)}{dt^2}=\frac{V_{out}(t)}{R_{ef}C_LV_T}\frac{dV_{in}(t)}{dt}+\frac{1}{V_T}\frac{dV_{in}(t)}{dt}\frac{dV_{out}(t)}{dt}-\frac{1}{V_T}\left(\frac{dV_{out}(t)}{dt}\right)^2-$$

$$-\frac{1}{R_{ef}C_LV_T}\frac{dV_{out}(t)}{dt}\left(V_{out}(t)+V_T\right) \tag{3.16}$$

In order to investigate the rise and fall times for the two EF implementation approaches, equations (3.12) and (3.16) were solved by means of a differential equation solver software. The results are shown in Fig. 3.21 (a) and (b) for the rise and fall time, respectively. As it can be seen, the two EFs show similar rise and fall times. Hence, it can be concluded that the proposed implementation approach for the EFs by means of resistors does not impair the large-signal performance in terms of rise and fall time compared to the usual approach where the bias currents are provided by current sources.

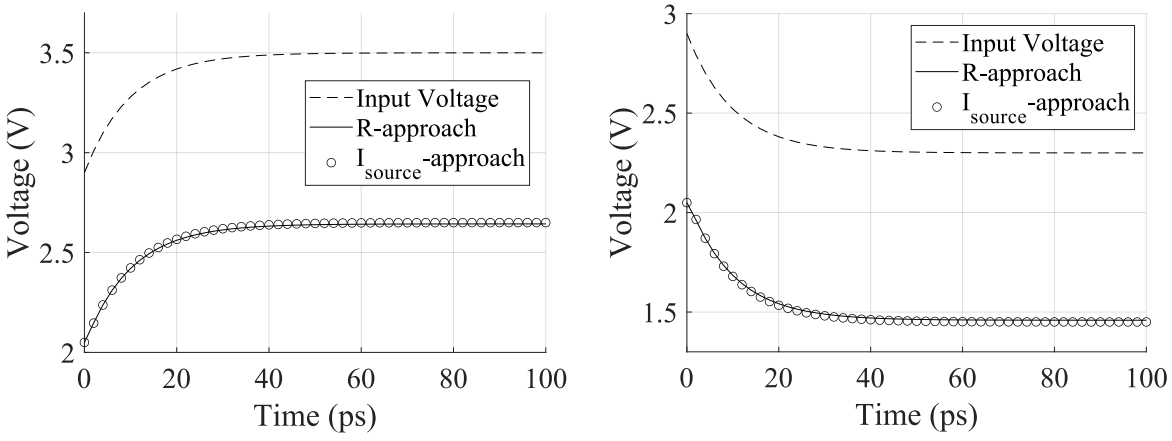


Figure 3.21: (a) Rise time and (b) fall time of the EF for the resistor (straight line) and current-source (circles) implementation approach.

We can therefore proceed to the dimensioning of the EFs T_6/T_6' and T_3/T_3' (Fig. 3.19) in order to optimize the bandwidth and the linearity of the whole circuit and thus prove that the proposed EF implementation approach offers a superior performance in terms of speed and linearity compared to the conventional one which uses current sources (for the same power consumption).

EF Dimensioning and Optimization

Next, we investigate the dimensioning of resistors R_6 and R_3, since they provide the bias currents for the EF stages T_6/T_6' and T_3/T_3' that drive the transistor pairs T_4/T_4' and T_2/T_2', respectively. Fig. 3.22 (a) and (b) show the dependency of the driver's bandwidth and THD (at 1 GHz), respectively, on resistors R_6 and R_3. The resistors are normalized to the small-signal transconductances $g_{m,T4}$ and $g_{m,T2}$ of transistors T_4 and T_2, respectively. For $R_6 = 20/g_{m,T4}$ and $R_3 = 40/g_{m,T2}$, the bias currents of transistors T_6/T_6' and T_3/T_3' correspond to 120% of their respective $I_{fT,max}$. As it can be seen in Fig. 3.22, the bandwidth is enhanced by 14% and the THD is improved by 16% compared to the case where the same bias currents amount to 80% of $I_{fT,max}$ (i.e. for $R_6 = 40/g_{m,T4}$ and $R_3 = 80/g_{m,T2}$). Nevertheless, for the case with higher bias currents, the overall power consumption of the circuit is increased by 33% in comparison to the case where the bias currents amount to 80% of $I_{fT,max}$. As a compromise between bandwidth, linearity and power

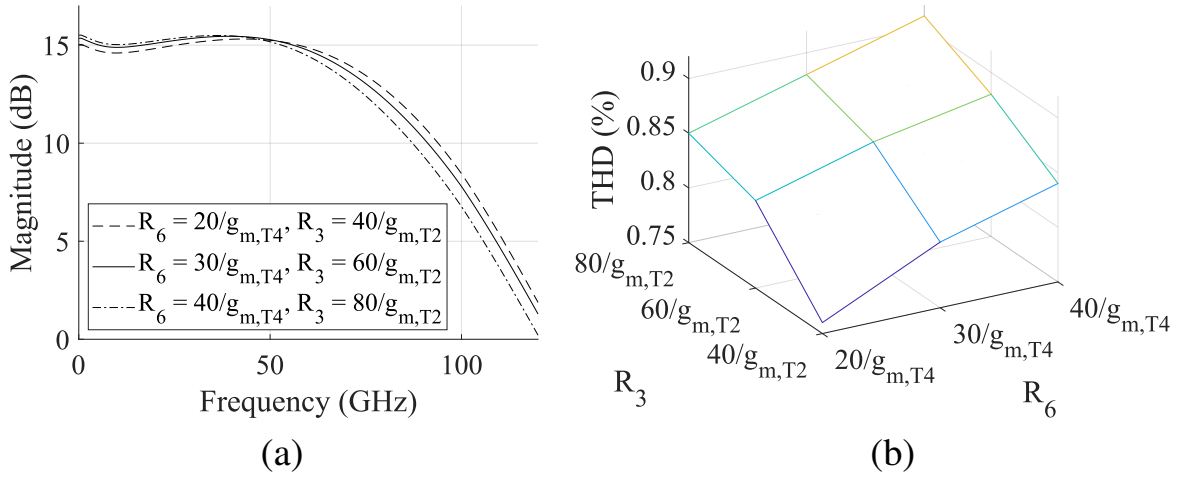


Figure 3.22: Influence of resistors R_6 and R_3 on (a) bandwidth and (b) THD, post-layout simulations.

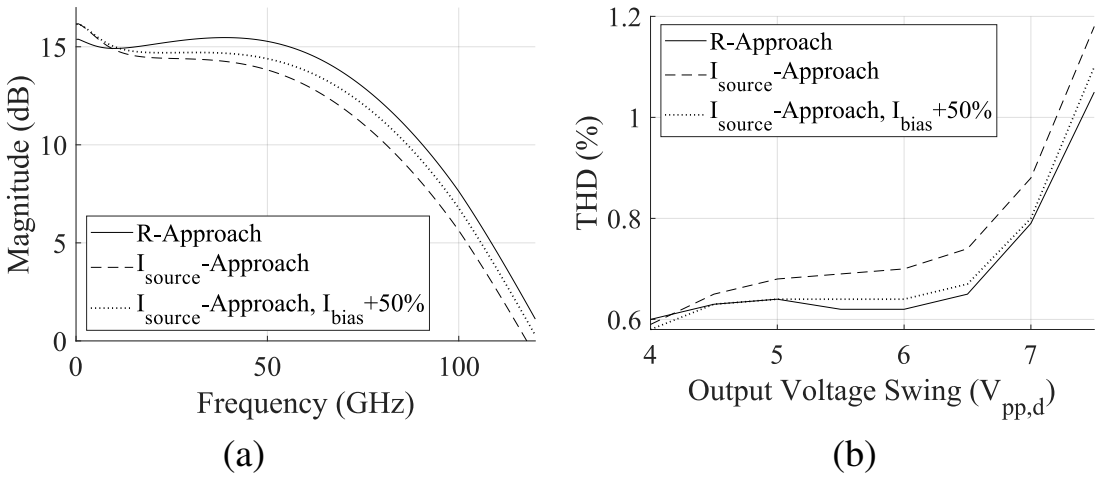


Figure 3.23: Comparison of (a) bandwidth and (b) THD for different EF realization approaches: with resistor (continuous line), current source (dashed line) and current source providing 50% more current (dotted line), post-layout simulations.

consumption, the values $R_6 = 32/g_{m,T4}$ and $R_3 = 62/g_{m,T2}$ were chosen.

With the selected values of R_6 and R_3 and the corresponding EF bias currents, a comparison study was done in terms of driver bandwidth and linearity for the cases where the bias currents of the EFs T_6/T_6' and T_3/T_3' are provided either by means of resistors or by current sources (i.e. the resistor or the current-source approach for the EF implementation, respectively). For the current-source approach, carefully dimensioned current mirrors were employed in order to provide the same bias currents to the EFs as for the resistor approach. As it can be seen in Fig. 3.23 (a), the simulated driver bandwidth in the case of the current-source approach is 23% lower compared to the resistor approach. This is explained by the parasitic capacitance of the current mirrors. Fig. 3.23 (b) shows the driver's THD simulated at 1 GHz for the two approaches. For output voltage swings of the driver above 4.2 $V_{pp,d}$, the THD for the current-source approach is higher compared to the resistor approach. Thus, at 7.2 $V_{pp,d}$ output swing, the driver with EFs implemented by means of current-sources shows a 12% higher THD than for the resistor-approach case. The loss in performance in terms of linearity and bandwidth for the current-source approach can be partially compensated by increasing the EF bias currents provided by the current mirrors by 50%, as shown in Fig. 3.23

(a) and (b). Nevertheless, this would result in an increase of 24% of the overall power consumption of the circuit with respect to the resistor-approach case.

Driver Linearization

The driver was linearized by means of the emitter degeneration resistors $R_{E,2}$. The choice of these resistors was done considering a trade-off with the DC gain of the driver. A higher resistance means a higher linearity and thus a lower THD, however it considerably reduces the gain. Fig. 3.24 (a) illustrates the trade-off between linearity and gain. The THD was simulated at 1 GHz and corresponds to a differential output voltage swing of 7.2 $V_{pp,d}$. $R_{E,2}$ is normalized to $1/g_{m,T2}$, where $g_{m,T2}$ is the small-signal transconductance of transistor T_2. For a high linearity of the circuit, the product $g_{m,T2}R_{E,2}$ must be much greater than 1 [SS16]. Targeting a THD below 1% and without neglecting the DC gain, the value of $R_{E,2} = 5.5/g_{m,T2}$ was selected. The gain was chosen so that the driver provides the full swing of 7.2 $V_{pp,d}$ when 1.3 $V_{pp,d}$ (650 mV_{pp} single-ended) is applied at the input.

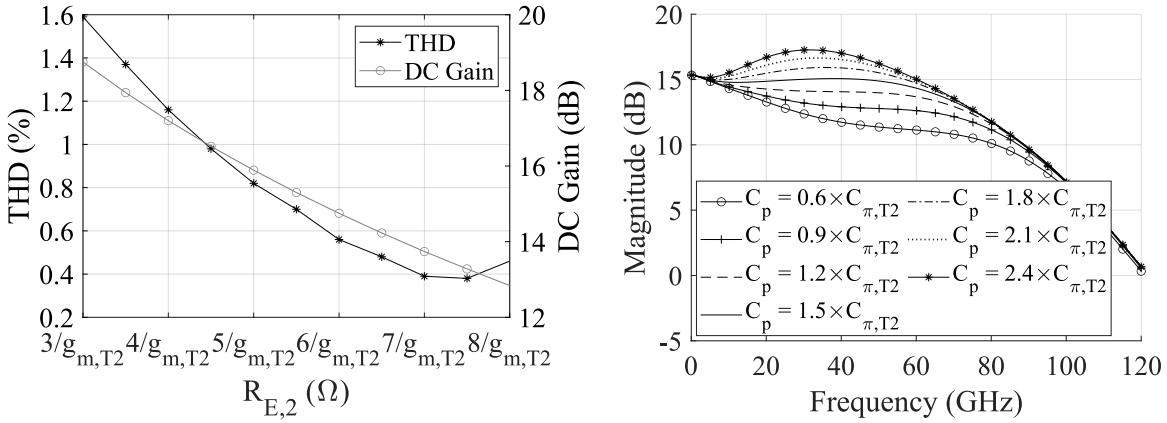


Figure 3.24: (a) Dependency of THD and DC gain on $R_{E,2}$ [GKB+22]† ©[2022] IEEE; (b) amplitude frequency response for different capacitances C_p. Post-layout simulations.

Bandwidth Enhancement

In order to enhance the bandwidth, an emitter degeneration capacitor C_p was used. Fig. 3.24 (b) shows the amplitude frequency response of the driver for different capacitances C_p normalized to the parasitic base-emitter capacitance $C_{\pi,T2}$ of transistor T_2. The value $C_p = 1.5 \times C_{\pi,T2}$ was chosen in order to effectively enhance the bandwidth while avoiding a high peaking.

Fig. 3.25 shows the simulated single-ended eye diagrams of the proposed driver for non-return to zero (NRZ) and 4-level pulse-amplitude modulation (PAM-4), respectively. The input voltage has an amplitude of 650 mV_{pp}. In simulations, the driver achieves a symbol rate of at least 72 Gbaud for NRZ and 45 Gbaud for PAM-4 modulation, respectively (the latter corresponding to 90 Gb/s), while yielding an output voltage swing of 3.6 V_{pp} (single-ended).

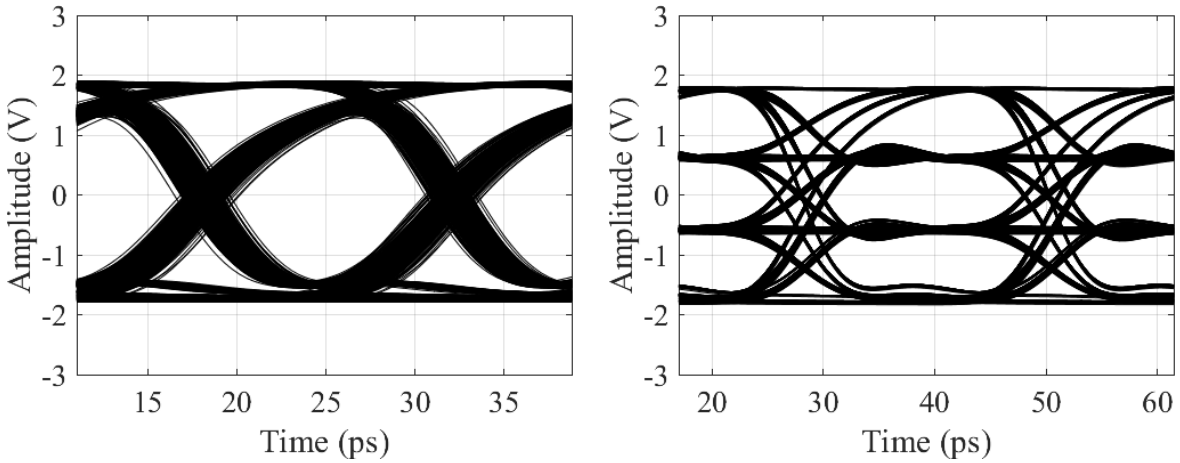


Figure 3.25: Simulated single-ended eye diagrams at (a) 72 Gbaud (NRZ) and (b) 45 Gbaud (PAM-4) (post-layout transient simulations).

3.2.3 Experimental Characterization

In order to study the functionality of the driver and to prove the design concepts presented in the previous section, the circuit was fabricated and subsequently measured. The photograph of the chip is shown in Fig. 3.26. The

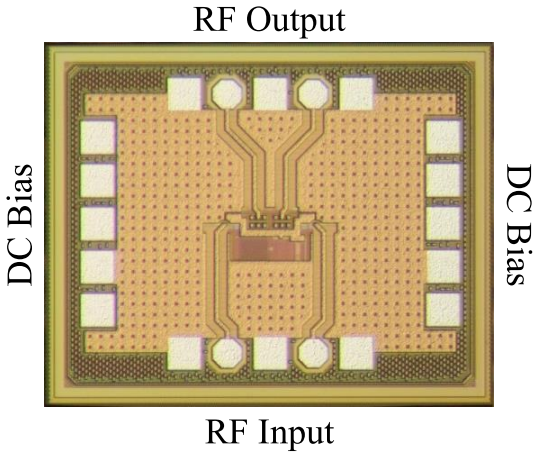


Figure 3.26: Chip micrograph; size: 1×0.8 mm^2 [GKB+22]†. ©[2022] IEEE

chip has a size of 1×0.8 mm^2. The total DC power consumption is 670 mW.

S-Parameter Measurement

The S-parameters of the circuit were measured differentially by means of a 67-GHz 4-port network analyzer. The measurement setup is shown in Fig. 3.27. The driver's output common mode level was provided by means of the network analyzer's integrated bias tees, and the load was represented by the 50-Ω impedance of the measurement device. The measured differential

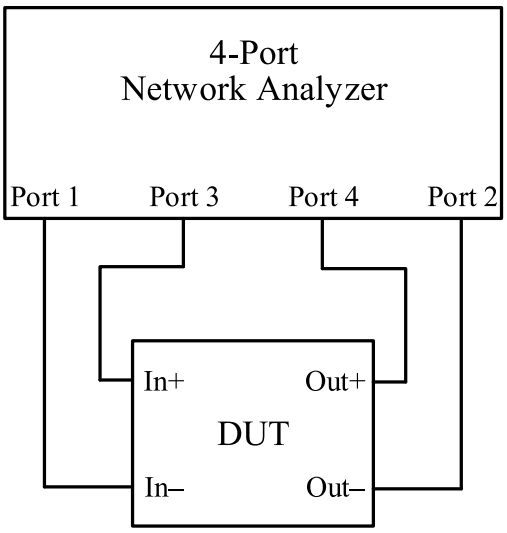


Figure 3.27: S-parameter measurement setup.

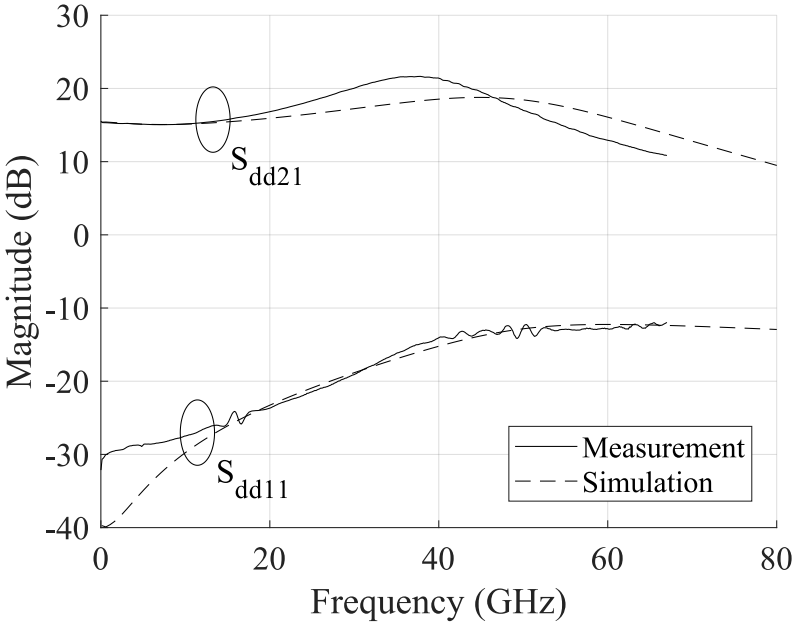


Figure 3.28: Differential S_{dd21} and S_{dd11}; comparison between measurement (solid lines) and post-layout simulation (dashed lines) [GKB+22]†. ©[2022] IEEE

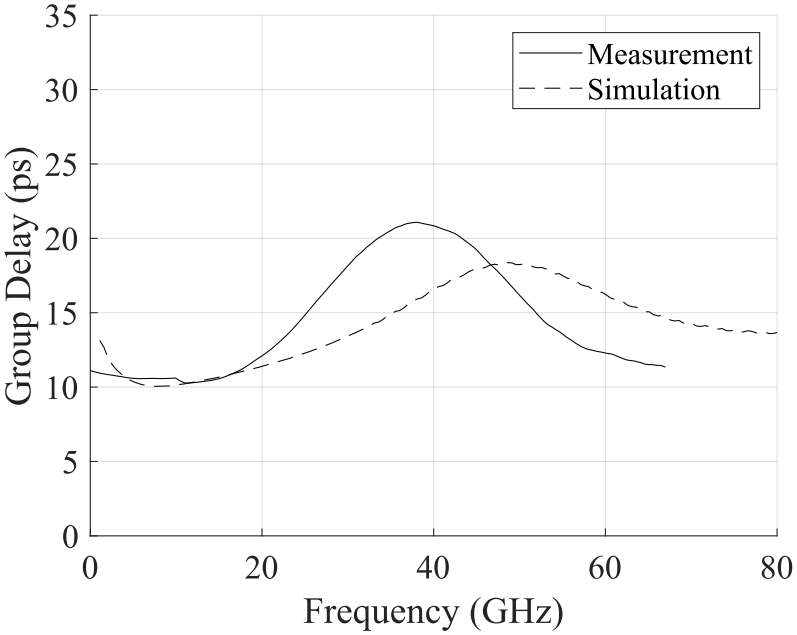


Figure 3.29: Group delay (calculated based on the differential S_{dd21}); comparison between measurement (solid line) and post-layout simulation (dashed line) [GKB+22]†. ©[2022] IEEE

S_{dd21} and S_{dd11} are shown in Fig. 3.28. The driver has a small-signal differential gain of 15.5 dB and a 3-dB bandwidth of 61.2 GHz. The circuit shows a very good input matching to 50 Ω, as the differential S_{dd11} stays below -12 dB for the whole measured frequency range.

The group delay of the driver was calculated based on the measured differential S_{dd21} and the results are shown in Fig. 3.29. Considering the middle group delay value of 16 ps, the group delay variation is limited to ± 5 ps for the entire measured frequency range.

Linearity Measurement

In order to evaluate the linearity of the driver, the THD was measured by means of a 67-GHz spectrum analyzer. The input signal was a sine wave with a frequency of 1 GHz provided by a low-distortion signal generator. The measurement setup is shown in Fig. 3.30. Since the input and the output of the spectrum analyzer and the signal generator, respectively, are single-ended and the driver is fully differential, baluns had to be employed at the driver's

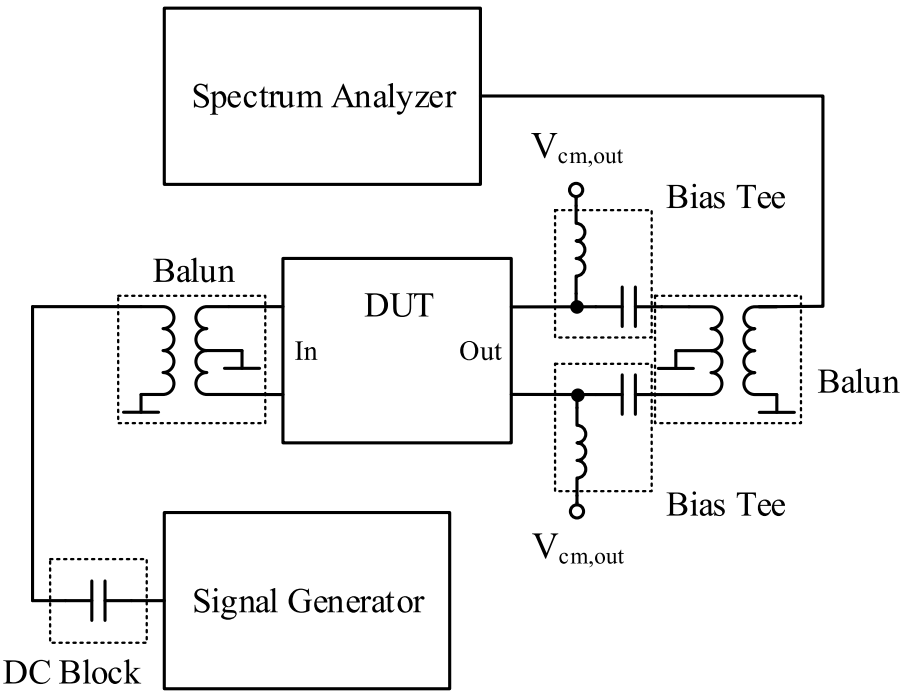


Figure 3.30: Linearity measurement setup [GKB+22]†. ©[2022] IEEE

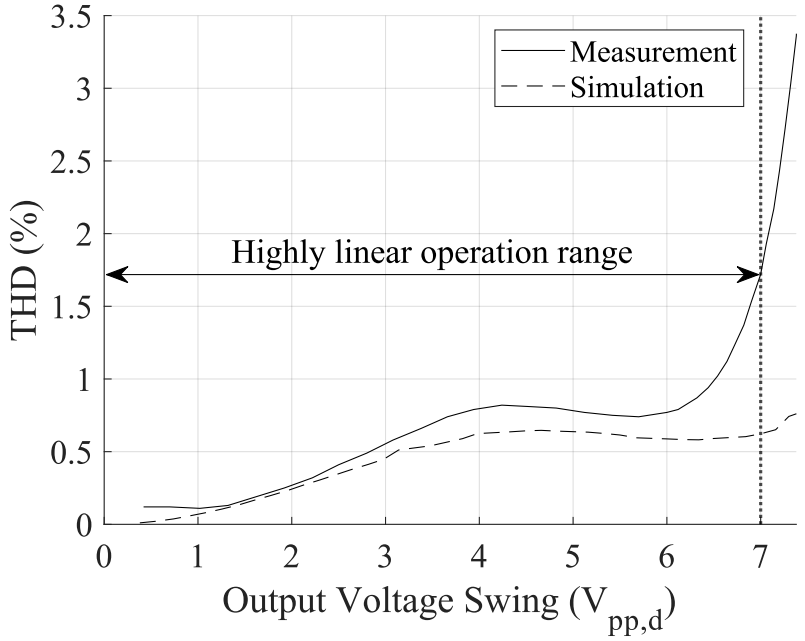


Figure 3.31: THD at different output voltage swings; comparison between measurement (solid line) and post-layout simulation (dashed line) [GKB+22]†. ©[2022] IEEE

input and output in order to convert the single-ended signal into differential one and vice versa. The driver's output common mode voltage was provided by means of external bias tees.

The measurement results are shown in Fig. 3.31. The driver shows a very high linearity up to the output voltage swing of 6.5 $V_{pp,d}$, the THD staying below 1%. At 7 $V_{pp,d}$ the THD increases to 1.7%, which still indicates a high linearity of the circuit.

Time-Domain Measurement

Fig. 3.32 depicts the measurement setup for the time-domain measurement. As input signals, two differential 2^{31}-1 pseudo-random bit sequences (PRBS) were used. The bit sequences were provided by a 64-Gb/s bit pattern generator (BPG). One output of the circuit was attenuated by 20 dB and fed into a sampling oscilloscope in order to measure the eye diagrams. The other output was connected to a 50-Ω termination. The output common mode voltage was provided by means of external bias tees. Since the BPG's maximum data rate

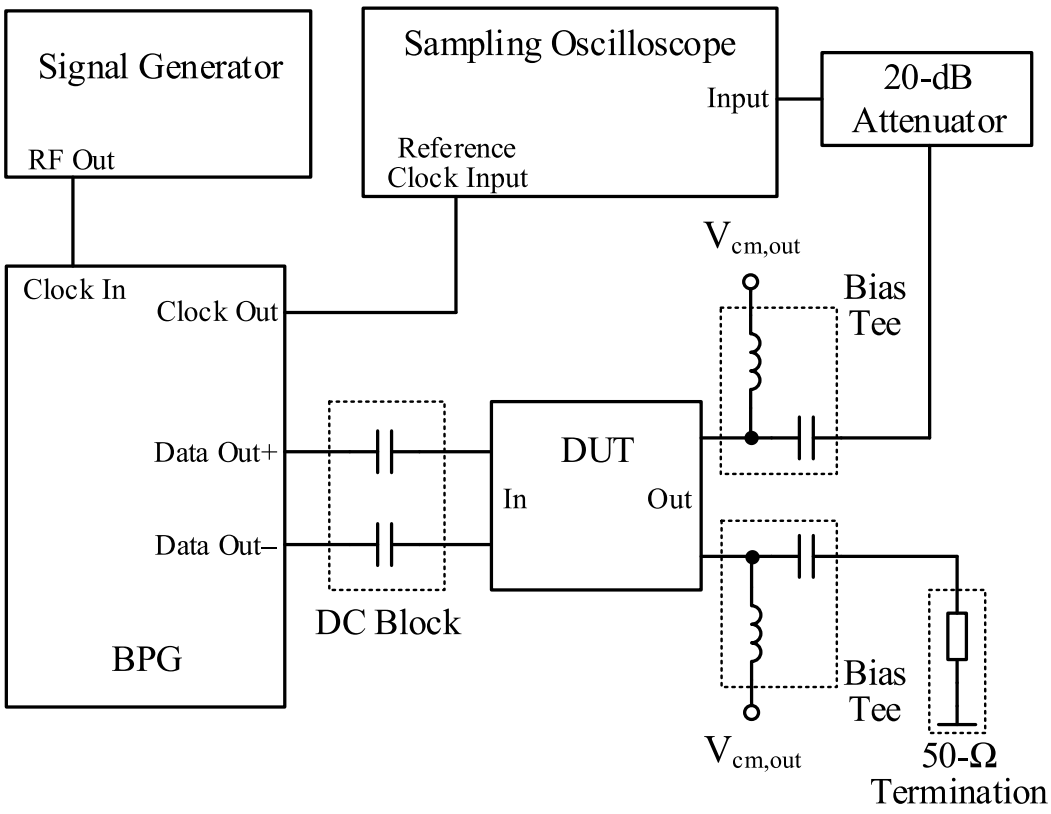


Figure 3.32: Time-domain measurement setup [GKB+22]†. ©[2022] IEEE

is limited to 64 Gb/s, a multiplexer was used in order to measure eye diagrams at higher data rates. For the measurement of PAM-4 eye diagrams, a PAM-4 input signal (2^{31}-1 PRBS) was generated by means of a 6-bit DAC.

Fig. 3.33 (a)–(d) show the measured single-ended output eye diagrams at various data rates. For an input signal with an amplitude of 650 mV_{pp}, a maximum output voltage swing of 3.6 V_{pp} was achieved, which corresponds to a differential swing of 7.2 $V_{pp,d}$. For NRZ data rates above 64 Gb/s (Fig. 3.14 (b)), the full output swing could not be reached since the output amplitude of the multiplexer is limited to 430 mV_{pp}. Fig. 3.14 (c) and (d) illustrate the PAM-4 eye diagrams at 35 Gbaud and 45 Gbaud, respectively, which correspond to 70 Gb/s and 90 Gb/s, respectively.

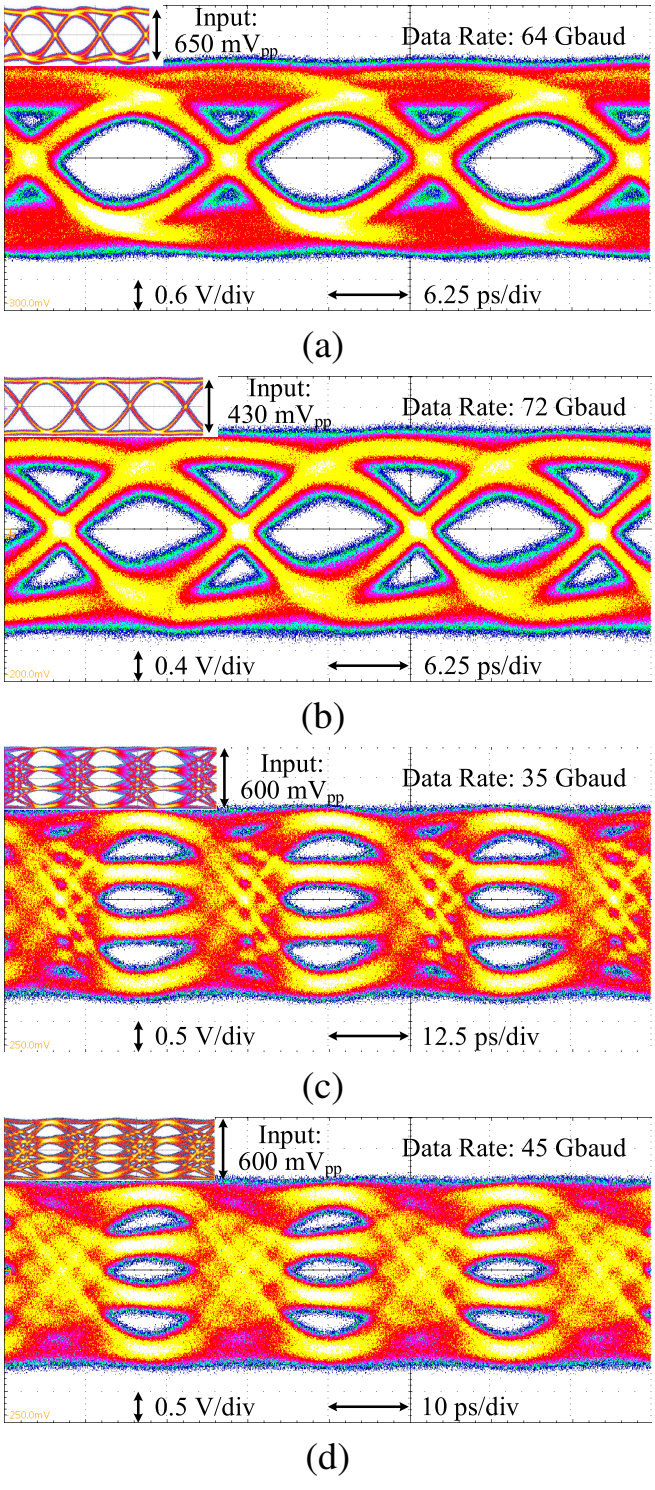


Figure 3.33: Measured single-ended output eye diagrams at (a) 64 Gbaud (NRZ), (b) 72 Gbaud (NRZ), (c) 35 Gbaud (PAM-4), (d) 45 Gbaud (PAM-4) [GKB+22]†. ©[2022] IEEE

3.2.4 Achievements of the Basic Scientific Research

In this section, the concept of a linear and power-efficient modulator driver capable of reaching high output voltages swings was presented. The circuit is based on a breakdown voltage doubler architecture, which allows the overcoming of the limitation imposed by the collector-emitter breakdown voltages of the output transistors, thus enabling output voltage swings above 6.5 $V_{pp,d}$.

The first part of the study was focused on the optimization of the breakdown voltage doubler topology with regard to the output voltage swing distribution between the cascaded transistors of the output stage. Next, we have investigated and compared two implementation approaches for the EF stages of the circuit, namely the conventional approach where the bias currents are provided by current sources, and a new approach where the bias currents are provided by means of resistors. Following the mathematical analysis of the two approaches as well as their comparison by means of circuit simulations, we have concluded that the proposed approach – i.e. where the bias currents are provided by resistors – shows both a higher bandwidth and linearity than the conventional approach, without dissipating extra DC power. Next, we have investigated the trade-offs for the choice of the aforementioned bias currents, since a higher bandwidth and linearity require larger currents, which increase the power consumption. An additional trade-off between linearity and driver gain was studied, based on which the emitter degeneration resistors of the output differential pair were chosen. Moreover, the use of an open-collector topology for the output stage helped to increase the speed of the circuit while reducing the power consumption. Finally, the studies and considerations described above were successfully validated by means of the experimental characterization of the circuit.

Table 3.2 summarizes the performances of different high-swing, linear modulator drivers in the literature. The design presented in [AML+20] uses a breakdown voltage doubler topology as well. Nevertheless, compared to the driver proposed in this work, it reaches a 17% lower output voltage swing, a 35% lower bandwidth, a lower linearity and consumes 49% more DC power. The design presented in [RGA+17] uses a distributed amplifier topology and has a 47% higher bandwidth and a 18% lower power consumption than the

proposed driver, however it has a 44% lower output voltage swing and a much lower linearity. The design in [RJA+19] (cascode topology) reaches a 42% higher bandwidth, but its linearity is much lower, its DC power consumption is 79% higher and it has a 32% lower output swing. The driver presented in [BHSV17] (distributed amplifier topology) is superior in terms of bandwidth (14% higher) and gain, however it is inferior in terms of output swing (33% lower), linearity and power consumption (64% higher). The driver shown in [ZSV17] (series-stacked differential EF and MOS-HBT cascode topology) has a comparable bandwidth (though 6% lower), however it has a 22% higher power consumption, a 33% lower output swing as well as a lower linearity.

In conclusion, the driver presented in this section reaches the highest linearity and output voltage swing among linear modulator drivers reported in the literature with bandwidths above 40 GHz: the THD is 1% at 1 GHz for 6.5 $V_{pp,d}$ output swing and 1.7% for 7 $V_{pp,d}$. Comparing the ratio between the consumed DC power and the output voltage swing (P_{DC}/V_{out}), the proposed driver concept achieves the highest power efficiency among the designs presented in Table 3.2.

Table 3.2: Performance Summary and Comparison of High-Swing, Linear Modulator Drivers [GKB+22]†. ©[2022] IEEE

	Bandwidth (GHz)	Output Swing ($V_{pp,d}$)	THD (%)	Differential Gain (dB)	NRZ Data Rate (Gb/s)	PAM-4 Data Rate (Gbaud)	DC Power (mW)	P_{DC}/V_{out} ($W/V_{pp,d}$)	Technology
[RGA+17]	90	4	5* (for 3 $V_{pp,d}$)	12.5	120	45	550	0.14	130 nm SiGe BiCMOS
[RJA+19]	86.8	4.9	5⋆ (for 2.5 $V_{pp,d}$)	15.1	100	50	1200	0.24	700 nm InP DHBT
[BHSV17]	70	4.8	2◇ (for 4.5 $V_{pp,d}$)	20	120	64	1100	0.23	55 nm SiGe BiCMOS
[ZSV17]	57.5	4.8	2.5⋆ (for 2.5 $V_{pp,d}$)	18.8	64	64	820	0.17	55 nm SiGe BiCMOS
[AML+20]	40	6	3.6* (for 6 $V_{pp,d}$)	30	64	69	1000	0.17	130 nm SiGe BiCMOS
This Work	61.2	7.2	1* (for 6.5 $V_{pp,d}$)	15.5	72	45	670	0.09	130 nm SiGe BiCMOS

*at 1 GHz; ◇at 4 GHz; ⋆at 10 GHz.

3.3 A PAM-8 Modulator Driver Implemented as a Digital-to-Analog Converter

3.3.1 Introduction

While Section 3.1 focused on the NRZ data transmission, Section 3.2 presented a circuit suitable for higher-order modulation, namely PAM. For an m-level PAM signal with m different discrete pulse amplitudes, a number of $\log_2(m)$ different bits can be transmitted simultaneously within one symbol. In Section 3.2 we presented PAM-4 output eye diagrams, thus doubling the maximum achievable bit rate (since for the PAM-4 modulation, the baud rate corresponds to double the bit rate for a given bandwidth). In this section, we investigate the further increase of the modulation order of data transmission. To this end, we present the design concept of a PAM-8 modulator driver, realized as a 3-bit DAC. This topology converts three different input bit streams into an 8-level output signal, thus transmitting simultaneously three different bits within one symbol. Therefore, the bit rate corresponds to three times the baud rate. Hence, a significant increase in the speed of the circuit can be achieved while circumventing the limitations imposed by the bandwidth. One of the main advantages of DAC-based topologies in comparison with linear architectures is the reduced DC power consumption (for the same output voltage swing): while the linear circuits need to trade off linearity and power consumption, the DAC-based circuits switch the entire tail current between the output transistors, since these drivers operate as limiting amplifiers. Another important advantage of the DAC-type topologies is the fact that the parallel input bit streams can be fed directly into the driver, whereas in the case of a linear topology, the PAM signal must first be generated by means of additional circuit blocks, which increase the overall power consumption and design complexity.

The PAM-8 modulator driver presented in this section was realized as a binary-weighted DAC. The choice of this DAC architecture was motivated by its low power consumption (which is one of the main design targets for the proposed driver), as well as by the low design complexity and the small area [LSZ18]. A thermometer-coded DAC architecture would significantly

increase the design complexity, since it would require, for an *n*-bit DAC, 2^n-1 different units that are switched simultaneously as well as an additional thermometer decoder circuit, which would increase the power consumption [CCH14]. An advantage of the thermometer-coded topology compared to the binary-weighted one is the reduced glitching [GP17]. However, as it will be shown in the measurement results section, the driver does not exhibit glitches or any additional voltage peaks.

The driver achieves an output voltage swing of 4 $V_{pp,d}$, which is suitable for driving MZMs and reaching high ERs [RLP+16]. The driver can operate up to a symbol rate of 50 Gbaud, which for the PAM-8 modulation corresponds to a bit rate of 150 Gb/s. Furthermore, depending on the given requirements, the driver can also operate as a PAM-4 driver by turning off one of the tail currents of the output stage.

3.3.2 Circuit Design

The block diagram of the circuit is shown in Fig. 3.34. It consists of two stages, namely the single-ended to differential converters (SDC) and the output stage (PAM-8 core). The circuit has three inputs ($V_{in,B1/2/3}$), since it needs three different input bit streams to produce a PAM-8 signal. The three inputs are single-ended. After conversion to differential signals in the SDCs, they are fed into the PAM-8 core (the DAC), where they are amplified and

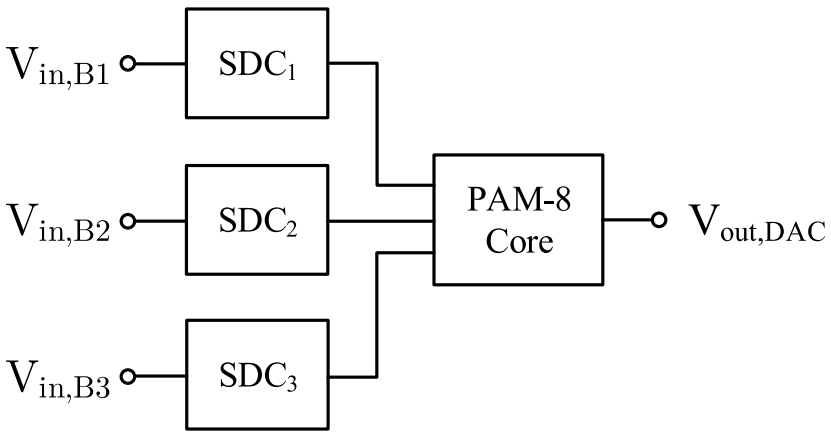


Figure 3.34: Circuit block diagram [GKB+21]†. ©[2021] IEEE

converted to an 8-level signal. The driver's output $V_{out,DAC}$ is differential.

The circuit was realized in a 130-nm SiGe BiCMOS technology with an f_T/f_{max} of around 350/450 GHz.

Single-Ended to Differential Converter

A total of three SDCs were employed at the input of the PAM-8 core circuit, in order to convert the single-ended input bit streams into differential signals. Therefore, no external single-ended to differential signal conversion is needed, hence relaxing the requirements on the stages preceding the driver. Moreover, having on-chip SDCs allows for a less complex and more accurate measurement setup, since the issues related to phase mismatch in differential channels are avoided [BSH+14].

The diagram of the SDC is shown in Fig. 3.35. The single-ended to differential signal conversion is performed by means of the two transistor pairs T_2-T_2' and T_3-T_3'. The purpose of having two distinct transistor pairs is to ensure a high quality differential signal with low rise and fall times. Additionally, the SDC has an emitter follower which serves as an input buffer and a 50-Ω resistor which provides input matching to the impedance of the measurement equipment.

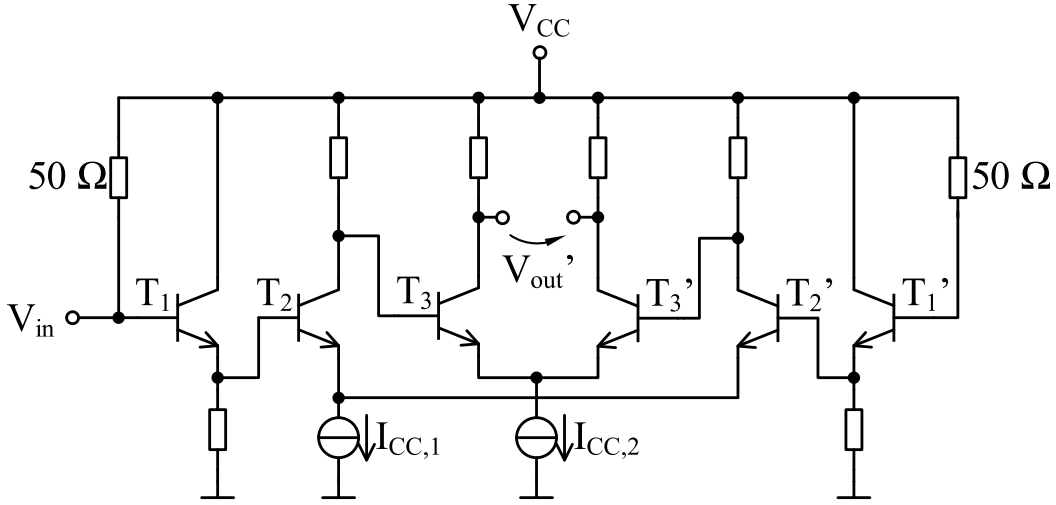


Figure 3.35: Diagram of the SDC [GKB+21]†. ©[2021] IEEE

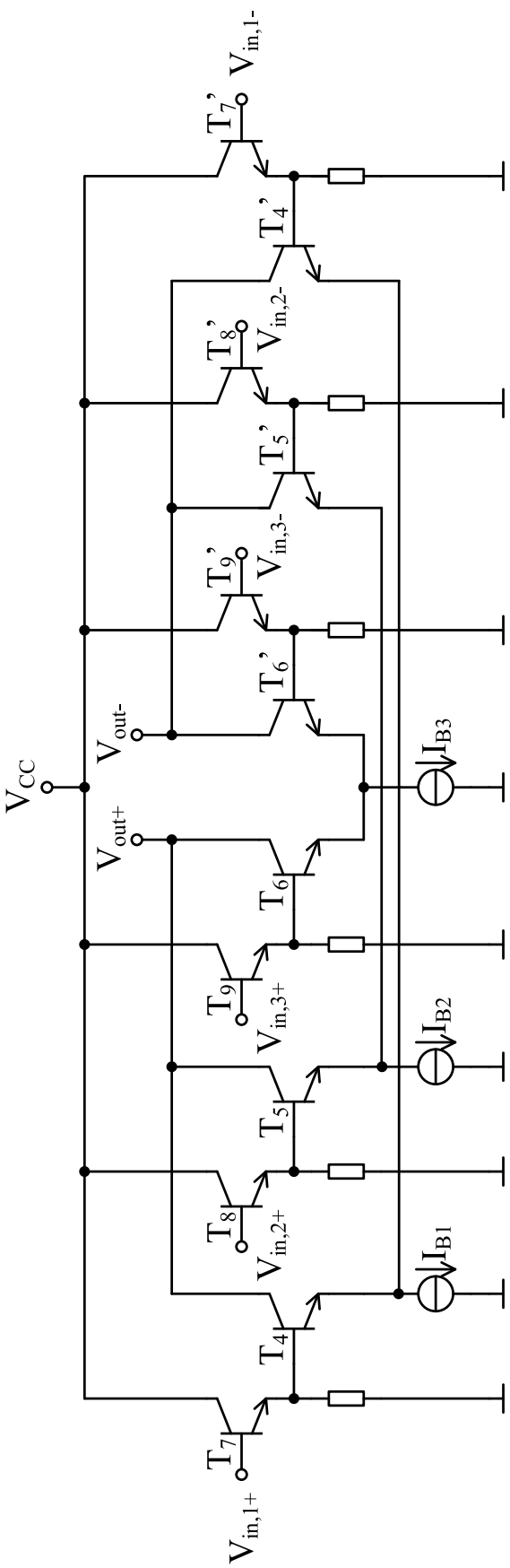


Figure 3.36: Diagram of the PAM-8 core [GKB+21]†. ©[2021] IEEE

PAM-8 Core

The circuit diagram of the PAM-8 core is depicted in Fig. 3.36. It represents the output stage of the driver and fulfills the function of a 3-bit DAC. This stage consists of three differential pairs, each corresponding to a particular bit. The tail currents I_{B1}, I_{B2} and I_{B3} are switched by the differential pairs depending on the three input bit streams, thus realizing 8 distinct output signal levels. The tail currents relate to each other as $I_{B2} = 2 \times I_{B1}$ and $I_{B3} = 2 \times I_{B2}$. Moreover, the PAM-8 core stage is provided with emitter followers in order to avoid the capacitive loading of the SDCs.

This stage was implemented as an open-collector, due to the advantages mentioned previously in sections 3.1 and 3.2 in terms of speed and power consumption.

The micrograph of the chip is shown in Fig. 3.37. The transmission lines connecting the RF input pads ($V_{in,B1/2/3}$) were designed to have the same length, in order to ensure the same delay for the three input signals. Additionally to supply (V_{CC} = 3.3 V) and ground (*gnd*) pads, the chip has three DC pads for the reference currents $I_{ref,B1/2/3}$ of the current mirrors that provide I_{B1}, I_{B2} and I_{B3} (Fig. 3.36). Thus, the three tail currents of the PAM-8 core can be tuned in case the current sources exhibit mismatches due to process variations.

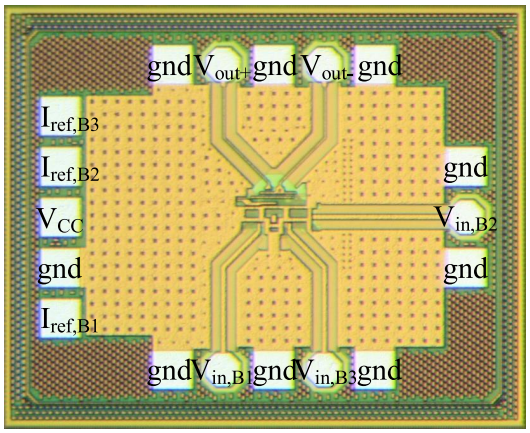


Figure 3.37: Chip micrograph; size: 1×0.8 mm^2 [GKB$^+$21]†. ©[2021] IEEE

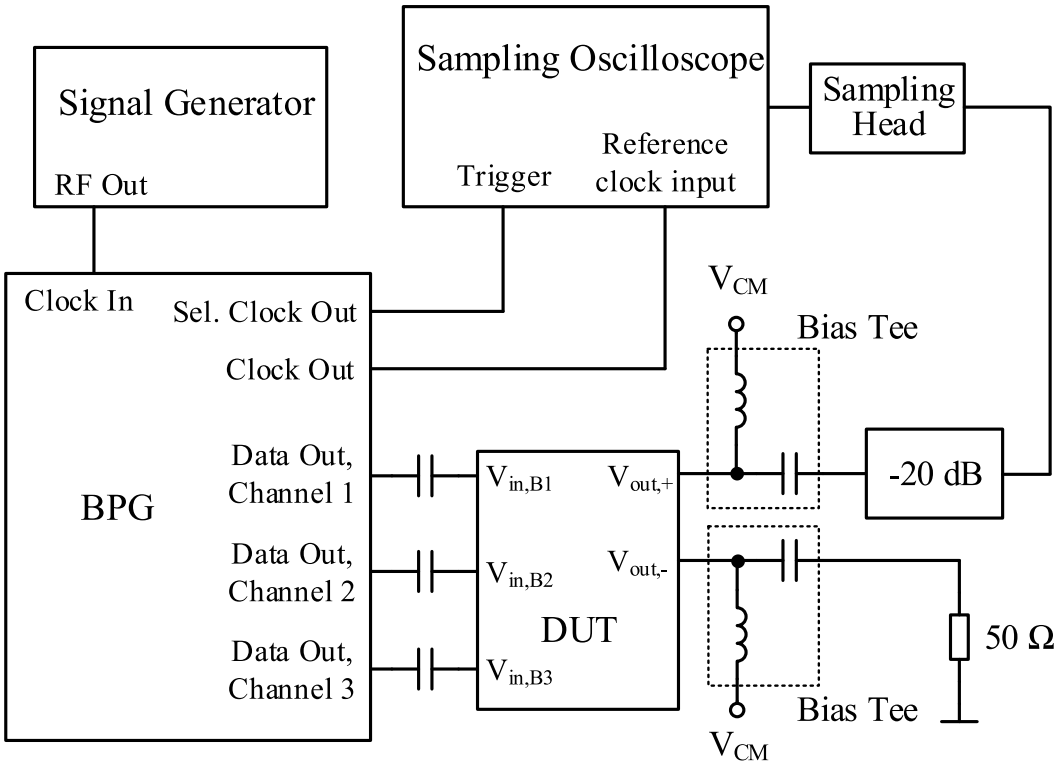


Figure 3.38: Measurement setup [GKB+21]†. ©[2021] IEEE

3.3.3 Experimental Characterization

Time-domain measurements have been performed in order to investigate the functionality of the circuit. The measurement setup is illustrated in Fig. 3.38. The input signals were three different non-return-to-zero (NRZ) 2^7-1 long pseudo-random bit sequences (PRBS) with 300-mV amplitude provided by a bit pattern generator (BPG). The output common mode level V_{CM} = 3.1 V was set by means of bias tees. One of the driver outputs was fed into a sampling oscilloscope after attenuation by 20 dB in order not to exceed the oscilloscope's maximum input amplitude. The other output was terminated by a 50-Ω resistor.

The measured single-ended PAM-8 output eye diagram at 50 Gbaud is displayed in Fig. 3.39 (a). This corresponds to a data rate of 150 Gb/s. The equivalent single-ended output voltage swing (considering the 20-dB attenuation) is 2 V_{pp}, which corresponds to a differential output swing of 4 $V_{pp,d}$. By turning off the DAC's tail current I_{B1}, the circuit works as a PAM-4 driver,

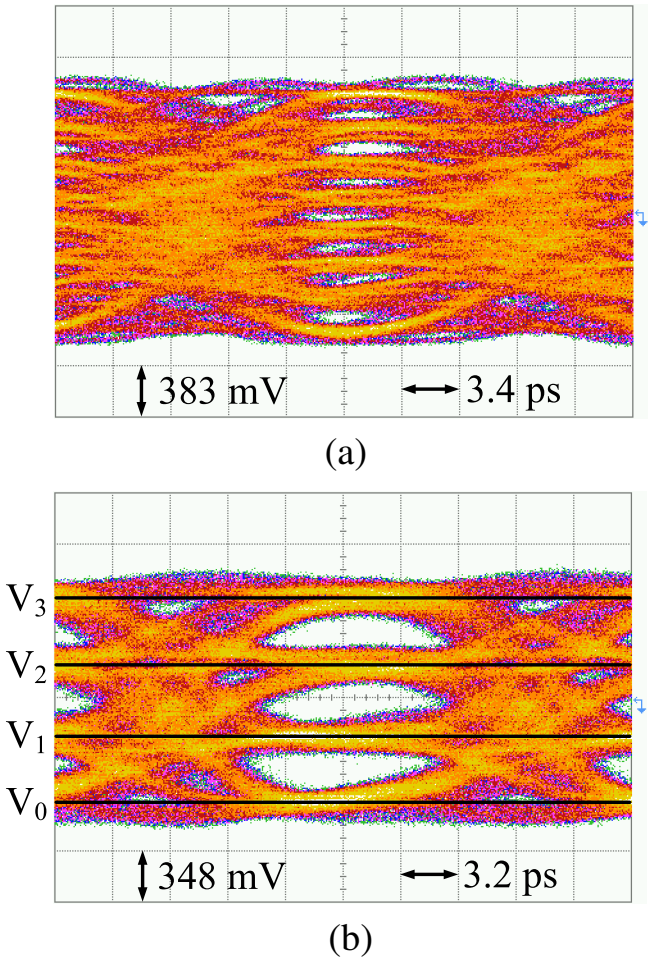


Figure 3.39: Measured single-ended (a) PAM-8 and (b) PAM-4 output eye diagram at 50 Gbaud (corresponding to 150 Gb/s and 100 Gb/s, respectively) [GKB+21]†. ©[2021] IEEE

however with a reduced output voltage swing of 3.4 $V_{pp,d}$ (Fig. 3.39 (b)). Based on this figure, the level separation mismatch ratio (RLM) of the driver was calculated according to the four voltage levels V_0, V_1, V_2 and V_3 of the PAM-4 eye. The calculated value of the RLM is 0.95, which indicates a high linearity of the eye diagram that corresponds to existing standards [KKRC21].

The total DC power consumption of the circuit is 590 mW. The PAM-8 core consumes 290 mW, while the rest is consumed by the SDCs.

3.3.4 Achievements of the Basic Scientific Research

In this section, the concept of a PAM-8 modulator driver was presented. The circuit uses a binary-weighted 3-bit DAC architecture and was realized in a 130-nm SiGe BiCMOS process. The driver has an output voltage swing of 4 $V_{pp,d}$, thus being suitable for driving MZMs and achieving high ERs. A symbol rate of 50 Gbaud was reached, which corresponds to a data rate of 150 Gb/s for the PAM-8 modulation. The circuit has a total DC power consumption of 590 mW (out of which, 290 mW is the power consumed by the DAC core).

The investigation presented in this section showed that a tunable modulator driver can be realized, which can switch between two modulation formats – PAM-8 and PAM-4, respectively – without the need of extra circuit blocks and without affecting the circuit's performance in terms of speed or power consumption. The open-collector design approach for the output stage, while increasing the speed of the driver (as explained in sections 3.1 and 3.2), does not close the seven eyes of the PAM-8 output eye diagram. Finally, by employing on-chip SDCs, the requirements on the stages preceding the circuit are relaxed, while the issues related to phase mismatch in differential signal paths are mitigated.

Table 3.3 shows a comparison with other DAC-type PAM modulator drivers presented in the literature. The comparison is done in terms of speed, output voltage swing and DC power consumption. The relation between these factors is given by two figures of merit, namely the energy efficiency and the ratio between the DC power and the output voltage swing. Compared to the other works listed in Table 3.3, the proposed circuit yields a high energy efficiency of 3.9 pJ/bit as well as a low DC power to output swing ratio of 0.15 $W/V_{pp,d}$. Inductive or capacitive peaking techniques may be used in order to increase the data rate and thus improve the efficiency, however this would considerably increase the chip area and would require further investigation concerning the stability of the circuit.

In conclusion, the modulator driver concept presented in this section is one of the most energy efficient DAC-based PAM drivers reported in the literature for symbol rates above 40 Gbaud. Moreover, the driver is able to switch

between PAM-8 and PAM-4 modulation formats thanks to its tunable DAC core and without penalty in performance or increased circuit complexity.

Table 3.3: Performance Summary and Comparison of DAC-Based PAM Modulator Drivers [GKB+21]†.
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	Symbol Rate (Gbaud)	DAC-Type	Output Swing ($V_{pp,d}$)	DC Power (mW)	Efficiency (pJ/bit)	DC Power/Output Swing (W/$V_{pp,d}$)	Technology
[KDJ+18]	100	2-bit (PAM-4)	3.7	-	-	-	700 nm
	64	3-bit (PAM-8)	4.3	1000*	5.2	0.23	InP DHBT
[LCG+17]	56	2-bit (PAM-4)	-	155	1.4	-	130 nm SiGe BiCMOS
[BRG+20]	53	2-bit (PAM-4)	2	385	3.6	0.19	55 nm SiGe BiCMOS
[RLA+17]	50	2-bit (PAM-4)	4	390	3.9	0.1	130 nm SiGe BiCMOS
[GKD+11]	42	3-bit (PAM-8)	3.25	1900*	15.1	0.58	700 nm InP DHBT
This Work	50	3-bit (PAM-8)	4	590$^{\diamond}$	3.9	0.15	130 nm SiGe BiCMOS

*only the output stage; *including three D flip-flop cells; $^{\diamond}$including three SDCs.

4 Conclusion and Further Research

In this thesis, the fundamentals of transmitter circuits for electro-optical communication networks have been studied, with focus on their front-end part. The theoretical analyses have been verified by means of conceptual implementation of different circuits, which have been simulated and subsequently measured in order to prove their functionality and to validate the studied concepts.

First, we have presented the concept of a monolithically integrated electro-optical transmitter consisting of an optical MZM and its electrical driver. Owing to the high output voltage swing of the driver, we showed that a compact modulator with short-length phase shifters can be realized, while achieving high ERs. Thus, we proved that one of the main disadvantages of MZMs, i.e. their large area, can be mitigated without sacrificing the ER. The transmitter was measured bit-error-free (10^{-10}) up to the data rate of 37 Gb/s, which is a record among monolithically integrated MZM-based transmitters in the literature. The achievement of this data rate was significantly facilitated by the use of an open-collector topology for the output stage of the driver.

Next, we have investigated an improved modulator driver architecture, which in addition to delivering a high output voltage swing, achieves a high linearity, a high power efficiency and a bandwidth above 60 GHz. The circuit shows a THD of 1% at 6.5 $V_{pp,d}$ output swing and 1.7% at 7 $V_{pp,d}$, which is a record among linear drivers in the literature in terms of linearity and output swing. Moreover, the circuit has a relatively low power consumption of 670 mW when considering its large output swing. This performance was enabled by the use of an open-collector topology for the output stage as well as by means of a new implementation approach for the EFs, where the EFs' bias

currents are provided by resistors instead of current sources. We showed that for the same bandwidth and linearity, the driver consumes 19 % less power when the EFs are implemented by means of the resistor approach.

Finally, we have focused on the way of enhancing the bit rate by using higher-order modulation formats. To this end, a PAM-8 driver concept was studied, implemented as a binary-weighted 3-bit DAC. The driver achieves a symbol rate of 50 Gbaud, which corresponds to a bit rate of 150 Gb/s for the PAM-8 modulation. By using a DAC architecture, which is non-linear, extra power could be saved, since the driver can switch the entire tail current between the output transistors. The circuit thus reaches one of the highest power efficiencies among DAC-based drivers in the literature. Moreover, due to its tunable tail currents, the driver can also yield PAM-4 output signals, thus showing that the modulation format can be switched without extra power or additional circuit parts. In addition to this, the driver features on-chip SDCs, which relax the requirements on the preceding stages.

The research done within this work offers the possibility of further investigations. First, the realization of faster monolithically integrated transmitters can be studied. By realizing MZMs with phase shifters of shorter length, it is possible to investigate the maximum achievable speed in a monolithically integrated transmitter, while taking into account the reduction of the ER. Furthermore, the co-integration of linear or DAC-based drivers with a Si MZM would allow to study the enhancement of the bit rate for monolithically integrated transmitters, since this would enable the use of higher-order modulation formats. In this regard, coherent systems could be realized that modulate both the amplitude and the phase of the signal (e.g. the 16-QAM or 64-QAM modulation formats), thus significantly increasing the number of bits that can be sent within one symbol of data for a given bandwidth of the system.

Finally, further research can be done on the electro-photonic technology. On the one hand, the co-integration of transistors with higher f_T/f_{max} would considerably extend the boundaries of the maximum achievable data rate of a transmitter. On the other hand, a particularly promising research field is the co-integration of III-V laser diodes on the Si chip [SVB+18], which would allow the realization of fully-integrated electro-optical transceivers. Such a manufacturing process would eliminate the coupling losses of the external

laser source into the electro-photonic chip, thus enabling the reduction of the laser's output optical power and therefore its electrical power consumption. Moreover, the full co-integration of III-V laser diodes on Si photonics platforms would present the cost advantages of the CMOS manufacturing processes.

Own Publications

Journal Articles

1. A. Giuglea, G. Belfiore, M. M. Khafaji, R. Henker and F. Ellinger, "A 37-Gb/s Monolithically Integrated Electro-Optical Transmitter in a Silicon Photonics 250-nm BiCMOS Process," *Journal of Lightwave Technology*, 2022. (Reference in text: [GBK$^+$22]†)

2. A. Giuglea, M. M. Khafaji, G. Belfiore, R. Henker and F. Ellinger, "A Low-Distortion Modulator Driver With Over 6.5-V_{pp} Differential Output Swing and Bandwidth Above 60 GHz in a 130-nm SiGe BiCMOS Technology," *IEEE Access*, 2022. (Reference in text: [GKB$^+$22]†)

Conference Proceedings

1. A. Giuglea, M. M. Khafaji, G. Belfiore, R. Henker and F. Ellinger, "A 50-Gbaud PAM-8 Modulator Driver Realized as a 3-Bit Digital-to-Analog Converter," *2021 International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME)*, 2021. (Reference in text: [GKB$^+$21]†)

2. A. Giuglea, G. Belfiore, M. M. Khafaji, R. Henker, D. Petousi, G. Winzer, L. Zimmermann and F. Ellinger, "Comparison of Segmented and Traveling-Wave Electro-Optical Transmitters Based on Silicon Photonics Mach-Zehnder Modulators," *2018 Photonics in Switching and Computing (PSC)*, 2018. (Reference in text: [GBK$^+$18b]†)

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List of Abbreviations

III-V	semiconductor alloy containing elements from the groups III and V of the periodic table of elements
AC	alternating current
BER	bit error rate
BiCMOS	integration of bipolar junction transistors and complementary metal-oxide-semiconductor transistors
BJT	bipolar junction transistors
BPG	bit pattern generator
BVD	breakdown voltage doubler
CMOS	complementary metal-oxide-semiconductor
dB	decibel
DAC	digital-to-analog converter
DC	direct current
DEMUX	demultiplexer
DFB	distributed feedback laser
DHBT	double heterojunction bipolar transistor
div	division
DUT	device under test
e.g.	*exempli gracia* (for example)
EA	error analyzer
EDFA	erbium-doped fiber amplifier
EF	emitter follower
EPIC	electro-photonic integrated circuit
ER	extinction ratio
et al.	*et alius* (and others)
FET	field-effect transistor
FF	flip-flop

Fig.	figure
GaAs	gallium arsenide
Gb/s	Gigabits per second
Gbaud	Gigabaud
H	Henri
HBT	heterojunction bipolar transistor
Hz	Herz
i.e.	*id est* (that is)
IEEE	Institute of Electrical and Electronics Engineers
InP	indium phosphide
ISI	intersymbol interference
IT	information technology
$LiNbO_3$	lithium niobate
log	logarithm
m	meter
MMI	multi-mode interference coupler
MUX	multiplexer
MZM	Mach-Zehnder modulator
n-doping	doping of semiconductor with electrons
NRZ	non-return-to-zero modulation
OP	operating point
p-doping	doping of semiconductor with holes
PAM	pulse amplitude modulation
PCB	printed circuit board
PIC	photonic integrated circuit
PLL	phase-locked loop
pn-junction	boundary between *p*-doped and *n*-doped semiconductor region
PRBS	periodic random bit sequence
QAM	quadrature amplitude modulation
RC circuit	circuit consisting of a resistor and a capacitor
RF	radio frequency
RLM	level separation mismatch ratio
s	second

SDC	single-ended to differential converter
Si	silicon
Si MZM	silicon photonics Mach-Zehnder modulator
SiGe	silicon-germanium
SNR	signal-to-noise ratio
THD	total harmonic distortion
TIA	transimpedance amplifier
TL	transmission line
V	volt
W	watt

List of Symbols

Large signal parameters are written with capital letters, while small-signal parameters are written with lowercase letters.

α	MZM insertion loss factor
Ω	Ohm
A_v, a_v	voltage gain
B	base of transistor
B_i, b_i	current gain
BV_{CE}	collector-emitter breakdown voltage of transistor
c	speed of light in vacuum
C	collector of transistor
C_μ	parasitic capacitance of transistor's base-collector *pn*-junction
C_π	parasitic capacitance of transistor's base-emitter *pn*-junction
C_{Load}	load capacitor
C_p	emitter degeneration capacitor
C_S	parasitic substrate capacitance of transistor (between collector and substrate)
C_u	capacitance per unit of length
cos	cosine function
E	emitter of transistor
f	frequency
f_{max}	maximum frequency of oscillation
f_T	transit frequency
g_m	transconductance of transistor
I_{bias}	bias current
I_B, i_B	base current

I_C, i_C	collector current
I_{CC}	tail current
I_E, i_E	emitter current
$I_{fT,max}$	current at which the transistor's maximum transit frequency is reached
I_{in}, i_{in}	input current
I_{out}, i_{out}	output current
I_{ref}	reference current for current mirror
I_S	reverse saturation current
k	Boltzmann constant
L	length
L_u	inductance per unit of length
n_g	refractive group index of optical waveguide
P_{DC}	DC power consumption
P_{in}	input power
P_{out}	output power
q	elementary charge of an electron
r_π	resistance between base and emitter of transistor
r_o	output resistance of transistor
R_C	collector resistor
R_E	emitter resistor
R_{end}	transmission line termination resistor
R_{Load}	load resistor
R_u	resistance per unit of length
sin	sine function
t	time
T	temperature
t_{el}	propagation delay in the transmission line
t_{op}	propagation delay in the optical waveguide
T_x	transistor with designator "x"
tanh	tangent hyperbolic
V_π	voltage required to reach a 180° phase shift in a phase shifter
V_A	early voltage

V_B	voltage potential at transistor's base
V_C	voltage potential at transistor's collector
V_{CC}	supply voltage
V_{BE}, v_{BE}	base-emitter voltage
V_{bias}	bias voltage
V_{CB}, v_{CB}	collector-base voltage
V_{CE}, v_{CE}	collector-emitter voltage
V_{cm}	common-mode voltage
V_{drv}	driver output voltage
V_E	voltage potential at transistor's emitter
V_{in}, v_{in}	input voltage
V_{out}, v_{out}	output voltage
V_{pp}	peak-to-peak voltage
$V_{pp,d}$	peak-to-peak differential voltage
V_T	thermal voltage
Z_0	characteristic impedance of transmission line
$Z_{0,loaded}$	characteristic impedance of loaded transmission line
$Z_{0,unloaded}$	characteristic impedance of unloaded transmission line

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