A Class-AB/D Audio Power Amplifier for Mobile Applications Integrated Into a 2.5G/3G Baseband Processor

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***Abstract*—A filterless class-AB/D audio power amplifier integrated into a feature-rich 2.5G/3G baseband processor in standard 65-nm CMOS technology is designed for direct battery hookup in mobile phone applications. Circuit techniques are used to overcome the voltage limitations of standard MOS transistors for operation at voltage levels of 2.5–4.8 V. Both amplifiers can drive more than 650 mW into an 8-Ω load with maximum distortion levels of 1% and 5% for class-D and class-AB, respectively, all from a 3.6-V power supply. The achieved power-supply-rejection ratios are 72 and 84 dB, respectively. The mono implementation of both amplifiers together is 0.44 mm^2.**

***Index Terms*—Baseband processor, class-AB amplifier, class-D amplifier, CMOS, SoC, system-on-chip**

I. Introduction

TODAY'S CELLULAR phone market can be roughly divided into three segments: the smart phone, the feature, and the entry segment. The data-centric smart phone market is the high-end segment using the so-called "Open OS" architectures (e.g., Symbian, Linux, etc.) supporting the installation of third-party applications. The feature market is more based on elaborate real-time (proprietary) operating systems which support mid- to high-end multimedia components and applications. Finally, the entry segment is mostly based on voice- and text-message-centric 2G and 2.5G handsets, possibly also encompassing 3G in the near future. Cost is the main driver in the entry market, while applications drive the high-end segment. The segmentation is also reflected in the bill of material of cellular phones: higher price pressure and, as a result, a higher level of integration is required for feature and entry phones, whereas smart phones more often feature stand-alone high-end and thus more expensive components. The latter is particularly true for multimedia and audio applications.

This paper mainly focuses on feature- and entry-type phones, where cost is the main driver and a balance between bill of material and performance is sought. More particularly, we focus on a 2.5/3G baseband processor, including EGPRS class 12, HSDPA up to 7.2 Mbit/s, and HSUPA up to 2 Mbit/s with analog input and analog output as the main features on the telecom side. This baseband IC also includes a highly integrated multimedia pipe featuring TV out; various codecs such as MP3, AAC+, and eAAC; several analog and digital microphone inputs used for interference cancellation purposes; and audio handset and headset mode as well as a high-drive stereo class-AB/D audio amplifier. A high-level block diagram of the IC is shown in Fig. 1. In this paper, we will mainly focus on the audio part—more specifically, on the design and implementation of the class-AB/D audio amplifier.

High-power audio amplifiers are increasingly used in portable applications. Solutions mainly take advantage of class-AB [1] or class-D amplifiers [2]–[5]. In particular, the latter one is becoming a standard in portable electronic devices such as MP3 players, personal digital assistants, and cellular phones. The high efficiency of class-D amplifiers reduces supply current and heat, increases output power, and extends the battery lifetime. This makes them best suited for low-voltage low-power applications. In particular, multichannel audio products are perfect candidates for class-D amplifiers in system-on-chip (SoC) designs, where the generated heat is a critical parameter because of the high thermal resistance of the package. Unfortunately, class-D amplifiers suffer from a slightly lower power supply rejection ratio (PSRR) than class-AB amplifiers because they use the power-supply voltage directly to generate the output. Any PSRR must be achieved via the feedback loop and the matching between the channels. In class-AB, the supply is decoupled as long as the output signal is within the linear range. PSRR is a parameter of predominant importance in cellular phone applications. Additionally, customers may want to choose between a class-AB amplifier, e.g., for the so-called receiver mode applications, and a class-D driver, e.g., for high-drive applications. In the case of the so-called single-speaker applications, only one speaker is used, both for high power as well as for receiver mode applications. The latter one is typically used in single-ended configuration, and hence, the class-AB configuration is the preferred solution. Accordingly, offering both class-AB and class-D amplifiers in one design provides additional flexibility to the customer.

Prior work in the class-D field mainly focuses on improving parameters like output power, efficiency, and distortion, as well as reducing the system cost through a higher level of integration.

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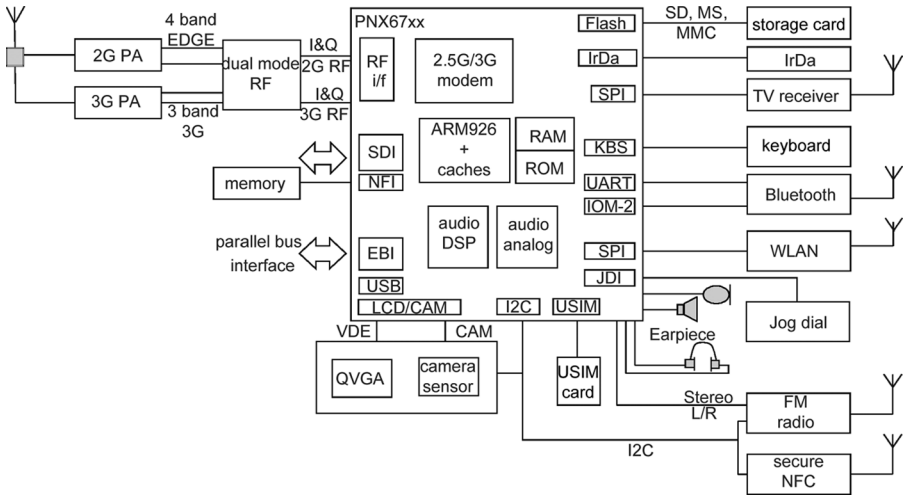

Fig. 1. Top-level block diagram and configuration example of a baseband IC including an audio codec.

All of these improvements are based on enhanced architectures and/or topologies. State-of-the-art class-D amplifiers for mobile applications are now fully implemented on-chip [2]–[5]. Many of them take advantage of a high-voltage process (up to 7 V) or special MOS transistor options (i.e., extended drain) to sustain the battery supply voltage (up to 4.8 V). Similarly, previous work on class-AB amplifiers is mostly based on elaborate circuit techniques such as in [1]. Little work has been presented on class-AB/D amplifiers combined with a baseband IC in a standard deep-submicrometer CMOS process.

The audio class-D amplifier presented here is based on a frequently used analog pulsewidth modulation (PWM) modulator topology, which includes an integrating feedback loop and supports filterless operation. The class-AB amplifier is similar to that in [1] and uses the same power output stages as the class-D part. Shown here is the implementation of a class-AB/D amplifier for a SoC for cellular phones using a 65-nm digital deep-submicrometer CMOS technology with thick-oxide option with 2.5-V capability. Special circuit techniques overcome the voltage limitations of thick-oxide transistors in the output stage that is connected to the battery supply voltage. The class-D design incorporates slew-rate control of the output driver to minimize the high-frequency content. The carrier frequency is programmable from 150 to 580 kHz, and the closed-loop gain is programmable from -30 to $+15$ dB to give increased flexibility to the system architecture level.

The class-D amplifier achieves a power efficiency of 84% with 650-mW output power into 8 Ω at 1% total harmonic distortion (THD) with 3.6-V supply. The THD is 0.02%, and the signal-to-noise ratio (SNR) is 96.5 dB. The class-AB amplifier, on the other hand, achieves 675-mW output power into 8 Ω at 5% THD. The power supply rejection of this amplifier is 84 dB.

This paper is organized as follows. Section II explains the top-level architecture. In Section III, the implementation of the class-AB amplifier is explained, showing the improvements compared to [1]. The class-D amplifier, including modulation scheme and the implemented architecture, is presented in Section IV. The common output driver stage with predriver and biasing network of the class-D amplifier is shown in Section V, and finally, measurement results are given in Section VI.

II. Top-Level Architecture

Fig. 1 shows the block diagram of the multimedia and baseband processor. In addition to multimedia and connectivity features, the IC incorporates an audio subcircuit that is used to drive audio devices such as the headset, a receiver speaker for phone conversation, and two hands-free speakers for melodies and ringtones.

Several analog microphone inputs and an input for digital microphones are available. For a detailed description of the whole mixed-signal audio section, the reader can refer to [7]. This paper focuses on a dual-mode class-AB and D driver for hands-free applications.

Class-AB amplifiers are the most widely used power amplifiers [8]. To improve linearity, a class-AB amplifier provides for a quiescent current in both output devices around the crossover point between push and pull currents. This needs to be accurately controlled; too much current can be worse than no current. As a rule of thumb, the quiescent current is 0.1% of the maximum peak output current. The efficiency for class-AB amplifiers is max. 70%, but with common audio signals, it generally does not rise above 50%.

The primary advantage of a class-D amplifier is certainly its excellent efficiency. However, a few disadvantages should not be hidden. Switching amplifiers generate a considerable amount of high-frequency components [electromagnetic interference (EMI)] which might have an impact on other circuits in the application. Depending on the modulation scheme, an external filter may be required to reconstruct the signal. More often, coils are added to the signal or supply path in order to suppress high-frequency noise. Furthermore, a filterless class-D amplifier cannot be used as two individual single-ended amplifiers. A class-AB amplifier, on the other hand, offers the following advantages over its counterpart: more flexible system applications (e.g., single-ended stereo configuration), less EMI, and possibly better PSRR. In short, these advantages and disadvantages of the two driver stages were the main motivation to offer the customer a choice to use either a class-AB or a class-D solution.

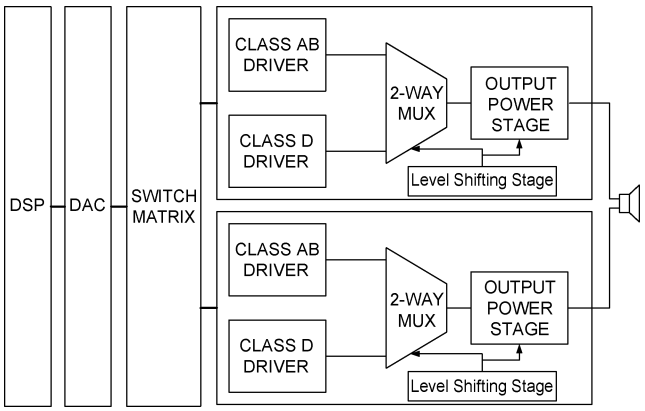

Fig. 2. From DSP to loudspeaker: Block diagram of class-AB/D audio amplifier including DSP, DAC, switch matrix, AB and D driver, and output power stage.

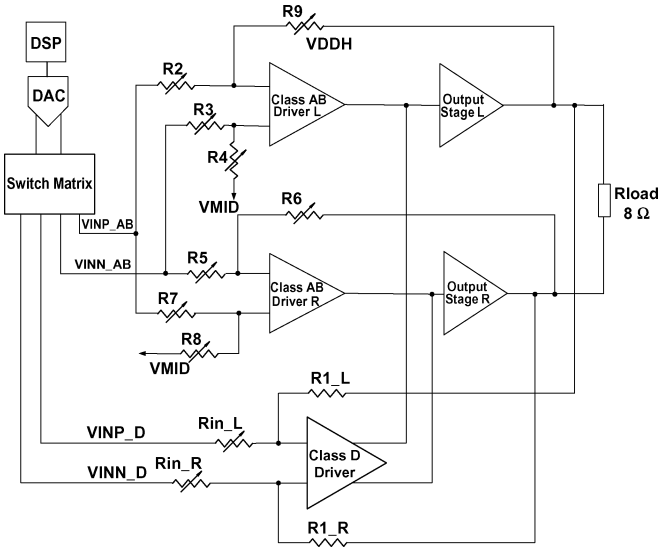

Fig. 3. Programmable class-AB/D amplifier (from DSP to load).

Despite the use of a 65-nm CMOS process, the hands-free amplifiers are directly hooked up to the battery voltage for delivering high power. The interface between the DSP audio stream and the amplifier is established through a digital-to-analog converter (DAC) and a switch matrix which redirects either the class-AB or the class-D audio path to the shared audio power stage (see Fig. 2). More specifically, Fig. 3 shows a block diagram of the class-AB/D amplifier. Inputs $VINN\_AB/VINN\_D$ and $VINP\_AB/VINP\_D$ are driven by a differential DAC. The DAC is supplied by a locally regulated analog voltage ($VDDA$) which is nominally 2.65 V, regulated from the battery voltage ($VDDH$, nominally 3.6 V). $VMID$ is an on-chip filtered reference set to half of $VDDH$. Gains can be set between -30 and 15 dB by the ratios of the resistors, and a bridge-tied load (BTL) setup is chosen for high output swing and good common-mode rejection. By using the quasi-instrumentation amplifier topology, level shifting for the common-mode voltage from a bandgap reference for the DAC to $VMID$ for maximum output swing is achieved. In addition to the input coming from the DAC, alternative external inputs can be connected, for example, an FM radio IC.

On any transistor, the VGS and VGD must be kept below a maximum of 3.6 V, and VDS must be kept below a maximum of 2.5 V. This part is explained in detail in Section V.

III. Class-AB Amplifier

The design of the class-AB amplifier closely follows [1]. However, as this circuit is now combined with the class-D amplifier, the output stage, bias circuitry, and common reference buffers could be simplified in order to save area as well as reduce power consumption. The following paragraph only addresses the differences compared to [1].

A. Architecture and Circuit Description

A proper biasing circuit for the OTA and the output driver is needed in order to keep all device voltages below the limits imposed by the process (both shown in Fig. 5). In the first step, the supply voltage $VDDH$ is divided by two, to arrive at $VMID$, a voltage which stays below the allowed 2.5–2.75 V—if this voltage is generated from a battery voltage of 4.8 V, see Fig. 4(a). This is accomplished by using MP1 and MP2, and two long p-channel devices acting as a voltage divider.

This voltage is also available in power-down mode of the circuit and tracks $VDDH$. All necessary bias voltages and currents are generated in the bias block, as shown in Fig. 4. During power-down mode, only the bias current $I_{\rm ref}$ is switched off; the divider keeps $VMID$ running. During power-up, the divider tracks the supply, keeping all voltage terminals in a safe operation region. Overdrive on each of the transistors is prevented due to the presence of $VDDH$ and $VMID$ in the so-called "always-on" domain.

The purpose of the bias circuit in Fig. 4(a) is to keep all MOS transistors in the OTA and in the output driver within the process limits.

The biasing circuit is centralized such that all currents and bias voltages originate from the same source; to this end, it is placed in the middle of the layout. This improves the offset between the two channels of the BTL amplifier. For simplicity, only two P-side and two N-side current generators are shown in Fig. 4(a): The core of the bias circuit is an accurate 4-μA current generator, tied to a bandgap voltage in the $VDDA$ domain. This bias block provides bias currents as well as bias voltages to the OTA (shown in Fig. 5) and the output driver including the error amplifiers. Fig. 4(b) shows how the P-side and the N-side generators are protected during power-down state: level shifting between ground, $VMID$, and the $VDDH$ domain drives the gate of the switches into the OFF state, thus copying the $VMID$ voltage on to the output node. Finally, Fig. 4(c) shows a simplified block diagram of the $VMID$ generator: dividing $VDDH$ though an active resistor chain results in $VMID = VDDH/2$ and $VRLO = VDDH/4$. These voltages are then further buffered as shown in Fig. 4(d).

The predriver is shown in Fig. 5 as well as in Fig. 11. The description of the functionality mainly follows [1]. However, bias and power-down currents have been optimized. More detailed, P33 and N33 have been added as switches, and LS_P (LS_N is inverted) is a level-shifted output ranging from 0 to $VDDH$. In power-down state, these switches open the path to avoid any current flowing into or shorting the $VMID$ buffer's output. In

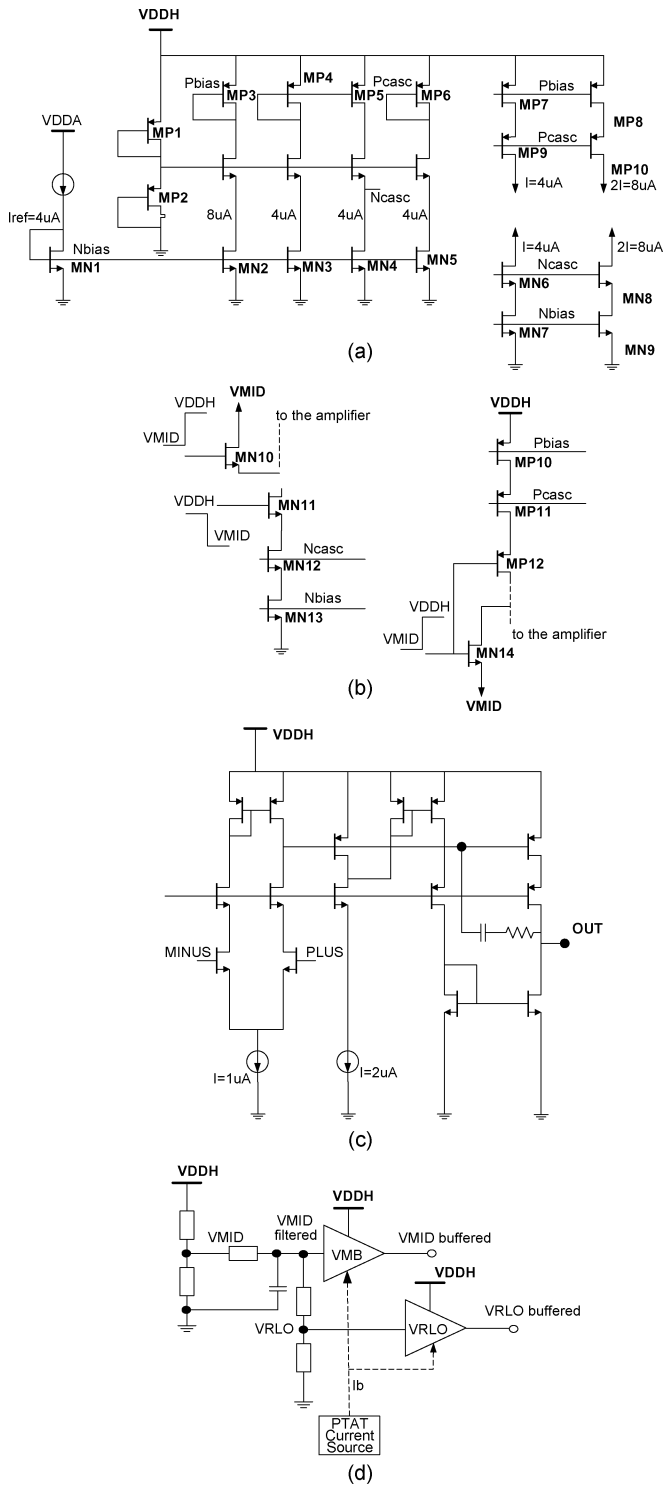

Fig. 4. Bias network of class-AB driver. (a) Voltage and current biasing. (b) Details of overvoltage protection in power-down mode. (c) $VMID$ generator. (d) Buffering of $VMID$ generator.

power-on state, these switches are fully conducting and hence do not have an impact on the functionality. It is important to note that the current generators shown are critical with regard to PSRR. Hence, a high output impedance and good matching between the N and P sides are prerequisites.

This circuit has been simulated in all the corner conditions, ensuring proper stability in all cases, with at least 60 ° phase margin.

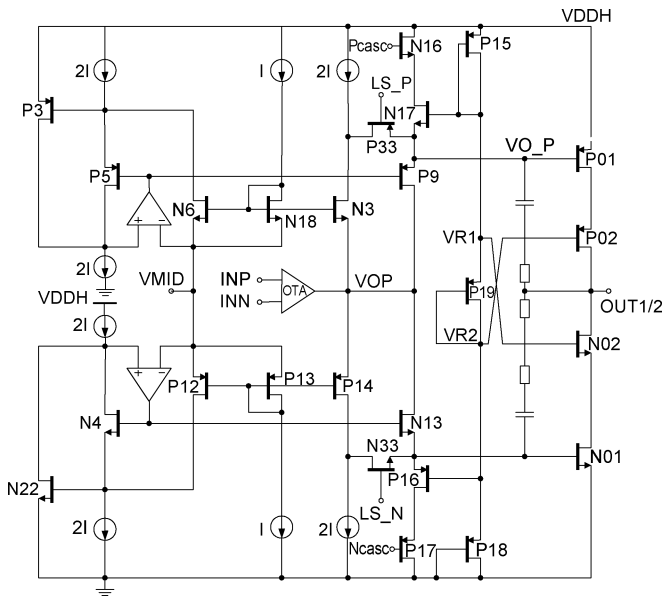

Fig. 5. Class-AB driver.

B. Overcurrent Protection

In an output stage, high currents can occur due to incorrect load impedance or a short-circuit connection to one of the supply voltages. The resulting overcurrent can damage the circuit, even if the current spike has a very short duration.

The class-AB stage presented in this paper has a protection circuit that prevents overcurrents by increasing the impedance of the output driver stage as soon as a high current is detected. In principle, a protection circuit should be able to derive the dissipated power within the output stage.

The simplest way to measure the current in an output stage is by adding a small resistor in series with the stage and sensing the voltage drop across it. This is widely employed in mains-powered stereo amplifiers. For these devices, an additional voltage drop can be tolerated because the supply voltage is large and the power loss is relatively small. For a battery-powered device (such as a cellular telephone), the output power in hands-free mode is considerably affected if a series resistor of approximately 0.5 Ω were to be added.

To avoid this resistor, a replica of the power output stage can be used. A replica is a copy of the output driver, with the same gate voltage and the same source and drain voltage as the output driver itself, but a scaled down size to save current and area.

The block diagram for this implementation is shown in Fig. 6. The power stage consisting of CMOS transistors N1 and P1 drives the output. The replica devices are contained in N2 and P2. The gate drive of the replicas is the same as for the output drivers. Current delivered by the output is also visible in the replicas, at a much lower current level due to scaling by a factor of 100. In series with the replicas, resistors R2n and R2p have been inserted to measure the current. The slightly lower drain voltage of the replica does not affect the current matching, since the output drivers N1 and P1 will also have a small drain resistance due to the wiring (R1n and R1p). A good value for R2n and R2p is 10 Ω, which is a factor of 100 larger than the wiring resistance indicated by R1n and R1p (0.1 Ω). The output driver N1/P1 layout consists of a large number of fingers. Matching

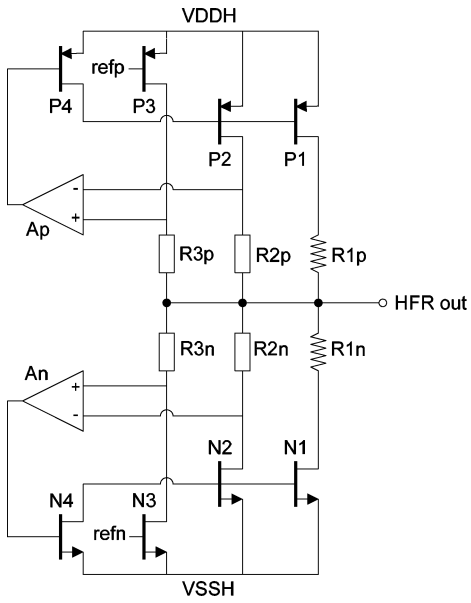

Fig. 6. Class-AB overcurrent protection simplified diagram.

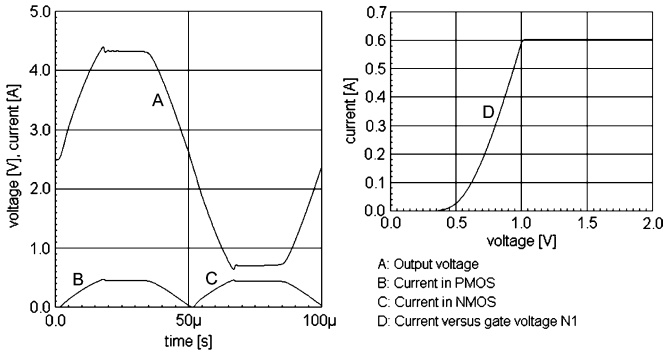

Fig. 7. Overcurrent protection circuit. (a) Output voltage, clipped by protection. (b) Current in PMOS output driver. (c) Current in NMOS output driver. (d) Clipping action on rising gate voltage (NMOS).

of the replicas N2/P2 is optimized by using an adjacent and integer number of fingers. The devices N3 and P3 are reference currents, which, in conjunction with R3n and R3p, form a reference voltage that is used to set the trigger level for the output current sensor. The value of the reference can be programmed to obtain maximum current levels of 300 mA up to 750 mA in steps of 75 mA. The difference between the voltage drop on the resistors in the replica path and the drop on the reference resistors is amplified by the differential amplifier stages An and Ap and drives N4 and P4. The gate drive of N1 and P1 is reduced to limit the maximum current in the output stage to the preset value. Due to limiting, the gain of the control loop is small enough to prevent oscillation.

In practice, we use a slightly more elaborate circuit for the drivers N1 and P1. These driver stages are cascoded to sustain a larger supply voltage than each individual transistor can handle. If we would replicate the driver and its cascode, a large voltage swing from the output would be present at the input of the amplifiers An and Ap. This causes a problem for the design of the amplifiers, since their gate inputs might be destroyed by the large signal swing from the output node. The solution to this problem is to put the sensing resistors R2n and R2p between the driver transistor and the cascode. In this way, the swing at the input of An (Ap) is limited to half of the output swing. Simulations of this topology show that the matching of the sensing resistor voltage and the reference voltage is even better than without the cascodes.

Fig. 7 shows the function of the protection circuit if the load resistance is too small (or zero). Curve A shows the sine-wave voltage (frequency 10 kHz) at the output which is effectively clipped by the protection circuit. Curves B and C are the currents (PMOS side inverted) through the driver devices (max. 450 mA). The slight overshoot is caused by the speed of the amplifier path within the protection circuit. Curve D shows the current clipping in N1 for a rising gate voltage; for this example, the clipping level is 600 mA.

The same principle of overcurrent protection can also be used for a class-D amplifier. The biggest difference between the class-D and the class-AB amplifier is that the switching frequency of class-D produces numerous current peaks that need to be individually checked for overcurrent. In addition, the bandwidth of the control loop has to react within one μs. This is a factor of 50 faster than for a 20-kHz audio signal. As an example, the current needed for the control loop will rise from 20 μA to 1 mA. This is the reason to also consider other systems: averaging control loops and fast temperature sensors in the output stage (for additional solutions, see [9]).

IV. Class-D Amplifier

A good introduction into various class-D modulation schemes is given in [7] and the references therein. In the following sections, we will explain the modulation system used and show the implemented architecture [10]. Measured results will be shown in Section VI.

A. Modulation Principle

Switched mode amplifiers rely on pulse modulation schemes, in which the signals are represented by the properties of the pulse (width, density, position, or others) rather than the amplitude. The most frequently used methods of encoding a signal into a pulse train are PWM and pulse density modulation, as they both achieve high efficiency and have a relatively low implementation complexity when compared to other methods like pulse position modulation. The PWM has been chosen for the class-D amplifier because it features the lowest possible switching frequency and therefore minimizes the switching losses in the output stage [7].

Naturally sampled PWM has been chosen because it is an analog process which fits to the analog nature of the input signal provided by the DAC (see Figs. 3 and 8). It is implemented by comparing the input signal with a fixed carrier. The switching time of the width-modulated pulses is determined by the instantaneous intersection of the carrier and the input signal. The carrier waveform is usually a triangle or a sawtooth signal. Natural sampling (at least theoretically) has the advantage over other sampling methods (e.g., uniform sampling in digital PWM modulator) in that it does not generate harmonics of the audio signal

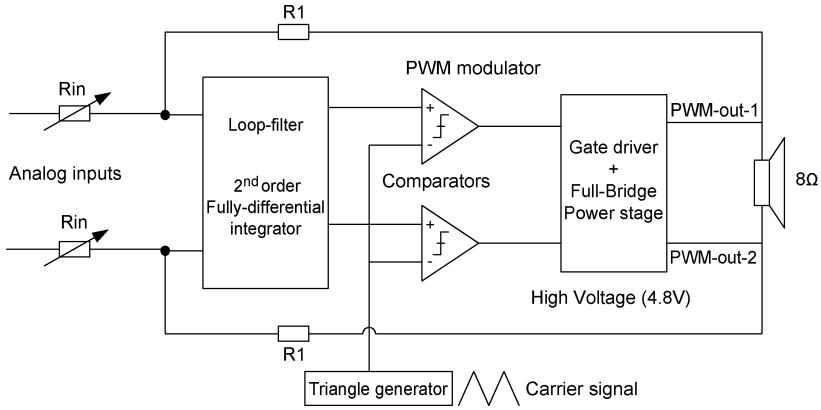

Fig. 8. Simplified block diagram of closed-loop filterless class-D amplifier. (For simplicity reasons, the left/right channel labels are omitted.)

and can thus be regarded as a perfect sampling process—as far as distortion is concerned.

The aforementioned PWM signals are binary signals ("AD" modulation [11]) whose frequency spectrum contains the audio signal, the carrier frequency with its harmonics, as well as intermodulation products around the harmonics. AD modulation requires an external filter to reconstruct the signal. The requirements for filtering can be improved with a ternary PWM signal ("BD" or filterless modulation [11]). PWM signals with three levels are obtained with a differential output stage driven by two binary PWM signals; the difference between the two phase-shifted signals therefore generates a ternary signal. With BD modulation only, the intermodulation products around the carrier and its harmonics are present and thus relax the requirements on the output filter. The intrinsic inductance of the speaker can be used as a low-pass filter.

The BD modulation also has a nice property in that no current flows through the load when a zero input voltage is applied, which occurs since both outputs of the differential stage (full-bridge) are in phase, with a 50% duty cycle. BD modulation is therefore well suited to filter-free applications. The implementation shall have a differential input as well as a differential output; single-ended operation is not possible.

B. Architecture and Circuit Description

The class-D amplifier is a differential input–output topology with analog inputs based on the natural sampling PWM process. Analog inputs are required because of the intended applications. The block diagram of the closed-loop class-D amplifier is shown in Fig. 8. It consists of four blocks: the analog PWM modulator, the second-order loop filter with the resistive feedback, the output stage, and the inductive speaker. Systemwise, the speaker must be treated as an integral part of the amplifier because it is acting as a demodulation filter. In literature, this is referred to as filterless configuration. The fully differential configuration does not need decoupling capacitors. Another advantage is good inherent common-mode rejection ratio (CMRR) and PSRR performance. The differential input requires a differential audio source (preamplifier or DAC) to create both the audio signal and its inverse. The output stage is directly connected to the high supply voltage of the battery ($VDDH$). The modulator and the loop filter are supplied by the regulated supply voltage of the baseband and audio chip $VDDA$ (2.65 V).

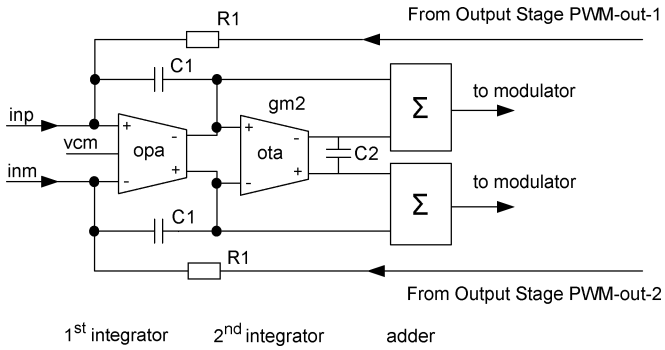

Fig. 9. Second-order loop filter.

C. Analog PWM Modulator and Carrier Generator

The integrated audio signals from the summed integrator outputs (refer to Fig. 8) are compared with a carrier signal by two comparators. The two binary PWM signals from the comparators are level shifted from 2.65 V to the battery level before being applied to the outputs. The resulting differential signal across the full-bridge is the three-level natural sampled PWM signal. The carrier signal is a free-running triangle waveform. Its frequency tracks the integrator time constants. The latter feature allows one to design the time constants with a smaller tolerance margin, therefore saving silicon area.

D. Control Loop

The closed-loop system uses negative feedback to improve the performance of the class-D amplifier. It offers excellent distortion, good supply rejection, and relaxed requirements for the active components of the control loop. The aforementioned performance can theoretically be improved by using a higher order loop filter. However, any order above two increases the complexity of the design, while practical performance is not significantly better. Therefore, a second-order loop filter was chosen [6].

The class-D amplifier uses a differential feedback loop with the loop filter embodying a second-order integrator as shown in Fig. 9 [10]. The inputs inp and inn can be driven by currents but can also contain a resistive ladder gain control, as done in the current design. The two feedback resistors, together with the first-stage feedback capacitors, form the first integrator which filters the high-frequency components generated by the

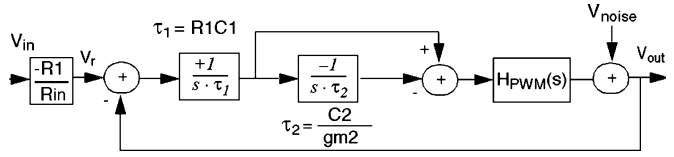

Fig. 10. Second-order feedback loop including the noise source.

BD modulation. A second pole is given by the OTA integrator. The poles and the zero of the open-loop response are defined by the time constant of the two differential integrators.

The second-order closed-loop amplifier can be approximated by linear models if the gain of the PWM modulator and output stage is assumed to be constant. The linear model of the closed-loop amplifier is shown in Fig. 10, where $H_{\rm PWM}(s)$ is the transfer function of the modulator and switching output stage.

Furthermore, $H_{\rm PWM}(s) = G_{\rm PWM}e^{-s\tau_d}$, where $G_{\rm PWM}$ and τ_d are the equivalent small signal gain of the modulator and output stage and the associated time delay, respectively. The phase shift due to τ_d is negligible for carrier frequencies up to 500 kHz and can be omitted.

The system transfer function STF is the closed-loop voltage gain $A_{\rm VCL}(s)$ of the amplifier

$$\begin{aligned} STF &= A_{\rm VCL}(s) \\ &= \left.\frac{V_{\rm out}}{V_{\rm in}}\right|_{V_{\rm noise}=0} \\ &= -\frac{R_1}{R_{\rm in}} \cdot \frac{s\cdot\tau_2+1}{s^2\cdot\frac{\tau_1\tau_2}{G_{\rm PWM}}+s\cdot\tau_2+1}. \end{aligned} \tag{1}$$

In the audio frequency range, the closed-loop voltage gain is determined by the ratio of the feedback and the input resistor $(R_1/R_{\rm in})$ as in a linear amplifier. The noise transfer function (NTF) is the transfer function between the output $V_{\rm out}(s)$ and the noise in the output stage $V_{\rm noise}$

$$NTF = \left.\frac{V_{\rm out}}{V_{\rm noise}}\right|_{V_{\rm in}=0} = \frac{s^2\cdot\frac{\tau_1\tau_2}{G_{\rm PWM}}}{s^2\cdot\frac{\tau_1\tau_2}{G_{\rm PWM}}+s\cdot\tau_2+1}. \tag{2}$$

The NTF transfer function has a second-order high-pass characteristic. Low-frequency noise is rejected, resulting in a good PSRR at these frequencies. AC simulation with 217-Hz noise showed 100-dB rejection. However, the measured PSRR is 72 dB, due to nonideal matching characteristics.

The gain block of the first integrator is a differential-input–differential-output amplifier. Since the bidirectional type of class-D modulation causes a large common-mode signal in the feedback to the first integrator input, the CMRR of the stage must be large. The time constant is derived in conjunction with the carrier frequency. This enables one to choose the carrier for optimum efficiency. The time-constant tolerance does not impair the loop stability, since the time-constant components track the components that determine the carrier frequency.

The second integrator is a differential C/gm type. The time constant consists of a 1/gm output resistance with an antiparallel gate-capacitor load. The advantages of this configuration are small current consumption (11 μA), inherent stability (compensated by the load), and high output resistance to get a low capacitance area.

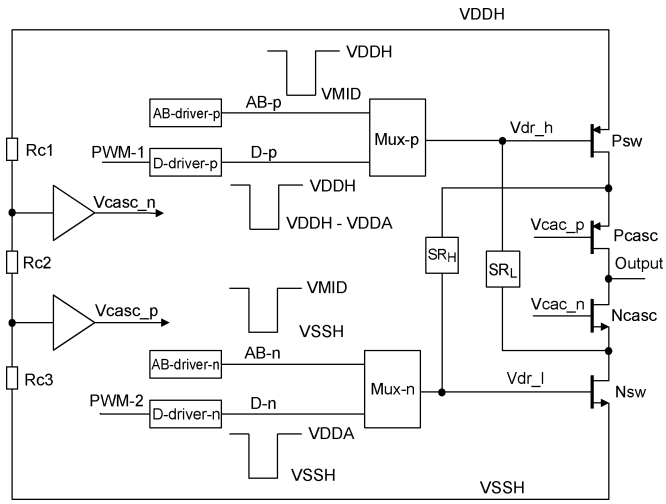

Fig. 11. Block schematic of the half-bridge output stage.

The zero in the STF in (1) is synthesized with two feedforward adders which are directly implemented in the comparator input circuit, without the use of a dedicated adder stage.

E. Stability Considerations

Both large- and small-signal stabilities have been considered. For large-signal stability, the slew rate of the first integrator must be lower than the slope of the triangle clock generator [6]. The time constant (τ_1) is dimensioned for worst case conditions, i.e., maximum supply voltage, minimum oscillator frequency, smallest capacitor values, and smallest resistor values. Small-signal stability, on the other hand, must be maintained by proper choice of the second integrator's time constant (τ_2), i.e., $\tau_2 > \tau_1$.

V. Output Stage

The output stage uses a full-bridge topology to achieve a high output power. Fig. 11 shows the block diagram of a half-bridge consisting of the power MOS transistors Nsw, Ncasc, Pcasc, and Psw, the multiplexers connecting the class-AB or class-D signals to the transistors Nsw and Psw, the drivers of the cascode transistors Ncasc and Pcasc as well as level shifters, and control circuitry. The output stage also includes the circuits SR_H and SR_L to control the output slope in class-D operation. Sharing the same output stage helps to reduce the silicon area, particularly for high-power applications, where the output transistors occupy a significant part of the amplifier's area.

A. Power MOS Transistor Topology

The output stage is designed to operate up to a supply voltage of 4.8 V $(VDDH)$ and has therefore to withstand high voltages at its terminals. The technology used dictates that the source-to-drain voltage of the thick-oxide devices shall not exceed 2.5 V $(VDDA)$ and that the gate-to-source and gate-to-drain voltages shall be lower than 3.6 V. Note that these maximum ratings for hot carrier injection (HCI) are based on foundry lifetime data

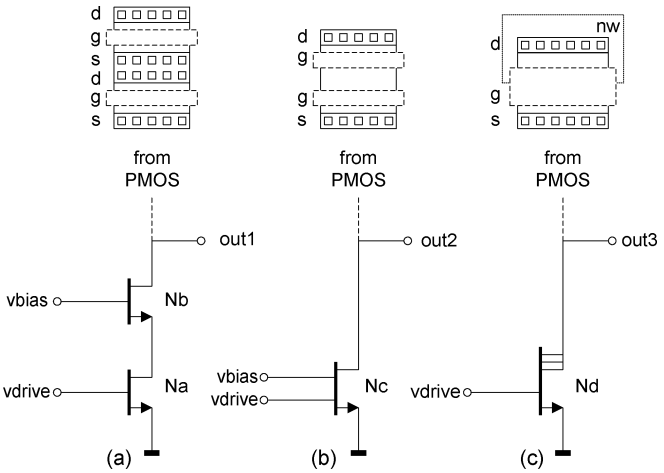

Fig. 12. Comparison of transistor topologies. (a) Normal cascode stage, (b) dual-gate transistor, and (c) drift transistor. The equivalent layouts are shown above the schematics (gates have a striped outline).

for minimum length transistors. For example, a maximum dc operating voltage of 2.5 V translates to a transistor lifetime of ten years, and similarly, a dc voltage of 2.75 V translates also to a lifetime of ten years but with a transistor on/off ratio of 2%. Correspondingly, longer transistors can sustain higher voltage levels. Therefore, circuit techniques such as stacked (cascoded) designs or technology options are used to prevent high voltage stress on any of the terminals. An assessment of these solutions will now be discussed.

In Fig. 12, three different implementations are shown: (a) a regular cascode design, (b) a stage with a dual-gate transistor, and (c) a drift transistor. The regular cascode (a) consists of the driver Na, with its source attached to the ground supply line, and a cascode stage Nb, stacked on top of the driver. The gate of Na is driven by the voltage vdrive, and the gate of the cascode Nb is driven by the voltage vbias. Such a structure can handle nearly twice the regular voltage. The dual-gate transistor (b) also has a driver and a cascode, but the drain of the driver and the source of the cascode are omitted. The bias voltage vbias must in both cases be about one threshold voltage higher than the drain–source voltage of the driver transistor.

Advantages $(+)$ and drawbacks $(-)$ of the cascode and the dual gate stages with respect to drift transistors are the following.

$(+)$ Designed with standard transistors, with well-known simulation models and layout structures.

$(+)$ Has an area advantage over drift transistors, as will be shown below.

$(-)$ Requires a bias voltage for the cascode transistor. The bias value and the driving strength must be chosen carefully.

$(-)$ Can only be used slightly below the limit of twice the nominal voltage of each of the transistors, because of the tolerances in bias and threshold voltages.

The cascode has one advantage over the dual gate:

$(+)$The point between the gates is available if the function or the bias of the circuit requires it.

A drift transistor is shown in Fig. 12(c). The large voltage capability is achieved by extending the drain under the gate and doping it with an N-Well-type high-resistive layer. This way, the electric field is distributed evenly over the active region, reducing the effective voltage over the channel. The maximum drain–source voltage (VDS) can be up to 8 V for the same technology as that used for the stacked transistor case. However, the voltage capability of the gate against the source is not increased (3.6 V).

TABLE I
CURRENT CAPABILITY COMPARISON. NMOS GATE WIDTH OF 5.0 mm AND PMOS GATE WIDTH OF 14 mm

VGS [V]	NMOS drift type [mA]	NMOS cascode type [mA]	PMOS drift type [mA]	PMOS cascode type [mA]
1.8	227	369	219	370
2.5	298	490	267	497

Advantages $(+)$ and drawbacks $(-)$ of the extended-drain transistor are the following.

$(+)$ Features large VDS voltages.

$(+)$ Needs no biasing as opposed to a cascode transistor.

$(-)$ Requires larger area than the cascode or the dual-gate transistor (see below).

$(-)$ Missing models and precise layout hints for newest technologies.

Comparing the voltage capability of the three topologies shows that the drift transistor has an advantage over the other two solutions. However, the cascode, as well as the dual-gate types, also fulfills the required maximum voltage for this application. Therefore, we will base the comparison rather on the chip area of the three topologies. First, a value for the current capability per area unit shall be determined. To this end, a simulation setup was made with each of the three topologies of Fig. 12. All transistors have the minimum length, which is 0.5 μm for the drift type and 0.28 μm each for the normal types. The NMOS width for the simulation is 5 mm; the PMOS width is 14 mm. The drain voltage was set to 0.3 V which is the worst case for an audio output driver, which is just at the edge of where clipping of the audio signal can occur. The gate voltage was set to either 1.8 or 2.5 V, which corresponds to half the value of two power supply values, i.e., 3.6 and 5.0 V, respectively. The temperature and technology case were worst case (125 °C, slow corner). The current capability of a dual-gate transistor is the same as for the normal cascoded stage, which leads to the four columns in Table I. The cascoded topology has a considerably larger current capability (factor of 1.6) than the drift transistor for the same transistor width. This means that a larger width has to be chosen for the drift transistor output.

The area of the output transistors can now be compared. The transistor size shall be adjusted to get 520-mA current capability at 1.8-V gate drive for each topology. This leads to larger transistor widths than used for the current capability simulation. The area is calculated for an NMOS transistor of 7 mm and a PMOS transistor with a width of 20 mm. Furthermore, transistor fingers with two "flipped" devices aside will be used. The upper part of Fig. 12 shows an example of each transistor's layout.

For a whole BTL stage (differential push–pull), the areas from Table II have been added. The drift type is more than 1.8

TABLE II
AREA CALCULATION WITH TRANSISTOR WIDTH ADAPTED TO 520 mA

type / total	topology	width [mm]	length [μm]	area [mm^2]
NMOS	cascode type A	7	1.96	0.0137
	dual gate type B	7	1.51	0.0106
	drift type C	11.5	1.45	0.0167
PMOS	cascode type A	20	1.9	0.0392
	dual gate type B	20	1.51	0.0302
	drift type C	33.2	1.45	0.0481
TOTAL	cascode type A	2 N & 2 P		0.1058
	dual gate type B			0.0816
	drift type C			0.1966

times larger than the cascoded type and 2.4 times larger than the dual-gate type. As a result, the design was implemented with the cascode transistor design and has potential to be further reduced in area using the dual-gate approach.

To conclude, the design was implemented with the cascode implementation (not dual-gate) because it offers the flexibility to use the middle node for circuit optimization. Additionally, it offers the flexibility to apply circuits for slope control (as in Fig. 11, SR_H and SR_L).

B. Multiplexer

Multiplexers are used to connect either the class-AB or the class-D amplifier to the common output stage, as shown in Fig. 11, for both the PMOS and NMOS transistors. The class-AB voltage swing is approximately $VDDH/2$ (also referred to as $VMID$), whereas the voltage swing of the class-D amplifier is $VDDA$ (2.5 V). The power PMOS is driven between $VDDH$ and $VDDH-VMID$ in class-AB mode and between $VDDH$ (4.8 V) and $VDDH-VDDA$ in class-D mode. The power NMOS transistor is driven between $VMID$ and $VSSH$ in class-AB mode and between $VDDA$ and $VSSH$ in class-D mode.

C. Driver for Cascoded Output Stage

Next, we discuss how to properly bias the cascode transistor, i.e., Pcasc and Ncasc in Fig. 11, in functional as well as in power-down mode, taking into account overvoltage stress, the maximum gate-oxide breakdown voltage, and HCI.

The cascode transistors Ncasc and Pcasc are used to decouple the drain terminals of the switching transistors Nsw and Psw from the power stage output and thus limit the maximum drain–source, gate–drain, and gate–source voltages. The bias voltages $V_{\text{casc\_}n}$ and $V_{\text{casc\_}p}$ are chosen such that the cascode transistors do not experience gate-oxide or HCI stress. Both class-AB and class-D modes are driven using the same biasing network.

For given values of maximum and minimum output voltages, $V_{\text{out\_max}}$ and $V_{\text{out\_min}}$, respectively, a first upper and lower bound for the bias level of $V_{\text{casc\_}n}$ can be calculated given the maximum gate-oxide breakdown voltage $V_{g\_\max}$ of the cascode transistor Ncasc [see (3) and (4)]. Note that $V_{g\_\max}$ equally stands for the maximum gate–source as well as for the drain–gate voltage

$$V_{\text{casn\_}n} \le V_{g\_\max} + V_{\text{out\_min}} \tag{3}$$
$$V_{\text{casc\_}n} \ge V_{\text{out\_max}} - V_{g\_\max}. \tag{4}$$

Taking the $V_{g\_\max}$ voltage of transistor Nsw into account, an additional boundary condition can be derived for $V_{\text{casc\_}n}$ if the output is at its maximum value, i.e., $V_{\text{out\_max}}$

$$V_{\text{casc\_}n} \le V_{\text{dr\_}l} + V_{g\_\max} + V_{\text{th\_Ncasc}}. \tag{5}$$

Similar equations can be derived for $V_{\text{casc\_}p}$

$$V_{\text{casc\_}p} \le V_{\text{out\_min}} + V_{g\_\max} \tag{6}$$
$$V_{\text{casc\_}p} \ge V_{\text{out\_max}} - V_{g\_\max}. \tag{7}$$

Taking the $V_{g\_\max}$ voltage of transistor Psw into account, an additional boundary condition can be derived for $V_{\text{casc\_}p}$ if the output is at its minimum value, i.e., $V_{\text{out\_min}}$

$$V_{\text{cacs\_}p} \ge V_{\text{dr\_}h} - V_{g\_\max} + V_{\text{th\_Pcasc}}. \tag{8}$$

For the bidirectional output terminal powered at $VDDH$, $V_{\text{out\_max}}$ and $V_{\text{out\_min}}$ are $VDDH + V_F$ and $-V_F$, respectively, where V_F is the forward bias voltage of the parasitic MOS diodes of the output transistors. Typically, V_F is in the order of 0.7 V for these transistors. Taking a margin of 0.1 V into account and substituting for V_F, $V_{\text{out\_max}}$ and $V_{\text{out\_min}}$ can be calculated as 5.6 and -0.8 V, respectively.

Not only bias but also HCI conditions must be maintained during normal operation as well as in power-down mode. To prevent the drain–source voltages from exceeding the HCI limits, the high supply voltage $VDDH$ is distributed equally over the cascode and the switch transistors. The resulting drain–source voltage drop $V_{\text{DS}} = 0.5\,VDDH$ must be below the voltage where transistors experience HCI. It follows that $V_{\text{DS}} < V_{\text{HCI}}$.

$$V_{\text{casc\_}n} = 0.5\,VDDH + V_{\text{th\_Ncasc}} \tag{9}$$
$$V_{\text{cacs\_}p} = VDDH - 0.5\,VDDH + V_{\text{th\_Pcasc}} \tag{10}$$

Worst case condition for gate-oxide and HCI stress occurs when $V_{\text{dr\_}l} = VSSH$, $V_{\text{dr\_}h} = VDDH$, and $V_{\text{th}} = V_{\text{th\_min}}$. Substituting values for $V_{\text{out\_max}}$, $V_{\text{out\_min}}$, V_{th}, $V_{\text{dr\_}l}$, and $V_{\text{dr\_}h}$ in the above, bounds for the conditions for $V_{\text{casc\_}n}$ and $V_{\text{casc\_}p}$ can be rewritten as follows.

For output voltages at maximum level, i.e., $V_{\text{out\_max}}$

$$2.0\text{ V} \le V_{\text{casc\_}n} \le 3.9\text{ V (Gate oxide)} \tag{11}$$
$$V_{\text{casc\_}n} = 2.7\text{ V (HCI)} \tag{12}$$
$$V_{\text{casc\_}p} \ge 2.0\text{ V (Gate oxide)}. \tag{13}$$

For output voltages at minimum level, i.e., $V_{\text{out\_min}}$

$$V_{\text{casc\_}n} \le 2.8\text{ V (Gate oxide)} \tag{14}$$
$$0.9\text{ V} \le V_{\text{casc\_}p} \le 2.8\text{ V (Gate oxide)} \tag{15}$$
$$V_{\text{casc\_}p} = 2.1\text{ V (HCI)}. \tag{16}$$

As can be seen, only $V_{\text{casc\_}n} = 2.7$ V and $V_{\text{casc\_}p} = 2.1$ V satisfy all of the aforementioned conditions.

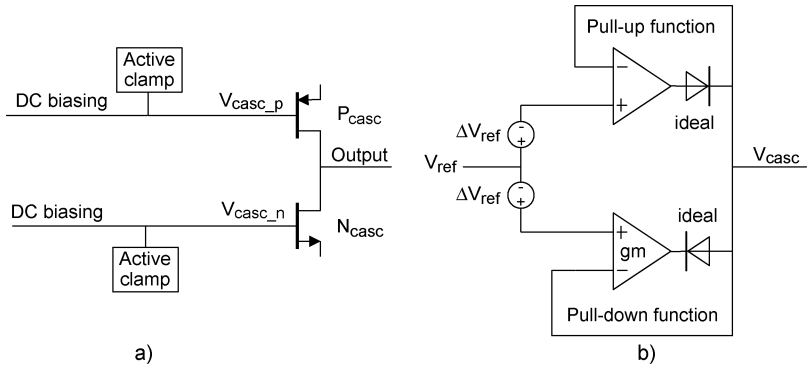

Fig. 13. Active clamp circuit. (a) Interconnection with gate terminal. (b) Block diagram showing $V_{\rm casc}$ generation.

Cross-circuitries SR_H and SR_L shown in Fig. 11 control the voltage across the cascoded transistors when the output goes from high to low, and vice versa, and limits the rise and fall times. Controlled switching helps to reduce large current spikes at the gates of the cascode transistors during the charge and discharge phases and thus relax the design of the bias voltage as well as improve EMI conditions. Additionally, the voltage spikes induced into the power and ground tracks of the half-bridge are also significantly reduced. These spikes are mainly due to fast switching currents through the inductance of the bonding wires and the package and get even worse because of the reverse-recovery current in the parasitic diodes of the output MOS transistors.

D. Active Clamp

The dc bias voltages for the gate terminals $V_{\rm casc\_n}$ and $V_{\rm casc\_p}$ are generated with a voltage divider connected between the power rails $VDDH$ and $VSSH$ (Fig. 11). As will be shown next, low output impedance and, thus, high drive capability are achieved by using active clamps.

In class-D operation, fast and almost rail-to-rail output signals result in fast voltage changes at the power transistor's gate. This, in turn, results in large voltage spikes at the gates of both cascode transistors. The active clamps aim at maintaining the bias voltage of the cascode transistors within a certain tolerance even when fast switching transients occur. These clamps feature low output impedance and facilitate the sourcing or sinking of full peak currents within a short period of time. A block diagram of the clamp is shown in Fig. 13(a).

It is worth noting that the voltage of the active clamp is superimposed on top of the voltage level of the bias generator. A current spike that is sufficient to raise the gate voltage above a threshold $\Delta V_{\rm ref}$ causes the active clamp to turn on and deliver the required charging current. The active clamp can be thought of as two single-ended unity-gain transconductance amplifiers in a unity-gain configuration [see Fig. 13(b)]. The pull-down function is only active when $V_{\rm casc} > V_{\rm ref} + \Delta V_{\rm ref}$, while the pull-up function is only active when $V_{\rm casc} < V_{\rm ref} - \Delta V_{\rm ref}$. Hence, both functions can never be active at the same time.

The reference voltage $V_{\rm ref}$ and the auxiliary bias voltages $V_{\rm det\_high}$ and $V_{\rm det\_low}$ are generated in a similar way to the bias voltages $V_{\rm casc\_n}$ and $V_{\rm casc\_p}$. Fig. 14 shows the implementation of the p-type active clamp with the pull-up and pull-down transconductance circuits. $V_{\rm det\_high}$ and $V_{\rm det\_low}$ are used to set

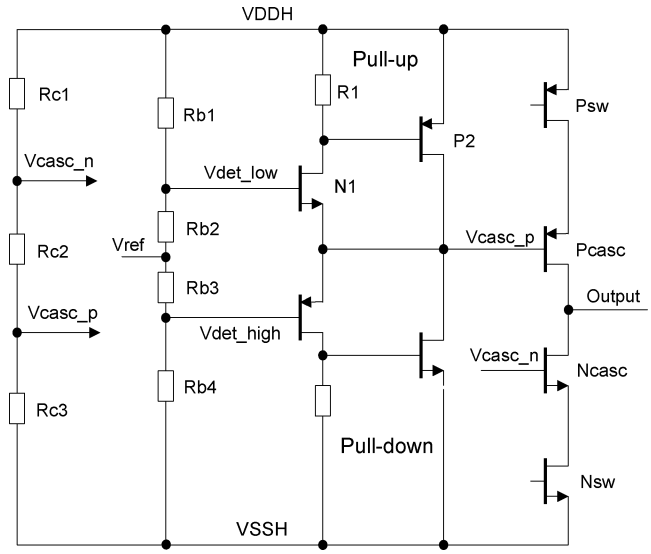

Fig. 14. Active clamp of the cascode transistor Pcasc.

the tolerance band $\Delta V_{\rm ref}$. The spike detection circuit for pull-up operation consists of resistor R_1, transistor N1, with its bias voltage $V_{\rm det\_low}$ that command the clamp transistor P2. The total transconductance is the g_m of the clamp transistor P2 times the voltage gain of the common gate input stage.

E. Driver and Level Shifter for the Switch Transistors

The previous sections have described protection circuits for the output stages. In addition, the driver circuits need protection against overvoltage as will be shown in this section.

The switches Nsw and Psw in Fig. 11 are driven by the binary PWM signals of the modulator output via two drivers. Their swing is from $VSSA$ to $VDDA$. The gate of Nsw is driven directly from a standard CMOS buffer supplied by $VDDA$; the gate of Psw is driven by a level-shifting buffer, operating between $VDDH$ and $VDDH-VDDA$. The level-shifting buffer is connected to $VDDH$ and consists of a low-current static level shifter driving a dynamic buffer stage as shown in Fig. 15. This two-stage structure reduces both static and dynamic power consumption and the overall propagation delay. The latter is required to avoid cross-currents in the output stage.

The static level shifter in Fig. 16 creates a level-shifted input for the PMOS driver. Again, cascode techniques are used to prevent the NMOS transistors from exceeding process limits. The voltage swing across P1and P2 is fixed by design and equal

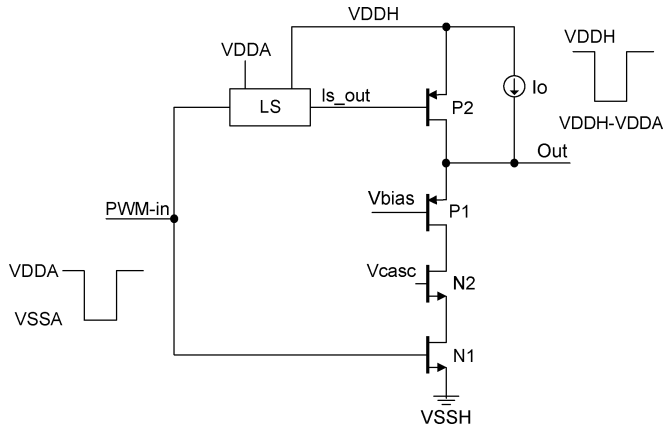

Fig. 15. Cascoded PMOS driver.

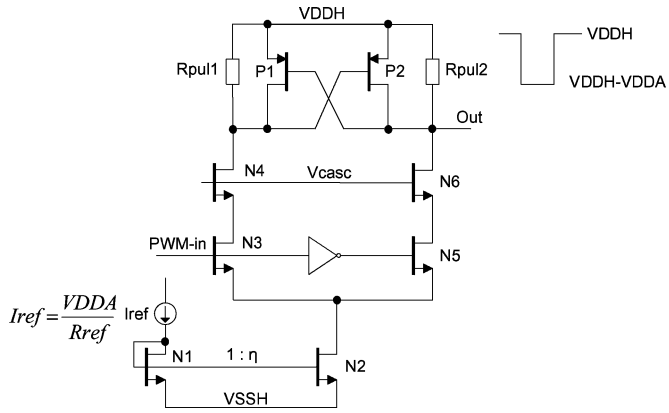

Fig. 16. Cascoded static level shifter for the PMOS driver.

to $VDDA$. P1and P2 also form a positive feedback loop to increase the overall speed. In power-down mode, when $I_{\rm ref}$ is disabled, both gate and drain terminals are tied to $VDDH$ through the pull-up resistors, Rpul1 and Rpul2, respectively. The driver (Fig. 15) consists of the pull-up transistors P2, the source-follower transistor P1, the cascode transistor N2, and the switch transistor N1. P2 and N1 are controlled by the level-shifter output signals ls_out and the modulator output signal PWM-in, respectively. The maximum voltage swing of $VDDH-V_{\rm out}$, which is roughly equal to $VDDA$, is limited to 2.75 V by the bias voltage $V_{\rm bias}$. The bias voltage of P1 is one $V_{{\rm th}\_p}$ lower than $V_{\rm out}$ and equals $VDDH-VDDA-V_{{\rm th}\_p}$, resulting in a maximum gate–source voltage of 3.2 V which is still below the process limit of 3.6 V. The current source I_o is necessary to maintain the output of $VDDH-VDDA$. The cascode transistor N2 protects the NMOS transistors from overstress.

F. Break-Before-Make Slope Control Circuit and EMI

The performance of class-D audio amplifiers (efficiency, THD, and EMI) is limited by the quality of the switching output stage that usually includes a break-before-make arrangement to prevent cross-conduction between the supply lines. The resulting delay or dead time during each output transition causes distortion and EMI radiation in the switching power stage. Best performance in terms of efficiency and linearity can be achieved if the dead time is reduced to a minimum value. A technique called zero dead time [6], [13] reduces the dead time to zero while avoiding any cross-current conduction. Zero dead time is based on the proper dimensioning of the drivers for the power transistors as well as accurate matching of the NMOS and PMOS on–off timing.

This technique has been adapted for the cascoded power stage by connecting two cross-coupled capacitors between the gate-driver outputs and the drain of the power switch transistors Msw and Psw (Fig. 11). The capacitors SR_H and SR_L match the gate–drain capacitance $C_{\rm gd}$ of the transistors Msw and Psw to obtain linear output change and low distortion. The slew rate can be adjusted by changing the size of the driver transistors. There is a tradeoff between fast slew rates to minimize the switching losses and slow slew rates to reduce EMI radiations, current spikes at the gate of the cascode power transistors, and reverse-recovery current in the parasitic diodes of the output MOS transistors.

G. ESD Protection

In addition to observing the reliability rules for nominal operation, the power stage output also has to meet certain requirement rules during an electrostatic discharge (ESD) event. During an ESD, currents up to several amperes flow during about 100 ns. An ESD protection circuit is connected to the power stage output to absorb the energy in the ESD pulse and to limit the overvoltage during an ESD discharge. Nevertheless, special care must be taken in the layout of the output stage to prevent parasitic bipolar NPNs to trigger during an ESD event.

Characterization of the devices under ESD conditions has shown that the drain of an NMOS transistor goes into avalanche breakdown (which will trigger the related parasitic NPN) to the bulk at a voltage $V_{t1} \approx 4.9\,{\rm V}$ in this technology, which is within the nominal operating range. In that case, the NMOS transistor would be destroyed through current filamentation, unless it is laid out according to special ESD design rules provided by the IC foundry. Application of the usual ESD design rules would, however, lead to an unacceptably large size of the output transistor and reduce the efficiency of the power stage.

Therefore, a different approach was chosen, involving V_{t1} engineering [14]. By proper layout of the cascoded output NMOS transistors, it is possible to increase the combined V_{t1}. By putting each NMOS in a separate active region and applying a minimum distance between the two regions of 4.5 μm, it is possible to increase the combined V_{t1} beyond the design target of 6.5 V.

Note that similar ESD measures are not required for the PMOS transistor, since PMOS transistors do not snap back, and furthermore, the avalanche breakdown voltage for a single PMOS is about 7.0 V, which is above the design target.

VI. Verification and Measurement Results

Before presenting the measurement results, a few words shall be given on how layout and verification was performed.

A. Postlayout Verification

In order to achieve maximum power and best performance, effort has been spent to optimize layout symmetry as an iterative

TABLE III
MEASUREMENT RESULTS ($T_A = 25\ ^\circ\mathrm{C}$ AND $R_{\mathrm{Load}} = 8\ \Omega$)

Parameter / conditions	Class-AB	Class-D
Supply voltage (VDDH)	2.7 V to 4.8 V	
Idle current (VDDH 3.6 V)	2.2 mA	1.9 mA
Power Down current (VDDH 3.6 V)	2 μA	3 μA
Output power (VDDH 3.6 V)	675 mW 5% THD	650 mW 1% THD
Output power (VDDH 4.8 V, THD: 1%)	1200 mW 5% THD	1100 mW 1% THD
Power Efficiency (VDDH 3.0 V to 4.8 V)	70 %	84 %
THD (VDDH 2.8 V - 3.6 V) (VDDH 4.8 V)	0.15 % [b]	0.02 % [a] 0.03 % [a]
PSRR (217Hz, VDDH 3.0 V to 4.8 V)	85 dB	72 dB
SNR (A-weighted, 12 dB gain)	97 dB	96.5 dB
Chip area (one Full-Bridge amplifier)	0.44 mm^2	

a. 1 KHz, Output power: 1 mW to $0.5\mathrm{x}\mathrm{Pout}$ at THD 1 %.
b. THD @ 1 kHz, -3 dB below max power.

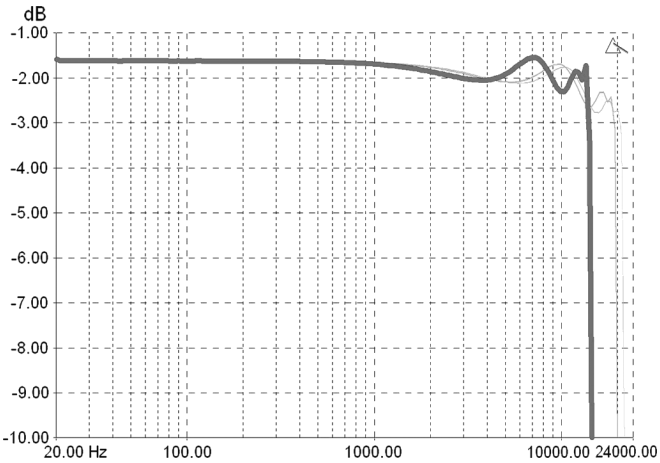

Fig. 17. Measured transfer function of audio codec for sampling rates of 32 kHz (bold), 44.1 kHz, and 48 kHz (highest cutoff frequency).

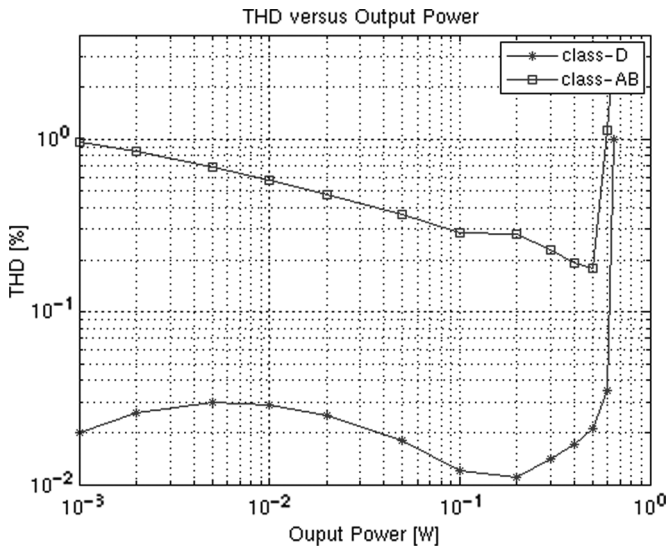

Fig. 18. Measured THD versus output power for class-AB/D amplifier.

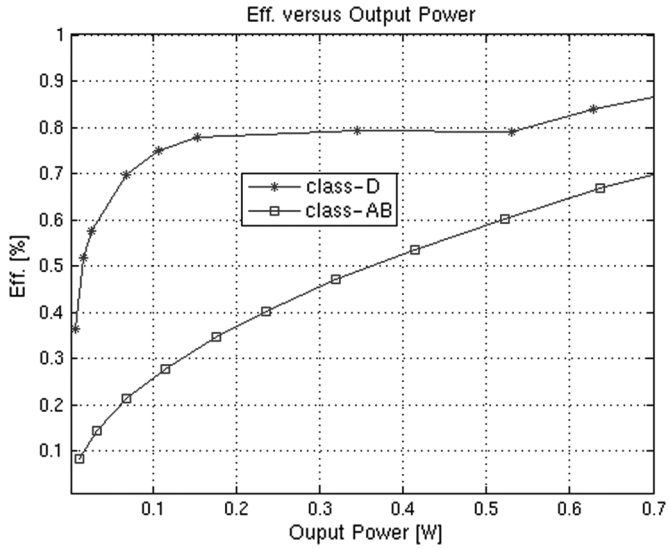

Fig. 19. Measured efficiency versus output power for class-AB/D amplifier.

process in conjunction with back-annotated simulations prior to delivery to the foundry. Generally, this allows a proper verification of the output stage and, hence, a reduction in the number of tape-outs until production ramp-up. This is even more important in submicrometer technologies where mask costs are high and, in this particular case, where analog functionality occupies only a minor part of the overall silicon area.

Maximum efficiency and, thus, maximum output power can only be achieved if the parasitic routing resistance from supplies ($VDDH$ and $VSSH$) to the sources of the PMOS and NMOS output transistors can be minimized. Similarly, the parasitic routing to the load, as well as the interconnect resistance between the drivers, must also be minimized. Additionally, supply routing shall be star connected at pad level. Taking advantage of the very low ohmic copper interconnect and by stacking as many layers as possible on top of each other helped in further reducing the parasitic resistance. Furthermore, PSRR and offset can significantly be improved if perfect layout symmetry between the two halves of the BTL stages is applied. Note that, with this respect, also the feedback points must be carefully placed and even parasitic resistances must be balanced. After several improvement steps, layout extractions showed the following parasitic resistances: 20 $\mathrm{m}\Omega$ from supply $VDDH$ down to the source of the PMOS output stage; 10 $\mathrm{m}\Omega$ from the source of the NMOS ground connection of the output stage; and 10 $\mathrm{m}\Omega$ from the common output connection of the output stage to the output pad connection (load connection). Hence, an overall on-chip resistance of 0.65 Ω could be achieved, corresponding to 8% of the load. By using the earlier described values, we see a very good correlation between layout simulations and measurement results.

Furthermore, transient and, more specifically, reliability simulations require proper modeling of bonding wires as well as the package parasitics. In general, all parasitic elements are combined in a lumped Pi-network with a capacitor C on both ends and an inductor L in series with a resistor R in between. Foundry models for bonding wires and package yield $L = 1$ nH, $R_1 = 100\ \mathrm{m}\Omega$, $C = 30$ fF and $L = 70$ pH, $R_1 = 1\ \mathrm{m}\Omega$, $C = 200$ fF, respectively. Bonding has been implemented with three wires in

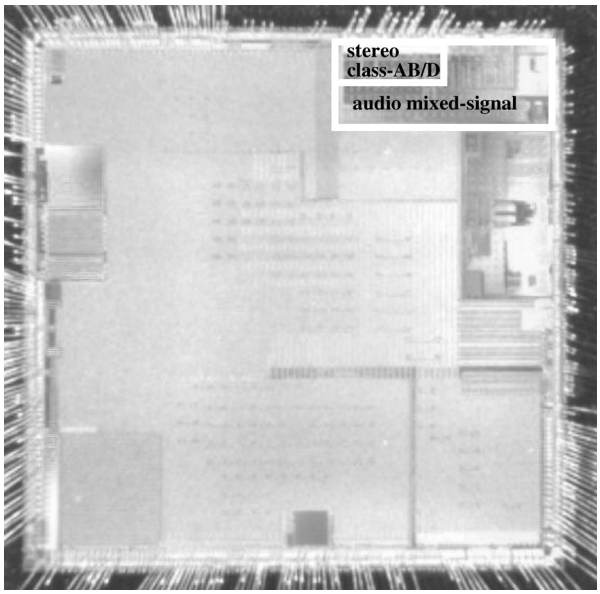

Fig. 20. Chip micrograph of full baseband including mixed-signal IPs. The audio IP is shown in the upper right corner.

parallel for each of the supply connections and with five wires in parallel for the outputs and the ground connection.

Above model and parameters have been extensively used in simulations and the overall optimization of the driver stage. Correlation between simulation and measurements is found to be better than 5%.

B. Measurement Results

Table III summarizes the measurement results of the class-AB/D amplifier. Both amplifiers show power drive capabilities of more than 650 mW. This is remarkable since power levels above 500 mW have, up to now, been shown in stand-alone components only and not in fully integrated solutions [2]. Additionally, both amplifiers have a similar SNR and can thus clearly handle MP3 or CD quality. Fig. 17 shows the transfer characteristic of the audio codec for various sampling rates (32, 44.1, and 48 kHz) with a passband ripple of less than 0.5 dB and a stop-band attenuation of better than 70 dB (latter part not shown). Note that the attenuation seen at higher frequencies is mostly due to the high-frequency performance of the FIRDAC (see also [12]). The class-D amplifier achieves excellent THD across the full supply and power range, whereas the class-AB amplifier shows higher output distortion at lower power levels mostly because of higher crossover distortion in the output stage (see also Fig. 18). As expected, efficiency is much better in the class-D case, particularly for low-to-medium power levels (see Fig. 19). The class-AB amplifier, on the other hand, shows a good PSRR level of 84 dB which could further be improved by adding a simple gain stage. Note that all reported values are valid across process and temperature. In a stereo application, both amplifiers together only occupy 0.88 mm^2. For a chip micrograph, see Fig. 20.

VII. Conclusion

A combined class-AB/D power amplifier for audio applications integrated in a feature-rich baseband processor in a 65-nm standard technology has been presented. The output stage can be directly connected to the battery without causing high-voltage gate-oxide or drain-to-source overstress. The class-D amplifier is capable of providing 100-mW output power with 75% efficiency, whereas the class-AB amplifier shows 25% efficiency for the same power level. The switch-mode amplifier can drive more than 700 mW with 84% efficiency, whereas the AB one features 70% efficiency—again for the same power level. The performance of the class-D driver in terms of distortion, output power, efficiency, and silicon area is superior compared to competing designs integrated in SoC [2]. The audio class-AB/D amplifier described here is integrated in a stereo configuration and occupies less than 0.44 mm^2 per channel. The driver coexists with critical mixed-signal blocks like microphones or baseband receive inputs.

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References

[1] R. Becker and W. Groeneweg, "An Audio amplifier providing up to 1 Watt in standard digital 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1648–1653, Jul. 2006.

[2] P. Bonnaud, M. Hammes, A. Hanke, J. Kissing, R. Koch, E. Labarre, and C. Schwoerer, "A fully integrated SoC for GSM/GPRS in 0.13 $\mu\mathrm{m}$ CMOS," in *Proc. ISSCC*, 2006, pp. 1942–1951.

[3] B. Forejt, V. Rentala, G. Burra, and J. Arteaga, "A 250 mW class D design with direct battery hookup in a 90-nm process," in *Proc. IEEE CICC*, 2004, pp. 169–172.

[4] B. Forejt, V. Rentala, J. D. Arteaga, and G. Burra, "A 700 + -mW class D design with direct battery hookup in a 90-nm process," *IEEE J. Solid-States Circuits*, vol. 40, no. 9, pp. 1880–1887, Sep. 2005.

[5] P. Muggler, W. Chen, C. Jones, P. Dagli, and N. Yazdi, "A filter free class D audio amplifier with 86% power efficiency," in *Proc. ISCAS*, 2004, pp. 1036–1038.

[6] M. Berkhout, "An integrated 200 W class-D audio amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1198–1206, Jul. 2003.

[7] M. Berkhout, L. Breems, and E. van Tuijl, "Audio at low and high power," in *Proc. ESSCIRC*, 2008, pp. 40–49.

[8] D. Self, *Audio Power Amplifier Design HandBook*. Amsterdam, The Netherlands: Elsevier, 2006, p. 130.

[9] M. Berkhout, "Integrated over-current protection system for class-D audio power amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2237–2245, Nov. 2005.

[10] W. Groeneweg, "Analog signal processing for a class D audio amplifier in 65-nm CMOS technology," in *Proc. ESSCIRC*, Sep. 2008, pp. 322–325.

[11] K. Nielsen, "A review and comparison of pulse width modulation (PWM) methods for analog and digital input switching power amplifiers," in *Proc. 102nd AES Conv.*, Munich, Germany, Mar. 1997.

[12] B. Baggini, P. Basedau, R. Becker, P. Bode, R. Burdenski, F. Esfahani, W. Groeneweg, M. Helfenstein, A. Lampe, R. Ryter, and R. Stephan, "Baseband and audio mixed-signal front-end IC for GSM/EDGE applications," *IEEE J. Solid-State Circuits*, vol. 6, no. 6, pp. 1364–1379, Jun. 2006.

[13] M. Berkhout, "A class-D output stage with zero dead time," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2003, vol. 1, pp. 193–196.

[14] J. W. Miller, M. G. Khazhinsky, and J. C. Weldon, "Engineering the cascoded NMOS output buffer for maximum Vt1," in *Proc. EOS/ESD Symp.*, 2000, pp. 308–317.

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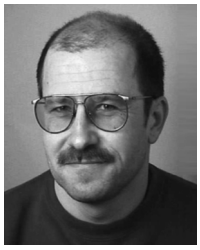

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