Logic Functions, Devices, and Circuits Based on Parametric Nonlinear Processes

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***Abstract*—Second-harmonic generation and parametric down-conversion processes have been studied as the basis of all-optical logic gates. All possibilities that are obtainable with both the low and high conversion efficiencies of such processes have been analyzed here.** XOR **and** AND **gates are also experimentally proven by using 1-ps pulses at 800 nm within a β-BaB_2O_4 crystal, reaching conversion efficiencies of as high as 80%. Based on these phenomena, complex algebraic operations are proposed for performing several different logic functionalities particularly concerning network switching and arithmetic calculation.**

***Index Terms*—Logic gates, nonlinear optics, optical computing, second harmonic generation.**

I. Introduction

ALL-OPTICAL signal processing such as demultiplexing, wavelength conversion, regeneration, and digital algebra will play a critical role in the development of ultrafast photonic network architectures. The capability of this technology to handle a single ultrahigh speed data channel exclusively in the optical domain without optoelectrical conversions can significantly improve the performance of photonic systems in terms of flexibility, scalability, wavelength management simplification, optical components minimization, and cost reduction. To realize all-optical signal-processing functions, several solutions have been proposed. Among all, the first realizations were based on spatial soliton interactions, dragging, and fusion in Kerr nonlinear waveguides [1]–[4] and, later on, in saturable nonlinear media, e.g., photorefractive media [5], [6]. Even if such configurations are very promising, they present some experimental limitations that are mainly given by the very high intensity that is necessary for Kerr nonlinear media and by the relatively slow dielectric relaxation in photorefractive media. Three main lines were then followed to overcome such limitations: all-optical switching 1) using spatial light modulators [7], 2) using semiconductor optical amplifiers [8]–[11], and 3) using parametric nonlinear second-order processes [12]. All-optical processing via parametric generation was first analyzed by Andreoni *et al.* [13]–[15] mainly during holographic second-harmonic generation [16], [17] (SHG). Following such works, we have analyzed all the possibilities of realizing all-optical processing and logic gates using SHG and parametric downconversion (PDC) processes. With respect to the previously described technologies, parametric techniques require much lower energy than that necessary for Kerr solitons, are much faster than photorefractive nonlinearity techniques, and, last but not the least, can be easily parallelized, making them a very promising technology. Its main limitation is given by the conversion efficiency, which can be at 100% only in the quantum regime, where the conversion is now digital. In such case, the proposed technology becomes very attractive and applicable.

Among logic units, the XOR and AND gates are fundamental in accomplishing a binary algebra that is useful for various functionalities, such as packet switching, binary addition and counting, data encoding, and, more generally, optical processing. Following this line, all-optical XOR and AND gates have been implemented, exploiting second-order nonlinear processes, such as SHG and optical PDC. In this configuration, two binary strips, which were encoded by transverse amplitude modulation, are processed directly bit by bit in an intrinsic parallel way.

II. Boolean Logics by Parametric Processes

In the early 1960s, SHG [18] and PDC [19] were well studied, both in their experimental [20] and theoretical aspects. Recently, the discovery of photonics structures [21] and new optical materials [22] has yielded the increase in the efficiencies of nonlinear processes and stimulated technical research.

We examine here how these processes may be used to create a completely optical Boolean logic.

The behaviors of parametric interactions such as SHG and PDC, both in the low- and high-efficiency regimes, are summarized by the notation shown in Fig. 1.

The considered SHG process is actually a type-II SHG, where two input beams at fundamental frequency (FF) ω (distinguishable by their orthogonal polarizations), interacting through the second-order susceptibility of a nonlinear crystal, generate a third channel at the second-harmonic frequency 2ω. The presence or absence of a further arrow in the symbols in Fig. 1 describes whether the process happens under high- or low-efficiency conditions. In particular, under these efficiency conditions, the two input beams can be present or absent at the output, with important consequences, as will be explained later on.

In the same way, the considered type-II PDC process consists of the parametric interaction, which is inverse to the SHG, where the two input beams are one at FF ω and one at its second-harmonic frequency 2ω, and generate a third channel at FF ω (distinct from the input one by the polarization). Again, according to the low- or high-efficiency conditions, the second-harmonic

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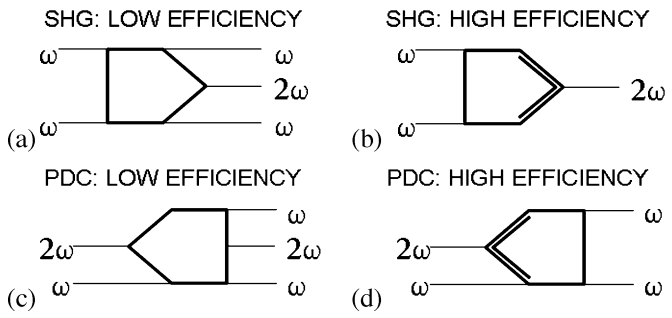

Fig. 1. Notation: (a) SHG signal has low-efficiency conditions. (b) SHG signals in high-efficiency conditions, where the dotted line means that, if they are present, both the inputs and the outputs are depleted. (c) PDC signals in low-efficiency conditions. (d) PDC signals in low-efficiency conditions with a dotted line for the second harmonic, which is possibly depleted. The arrows pertain to the double frequency 2ω with respect to fundamentals ω. For SHG and PDC, the reverse symbols are used.

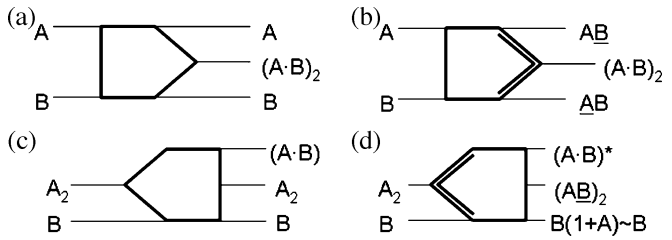

Fig. 2. Logic functionalities: (a) In low-efficiency conditions, the SHG and and function of the inputs are present at the output on the second harmonic. (b) In high-efficiency conditions, the SHG at the output of FF are present as $A \cdot \underline{B}$ on the first polarization and $B \cdot \underline{A}$ on the orthogonal one and on the SHG and and function of the inputs. (c) In low-efficiency-condition PDC, the FF not present at the input gives the and function of the inputs at the output. (d) In high-efficiency-condition PDC, the FF not present at the input gives the complex conjugate of the function of the inputs at the output.

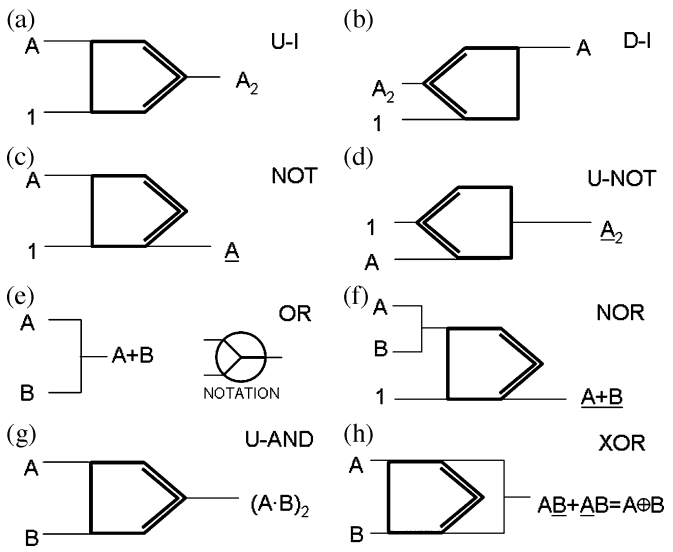

Fig. 3. Single-operation logic gates: (a) U-I transforms a signal in FF to the second harmonic. (b) D-I changes a signal that is present on the SHG to FF. (c) NOT function at the FF. (d) U-NOT gives the negation of the input. (e) OR function obtained by overlapping two inputs. (f) NOR gives the negation of OR at the FF. (g) U-AND function gives the and of the inputs on SHG. (h) XOR function obtained by combining the two output polarizations on the FF of an SHG in high-efficiency conditions.

beam can be present or absent at the output. As a notation, this process is sketched by a pentagon with the apex toward the left-hand side, and again, the efficiency conditions are represented by the presence or absence of a further arrow in the symbol.

Fig. 2 shows that the SHG and PDC processes can perform logic functionalities. Consider the optical information as binary, i.e., as 0 (no light) or 1 (light above some given intensity threshold) bits injected at the input of any of these parametric processes. Each channel, according to the specific parametric process and efficiency, experiments on a different logical functionality. Thus, low-efficiency SHG [Fig. 2(a)] realizes an AND functionality, because the 2ω beam is generated only in the presence of both ω beams at the input. Consequently, from the logical point of view, the output state (carried by the second-harmonic beam) will be 1 only if both input states are 1 and will be 0 otherwise. By notation, we write this as $(\mathrm{A} \cdot \mathrm{B})_2$, with the subscript stressing the fact that the output of the AND functionality is carried by the 2ω frequency. We find better expectations at the high-efficiency regime [Fig. 2(b)]. In this case, the $(\mathrm{A} \cdot \mathrm{B})_2$ is again realized, but now, the input beams A and B will not propagate unaffectedly to the output as before; they will carry the signature of the generation process, i.e., their intensity will decrease. In this case, the output channel corresponding to the input A state is now in the logic state $\mathrm{A}\underline{\mathrm{B}}$ [which means $\mathrm{A} \cdot \mathrm{NOT(B)}$]. Indeed, when A is 0 at the input, the corresponding output will be 0 independently on B; for $\mathrm{A} = 1$, it will be transferred unperturbed only if B is equal to 0 and will be forced to be in the 0 state by the parametric conversion otherwise. The output of the B channel, by symmetry, will be in the logic state $\underline{\mathrm{AB}}$.

The logic processing of PDC is even more interesting. The low conversion efficiency will always produce the AND functionality in the generated ω beam because of the simultaneous interaction of the two channels A_2 (at the 2ω frequency) and B [at the ω frequency, Fig. 2(c)]. In the high-efficiency regime, this AND channel will still be present (please note that the AND output channel will now be complex conjugate); the 2ω channel with the A_2 state at the input will carry the $(\mathrm{A}\underline{\mathrm{B}})_2$ at the output, whereas the B channel, at the ω frequency, will carry the $\mathrm{B}(1 + \mathrm{A})$ state at the output, which, in binary code, corresponds to the unperturbed B state.

Using the described functionalities, eight main logic gates can be identified using the high-efficiency regimes, as shown in Fig. 3. Using the SHG process, the UP-IDENTITY (U-I) gate is obtained, assigning always the 1 level to the B channel (supply of device power). In such case, the A state at FF ω will be transferred to the A_2 (at 2ω) channel [Fig. 3(a)]. Analogously, the DOWN-IDENTITY (D-I) gate [Fig. 3(b)] is realized by the PDC process, again assigning the 1 level to the B channel at the ω frequency (analogous to a supply of device power). The A state will be transferred from the 2ω to the ω channel. Going back to the experimental configuration of the U-I gate, the power supply channel will experience the NOT gate [Fig. 3(c)], i.e., it will be in the $\underline{\mathrm{A}}$ state, because it will remain in the 1 state if A is 0 and will be depleted by the parametric interaction being in the 0 state otherwise. In the same way [Fig. 3(d)], using the

TABLE I
AND AND XOR LOGIC GATE TRUTH TABLE

A	B	A·B	A⊕B
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

PDC process, an UP- NOT (U-NOT) gate, whose NOT information will be transferred to the 2ω frequency from the ω channel if the supply of power is now ensured in the 2ω frequency, can be realized.

In addition, one more logic gate that however does not require any nonlinear process can be found: the OR gate [Fig. 3(e)], for which the output state is 0 only if both inputs are 0 and is 1 otherwise. From the described point of view, this is easily realized by just overlapping the two input states. In such a way, there will always be light at the output (1 level) if light is present at the input; otherwise, the output is 0. Obviously, the NOR gate can be obtained by cascading the OR gate with one NOT gate [Fig. 3(f)].

Injecting two different A and B states at the input of an SHG process, the realization of the UP-AND (U-AND) and XOR gates is straightforward, as described in Fig. 3(g) and (h), respectively. The U-AND gate was already described before; the XOR gate is then realized by overlapping the two output channels $A\underline{B}$ and $\underline{A}B$. In fact, it is well known that $A \oplus B = A\underline{B} + \underline{A}B$. Thus, the SHG process in the high-efficiency regime will ensure the simultaneous availability of XOR and AND logic functions, which are the basis of every algebraic operation. In Table I, the XOR and AND truth tables are reported together, and it is clearly highlighted how the simultaneous combination of these gates yields the binary sum of the numbers encoded in A and B (here, single bits).

III. EXPERIMENTAL DEMONSTRATION OF XOR AND LOGIC GATES

The experimental demonstration of the SHG process in realizing logic functionality was performed using the setup shown in Fig. 4. The laser system consisted of an amplified Ti-sapphire laser providing 2-ps-long pulses at $\lambda = 800$ nm, with an energy of about 500 μJ at a repetition rate of 1 kHz. A 50% beam splitter divided the beam into two arms that represent the input logical states. A half-wave plate (WP) rotated the polarization of one beam to obtain, after the polarizing beam splitter, two cross-polarized beams. The crystal was a β-BaB_2O_4 (BBO) used in a type-II phase-matched SHG of 800 nm.

The mask used in this experiment was a 3-mm-wide pinhole, whose image was reproduced on the BBO crystal by a 1-m-long lens. The BBO crystal was, in fact, put 10 cm farther than the focal plane of the lens, and the mask was put at a distance of 11 m from that lens. In this way, the pinhole image was reduced, on the crystal, down to 10% in dimension. The output logical state, which is encoded on the FF, was separated from the second-harmonic signal (carrying the AND information) by a dichroic mirror and visualized by a charge-coupled-device camera. Following the XOR gate's truth table (Table I), we demonstrate the possibility of implementing such logical gate using type-II SHG in high-efficiency conditions. In these conditions, as previously discussed, while the interacting beams are generating the second harmonic, they will get depleted, yielding 0 at the output.

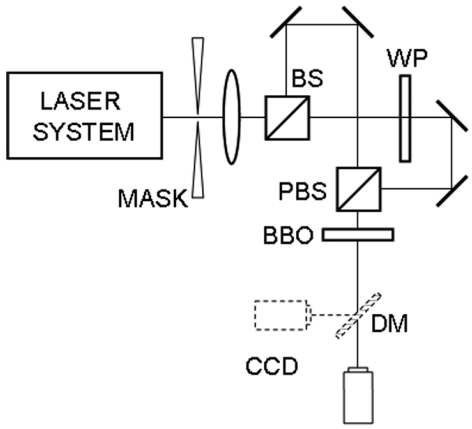

Fig. 4. Experimental setup: The beam exits from the laser and passes through the mask, which is a pinhole whose image is formed on the crystal by a long-focal lens. Then, the beam is divided into two arms by a beam splitter: The refracted beam passes through a $\lambda/2$ WP, thus rotating its polarization, whereas the reflected beam passes through a delay line and is combined with the other by a polarizing beam splitter. The two beams interact with the crystal, and then, the FF is separated from the SHG by a dichroic mirror and could be seen in the camera.

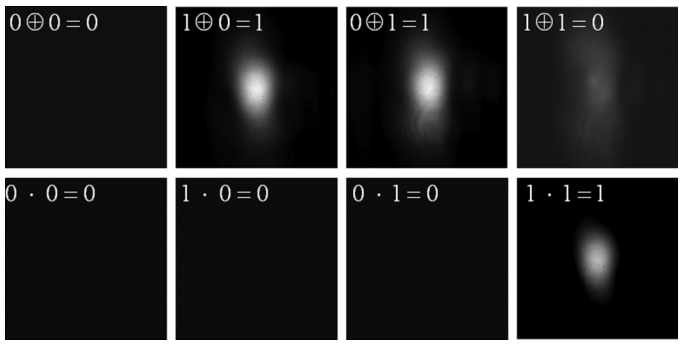

Fig 5. Images of the output states for the logic XOR and AND gates. The $1 \oplus 1$ state is not perfectly 0, as expected, but has a residual power in the range of 15%–20%. Perfectly 0 states can be achieved using flat-top beams or in single-photon regimes.

The depletion of the ω beams because of the 2ω generation was as high as 80%, which is almost the highest conversion efficiency that can be reached with Gaussian beams (particularly considering the extreme thinness of the nonlinear crystal). The XOR operation was demonstrated to be monitoring the residual A and B channels at the FF, as shown in Fig. 5(a). When both input states were 0, the trivial solution 0 was obtained. When one of the input beams was in the 1 state, the output was exactly that 1 state; when both input channels were in the 1 state, the 2ω beam was generated by depleting the FFs. Due to the incomplete conversion, a residual light was present in the channel. The AND operation was instead demonstrated to be monitoring the second-harmonic channel that is generated only when both fundamental channels are simultaneously present [Fig. 5(b)].

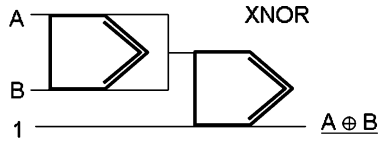

Fig. 6. XNOR gate obtained using two nonlinear processes.

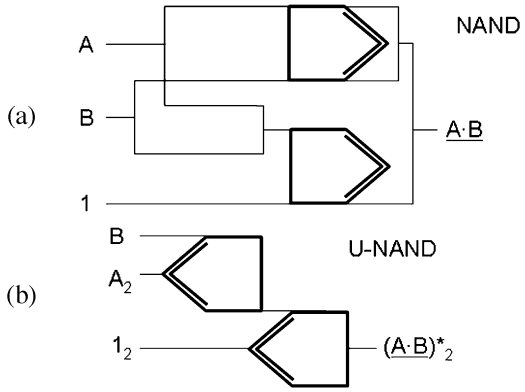

Fig. 7. Two nonlinear processes are also necessary for the NAND gate. In this way, the NAND gate can be operated (a) at the FF or (b) in upconversion.

IV. Complex Logic Circuits

The preceding functionalities and gates are cascaded; thus, other logic gates or more complex circuits can be realized by just combining together several processes. In fact, it is well known that the AND and XOR gates are the basic elements for realizing a sum operation, which, by its own, is the basic element for every algebraic operation. Consequently, a full algebra can be arranged, as well as equivalent photonic circuits that synthesize complex behaviors in optical commutations, particularly, network switching and routing processes. Please note that the proposed logic gates can be easily cascaded even if the parametric processes might be phase dependent. In fact, it is well known that every parametric process is almost phase independent if just two of the three interacting beams are injected at the input, letting the third one be generated during the nonlinear process, as is the case for all of the following proposed gates.

A. XNOR Gate

The XNOR operation is given by $\underline{\mathrm{A} \oplus \mathrm{B}}$. Following exactly such calculation, which means cascading together XOR and NOT gates, the XNOR gate is obtained, as shown in Fig. 6.

B. NAND Gate

The realization of the NAND gate is a bit more complicated and might be realized using AND and NOT gates. This procedure however will not preserve the information frequency. In fact, as shown in Fig. 3, both the AND and NOT gates cross the frequency between the input and the output, and moreover, the D-NOT gate (i.e., the down- NOT gate) cannot be realized. Thus, it would be possible, using the configuration in Fig. 7(b), to realize U-NAND gates (cross-NAND gates) with one of the inputs at the 2ω frequency but not the pure NAND gate.

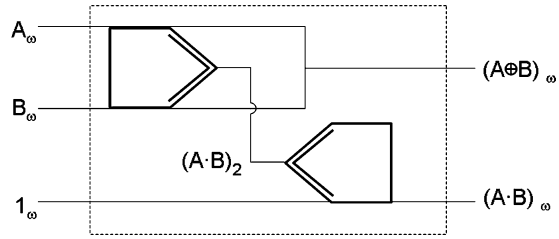

Fig. 8. All-optical 1-bit adder: Two inputs and an idler are injected into the SHG gate; the outputs on the FF are combined, giving the XOR function; and the output on the SHG is inserted into a personal digital assistant calculating D-I. The result is an all-optical half-adder.

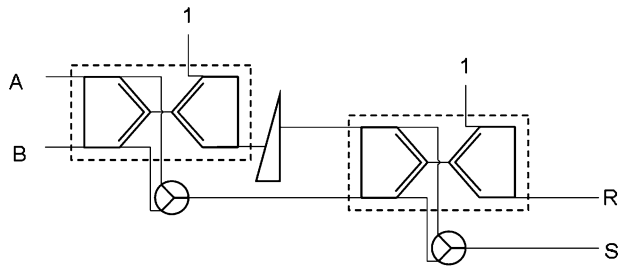

Fig. 9. All-optical 2-bit adder. The units in the dotted-line box are the same as that in Fig. 6 (optical half-adder). The rest of the first operation (AND) is shifted to the left at each calculation step.

The pure NAND gate can be obtained by following a different logical operation, i.e., by adding together the XOR gate output and the NOR gate outputs, as shown in Fig. 7(a).

C. 1-Bit Full Adder

It has been shown that high-efficiency SHG can operate like XOR and AND logic gates. Such gates are indeed the basic operations for performing a binary sum operation between two digital bits. In fact, every bit-to-bit sum can be obtained by the XOR operation, which will return 0 if the input bits are at the same logical state ($0+0=0$ and $1+1=0$) and 1 otherwise $(1+0=0+1=1)$. This would correspond to the operation of a half-adder given then by the XOR operation of each summed bit. Moreover, there is a carried-over digit that is brought about by the AND operation: In fact, the $1+1$ sum gives the binary number 10, where bit 0 is the result of the XOR function $(1 \oplus 1)$ and bit 1 (the carried-over digit) is the result of the AND function $(1 \cdot 1)$. However, combining together two parametric processes, as shown in Fig. 8, a 1-bit full adder can be realized. In such a configuration, the first parametric process would perform $\mathrm{A} \oplus \mathrm{B}$ as well as $(\mathrm{A} \cdot \mathrm{B})_2$. The XOR result is then carried out of the adder, and the carried-over supplementary digit is amplified and frequency downconverted by a D-I logic operation. In such a way, the outputs of the 1-bit full adder are 2 bits, which correspond to the adding digit sum and to the carried-over digit and are completely self-consistent and cascadable. Thus, consequently, to enlarge the number of bits that can be summed, the procedure just requires the cascading of as many 1-bit full adders as the number of digits of the summing records (Fig. 9).

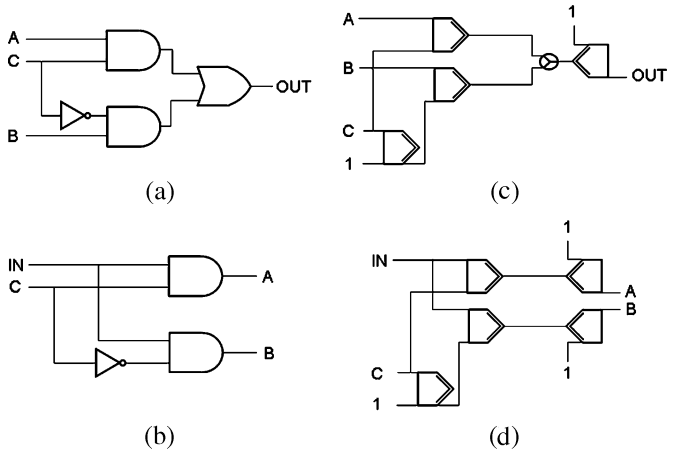

Fig. 10. Logical schemes of (a) multiplexing and (b) demultiplexing circuits and (c) and (d) their possible optical realizations, respectively.

Let us consider, for example, the sum of 2 numbers coded by n bits. To take advantage of the parallel nature of such operation, the bits will not be sequentially injected but will be spatially parallelized. The procedure for implementing the parallel calculation has five operations.

1) Make the bit-to-bit summation of two numbers (the A $\oplus$ B vector).
2) Make the carried-over calculation of two numbers (the A·B vector).
3) Spatially shift the obtained A · B carried-over number by one record toward the higher bits.
4) Make a new bit-to-bit summation of the previously obtained A $\oplus$ B and shifted A · B numbers.
5) Repeat steps 3 and 4 $n-1$ times until all the carried-over numbers are added. At the end of the process, the sum is carried by the last AND step, and the information on the rest (which is different from 0 only in case of overflow) is carried by the last XOR.

V. Commutation System

Fig. 10 shows the logical schemes of electronic multiplexing [Fig. 10(a)] and demultiplexing [Fig. 10(b)] circuits and their possible optical realizations [Fig. 10(c) and (d)]. In the case of a multiplexer [Fig. 10(a)], the two inputs A and B will be sent to the output, depending on the logical value of the control signal C [the output U is indeed given by A · B + B · $\underline{\text{C}}$, where $\underline{\text{C}}$ stands for NOT(C)]. The demultiplexer works in a similar way: Input A interacts in two different AND gates with C and $\underline{\text{C}}$; it can be routed in the selected path.

The clear advantage in using the described technology is that these processes are completely parallel and it is possible to code multibit information on the section of the beam without increasing the complexity of the network.

VI. Advanced Circuits

With the simple circuits previously described, it is possible to build complex functionalities as, for example, arithmetic products.

Fig. 11 presents a circuit called the optically controlled adder (CtA) that can select, depending on a control signal C, the sum

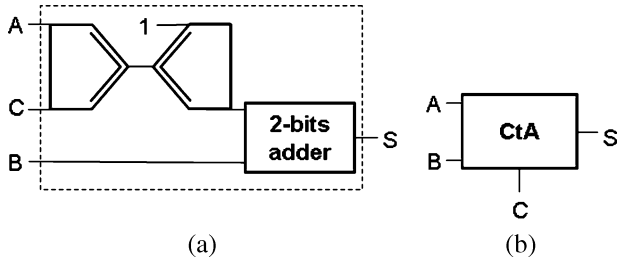

Fig. 11. Optical CtA: (a) Circuit implementation with optical gates, optical half-adder, and sequential adder, where C is the control signal that can select at the output the sum of the inputs (if C = 1, then S = A + B) or one of the inputs (if C = 0 , then S = B). (b) Symbolic representation.

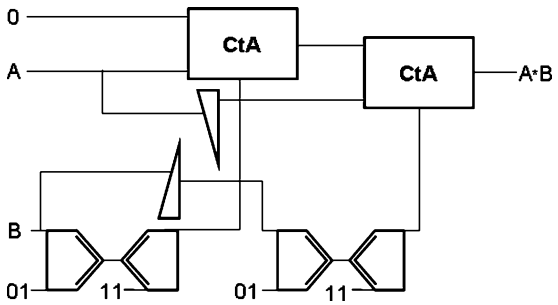

Fig 12. Optical product: Two CtAs are used to make the sums. Two AND gates control the values obtained from each sum to decide if another one is necessary. Two prisms are used to shift bits (upper) to the left and (lower) to the right.

of two numbers or one of the two inputs, thus giving a very simple arithmetic logic unit. Using this element, we will show the product of two 2-bit binary numbers.

The optical CtA works in this way: The two inputs are A and B, and C is the control signal, i.e.,

$$\text{if C} = 1,\ S = A(++)B$$
$$\text{if C} = 0,\ S = B$$

where (++) indicates the arithmetic sum. At the output, we have the sum or input B, depending on the value of control signal C (Fig. 12).

The arithmetic product, as shown in Fig. 10, implements the sequential algorithm given here.

1) The end-right bit of the multiplier is controlled: If it is 1, the multiplicand is summed to the product.
2) Shift 1 bit to the right of the multiplier and to the left of the multiplicand.
3) Repeat steps 1 and 2 for the total number of bits.

This corresponds to summing the multiplicand and itself a number of times corresponding to the value of the multiplier.

VII. Conclusion

In this paper, we have developed all-optical high-speed parallel solutions for several traditional problems of signal manipulation. We have discussed different gates and combinatory networks that are able to manage strips or matrixes of data, which are binary encoded as intensity modulation, showing how typical electronic problems can be solved using an all-optical technology. Indeed, such new solutions may suffer noise problems as in every nonlinear problem, which may be somehow minimized by very high or very low conversion efficiencies. An ex-

ample is the use of the single-photon regime, for which the proposed technology can be easily implemented, even with teleportation problems, to give crypto-safe communications (AMDG).

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