Optimized Design of Source Coupled Logic Gates in GaAs HEMT Technology

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***Abstract*— A simple model for the propagation delay of Source Coupled Logic gates composed of a differential pair and a common drain output buffer in III-V HEMT technology is proposed. The propagation delay model has been used to develop a design strategy that permits pencil-and-paper design of the gates, accounting for power-delay trade-off. The methodology has been applied to a charge-control high-frequency model of the HEMT, but is general-purpose and applicable also to different models. In the present case, percentage errors lower than 15 % have been found in propagation delay evaluation.**

I. Introduction

In recent years the bit rate of digital optical communication systems has reached 10 Gb/s for commercial systems and is moving over 40 Gb/s for experimental links. The very high values of f_T and f_{max} required in the linear and the decision blocks of both the transmitter and the receiver side, have pushed to the use of improved III-V technologies. Therefore, a research effort has been paid both to design high-speed digital circuits with such innovative technologies, and to correlate circuit performance to device parameters. Accurate models have been developed to evaluate the propagation delay of Source-Coupled Logic (SCL) gates, and to compare the results obtainable by means of classical and innovative topologies implemented in III-V technologies [1]. On the other hand, simple closed-form expressions for the propagation delay have been found also for bipolar [2] and CMOS [3] logic gates, in order to perform a pencil-and-paper design of the gates, able to deal with the power-delay trade-off in the early phases of the design flow. In this work, the previously developed design strategies have been extended in order to permit pencil-and-paper design of SCL gates based on III-V HEMT technologies. A closed-form expression of the propagation delay is presented, that is not dependent on the non-linear model chosen for the device. The proposed design guidelines allow the specification of the bias currents of both the differential pair and the output buffers (see Fig. 1) of the SCL gate, by considering the constraints on power dissipation and speed.

II. Model of the HEMT Device

The non-linear HEMT model chosen in this work is the EE_HEMT EEsof scalable model [4], a charge control model (see Fig. 2) that allows high accuracy up to 50 GHz. The total charge under the gate is divided into two contributions $Qgc(V_{gs},V_{gd})$ and $Qgy(V_{gs},V_{gd})$.

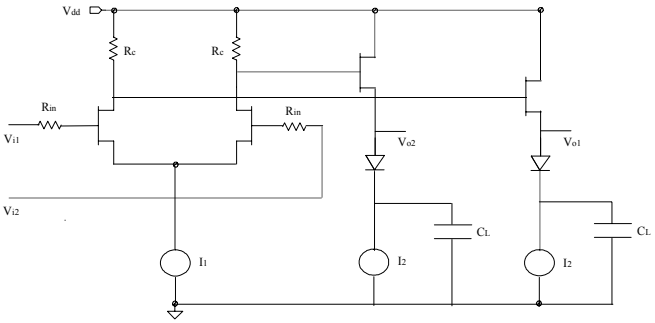

Fig. 1. SCL inverter with output buffers.

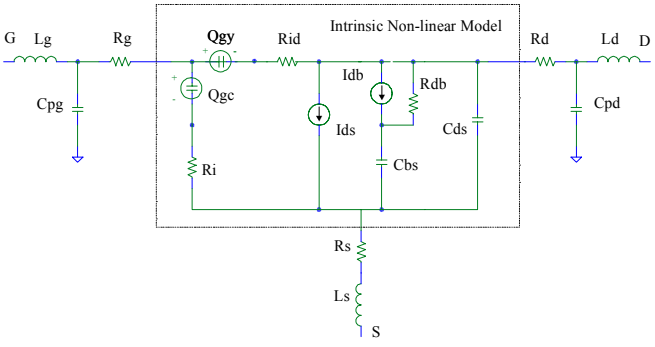

Fig. 2. Non-linear equivalent circuit of the HEMT device.

The capacitances *Cgs* and *Cgd*, as well as the trans-capacitances $Cgs_2 = \partial Qgc/\partial Vgd$ and $Cgd_2 = \partial Qgy/\partial Vgs$, can be evaluated from the two non-linear charge expressions above. The capacitance *Cds* is not bias-dependent. The drain current expression is compatible with the non-linear models proposed by Curtice for MESFET devices [5] and used also for HEMT devices [6]:

$$I_{ds} = W \cdot f(V_{gs}, V_{ds}) \cdot (1 + \lambda V_{ds}) \cdot \tanh(\alpha V_{ds}) = W \cdot I_{ds0}(V_{gs}, V_{ds}), \quad (1)$$

where *f*(*Vgs*,*Vds*) is a non-linear function of the instantaneous voltages across the device, I_{ds0} is the current of a device with unitary gate width, and *W* is the gate width. The transconductance (*gm*) and the output conductance (*gds*) are different from the static values gm^{DC} and gds^{DC}, and have to be evaluated by taking into account of the frequency dispersion of MESFET and HEMT devices [7], modeled by means of a second non-linear current source operating at frequencies greater than the cut-off frequency of the phenomenon:

$$I_{db} = W \cdot f_1(V_{gs}, V_{ds}), \quad (2)$$

where f_1(*Vgs*,*Vds*) is again a non-linear function of the instantaneous voltages across the device. The small-signal values of *gm* and *gds* can be evaluated as follows:

$$gm = gm^{DC} + \frac{\partial I_{db}}{\partial V_{gs}} = W \cdot gm_0(V_{gs}, V_{ds}), \quad (3)$$

$$gds = gds^{DC} + \frac{\partial I_{db}}{\partial V_{ds}} = W \cdot gds_0(V_{gs}, V_{ds}), \quad (4)$$

where gm_0 and gds_0 are the transconductance and the output conductance of a device with unitary gate width.

In this work, a non-linear model has been extracted and implemented in Agilent ADS CAD tool for a device from OMMIC D02AH monolithic process with gate length of 0.2 µm starting from Ids measurements and S-parameter measurements in the 1-50 GHz band. The procedure presented in [8] has been used to extract the model. Firstly, a multi-bias linear model (see Fig. 3) has been extracted at each bias point; then, the empirical parameters of the non-linear functions *Ids*, *Idb*, *Qgc*, and *Qgy* have been determined by means of the optimization procedure described in [8].

III. Modeling of Propagation Delay

The overall propagation delay τ_{PD} can be evaluated as in [2], by summing the propagation delay $\tau_{PD,Dif}$ of the unloaded differential pair to the propagation delay $\tau_{PD,Buf}$ of the buffers driven by the output resistance of the differential pair and loaded by the capacitance C_L:

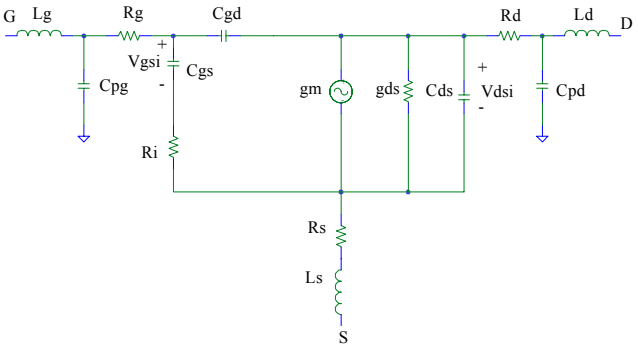

Fig. 3. Linear equivalent circuit of the HEMT device.

$$\tau_{PD} = \tau_{PD,Dif} + \tau_{PD,Buf}. \quad (5)$$

A. Differential Pair Model

The propagation delay $\tau_{PD,Dif}$ has been evaluated under the hypothesis of dominant pole, by computing the time constant τ of the circuit:

$$\tau_{PD,Dif} = 0.69 \cdot \tau = 0.69 \cdot [C_{gs} \cdot R_{Cgs} + C_{gd} \cdot R_{Cgd} + (C_{ds} + C_{load}) \cdot R_{Cds}], \quad (6)$$

where C_{load} is the input capacitance of the next stage (i.e. the output buffer in the present case). The following expressions have been found for the other elements:

$$R_{Cgs} = R_{in}, \quad (7)$$

$$R_{Cds} = \frac{R_c}{1 + gds \cdot R_c}, \quad (8)$$

$$R_{Cgd} = R_{in} + R_c \cdot \frac{1 + gm \cdot R_{in}}{1 + gds \cdot R_c}, \quad (9)$$

$$C_{gs} = \frac{\left| Q_{gc}(V_{gs2}, V_{gd2}) - Q_{gc}(V_{gs1}, V_{gd1}) \right|}{\Delta V_{gs}}, \quad (10)$$

$$C_{gd} = \frac{\left| Q_{gy}(V_{gs2}, V_{gd2}) - Q_{gy}(V_{gs1}, V_{gd1}) \right|}{\Delta V_{gd}}. \quad (11)$$

In particular, the capacitances *Cgs* and *Cgd* are evaluated by using the non-linear model for the HEMT, so that fast variation of the voltages across them when a step input waveform is applied, are accounted for. The trans-capacitances Cgs_2 and Cgd_2 have been neglected. The percentage errors found between the ADS simulations and the proposed model for three different bias points, three values of C_{load}, and two values of R_{in} are shown in Table I.

TABLE I. PERCENTAGE ERROR ON $\tau_{PD,DIF}$ EVALUATION

		Vgs = -0.3 V Vds = 2.6 V		**Vgs = -0.1 V Vds = 2.6 V**		**Vgs = -0.5 V Vds = 3.2 V**	
	R_{in}	0 Ω	50 Ω	0 Ω	50 Ω	0 Ω	50 Ω
C_{load}							
0.01pF		5.1	1.5	10.4	8.4	1.1	8.1
0.1pF		0.6	3.1	2.4	1.3	0.5	5.4
0.3pF		0.3	2.6	1.6	0.7	0.9	2.0

B. Output Buffer Model

The propagation delay $\tau_{PD,Buf}$ of the output buffer is evaluated by considering an input resistance (i.e. the output resistance of the differential pair, about equal to R_c, in the present case) and the output load capacitance C_L. The small-signal transfer function contains a zero *z*:

$$z = (Cgs + Cgs_2) / gm, \tag{12}$$

and a couple of poles with:

$$\omega_n = \sqrt{\frac{(gm + gds)/R_c}{(Cds + C_L)(Cgs + Cgd + Cgs_2) + CgsCgd}}, \tag{13}$$

$$\xi = p_1 \cdot \omega_n / 2, \tag{14}$$

where:

$$p_1 = \frac{1}{gm + gds}[gds \cdot R_c \cdot (Cgs + Cgs_2 + Cgd) + gm \cdot R_c \cdot (Cgs_2 + Cgd) + Cgs + Cds + C_L]. \tag{15}$$

The trans-capacitance Cgd_2 defined as $\partial Qgy/\partial Vgs$ has been neglected.

Finally, the propagation delay $\tau_{PD,Buf}$ has been evaluated as in [2], but taking also into account of the zero *z* that can not be neglected in the present case:

$$\tau_{PD,Buf} = \tau_{PDn} / \omega_n - z, \tag{16}$$

$$\tau_{PDn} = 0.57 \cdot (\xi - 0.1) + 1.1. \tag{17}$$

The non-linear model has been used to evaluate the capacitance *Cgd*, see (11). A constant value has been assumed for *Cgs*, as the voltage *Vgs* across it does not change during the step input waveform application. In Table II the percentage errors found between the ADS simulations and the proposed model are shown for three different bias points and three different values of C_L.

TABLE II. PERCENTAGE ERROR ON $\tau_{PD,BUF}$ EVALUATION

C_L	**Vgs = -0.3 V Vds = 2.6 V**	**Vgs = -0.1 V Vds = 2.8 V**	**Vgs = -0.5 V Vds = 2.4 V**
0.01 pF	7.8	12.3	1.6
0.1 pF	5.8	8.9	2.5
0.3 pF	5.6	7.3	2.8

If the trans-capacitance Cgs_2 is also neglected in order to find a simpler model, a further under-evaluation of the propagation delay of about 4.5 % is found.

IV. DESIGN STRATEGIES OF SCL GATES

The design of the SCL gate requires to set the optimal values for the bias currents I_1 and I_2 and the device gate widths W_1 and W_2, of the differential pair and the output buffers, respectively. The design goals are set in terms of the overall propagation delay τ_{PD}, the output dynamic

$$\Delta V = I_1 \cdot R_c, \tag{18}$$

expressed under the hypothesis that the output buffer does not affect ΔV, the output slew rate affected by the charge and discharge times of the load capacitances C_L operated by the output buffers. We have accounted for it by means of the output rise and fall times t_{LH} and t_{HL}, in particular the expression for t_{LH} is the following:

$$t_{LH} = \frac{C_L}{I_2} \cdot \alpha_0(\Delta V), \tag{19}$$

where

$$\alpha_0(\Delta V) = \int_{V_{ds0} - \Delta V/2}^{V_{ds0} + \Delta V/2} \frac{dV}{I_{ds0}(V_{gs}^{pk}, V_{dd} - V)/I_{ds0}(V_{gs}^{pk}, V_{ds0}) - 1} \tag{20}$$

In (20) the function α_0 depends on the expression chosen to describe I_{ds}, on the bias point, on the power supply V_{dd}, and on the dynamic range ΔV. Therefore, the current I_2 can be expressed as a function of the dynamic range, the output load, and the rise time.

It has to be noted that for HEMT devices the transconductance shows a maximum as a function of the gate-source voltage [7]. The devices in the SCL gate are

supposed to be biased at the gate-source voltage V_{gs}^{pk} which provides the maximal transconductance, and at a drain-source voltage Vds_0 that allows the device to work in saturation region for the overall dynamic range. This design choice implies that for each specified value of I_1 (I_2), the gate width W_1 (W_2) of the differential pair (of the buffers) is also determined.

The proposed design strategy can be summarized into the following two steps. Firstly, the bias current of the output buffers is chosen from the specifications on the output slew-rate and the output load, see (19); then, the optimal value for the current I_1 is found by evaluating the minimum of τ_{PD} versus I_1, as a function of the specified values of R_{in}, C_L, and t_{LH}. The expression of the minimum for τ_{PD} is the following:

$$I_1^{Min} = 2\sqrt{\beta_0(\Delta V)\cdot\frac{C_L}{t_{LH}\cdot R_{in}}}, \qquad (21)$$

where the following expression has been found for β_0 as a function of the unitary gate parameters of the devices in the differential pair and in the buffers:

$$\beta_0 = \frac{0.83\cdot\alpha_0\cdot\Delta V\cdot(Cgs_0+Cgd_0)}{Cgs_0+Cgd_0\cdot\dfrac{gm_0\cdot\Delta V/2}{1+gds_0\cdot\Delta V/2}}. \qquad (22)$$

The hypothesis has been done that the trans-capacitance Cgs_2 can be neglected and that the bias voltage Vds_0 chosen for the devices of the two cells, determines about equal values for the unitary gate parameters Cgs_0, Cgd_0, gm_0, and gds_0 of the two cells.

V. A Case Study

A CML gate has been designed by considering an input resistance R_{in} = 100 Ω, a load capacitance C_L = 0.1 pF, an output dynamic range ΔV = 300 mV, and output rise/fall times of about 20 ps. The V_{gs}^{pk} of the given technology is about 0.3 V, a Vds_0 = 2.5 V has been chosen so that the active devices are operating in saturation region during the voltage swing. A current I_2 = 19 mA has been found from (20) in order to fulfil the specification on the slew-rate. Then, the minimum current I_1^{Min} = 30 mA has been evaluated from (21), and a corresponding propagation delay τ_{PD} = 27.9 ps has been found. Finally, the CML gate has been implemented and simulated in ADS, and an overall propagation delay of 28.6 ps has been found, denoting an estimation error of about 2.5%.

VI. Conclusions

A simple model for the SCL gate has been proposed in order to perform a pencil-and-paper design of the cell, on the basis of design guidelines that allow optimization of the cell in terms of slew-rate and power dissipation. The model has shown percentage errors lower than 15 % in the evaluation of propagation delays through the differential pair and the output buffers which compose the SCL gate.

References

[1] Y. Umeda, K. Osafune, T. Enoki, H. Yokohama, Y. Ishii, and Y. Imamura, "Over-60-GHz Design Technology for an SCFL Dynamic Frequency Divider Using In-P-Based HEMT's", IEEE Trans. on MTT, Vol. 46, no. 9, pp. 1209-1214, Sep. 1998.

[2] Alioto, Palumbo, "CML and ECL: Optimized Design and Comparison", IEEE Trans. on CAS I, Vol. 46, no. 11, pp. 1330-1341, Nov. 1999.

[3] Alioto, Palumbo, "Design Strategies for Source Coupled Logic Gates", IEEE Trans. on CAS I, Vol. 50, no. 5, pp. 640-654, May. 2003.

[4] ADS 2003, Advanced Design Systems, Agilent Technologies, Reference Manual, 2003.

[5] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits", IEEE Trans. on MTT, Vol. 28, pp. 448-456, May. 1980.

[6] T. Tanimoto, "Analitycal Nonlinear HEMT model for Large Signal Circuit Simulation", IEEE Trans. on MTT, Vol. 44, no. 9, pp. 1584-1586, Sep. 1996.

[7] J. M. Golio, "Microwave MESFETs and HEMTs", Artech House, 1991.

[8] M. Cicolani, A. Di Martino, S. D'Innocenzo, S. Pisa, P. Tommasino, A. Trifiletti, "A New Instantaneous Model of MESFET and HEMT Devices for Large Signal Circuit Design," Microwave and Optical Technology Letters, Vol. 29, no. 3, pp. 187-190, May 2001