Optical receiver for IM-DD systems operating at 2.488 Gbit/s

Valter Cocco*, Giuliano Gatti**, Piero Marietti*, Giacomo Parafioriti^, Salvatore Rotolo^, Alessandro Trifiletti*

*Dip. Ingegneria Elettronica, Università degli Studi di Roma "La Sapienza", Via Eudossiana 18, 00184 Roma, Italy
**XRM ESTEC, Postbus 299, 2201 AG, Noordwijk, The Nederland
^ITALTEL, 20019 Castelletto di Settimo, Milano, Italy

ABSTRACT

In this paper we present the design approach and measurements of an optical receiver suited for IM-DD systems operating up to 2.5 Gbit/s bit-rate. The receiver is composed by a Ga-As MMIC transimpedance amplifier and a commercially available pin photodiode. The MMIC amplifier has been fabricated and it has been measured on wafer, showing a -3 dB cut-off frequency of 2.6 GHz, stability and low sensitivity to bias variations.

1. INTRODUCTION

The aim of this work is to obtain a module able to be used in a SDH frame at the level STM-16, with 2.488 GBit/s bit-rate and the constraints are to use a commercially available In-Ga-As pin photodetector in conjunction with a MMIC transimpedance amplifier. The main feature of such a receiver is its extremely wide fractional bandwidth, which is due to absence of line coding.

We have chosen an EPITAXX ETX 25B chip on carrier pin photodiode, which is characterized by 25 μm sensitive area, responsivity 0.8 A/W @ λ = 1.3 μm and dark current i_d = 3nA.

We have designed a monolithically integrated transimpedance amplifier (TIA) that was fabricated at Daimler-Benz using E05 process. The main design features of the TIA are as follows[1]: 1) It is a DC-coupled amplifier and this is very important for low-frequency cut-off performance of the receiver, 2) It can achieve a wide dynamic range, 3) TIA topology avoids the use of post-amplifier equalization of high-impedance configurations. Monolithic integration allows to choose the dimensions of the active devices to improve noise performances.[2-3] This topology has been used successfully in many MMIC designs using similar MMIC processes.[4-5]

The active devices of E05 process are MESFETs with 0.5 μm gate-length and gate-widths in the range between 200 and 1000 μm. The DC behaviour of all the MESFET is described by one I/V plot normalized to gate-width, while the AC behaviour of each device is represented by a set of S-parameters matrices and noise data for four different bias points.

2. THE DESIGN APPROACH

The photodiode has been mounted on a 635 μm alumina substrate and, through a reflection coefficient measurement, we have obtained a lumped elements model of the photodiode and its jig, which was used to optimize the amplifier. This measurement has shown resonance effects at 3.5 GHz as shown in Fig. 1 (first small loop) and above 7 GHz (second loop). Figure 2 shows the lumped elements model of the photodiode.

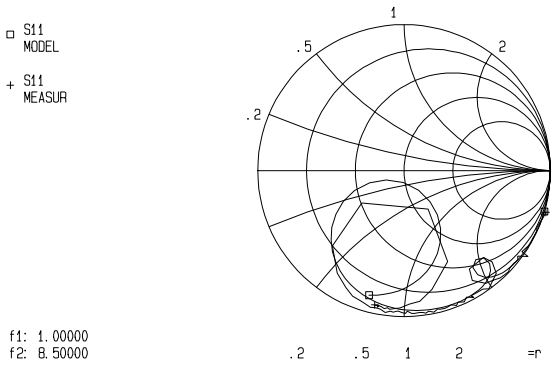

Fig. 1. Measured reflection coefficient of the photodetector test-jig and simulation of its lumped element model.

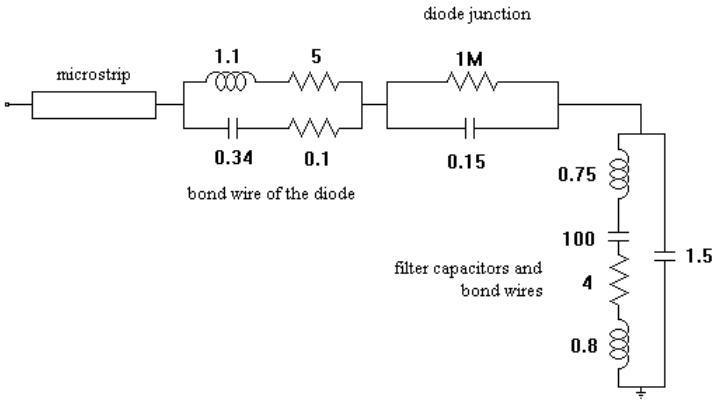

Fig. 2. Lumped element model of the photodiode.

To determine DC operating point of the TIA we have obtained a parameter set of the DC MESFET Curtice model[6] from I/V plot of E05 MESFETs. An extensive DC analysis was performed using SPICE to avoid incorrect biasing of single device in the TIA and to determine whether each MESFET remains in its safe operating area during power-switching transient of the module.

The schematic of the circuit is presented in Fig. 3; we have chosen to separate the DC pads V_{s2} and V_{g2} to allow post-fabrication trimming of bias levels, to avoid incorrect bias conditions and to tune AC behaviour of the TIA. The estimated and measured power consumption is about 500 mW.

The optimization of the circuit for AC performance was carried out using a software tool[7] able to evaluate the root-locus of the transimpedance transfer function of the TIA starting from a simple model of the forward amplifier.

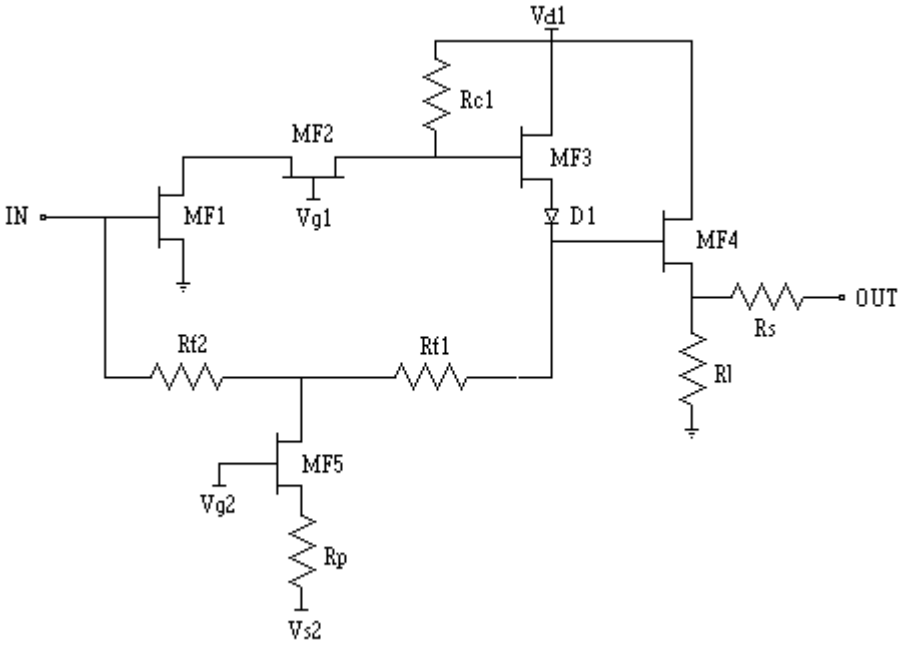

Fig. 3 Schematic of the MMIC amplifier.

The amplifier is composed by a cascode stage using two 260 μm MESFETs (MF1, MF2) with a buffer stage inside the feedback path, and by another buffer stage to match the external load. A large amount of available area was taken by on-chip capacitors to allow on-wafer measurements of the circuit (C1 - C4). The resistor Rp put in series to source of MF5 increases

its output impedance and it decreases the loading effects on the feedback network. The final layout of the TIA is shown in Fig. 4; the overall chip size is 900 x 1100 μm.

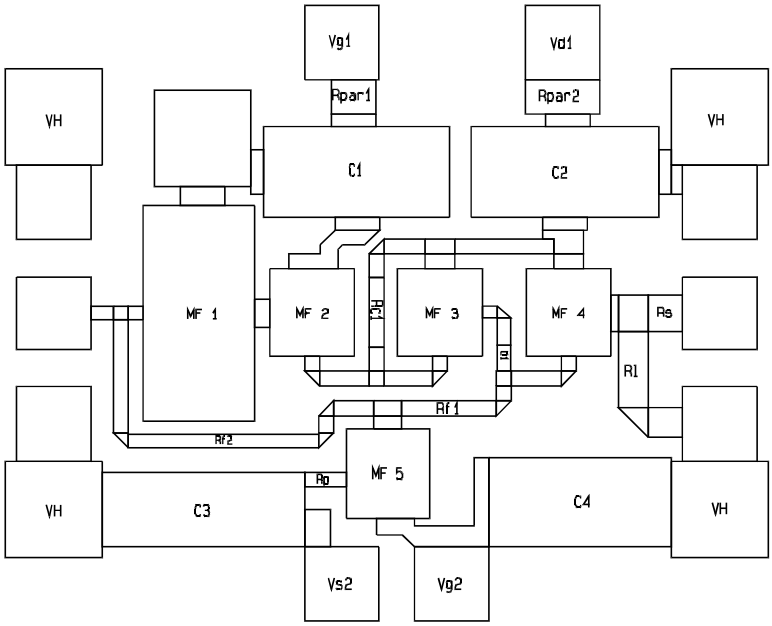

Fig. 4 Layout of the fabricated TIA.

We have designed two MIC to complete the receiver; in the input one we place photodiode, its biasing filter and a taper section in the signal path to increase the bandwidth, in the output one we place capacitors for DC decoupling.

3. COMPARISON BETWEEN SIMULATION AND MEASUREMENTS

In this section we present a comparison between AC simulation of the TIA and the on-wafer measurements of TIA. The plots of TIA S-parameters, simulated without DC filters (MODEL) and measured by a Cascade probe-station (MEASUR), are shown in Fig. 4. We can see a good agreement above 0.4 GHz, when on-chip capacitors carry out a good filtering action of bias pads.

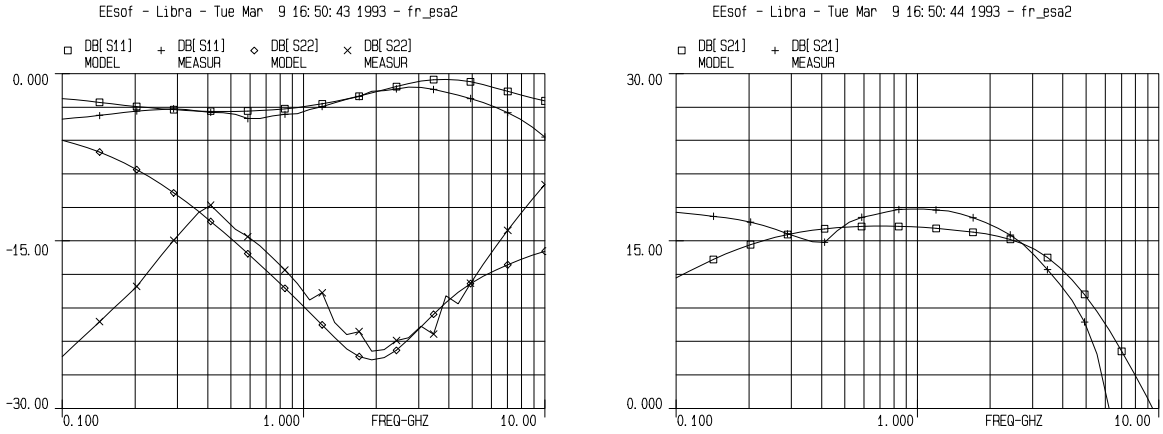

Fig. 5. Comparison between on-wafer measurements and simulations of the MMIC TIA.

In Fig. 6 we present a comparison between two circuit simulations: MODEL is the transimpedance transfer function of the receiver obtained from full circuit simulation, MEASUR is obtained by measured S-parameter of the photodiode and the MMIC TIA. In Fig. 7 calculated input equivalent current due to amplifier noise sources is shown.

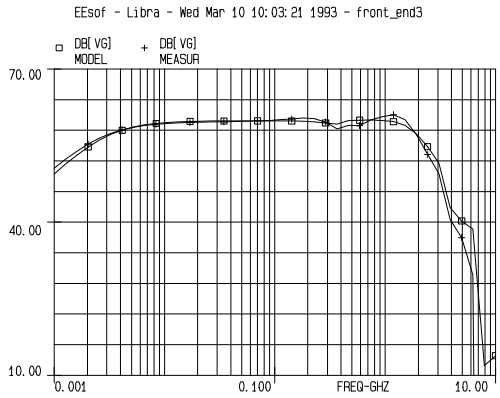

Fig. 6. Comparison between circuit simulation and extrapolated transimpedance.

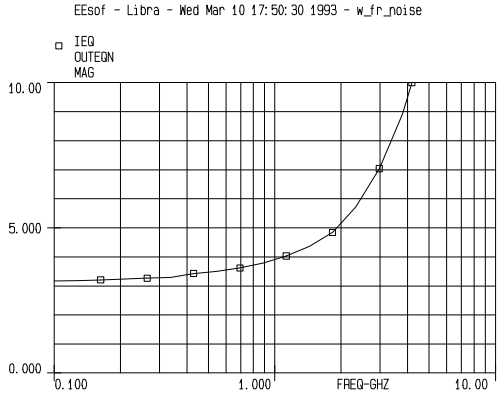

Fig. 7. Input equivalent noise current due to MMIC amplifier.

In conclusion a GaAs MMIC transimpedance amplifier has been designed and fabricated using E05 process of Daimler-Benz. It has been measured on wafer showing a good agreement with the simulation. The configuration we have chosen allow post-fabrication trimming of biasing and we will use this feature to tune the transimpedance transfer function of the final receiver.

4. REFERENCES

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