Non-linear Control of PLL Operation in Clock Recovery Circuits

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Abstract - In this paper the scheme of a new clock recovery circuit (CRC) based on the Charge-Pump PLL is presented. In this scheme a non-linear control which monitores the amplitude level of the protoclock, is used to open the PLL when the protoclock signal looses its well defined sinusoidal structure. The purpose of this work is twofold: to reduce the amount of sistematic jitter of the CRC without reducing the bandwith of the PLL, and to obtain a CRC with reduced sensitivity to bit-rate variations. The block scheme of the CRC requires minor modifications with respect to the basic structure of a PLL-based CRC and it obtains evident improvements in the output jitter. The non-linear control makes a closed form analysis very difficult, therefore computer simulations have been performed to obtain an estimation of the mean squared jitter as a function of the system parameters. In this paper we present the results in terms of output jitter for a CRC with a high degree of asymmetry in the prefilter section; the improvement we have obtained is of 6dB.

Introduction - Clock recovery function in NRZ systems can be achieved by using a non-linear block to regenerate the bit-frequency reference and a high-Q component (passive filter or PLL) to filter the reference. The non-linear block can be achieved either by using a filter and a non-linear element [1,2] or by an edge detector block [3]. As soon as a signal which contains a spectral component (protoclock [4]) has been obtained, a band-pass element (postfilter) is needed to perform a filtering action and to increase SNR of the protoclock. A PLL is often used to overcome mistuning effects and Q limitations [5,6] of passive postfilter. In Fig. 1 the scheme of a CRC based on CP-PLL is shown [7,8].

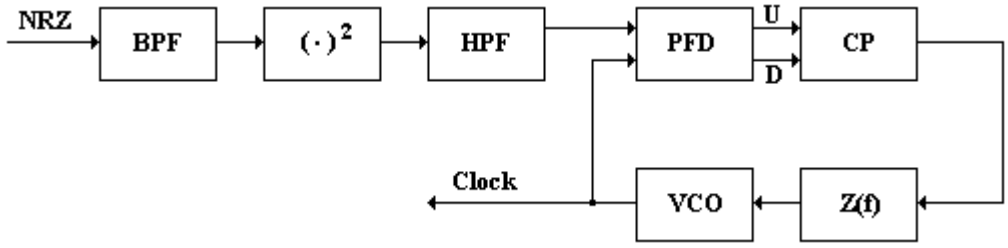

Fig. 1. Block scheme of the Clock Recovery Circuit based on Charge-Pump PLL.

A careful analysis of the protoclock is necessary to find the input data sequences which can cause a jitter burst. In principle, the protoclock is a quasi-sinusoidal signal [9] which is affected only by amplitude modulation and it could be used to drive a decision circuit. The lack of symmetry of the prefilter [10] causes a phase modulation in the protoclock which is the cause of the output jitter and therefore a postfilter becomes necessary. To decrease the effect of the phase modulation it is possible to reduce the bandwidth of the PLL, reducing the capture range. A comparison between protoclock phase deviation and internal noise sources (In-Phase and In-Quadrature noise) shows that the phase modulation burst has to be related mainly to amplitude reduction of the useful component of the protoclock.

We propose to use a non-linear control of the PLL operation to use the protoclock signal only when it has a high instantaneous SNR, whereas during low SNR time intervals the non-linear control causes the rejection of the protoclock and the PLL is disconnected.

Protoclock analysis - The signal y(t) at the output of the squarer block can be obtained in terms of the impulse response of prefilter and of the data stream $\{C_n\}$[11]:

$$y(t) = y_{LF}(t) + y_{HF}(t), \qquad (1)$$

$$y_{LF}(t) = \frac{1}{2}\left[x_c^2(t,\phi) + x_s^2(t,\phi)\right], \tag{2}$$

$$y_{HF}(t) = \frac{1}{2}\left[x_c^2(t,\phi) - x_s^2(t,\phi)\right]\cos\left[2\pi f_b t + 2\phi\right] + \left\{x_c(t,\phi)x_s(t,\phi)\right\}\sin\left[2\pi f_b t + 2\phi\right], \tag{3}$$

where the low-frequency components of the signal at the output of the prefilter are

$$x_c(t,\phi) = \sum_{n=-\infty}^{+\infty}(-1)^n c_n g_c(t - nT,\phi), \tag{4}$$

$$x_s(t,\phi) = \sum_{n=-\infty}^{+\infty}(-1)^n c_n g_s(t - nT,\phi), \tag{5}$$

g_c and g_s are the low-frequency components of the impulse response of the prefilter, and ϕ is their reference angle. By choosing the phase angle ϕ to satisfy the condition [11]

$$\overline{x_c(t,\phi)x_s(t,\phi)} = 0 \tag{6}$$

it becomes possible to separate the useful signal from In-Phase and In-Quadrature noise components. The phase deviation due to the noise components is given by

$$\Delta\phi(t) = \tan^{-1}\left[\frac{n'_s(t)}{1 + n'_c(t)}\right] \tag{7}$$

where the noise components n'_c, n'_s have been obtained dividing the noise component of the protoclock (Eq. 3) by the mean amplitude of the protoclock itself. In Tab. 1 the SNR of the protoclock as a function of the normalised detuning of the prefilter $\delta = \Delta f/BW$ defined as the ratio of the frequency detuning to the bandwidth (-3dB) for the filter used in the simulations is shown.

δ	SNR (dB)
0	22
0.05	20
0.125	12

Tab. 1. SNR of the protoclock versus normalised detuning of the prefilter.

Computer simulations have revealed that usually the worst condition from the point of view of the phase noise of the protoclock is due to a decrease in the amplitude of the useful signal (In-Phase component), and not by an increase in the In-Quadrature noise as it could be expected. In Fig. 2 the time plots of the normalised In-Phase component and the phase deviation of the protoclock, obtained by a first order Butterworth filter tuned to a half of the bit-frequency, are shown. In the time periods while In-Phase component is within -20 dB with respect its maximum value, the output phase deviation of the protoclock is within $|\Delta\phi| < 30°$, therefore the protoclock shows a low phase-noise contribution.

We propose a CRC made by a Charge-Pump PLL (CP-PLL) [7] and an amplitude control which opens the loop when the protoclock has a low SNR. The control signal could be the instantaneous amplitude of the In-Phase component which is compared to its weighted mean to reveal low SNR condition. During a phase noise burst the PLL has to remain on the latest value of the output phase (Hold state) to recover its filtering action as the SNR has reached a sufficient value (Track state). For this application the Charge-Pump PLL is the best candidate since it is a discrete-time system which receives an input signal (in terms of phase error) during the active periods of the PFD [7].

The control signal - The transitions between Track and Hold states should be controlled by the In-Phase component of the protoclock $y_{HF}(t)$

$$c(t) = y_{HF\_I}(t, 2\phi) = \frac{1}{2}\left[x_c^2(t,\phi) - x_s^2(t,\phi)\right]. \tag{8}$$

As shown in Eqs. 2, 3 the spurious low-frequency component $y_{LF}(t)$ is another possible control signal since the power contribution of the x_S component is usually negligible with respect to the x_C one

$$c'(t) = y_{LF}(t) = \frac{1}{2}\left[x_c^2(t,\phi) + x_s^2(t,\phi)\right].$$

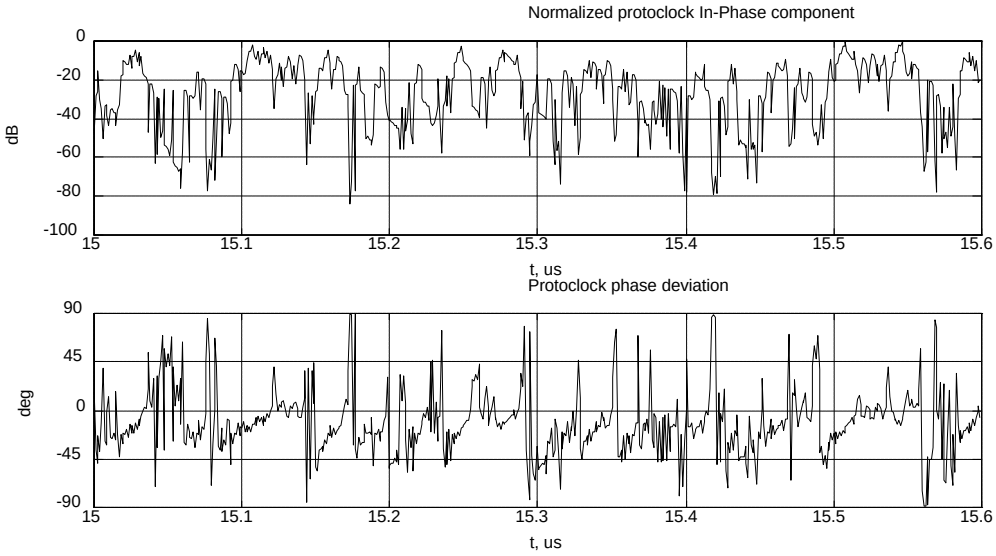

Fig. 2. Time plot of the In-Phase component of the protoclock and protoclock phase deviation.

The amplitude level of the control signal c'(t) has to be converted to a logic level TH to control the state of the loop (Track or Hold). The signal TH is defined by the following logical condition

$$TH = c'(t) > G\overline{c'(t)} \qquad (9)$$

and it can be obtained by using a low-pass filter, a gain element G and a threshold comparator. The Charge-Pump PLL is easily completed by the non-linear control proposed as it can be seen in Fig. 3.

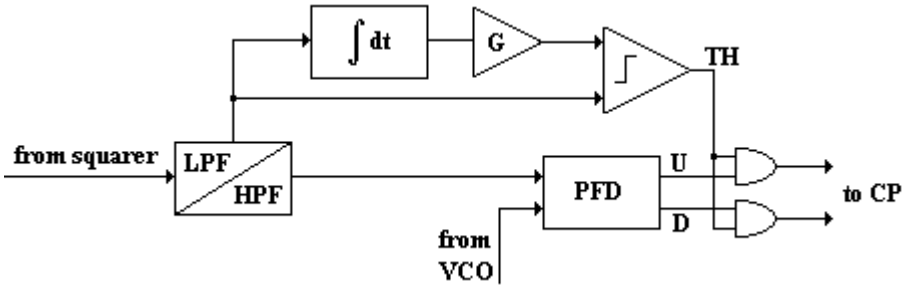

Fig. 3. Non-linear Control block of the CRC proposed.

The control lines U, D coming from the PFD are masked by the signal TH to lock the output phase of the PLL.

The simulation set-up - To evaluate the effectiveness of the proposed solution we have performed computer simulations on the structure shown in Figs. 1, 3. The non-linear operation chosen to regenerate the bit-frequency line is performed by a prefilter and an ideal squarer. A first order Butterworth filter with BW = 20 MHz has been chosen as the prefilter for a bit-rate B=1Gbit/s. The input data sequence is a period of a PRBS with 2^{14}-1 length without zero-filling and without additive noise. The output sequence has been considered after the transient due to the phase/frequency acquisition; in these simulations phase noise of the VCO is not included. The parameters of the third order PLL are listed in Tab 2. A large number of prefilters have been used to evaluate the effect of the control proposed here on protoclock signals obtained by slightly

asymmetrical pre-filters. Matlab and Simulink software tools have been used to perform time-domain simulations with non-linear models of the CP-PLL. The output signal has been post-processed to evaluate the mean squared value and the maximum value of the output jitter.

BW	Damping Factor	Maximum Peaking
200 KHz	1.73	0.62 dB

Tab. 2. Loop parameters of the PLL used in the simulations.

Simulation results - The parameters chosen to evaluate the performance of CRC proposed are the maximum value of the output jitter and its mean squared value; the histogram of the jitter distribution is another key figure for this system. The gain imposed to the mean value of the control signal is a critical parameter for this CRC since it sets a threshold level which controls the transitions between Hold and Track states. Therefore computer simulations have been performed by varying this gain and observing the output results in term of rms output jitter. In high Bit-Rate applications (B > 622 Mbit/s) crystal oscillators are not available, therefore it is very important to control both the ratio of time intervals in Track and Hold states and the longest time interval while the PLL is open to evaluate the influence of internal phase-noise of the VCO. In Fig. 4 the time plot of the output jitter obtained from a prefilter with normalised detuning $\delta = 0$ with non-linear control with control gain G = 0.1 and without control are shown. The effectiveness of the solution proposed is apparent. The maximum output jitter is reduced by a factor of 1.5 and the rms value is reduced by a factor of 2.

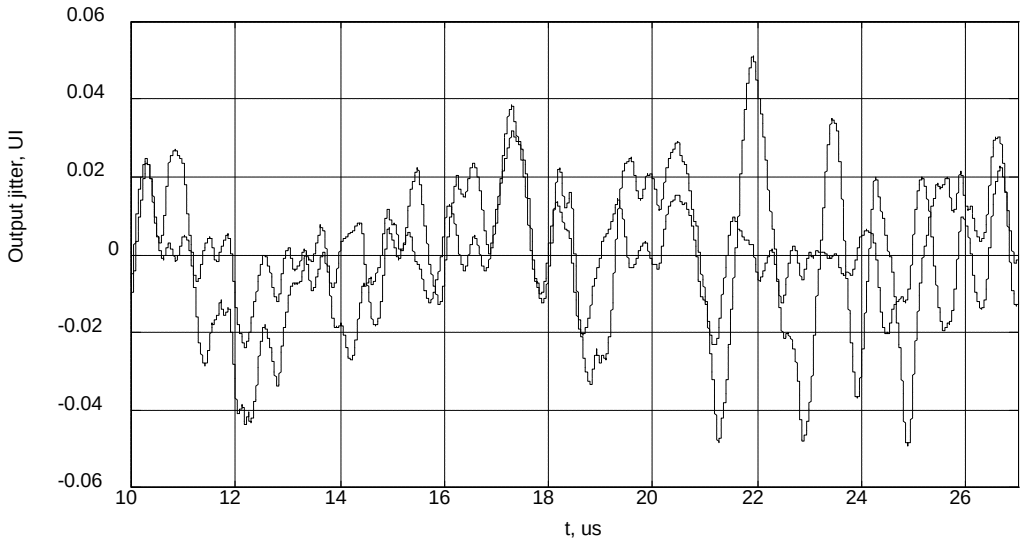

Fig. 4. Comparison between output jitter without non-linear control (dashed line) and with G = 0.1 (solid line).

In Figs. 5, 6 the histograms obtained from the output jitter sequences without non-linear control and with a non-linear control, with G = 0.1, for a protoclock obtained by the means of a prefilter with normalised detuning $\delta = 0$ are shown.

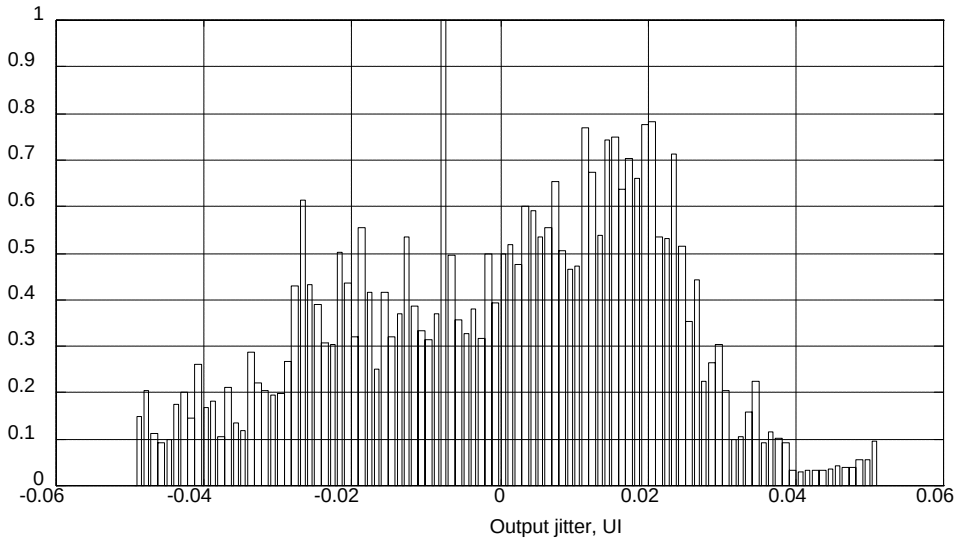

Fig. 5. Output jitter histogram without non-linear control and δ = 0.

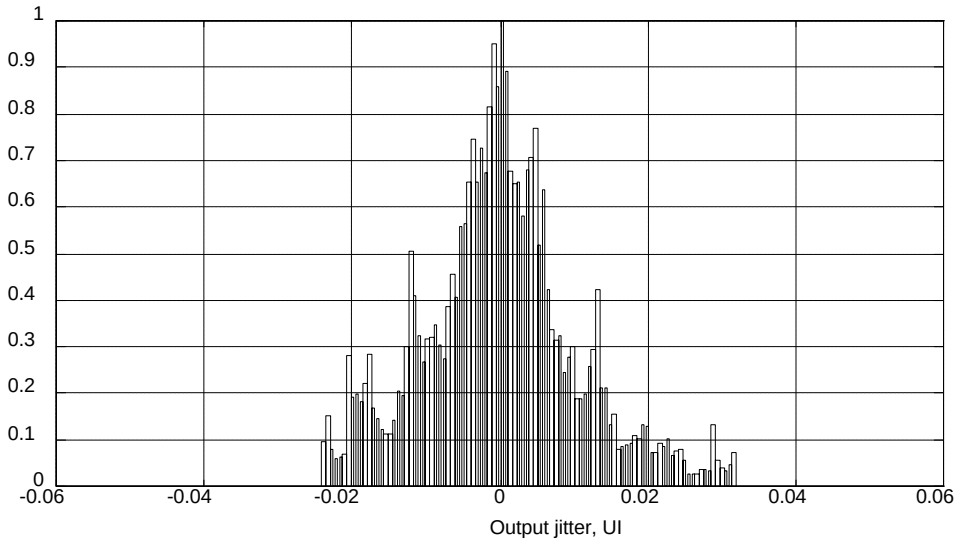

Fig. 6. Output jitter histogram with control gain G = 0.1 and δ€= 0.

In Fig. 7 the rms output jitter as a function of the control gain is shown (without prefilter detuning) and a best value for the control gain is found (G = 0.15).

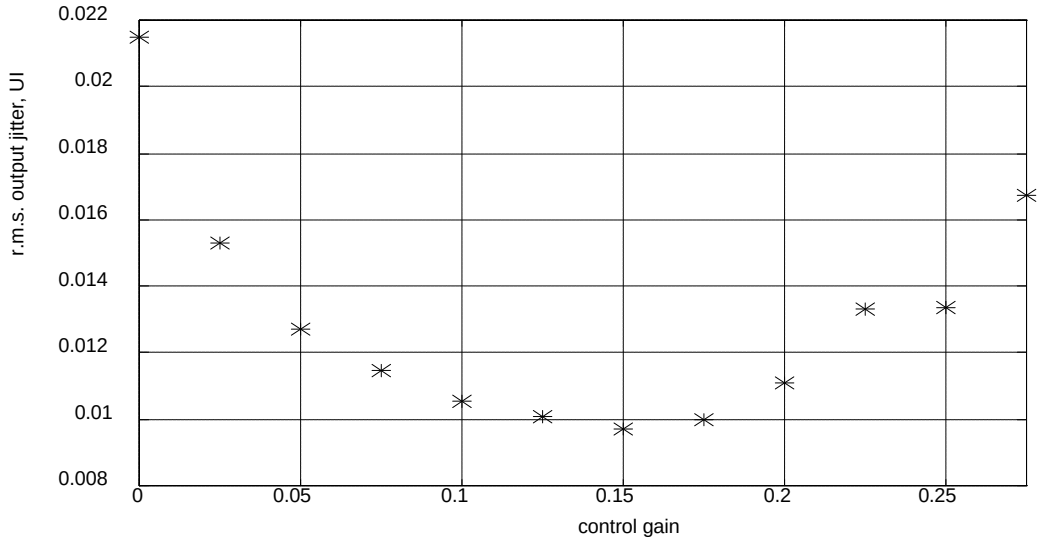

Fig. 7. Rms value of the output jitter as a function of the control gain G.

In Tab. 3 the results of simulations in terms of the output jitter as functions of control gain for three values of prefilter detuning (δ=0, 0.05, 0.125) are listed.

	G = 0	G = 0.05	G = 0.1	G = 0.15	G = 0.2	G = 0.25
$\delta = 0$						
r.m.s.	0.0215	0.0127	0.0105	0.0097	0.0111	0.0134
max.	0.0512	0.0358	0.0320	0.0334	0.0396	0.0328
$\delta = 0.05$						
r.m.s.	0.0255	0.0163	0.0180	0.0177	0.0155	0.0118
max.	0.0723	0.0424	0.0408	0.0398	0.0340	0.0414
$\delta = 0.125$						
r.m.s.	0.0376	0.0294	0.0264	0.0234	0.0190	0.0171
max.	0.1016	0.0837	0.0648	0.0556	0.0471	0.0450

Tab. 3. Maximum output jitter and rms jitter as functions of normalised detuning and control gain G.

As the detuning is increased, the control gain required to achieve the minimum output jitter is increased as well. We have evaluated the percentage of time (Toff/Ttot) and the maximum number of subsequent bits Nb while the PLL is open as functions of control gain G for the worst case of prefilter detuning (δ = 0.125). In the worst case (G=0.25) the PLL remains in the Track state for about 66% of the total time, and the maximum number of subsequent bit in the Hold state is 40. At the bit-rate under consideration, they correspond to 40 ns which seems to be a short time with respect to time constants of 1/f noise of the VCO.

	G = 0	G = 0.05	G = 0.1	G = 0.15	G = 0.2	G = 0.25
Toff/Ttot	0	0.0868	0.1670	0.2321	0.2862	0.3335
Nb	0	21	27	35	37	40

Tab. 4. Duty-cycle of the control signal TH (Toff/Ttot) and maximum number of bits Nb with PLL in the Hold state.

Conclusion - In this paper a new architecture for Clock Recovery Circuits has been presented. A preliminary analysis aimed at separating useful signals from noise sources in the protoclock has been necessary. A low-pass type control signal has been found to be the equivalent of the protoclock itself in terms of SNR and it is available in the symmetry protoclock. By using this control signal together with a Charge-Pump PLL, a

complete scheme of the CRC has been found, and it requires only minor modifications to the basic structure. Computer simulations have shown that the CRC proposed here is capable of reducing the output jitter in the presence of strong phase modulations without reducing the bandwidth of the PLL. Further investigation will be carried out to take the phase-noise contribution of the VCO into account.

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