Dual Op Amp, LDO Regulator with Power Supply Gain Suppression for CMOS Smart Sensors and Microsystems

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***Abstract*—In CMOS smart sensors and microsystems it can be very convenient to integrate both analog and digital circuits in the same chip; since the supply voltage for high-accuracy, high-precision interfaces should be as immune from disturbances as possible, low drop out regulators are often necessary. Here we show a CMOS, dual op amp, fast, low drop out regulator which allows to diminish the power supply gain by orders of magnitude up to very high frequencies.**

I. INTRODUCTION

In CMOS smart sensors and microsystems it is generally very convenient to integrate both analog and digital circuits into the same silicon chip; however, since in many cases the limited accuracy and precision of the electronic interface [1] critically affect the accuracy and precision of sensors, it can be necessary to supply the analog interface circuitry with a pre-regulated voltage, which should be as immune to disturbances as possible. Linear regulators are often the best solution to this problem; nevertheless, in deep sub-micron, low voltage, low power CMOS systems cascading two regulators for improving the power supply rejection can be problematic or impossible; it is therefore extremely important to design linear regulators which have both a low drop out and a low power supply gain up to high frequencies; the most popular CMOS low drop-out (LDO) regulator is shown in Figure 1. As an advantage, in comparison with other applications, in CMOS smart sensors and microsystems, the load of the LDO regulator is generally known with relatively little uncertainty; as we shall show, this information may allow to reduce the power supply gain by orders of magnitude up to very high frequencies.

Linear regulators use feedback; in fact, though on one hand feedback may introduce stability issues, on the other hand it permits, *if there is enough loop gain,* to relate the accuracy [1] of the closed loop system to the accuracy of the feedback network, rather than to the accuracy of parameters of active devices. However, in sub-micron CMOS circuits it can be difficult to design amplifiers with *enough loop gain*. First, low supply voltages make cascode techniques problematic; second, short channel effects reduce the dynamic drain-to-source resistances of MOSFETs. Both the aforementioned difficulties result in a lower gain per stage; if the gain per stage is limited, it is still possible to achieve a large loop gain by cascading more amplification stages; however, multistage have their own disadvantages, including a more complex frequency compensation [2-4]. An alternative approach is using, instead of a single op amp, more op amps so that their combination makes the circuit more accurate; in practice, many (relatively) "poor" op amps can cooperate for producing an accurate output signal (this idea is very old and has been named *composite amplifier* [5,6]). Traditionally, *composite amplifiers* have been used for merging the good qualities of two *different* op amps; as an example, a proper combination of an ultra-fast op amp and of a low-offset op amp may result in the same accuracy given by an hypothetic ultra-fast, low-offset op amp. However, the need for high accuracy analog CMOS circuits led to a different application of the same idea: two nominally *identical* op amps implement a single, high-accuracy amplifier; the resulting *replica amplifiers* [7,8] can compensate the finite op amp gain (gain enhancement); in practice, the gain enhancement would be limited by "op amp mismatch"; moreover the circuits [7,8] could not compensate the input offset voltages, even if they were matched (this is an important aspect, see later). Recently we proposed the circuits [9-15] which employ two nominally *identical* op amps for compensating both the finite op amp gain and (matched) input offset voltages; furthermore, we have shown that "op amp mismatch" can be effectively compensated by applying the dynamic element matching to the entire op amps; however, the resulting dynamic op amp matching technique still requires switching and is therefore only suitable for low frequency systems (*e.g.* many electronic interfaces for sensors). If accuracy is important up to rather high frequencies, we have suggested to use a dual amplifier strategy with a proper tuning for compensating the mismatch between the two amplifiers

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[16]; in particular, we applied this general approach to the design of a dual, CMOS, low voltage, low drop out linear regulator for smart sensors. However, the previously reported regulator only achieved an extremely low power supply gain (below -100dB) at rather low frequencies; here we show that the same circuit topology (see Figure 2), with a completely different design strategy, allows to keep the power supply gain at rather low levels up to very high frequencies.

II. Low Drop-Out Regulators for Deep Sub-Micron CMOS Systems

A. CMOS LDO

Figure 1 shows the classic low drop-out regulator (LDO). The regulator has been designed in the HCMOS9 0.13µm process from ST Microelectronics. The reference and the supply voltage are, respectively, *0.8V* and *1.2V*. The required maximum load current is *12.5mA* (enough for many system-on-chip applications). Although LDOs typically use large load capacitors (so that the pole associated to the output node is dominant), fully integrated CMOS LDOs cannot use *off-chip* capacitors. For this reason we have used the simple, single stage current mirror op amp shown in Figure 3 as the error amplifier; a resistor R_M and a small capacitance C_M are added between the gate and the drain of the PMOS power transistor (Miller compensation with cancellation of the right half plane zero); clearly, the cascode output stage of the error amplifier slightly increases the minimum output voltage of the error amplifier and, therefore, slightly reduces the maximum current capability of the LDO regulator; this is not an issue as in most CMOS microsystems the maximum current required from the regulator may be in the *mA* range. Table I summarizes the parameters of the CMOS LDO.

B. CMOS dual op amp LDO

The CMOS dual op amp regulator [16] is constituted by a *main regulator* (*MR*) and by an *auxiliary regulator* (*AR*) which interact through the compensation resistors (R_{C1},R_{C2}); assuming ideal matching, if op amps and transistors are replaced by their correspondent linearized models, it can be shown that the dual regulator compensates both the finite loop gain and "matched" input offset voltages. In practice, first, the compensation resistors (R_{C1},R_{C2}) and the two op amps should be well matched (the latter is, of course, more problematic); second, if the width of M_A is *n* times smaller than the width of

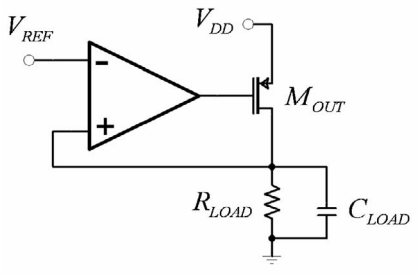

Figure 1. Classic low drop out regulator (LDO).

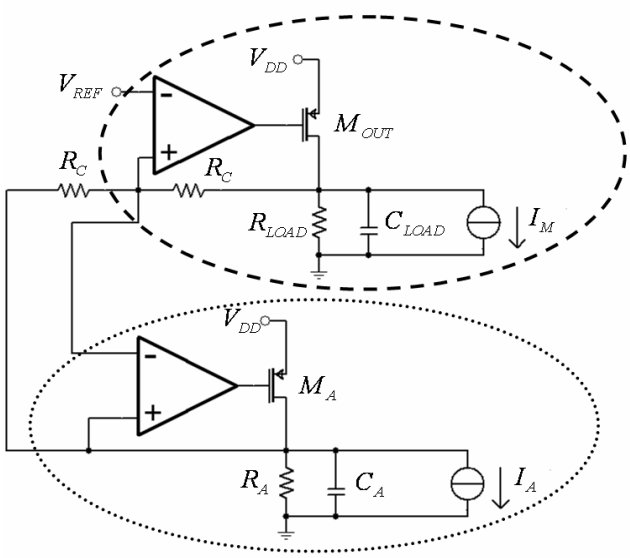

Figure 2. Dual op amp LDO (the *main regulator, MR,* is encircled by a dashed line; the *auxiliary regulator, AR,* is encircled by a dotted line).

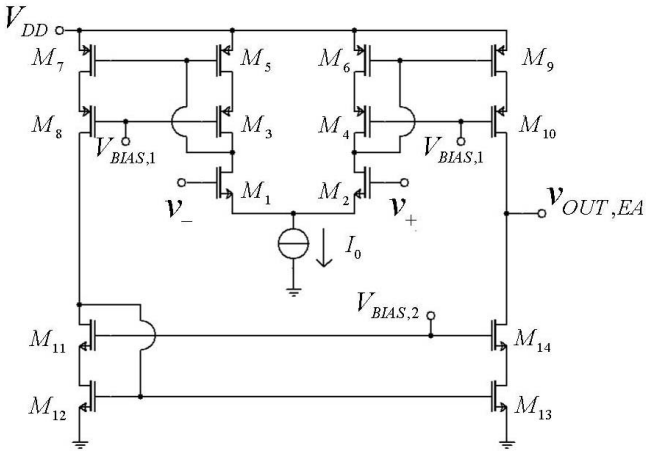

Figure 3. Single stage, current mirror op amp used as the error amplifier in both the classic and the dual op amp LDO.

TABLE I.

Parameters of the classic LDO and of the dual op amp LDO			
Parameter	***Value***	***Parameter***	***Value***
w_{n1}, w_{n2}	$26\mu m$	$R_{C1} = R_{C2}$	$5k\Omega$
w_{p3}, w_{p4}, w_{p5}, w_{p6}, w_{p7} w_{p8}, w_{p9}, w_{p10}	$20\mu m$	R_{LOAD}	$> 64\Omega$
w_{n11}, w_{n12}, w_{n13}, w_{n14}	$10\mu m$	C_{LOAD}	$100pF$
w_{OUT}	$65\mu m$	C_M	$1pF$
L *(all transistors)*	$0.13\mu m$	R_M	$5k\Omega$
I_0	$150\mu A$	n	10

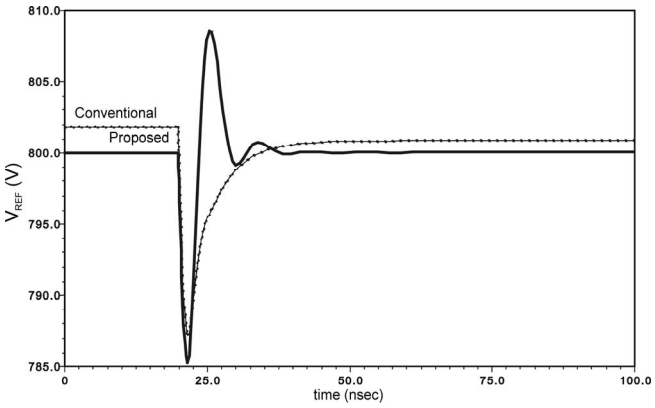

Figure 4. Transient response after a sudden load change.

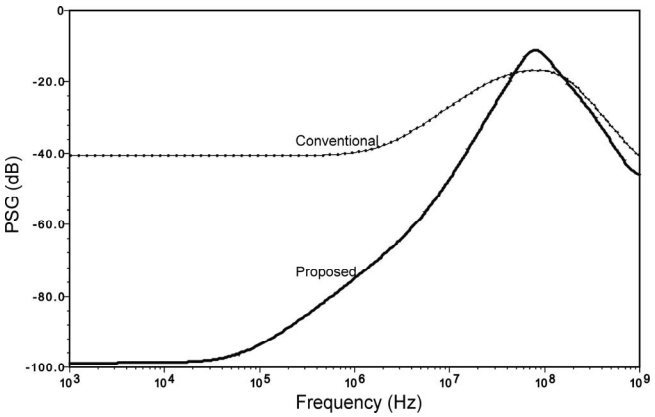

Figure 5. Power supply gain in ideal matching conditions

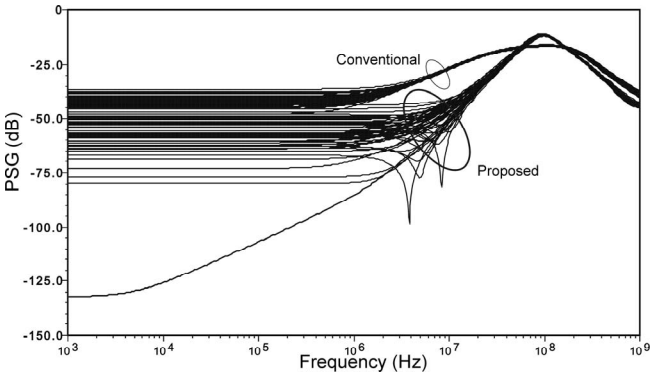

Figure 6. PSG of the dual op amp LDO regulator (MonteCarlo simulations before tuning).

M_{OUT}, R_A and C_A must be made, respectively, n times bigger than R_{LOAD} and n times smaller than C_{LOAD} ($n>1$ is important for power efficiency; the condition on capacitors is far less important as the pole associated with C_A is non-dominant). These "load conditions" would be impractical in many LDOs (where the *off-chip* load is often unpredictable), but are hardly a problem in CMOS smart sensors and microsystems (where the load is *on-chip*). The current sources (I_M,I_A) are necessary if proper operation must be guaranteed even when the load resistor (and accordingly, the auxiliary resistor) are very large [16]; this is not an issue as those currents are so small that very low currents suffice (much smaller than the quiescent current of the regulator). For the CMOS implementation, beside the modifications (according to the previous discussion) due to the choice *n=10,* two identical LDO regulators are used as the *main regulator* and as the *auxiliary regulator*; each error amplifier is identical to the error amplifier used in the standard LDO regulator (see Figure 3 and table I).

The proposed dual op amp regulator allows to suppress the power supply gain by orders of magnitude up to very high frequencies. In fact, if we consider the simple regulator shown in Figure 1, we recognize that the op amp and the following gain stage (M_{OUT},R_{LOAD}) may be regarded as a single op amp; with reference to this op amp, a variation of the supply voltage will result in $\Delta V_{off,in} = (\Delta V_{DD}/p)$, where p is the low frequency $PSRR_{VDD}$ of the op amp. In the proposed regulator, if the $PSRR_{VDD}$ of the two op amps (including the additional gain stages) are "matched", they will result in two "matched" variations of their input equivalent offset voltages; such "matched" variations are, however, compensated by the circuit topology. Clearly, the same discussion applies for high frequency variations of the supply voltage; it is therefore important to match the $PSRR_{VDD}$ of the two op amps (including the additional gain stage) up to high frequencies.

Although stability is ensured, transient analysis shows some ringing, which may be eliminated if the *main regulator* is made enough slower than the *auxiliary regulator* by increasing its compensation capacitor [16]; this choice is, however, non optimal for reducing the power supply gain at high frequencies; in fact, with different compensation capacitors, the $PSRR_{VDD}$ of the two op amps would not match at high frequencies. For this reason, (different from [16]) here we suggest to use identical compensation capacitors; though some ringing may occur, this could be acceptable in most practical cases (e.g. Figure 4 shows the transient response to a sudden load change). Figure 5 shows that, if mismatch is not taken into account, the PSG of the proposed regulator would be extremely low up to very high frequencies. Figure 6 shows Montecarlo simulations; if the PSG at low frequencies must be minimized, mismatch compensation is mandatory.

C. Tuning

In order to match the $PSRR_{VDD}$ of the two op amps, we can "tune" the transistor M_{13} by integrating an array of transistors ($M_{13,1}$,$M_{13,2}$,...,$M_{13,N}$) *nominally identical* to M_{13} (for our simulations N was equal to 64) and subsequently selecting the best transistor from the array. This is a different application of the tuning approach we already used in [16] (redundancy for improving the accuracy was first introduced in [17-20]). Figure 7 shows that tuning M_{13} gives almost the same PSG as with ideal matching; in fact, these simulations demonstrate that, *if the load is approximately known,* the high frequency PSG of the proposed regulator can be significantly better than the PSG of state-of-the-art commercial LDO regulators. Figure 7 shows that, if a second transistor can be tuned, the DC error of the regulator can also be tuned. If the variations of the load current are applied to both the load and the auxiliary load connected to M_A, the load regulation ($\partial V_{OUT}/\partial I_{LOAD}$, i.e.

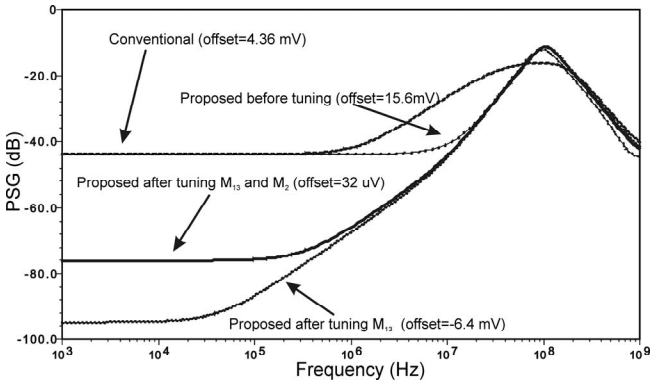

Figure 7. PSG of the dual op amp LDO regulator (before and after tuning).

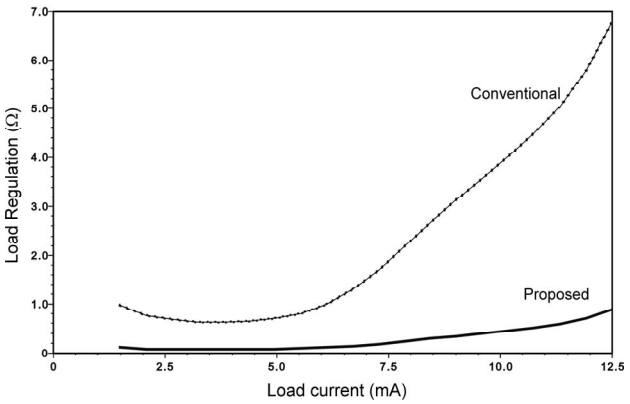

Figure 8. Load regulation of conventional and proposed LDO regulators.

output resistance) can also be significantly improved, as shown in Figure 8; otherwise (the load current changes and the current through the auxiliary load does not), the load regulation of the proposed regulator would be very close to the load regulation of the conventional LDO.

In principle, automatic tuning could be implemented (see [17-20,16]). We mention that, since M_{13} is a relatively small transistor, our tuning strategy is area efficient.

III. CONCLUSIONS

Here we have proposed a dual op amp, low drop out linear regulator for CMOS smart sensors and microsystems, which, in comparison with classic LDOs, permits to suppress the power supply gain by orders of magnitude up to very high frequencies. Transistor level simulations confirm theoretical results and demonstrate that, *if the load is approximately known,* our circuit performs significantly better than state-of-the-art commercial low drop out regulators. The presence of two op amps in our circuit results in a slightly larger output noise (approximately, the *rms* output noise voltage is increased by a factor $\sqrt{2}$). As to power consumption, at very light load, when the quiescent currents dominate, power consumption is approximately doubled; if the load current dominates and the ratio *n* (between the output power transistor and an auxiliary transistor) is enough large, power consumption is only slightly increased. Since our tuning strategy is area efficient, the chip area occupied by the dual op amp LDO would not be significantly increased if the area is dominated by the power transistor and the ratio *n* is enough large.

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