A 20-dB 200-MHz CMOS SINGLE-TO-DIFFERENTIAL AMPLIFIER

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Abstract. In this communication a novel CMOS amplifier providing a differential gain higher than 20 dB and a cut-off frequency of 200 MHz is presented. The circuit includes a single-to-differential input converter that, unlike traditional approaches, avoids reducing the very high input resistance of the main differential amplifier. Moreover, thanks to an auxiliary section, an extra 6-dB gain is achieved. The whole amplifier has been designed with a 0.8-μm *p*-well technology and uses a supply voltage of 3 V.

I. Introduction

Fully differential approach is usually required in high-frequency applications [1-5], due to its attractive and well-known properties of immunity to common-mode disturbances, rejection to parasitic couplings and increased dynamic range [6-7]. However, there are cases in which a single-ended source comes from an external filter although the differential approach must be preserved into the chip. Examples are the circuits, which are placed in cascade to RF image filters and IF filters. In addiction, there are circuits, such as four-quadrant multipliers, that require pure differential signals to perform their function. In all these cases, a stage able to convert a single-ended signal into a differential one is needed.

A differential pair with one grounded input terminal can perform this basic function, if the symmetry of the output is not the main goal. At this purpose, to provide a proper bias condition to the differential pair, the most common solution is that of using the R-C network around the main amplifier as shown in Fig. 1. For sufficiently high frequencies (where capacitor C can be assumed short-circuited) the gain of the amplifier is therefore

$$A = \frac{V_{out}}{V_{in}} = -g_{m1,2} R_{1,2} \tag{1}$$

where g_{mi} is the transconductance of the *i*-th transistor. The main drawback of this approach is represented by the heavy reduction of the input resistance of the amplifier. This can represent a serious problem in many applications. Additionally, the use of high values of resistance R is area consuming

and worsens the noise performance of the amplifier. Moreover, as the frequency increases, the *CMRR* decreases causing in turn a reduction in the symmetry of the output.

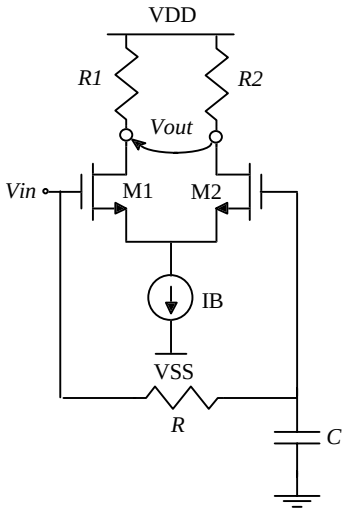

Fig. 1. Single-input differential-output amplifier with traditional input biasing

II. Proposed Solution

To overcome the previously mentioned limitations**,** the arrangement in Fig. 2 was developed.

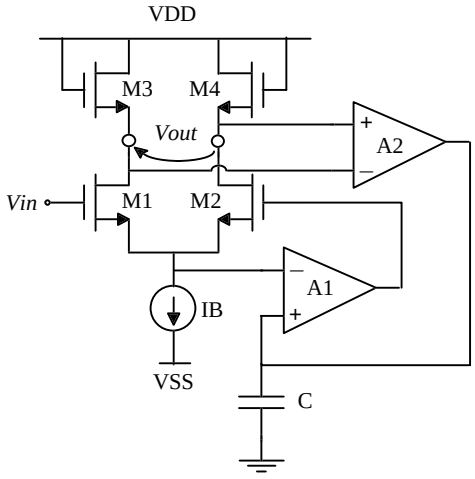

Fig. 2. Simplified schematic of the proposed amplifier

Observe that IF CMOS stages can profitably take advantage of active loads based on diode-connected transistors. Indeed, unlike bipolar transistors, amplifier gains which are set by the ratio of MOS transconductances of transistors with different dimensions can provide values higher than 20 dB at hundreds megahertz operating frequencies [8]. The DC condition of circuit in Fig. 2 is now accurately set by the auxiliary amplifier A2 which senses any deviation of the output voltage from zero, properly driving A1 and, in turn, the gate of M2. This feature reduces the output offset and compensate for any parameter mismatching in the differential stage. On the other hand, for frequencies where capacitor *C* can be assumed as short-circuited, the auxiliary amplifier A2 gives a virtual ground on the source of the coupled-pair M1-M2. More specifically, assuming a finite differential gain for A1 equal to A_1 and denoting with r_B the output resistance of current generator IB, the voltage at the gate of M2 is

$$V_2 = \frac{g_{m1}A_1}{g_{m1} + \frac{1}{r_B} - g_{m2}(1+A_1)} V_{in} \approx -\frac{g_{m1}}{g_{m2}} \frac{A_1}{(1+A_1)} V_{in} \tag{2}$$

Thus, if A_2 >>1 and $g_{m1} = g_{m2} = g_{m1,2}$, , a signal about equal to V_{in} but with a phase shift of 180° is provided to the gate of M2. This feature allows an extra 6-dB gain to be achieved. In fact the gain is now given by

$$A = -2\frac{g_{m1,2}}{g_{m3,4}} \tag{3}$$

The detailed schematic of the amplifier is shown in Fig. 3, where the auxiliary amplifiers were implemented with simple differential stages with mirror active load, and where a common drain transistor, M5, with the associated bias current generator IB2 was introduced for level-shifting purposes.

A final observation concerns the stability of the loop made up of A1, the main amplifier and M5. Let r_{o1} and C_{o1} be the equivalent output resistance and capacitance at the output of A1, respectively, and C_s the total capacitance at the source of M1-M2. By breaking the loop at the gate of M5 and restoring the load conditions we find the expressions of the loop gain, $T_o = g_{m6,7} r_{o1}/2$, the dominant pole, $\omega_1 = 1/r_{o1}C_{o1}$, and the second pole $\omega_2 = 2g_{m1,2}/C_s$. Hence, to achieve a given phase margin, ϕ, we have to set $\omega_{GBW} = \omega_2/\tan\phi$, that is

$$C_{o1} = \tan\phi \frac{g_{m6,7}}{g_{m1,2}} C_s \tag{4}$$

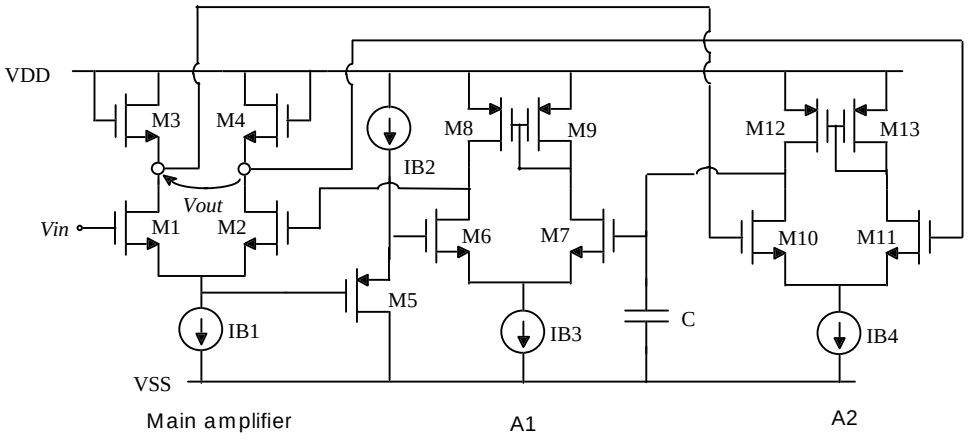

Fig. 3. Detailed schematic of the proposed amplifier

III. Simulations

The circuit in Fig. 3 was simulated with SPICE using the parameters of a 0.8-μm *p*-well technology. The supply voltage was set to 3 V. Transistor dimensions and bias currents are reported in Tab. I. The loop stability was ensured with these settings. Only an additional 1-pF capacitor was connected between the gate and source of transistor M5, to provide a feed-forward compensation.

Fig. 4 illustrates the frequency responses of the complete solution in Fig. 3 and that of the amplifier in Fig. 1. For the latter the same settings as in Tab. I were chosen. Moreover, R = 10 kΩ and

C = 10 pF was set. It can be observed that the proposed amplifier achieves a gain of 21.5 dB which is 6-dB higher than that in Fig. 1. The high cut-off frequency is higher than 200 MHz. The flat band with a gain variation of 0.5 dB ranges between 10 to 80 MHz (being the lower limit due to the chosen capacitor value of 10 pF). For the same two circuits, Fig. 5 illustrates the *CMRR*' defined as $CMRR' = \left| V_{o,dm} / V_{o,cm} \right|$, where $V_{o,dm}$ and $V_{o,cm}$ is the differential- and common-mode output voltage, respectively. For almost all the frequency range of interest the circuit in Fig. 3 exhibits a better *CMRR*' with a maximum difference of about 95 dB at 70 MHz.

Tab. I. Circuit Parameters

Parameter	Value
M1 M2	30/0.8
M3 M4	3/0.8
M5 M6 M7	20/0.8
M8 M9 M12 M13	6/0.8
M10 M11	2/0.8
IB1	80 μA
IB2 IB4	20 μA
IB3	160 μA
C	10 pF

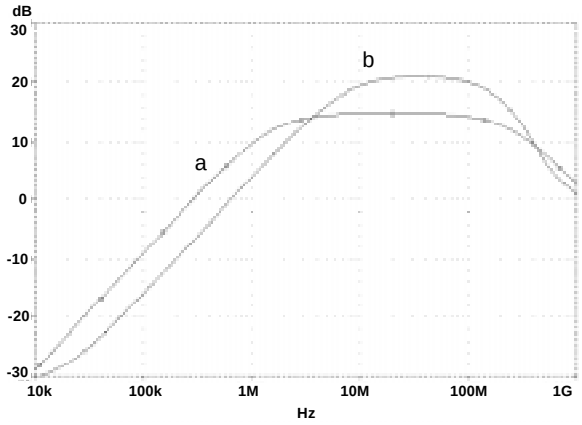

Fig. 4. Module of the frequency response for circuits in Fig. 1 (curve a) and Fig. 3 (curve b)

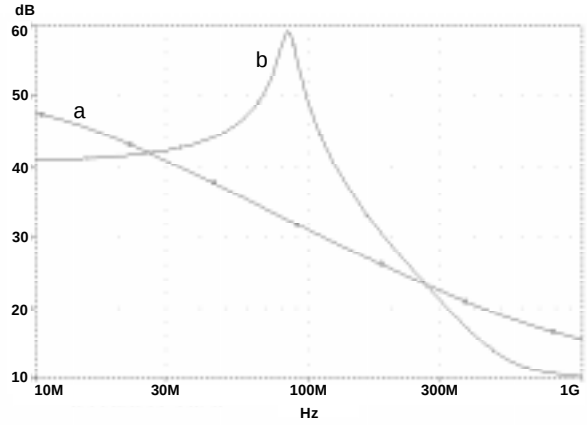

Fig. 5. *CMMR*' for circuits in Fig. 1 (curve a) and Fig. 3 (curve b)

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