Tekhnê
January - June 2020, Vol. 17, No. 1, pp. 69 – 75

ISSN 1692-8407

Configurable digital PWM for simple projects

PWM digital configurable para simples proyectos

Hector J. Centeno R.[1] and Gustavo A. Parra P.[2]
[1]Facultad Tecnológica, Universidad Distrital Francisco José de Caldas, Bogotá, Colombia
hjcentenor@correo.udistrital.edu.co
[2]Facultad Tecnológica, Universidad Distrital Francisco José de Caldas, Bogotá, Colombia
gaparrap@correo.udistrital.edu.co

This paper presents the software implementation of an adjustable PWM (Pulse Width Modulator) prototype, developed in Verilog code, which functions as a training tool at the undergraduate level, or for the development of small projects. At the schematic level, the prototype presents the main module called PWM which integrates three modules (frequency, useful cycle, and display), as a complement to carry out results under the conditions specified in the functional profile. The base module integrates combinational and sequential circuits, i.e. counters, comparators, flip flops, function generators, etc. The final results obtained by simulation show the expected behavior in terms of frequency setting, duty cycle, and display.

Keywords: Digital circuit, hardware description, PWM, Verilog

Este artículo presenta la implementación, en cuanto a software, de un prototipo de PWM (Modulador por Ancho de Pulso) ajustable, desarrollado en código Verilog, que funcione como herramienta de formación en el ámbito de pregrado, o el desarrollo de pequeños proyectos. En cuanto a esquema, el prototipo presenta un módulo principal llamado PWM el cual integra tres módulos (frecuencia, ciclo útil y display), como complemento para llevar a cabo resultados bajo las condiciones especificadas en el perfil funcional. La base de los módulos integra circuitos combinacionales y secuenciales, es decir contadores, comparadores, Flip Flops, generadores de funciones, etc. Los resultados finales obtenidos por simulación muestran el comportamiento esperado en cuanto a ajuste de frecuencia, ciclo útil y visualización.

Palabras clave: Circuito digital, descripción por hardware, PWM, Verilog

Article typology: Research

Received: June 9, 2020
Accepted: June 16, 2020

Research funded by: Universidad Distrital Francisco José de Caldas (Colombia).

How to cite: Centeno, H., Parra, G. (2020). *Configurable digital PWM for simple projects*. Tekhnê, 17(1), 69 -75.

Introduction

Pulse width modulation (also known as PWM) of a signal or power source is a technique in which the duty cycle of a periodic signal (sine or square, for example) is modified, either to transmit information over a communications channel or to control the amount of power sent to a load (Cooper & Stowe, 2018; Zope et al., 2012).

Some machines require partial or variable power. In the past, control (such as in a sewing machine foot pedal) was accomplished by using a rheostat connected with the motor to adjust the amount of voltage flowing through the engine. It was an inefficient scheme since this energy is also lost as heat in the resistance element of the rheostat but is tolerable because the total power was low. While the rheostat was one of several power control methods, a low-cost and efficient power switching adjustment method was still to be found. This mechanism also had to be capable of controlling fan motors, pumps, and robotic servos, and it had to be compact enough to interface with dimmers. The PWM emerged as a solution to this complex problem (Posada Contreras, 2005).

The main advantage of PWM is that the power loss in switching devices is shallow. PWM also works well with digital controls, which, due to its on/off nature, can easily adjust the duty cycle when necessary (Martínez & Gómez, 2007). PWM has also been used in some communication systems. For example, its duty cycle has been used to transmit information through a communication channel or even to control LED lamps in artistic visual schemes. Another application is to send data in an analog way. It is helpful to communicate analogically with digital systems.

The main disadvantage of PWM circuits is the possibility of radio frequency interference. However, these can be minimized by locating the controller close to the load and filtering the power supply (Zope et al., 2012).

Currently, there are many integrated circuits in which PWM modulation is implemented, in addition to other very particular ones to achieve functional circuits that can control switched-mode power supplies, motor controls, thermoelectric element controls, choppers for sensors in noisy environments, and some other applications. Companies such as Texas Instruments, National Semiconductor, Maxim, and others are known for manufacturing this type of integrated circuits (Zope et al., 2012).

For a digital system, it is relatively easy to measure how long a square wave lasts. However, suppose you do not have a digital-analog converter. In that case, you cannot get information from an analog value since you can only detect if there is a specific voltage, 0 or 5 volts, for example (digital values of 0 and 1), with a certain tolerance. Still, you cannot measure an analog value. However, with a digital oscillator, a counter, and an AND gate as a pass gate, the PWM could quickly implement an ADC (Zope et al., 2012).

Reduced costs of power electronic devices, increased reliability, efficiency, and power capacity, and lower development times, along with more demanding application requirements, have driven the development of several new inverter topologies recently introduced to the industry, particularly voltage converters. However, the new, more complex inverter topologies and fields of application are accompanied by additional control challenges, such as voltage unbalances, power quality issues, higher efficiency needs, and fault-tolerant operation, which necessarily require the parallel development of modulation schemes. Therefore, recently, there have been significant advances in the field of DC/AC converter modulation, which conceptually has been dominated for the last decades almost exclusively by classical PWM pulse width modulation methods (Leon et al., 2016).

The PWM technique is one of the most widely used strategies to control the AC output of the power electronic converter (Posada Contreras, 2005). In this technique, the duty cycle of the converter switches can be varied at a high frequency to achieve a low-frequency average output voltage or current (Peddapelli, 2017).

The different PWM techniques considered are Carrier Overlap PWM (CO-PWM), Variable Frequency PWM (VF-PWM), Phase Shifted PWM (PS-PWM), Alternate Phase Opposition Layout PWM (APOD-PWM), Phase Layout PWM (PD -PWM), Phase Opposition Layout PWM (POD-PWM) (Deepa et al., 2017).

Problem Statement

An adjustable PWM is a device capable of generating signals with which it is possible to control the frequency and duty cycle in motor drives, MCU, control-related circuits (PWM attenuation), speed regulation applications, etc. Among the main features of adjustable PWMs in the market are; frequency and configurable duty cycle, among others. However, the frequency range of most commercial devices starts from 1Hz, i.e., there is no adjustable PWM in the market with a frequency range below 1Hz as a starting point with which it can be practiced studiously.

Due to the academic necessity of wanting to control on many occasions experimentally, the energy that is taken to a load or to send information dynamically and under certain specific conditions in a digital circuit and as a consequence of the non-commercialization of PWMs with specific characteristics of operation, the exigency arises to implement an autonomous control system for the control of an adjustable PWM with which it is possible to explore digital circuits to low frequencies.

It is for such reason that this project will develop a sufficient theoretical methodology for the future implementation of an adjustable PWM. In such an adjustable PWM, the student will be able to control and visualize

the frequency range, and the duty cycle will be able to accommodate the PWM settings. Moreover, it will be able to obtain a second output relative to the inverse value.

The following (Fig. 1) is the state diagram of the adjustable PWM. In this case, and according to the logic, there is an initial state that represents the possibility of being able to increase or decrease the frequency and the duty cycle, change between these two states using the Set pushbutton or perform a Reset to the system. Resulting in a signal on display and, at the same time, a signal on the outputs.

The PWM frequency must be configurable between 1 kHz and 10 MHz. For this purpose, two push buttons and a display must be incorporated. One push button should increase the frequency value, and the other should decrease it. The values are to be shown on display. The system must incorporate a display to show general system information, including settings such as this. The increments and decrements must allow the frequency to be set and, at the same time, be functional.

The duty cycle should be controlled with another pair of push buttons, and the information should be displayed. The increments and decrements, in this case, should be every 10% of the maximum value (i.e., every 0.1).

Adjustments to the PWM should be implemented by pressing another push button called SET. All push buttons must incorporate software anti-bounce systems. In addition, the system must have a second output corresponding to the inverse value of the PWM (Q).

Research Method

The design of this PWM is based on the development and implementation of combinational, sequential circuits in which four modules are included and programmed; a display module, a frequency inverter module, and a duty cycle turner module.

The main variable PWM module contains the frequency, duty cycle, and display modules, it has the function of processing and integrating all the signals according to the frequency, and duty cycle settings entered and delivering two signals, one signal according to the configuration, and the other signal is the same but negated (Figs. 2 and 3).

The frequency module (Fig. 4) receives the increment and decrement signals from 1 kHz to 10 Mhz and delivers a signal to the duty cycle module according to the increment or decrement selection and delivers a signal to the display module to visualize the selection. If the frequency module sends a signal to the duty cycle module indicating an increment, that signifies that the clock must decrement; if it sends a signal to the duty cycle module indicating a decrement, it signifies that the clock must increment.

In general terms, the frequency module works as a divider, which using comparators is constantly comparing the present state of the clock signal through the maximum frequency obtained of 100 MHz to obtain more minor frequencies, utilizing a clock and a counter which counts the rising edges of the 100 MHz signal, according to the setting, this makes it change the low signal to a high signal, for example for a frequency of 1 kHz (minimum frequency supported) we have:

$$R = \frac{100MHz}{1KHz} = 100000 \tag{1}$$

This result is divided in two:

$$R = \frac{100000}{2} = 50000 \tag{2}$$

This means that we must create a counter that counts up to fifty thousand edges, changes from a low signal to a high signal, counts the period for a 1 kHz signal, and restarts. The approach we will use is to look at the maximum period observed and search for that in all possible starting periods.

The frequency variator integrates, of course, anti-rebound modules that will enable the elimination of the fluctuations created by the push buttons. A conditional was placed where a variable changes its value when the pushbutton is pressed. That is when it is in LOW. After the variable has its new value and the pushbutton is released, the desired action is performed in the module.

The duty cycle is the ratio of how long each cycle is HIGH versus how long it is LOW. So to change the duty cycle of the PWM signal, we would need to divide the time of each cycle by something other than 50/50. So, for example, to increase the duty cycle of the signal we have been working with, too, say, 75%, we need to make the HIGH delay time longer than the LOW delay time.

The duty cycle module (Fig. 5) is configured to receive, on the one hand, the decrement and increment signal of the desired cycle and the output signal of the frequency module that will serve as the base signal for the adjustment of the duty cycle, with the adjustment of the cycle basically what is intended is to know what percentage of the frequency signal is to be used.

The internal structure of this module contains anti-reboot, comparator, and counter sub-modules. The display module (Fig. 6) allows the visualization of the frequency, duty cycle, and set and reset signals. It receives the signal from the frequency and duty cycle module, indicating the frequency and duty cycle range in current status. The structure of the display module is composed of four multiplexers, gates, and memories.

Results and Discussion

Simulation results are obtained by ModelSim software. The Verilog codes are synthesized in Xilinx ISE, and the simulation is carried out in ModelSim, which provides

Figure 1

State diagram.

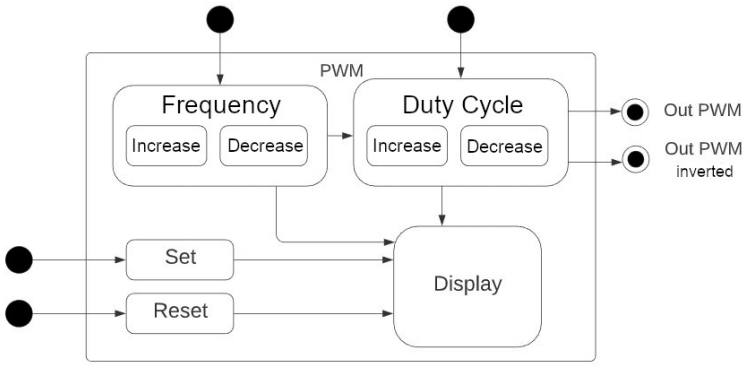
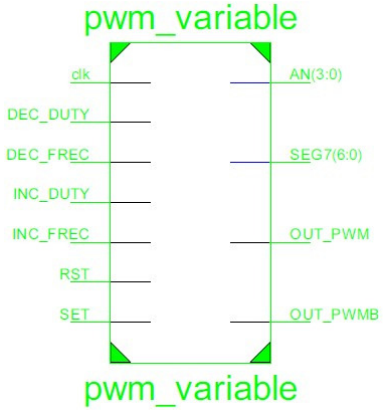


Figure 2

PWM module (schematic diagram).



the design output developed for each system's operating conditions.

Once the programming and synchronization of all the modules in the variable PWM system were done, the frequency test at 1 kHz and 10 MHz and the duty cycle increment and decrement test were performed. The simulation results are shown in Figs. 7 to 10.

Conclusion

This project is the development of a PWM module of low cost and wide versatility as a working tool for students in the area of electronics and digital control of electrical machines. The academic approach of the tool is supported by a fast, simple, and economical implementation, suitable for undergraduate students. The objective is to describe and implement the system using Verilog, evaluating its performance through simulation. The software adjustable PWM prototype is developed according to the conditions indicated in the design profile. From the performance tests, it was determined that the system operates as expected. However, at low frequencies, there is the possibility of having an error in thousandths of a second concerning the period of the signals, which is within the expected range of operation of the system. The prototype should be complemented with a system that guarantees its safe operation considering its use by students.

Acknowledgements

The authors thank Prof. Fredy Martínez for his guidance in this theoretical and practical learning process and the Universidad Distrital Francisco José de Caldas for his support in the development and testing.

References

Cooper, M., & Stowe, R. (2018). Chemistry education research: From personal empiricism to evidence, theory, and informed practice. *Chemical Reviews*, *118*(12), 6053–6087. https://doi.org/10.1021/acs.chemrev.8b00020

Deepa, K., Kumar, P., Krishna, V., Rao, P., Mounika, A., & Medhini, D. (2017). A study of comparative analysis of different pwm techniques. *2017 International Conference On Smart Technologies For Smart Nation (SmartTechCon)*, 1144–1149.

Leon, J., Kouro, S., Franquelo, L., Rodriguez, J., & Wu, B. (2016). The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics. *IEEE Transactions on Industrial Electronics*, *63*(5), 2688–2701.

Martínez, F., & Gómez, D. (2007). Fuzzy logic controller for boost converter with active power factor correction. *7th International Conference on Power Electronics ICPE*, 936–940.

Figure 3

State diagram (block detail).

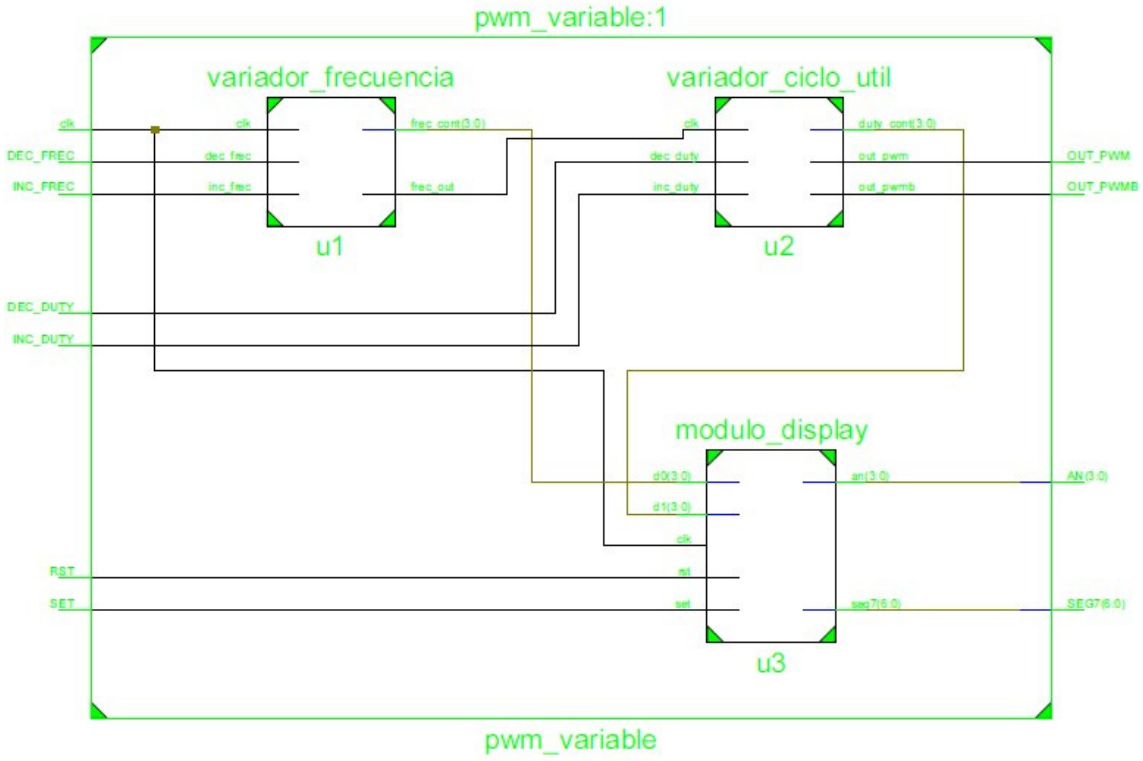


Figure 4

Frequency module.

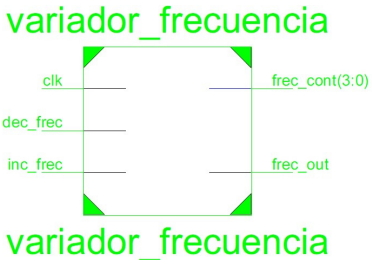


Figure 5

Duty cycle module.

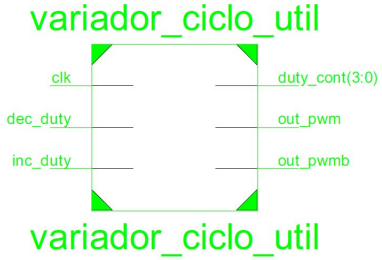
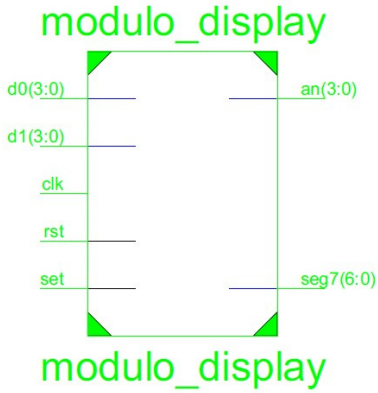


Figure 6

Display module.



Peddapelli, S. (2017). *Pulse width modulation: Analysis and performance in multilevel inverters*. De Gruyter Oldenbourg.

Posada Contreras, J. (2005). Modulación por ancho de pulso (pwm) y modulación vectorial (svm). una introducción a las técnicas de modulación. *El*

Figure 7

Frequency at 1 kHz.

Figure 8

Frequency at 10 MHz.

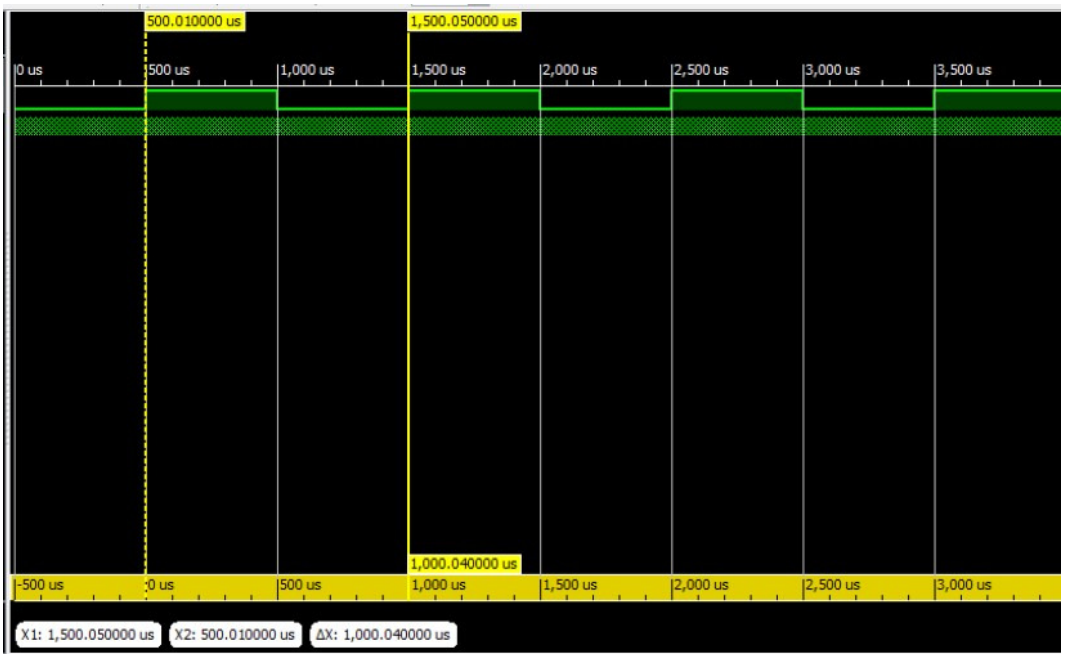


Figure 9

Increase of duty cycle.

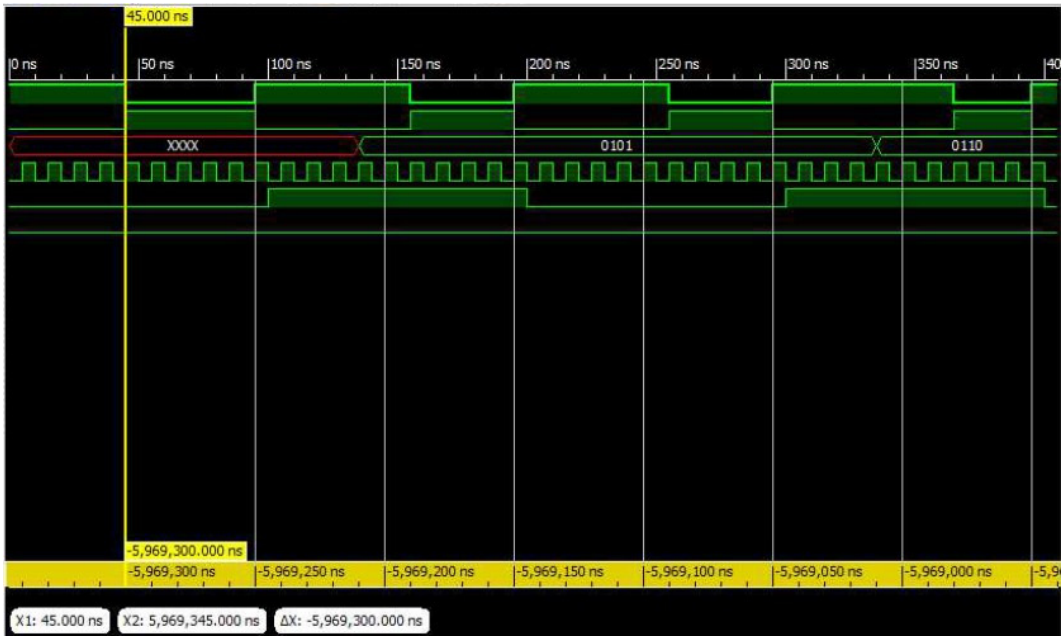
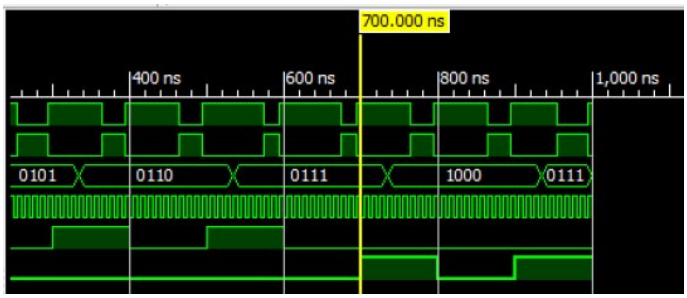


Figure 10

Decrease of duty cycle.



Hombre y la Máquina. https://www.redalyc.org/articulo.oa

Zope, P., Bhangale, P., Sonare, P., & Suralkar, S. (2012). Design and implementation of carrier based sinusoidal pwm inverter. *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, *1*(4), 230–236.