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Data acquisition systems with intelligent trigger capability

L. Angrisani [a,1], P. Daponte [b,2], S. Sangiovanni [c,*]

[a] Dip. di Informatica e Sistemistica, Università di Napoli Federico II, via Claudio 21, 80125 Napoli, Italy
[b] Facoltà di Ingegneria, Università del Sannio, Palazzo Bosco Lucarelli, Piazza Roma, Benevento, Italy
[c] Dip. di Ing. Elettrica, Università di Roma "La Sapienza", via Eudossiana 18, 00184 Roma, Italy

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Abstract

Two data acquisition systems, based on two solutions for improving the performance, are here presented. The first one, fully analog, is able to generate a voltage impulse at the occurrence of a transient phenomenon on the stationary waveform being monitored. In the second system the acquisition process is regulated by absolute value of the derivative of the signal under analysis. This system is realized with Field Programmable Gate Array technology.

All theoretical relations underlying the proposed solutions are first discussed. Their most relevant hardware and software features are then described. A suitable measurement apparatus is set up for assessing the performance of both solutions, and the obtained results are finally given.

Keywords: Data acquisition systems; Intelligent trigger capability; FPGA

1. Introduction

Nowadays, high performance and reliable data acquisition systems (DAS) able to meet a wide range of application requirements are more and more demanded [1–3]. The required performance is expressed in terms of not only maximum sampling frequency, resolution and memory depth but also intelligent triggering capability and real-time compression of acquired samples.

The first group of features has recently gained significant improvements thanks to the advances in system technology; DAS size and weight reduction, recording period extension and analog-to-digital conversion reliability are notable.

On the other hand, intelligent triggering capability and real-time compression seem to be less investigated; they are strictly required in those apparata susceptible to gather great amounts of data in order to reduce the size of their temporary and permanent memories. As an example, data loggers for power quality analysis are only able to collect large amounts of data related to the monitored signals;

* Corresponding author. Tel.: +39 06 44585509; fax: +39 06 4883235.
E-mail addresses: angrisan@unina.it (L. Angrisani), daponte@unina.it (P. Daponte), silvias@elettrica.ing.uniroma1.it (S. Sangiovanni).
[1] Tel.: +39 081 7683170; fax: +39 081 7683816.
[2] Tel.: +39 0824 305817; fax: +39 0824 21866.

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both great memory availability and off-line tedious operations to extract from the recorded data the information of interest, are thus required [4,5]. The same, with small differences, is true for biomedical signal acquisition and analysis [1].

In these cases, solutions able to grant both optimised acquisitions and memory saving are strongly advisable.

Two cost-effective solutions characterised by intelligent trigger capabilities, and oriented to substantial memory savings are presented in the paper.

The first one is an analog circuitry able to furnish a short-time voltage impulse at the occurrence of non-stationary phenomena superimposed on the stationary input signal. The obtained impulse can serve as a trigger for the acquisition to start only in presence of signals of interest avoiding the storing of meaningless samples.

The second solution is a digital apparatus, based on Field Programmable Gate Array (FPGA) architecture [6], which adopts an original strategy for managing the acquisition process. The beginning of the acquisition process is regulated by the absolute value of the derivative of the signal under analysis; in particular, a trigger is originated if the current, absolute value of the derivative is either greater or lower than a fixed threshold.

The two apparata can be seen as both an alternative pair and a complementary pair to be included and made operative into high performance DASs.

As an alternative pair, they both can be specialized to fulfil the same task, such as the management of an acquisition process aiming at the collection only of the samples related to that region of the stationary waveform affected by a transient phenomenon.

As a complementary pair, each of them can be addressed to a specific and different task; the analog solution may play the same role described before, the digital solution, on the other hand, may start the acquisition process whenever the current, absolute value of the derivative of the monitored signal goes below a fixed threshold (slowly variable signals).

After the description of all theoretical relations governing the proposed solutions, their architecture is presented in detail highlighting common and different features. Many experiments are, then, carried out in order to assess their performance as both an alternative pair and a complementary pair.

2. The analog solution

2.1. The basic idea

The analog circuit proposed is capable of signalling the occurrence of transient disturbing phenomena superimposed on the stationary waveform monitored.

A short-lived voltage impulse is provided as output whenever the following relation is satisfied:

$$|V(t) - V_r(t)| > \alpha, \tag{1}$$

$V(t)$ is the input signal, $V_r(t)$ is a stationary waveform free from disturbances, characterised by amplitude A, and used as reference, and α is a fraction of A. The criteria underlying the previous relation is clearly sketched in Fig. 1. The solid line stands for the monitored signal $V(t)$ (as an example, a sinusoidal voltage on which some transient disturbances are superimposed); the two dashed lines represent the sum between the reference stationary waveform $V_r(t)$ (a pure sinusoidal voltage) and a d.c. voltage the value of which is respectively equal to $+\alpha$ (upper) and $-\alpha$ (lower). Any excursion of $V(t)$ above the upper dashed line or below the lower dashed line (e.g. events P, Q, and R) is detected.

It is worth observing that the value of α determines the sensitivity of the detection algorithm; the lower the value of α the higher the assured sensitivity. Moreover, this value has properly to be regulated according to the signal-to-noise ratio of the input signal in order to prevent undesired detection due essentially to noise.

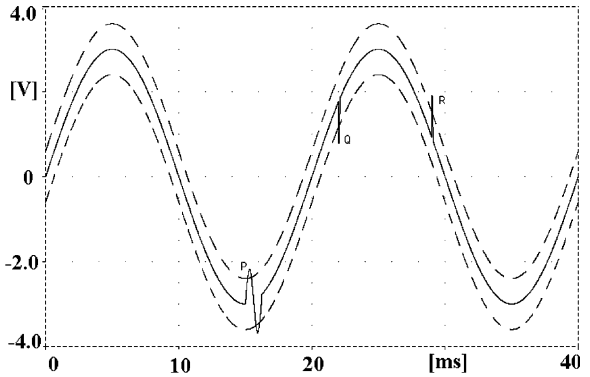

Fig. 1. The solid line represents a sinusoidal voltage on which three transient disturbances are superimposed: P, Q, and R. The two dashed sinusoidal lines are the boundaries given by Eq. (1).

2.2. Reference voltage generation

The voltage impulse is produced by suitably conditioning the signal obtained from the difference between the monitored signal $V(t)$ and the reference voltage $V_r(t)$ (Fig. 2).

Many solutions for generating $V_r(t)$ can be found in literature. Some of them exploit sophisticated oscillating circuits [7], other of them try to delay all the spectral contents of the same input signal $V(t)$ for 360° thus comparing two successive periods of $V(t)$, the actual one and the previous one [8]. With regard to the first solutions, only sinusoidal reference voltages can be generated; in addition, locking the phase of the so obtained $V_r(t)$ to that of $V(t)$ is often a difficult matter. As for the second solutions, all periodical transient disturbances cannot be detected because they do not appear from the comparison of successive periods.

To overcome these limitations, the suggested solution derives $V_r(t)$ by low-pass filtering the monitored signal $V(t)$. Before evaluating the difference, $V(t)$ is delayed for the same amount induced on $V_r(t)$ by the low-pass filter; this is accomplished by means of an all-pass filtering process. It is worth noting that both filters can suitably be designed according to the characteristics of the transient disturbances to be detected. The whole operation is sketched in Fig. 3.

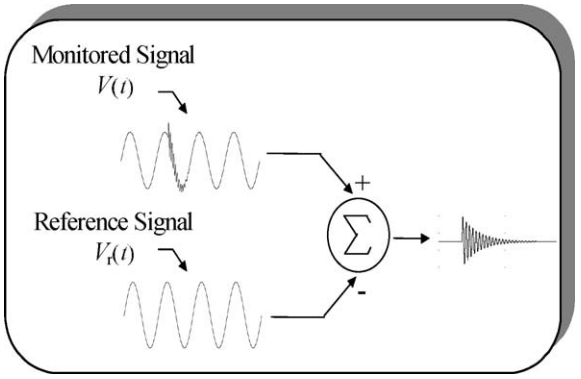

Fig. 2. The difference between $V(t)$ and $V_r(t)$ is utilised for generating a short-lived voltage impulse mandated to signal the occurrence of a transient phenomena.

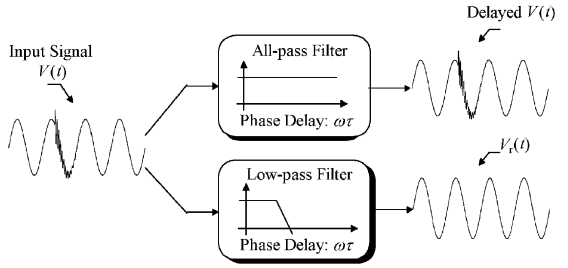

Fig. 3. $V_r(t)$ is generated by low-pass filtering the input signal $V(t)$. $V(t)$ is delayed for the same amount introduced by the low-pass filter in order to properly establish the difference between itself and the obtained reference signal.

2.3. The proposed circuitry

The block diagram of the proposed circuitry is shown in Fig. 4.

After the input stage for the generation of the reference voltage, the differential amplifier performs the subtraction given in Eq. (1). The two comparators and the logic OR gate implement the remainder of the relation (1). In particular, the output of the upper comparator is high if the following relation is satisfied:

$$V(t) - V_r(t) > \alpha. \tag{2}$$

On the other hand, the output of the lower comparator is high if

$$V(t) - V_r(t) < -\alpha. \tag{3}$$

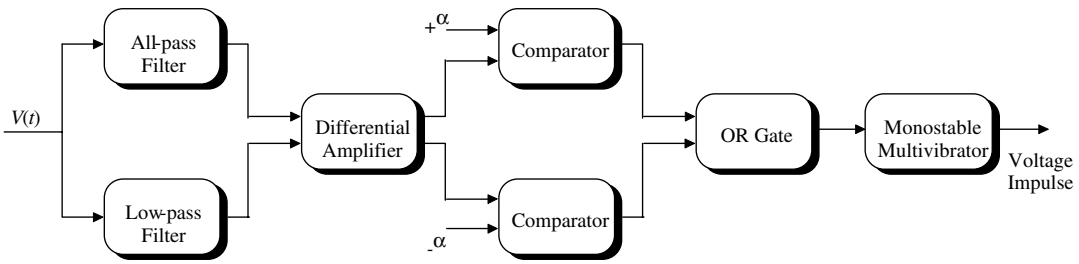

Fig. 4. Block diagram of the proposed circuit.

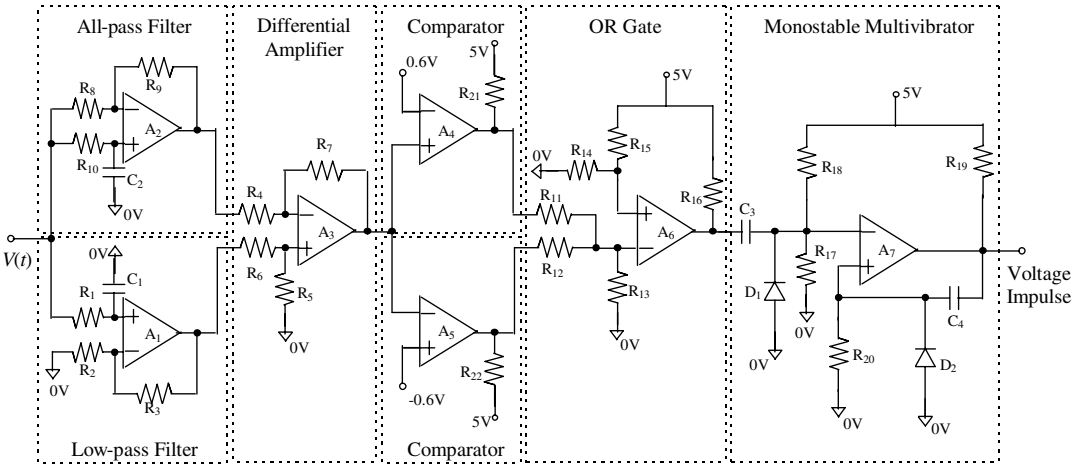

Fig. 5. The analog circuitry for detecting transient disturbances superimposed on a sinusoidal stationary voltage characterised by a frequency value equal to 50 Hz and a peak-to-peak amplitude ranging between 2 and 7 V.

A monostable multivibrator is adopted to assure that the output voltage impulse be always characterised by the same amplitude and polarity whatever the detected disturbance may be. The so obtained impulse can serve for triggering most of common data acquisition systems thus overcoming all problems arising if the shape of the impulse depends on the detected disturbance [8].

An implementation of the described block diagram is depicted in Fig. 5; the list of the adopted components is given in Table 1.

The shown circuitry has been specialised in detecting transient disturbances superimposed on a sinusoidal stationary voltage characterised by a frequency value equal to 50 Hz and a peak-to-peak amplitude ranging between 2 and 7 V. The value of the parameter α has been fixed equal to 0.2 V.

To enhance noise rejection, reduce response times, and avoid undesired detection, both the two filters, low-pass and all-pass, and the differential amplifier are based on low-noise, high speed, and low input offset voltage operational amplifiers.

Moreover, the frequency response of the low-pass filter has been designed with a -3 dB frequency value equal to 70 Hz.

The parameters of the all-pass filter have been chosen in order to assure both the same phase delay at 50 Hz and the same voltage gain granted by the low-pass filter.

The voltage gain of the differential amplifier has been fixed equal to 3; this choice along with the threshold value for both comparators determine the value of the parameter α and, as a consequence, the sensitivity of the circuitry.

With regard to comparators, logic OR gate, and monostable multivibrator, standard circuits have been adopted.

Table 1
List of the components for the circuit in Fig. 5

$R_1 = 22$ kΩ	$R_2 = 50$ kΩ
$R_3 = 12$ kΩ	R_4, R_6, R_{13}, $R_{14} = 1$ kΩ
R_5, R_7, R_{16}, R_{21}, $R_{22} = 3$ kΩ	R_8, R_9, = 33 kΩ
$R_{10} = 9.9$ kΩ	R_{11}, R_{12}, = 100 kΩ
$R_{15} = 200$ kΩ	R_{17}, R_{18}, $R_{20} = 1$ MΩ
$R_{19} = 10$ kΩ	C_1, C_2, = 100 nF
$C_3 = 0.1$ nF	$C_4 = 1$ nF
A_1, A_2 = LF351-National Semiconductor	
A_3 = RC4558-Texas Instruments	
A_4, A_5, A_6, A_7 = LM339-National Semiconductor	
D_1, D_2 = 1N4001-DIODES Incorporated	

3. The digital solution

3.1. The basic idea

The digital apparatus proposed can be thought of as a DAS whose acquisition process is regulated by the current, absolute value of the derivative of the signal under analysis. In particular, both sample acquisition and storing begin whenever one of the following relations is satisfied:

$$\left|\frac{\mathrm{d}}{\mathrm{d}t}V(t)\right| \geqslant \beta_1, \tag{4}$$

$$\left|\frac{\mathrm{d}}{\mathrm{d}t}V(t)\right| \leqslant \beta_2, \tag{5}$$

where $V(t)$ is the signal under analysis and β_1 and β_2 are constant, user-definable values.

Both relations are mandated to focus the acquisition process on significant portions of the input signal $V(t)$. If the relation (4) has to be satisfied, the apparatus (i) detects the occurrence (abrupt increase of the absolute value of the derivative) of transients on the stationary waveform monitored, and (ii) makes the acquisition start in their presence. Relation (5), on the contrary, accounts for collected samples belonging to those portions of the stationary waveform which are not affected by undesired short-lived phenomena. More specifically, relations (4) and (5) show themselves suitable for acquiring portions of the input signal characterised respectively by high-frequency and low-frequency contents.

The sensitivity assured by the digital apparatus is strictly connected to the values of the constant β_1 and β_2 adopted. The greater β_1 the higher the minimum amplitude of transients which can be detected and acquired, spectral contents being equal; the lower β_2 the smaller the minimum amplitude of transients which can be discarded, spectral contents being equal.

Moreover, differently from the analog solution, the sensitivity depends also on the specific location of the transient phenomenon inside the cycle of the monitored waveform. In particular, with reference to a sinusoidal input signal characterised by amplitude A and frequency f, transient phenomena such as impulses and spikes can be detected and acquired if and only if their amplitude B satisfies the following inequality:

$$B \geqslant \frac{\beta_1 T_p}{2\pi} - AfT_p \cos\gamma, \tag{6}$$

where T_p is the time duration of the transient, and γ is the value of the phase angle reached by the sinusoidal signal when the transient occurs. The assured sensitivity gets to its maximum in correspondence to zero-crossings characterised by positive slope; the minimum sensitivity is, in contrast, attained for zero-crossings with negative slope (Fig. 6).

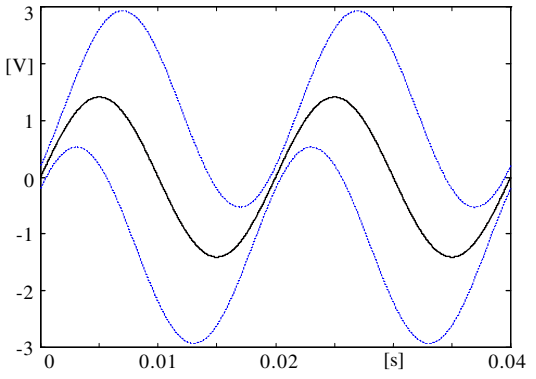

Fig. 6. A sinusoidal input signal (solid) and the boundaries (dashed) given by the relation (6) for $A = 1.4$ V, $f = 50$ Hz, $T_p = 14$ ms, and $\beta_1 = 540$ V/s.

3.2. Design and implementation

3.2.1. Design alternatives

Traditionally, digital signal-processing functions, like those represented by the previous relations (4) and (5), are either implemented in general purpose, programmable digital-signal-processors (DSPs) or built using application-specific integrated circuits (ASICs).

DSPs are essentially microprocessors tuned to digital-signal-processing applications. They are highly flexible because they can be programmed again and again using a familiar high level language like C, thus allowing fast design iterations and reducing time to market. In contrast, DSPs are intrinsically limited in performance; the more is needed to do to a data sample, the more cycles are required and the lower data are processed.

ASICs are chosen for two main reasons: either processing power beyond the capabilities of a general-purpose DSP is required, or production volumes are sufficiently high to justify a custom solution.

Advancements in Field Programmable Gate Arrays (FPGAs) provide new options for digital signal-processing design engineers. The FPGA maintains the advantages both of design flexibility and adaptability of a DSP and custom functionality like an ASIC without their respective limitations [9].

FPGA technology has been enlisted by the authors for setting up the proposed digital apparatus.

3.2.2. FPGA features

FPGAs feature a gate-array-like architecture, with a matrix of logic cells surrounded by a periphery of I/O cells. These commodity parts are customised by downloading a user defined configuration in the form of a binary bitstream, much the same as the loading of a DSP with its program. Segments of metal interconnections are thus linked in an arbitrary manner by programmable switches to form the

desired signal nets between the cells; design and production lead times can awfully be reduced.

To implement a digital signal-processing function in a FPGA device, some sequential stages have to be carried out. For the sake of brevity, they are summarised in the following; further details can be found in [10,11].

1. Design entry through schematics or hardware description languages (VHDLs).
2. Functional simulation for design verification.
3. Design implementation consisting of
   - *mapping*: conversion of schematic symbols and/or VHDL representations into the structures which the target device will consist of;
   - *placement*: the mapped logic blocks are settled into specific configurable logic blocks (CLBs) of the target device;
   - *routing*: connection between the selected CLBs by means of routing resources provided by the adopted FPGA device;
   - *bitstream*: a file is created that can be downloaded into the target device to make it operative;
   - *back annotation*: a representation of the place and routed design is produced including timing data for logic and routing delays.
4. Timing simulation for assessing design performance taking into account back annotation results.
5. Download of the bitstream file into the target device to make it operative.

The aforementioned steps are summarised in Fig. 7.

Fig. 8 shows the flow-engine panel of the design implementation adopted by the authors.

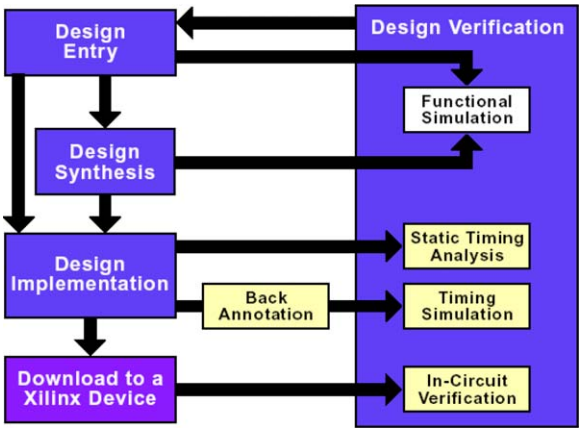

Fig. 7. Steps to implement a digital signal-processing function in a FPGA device.

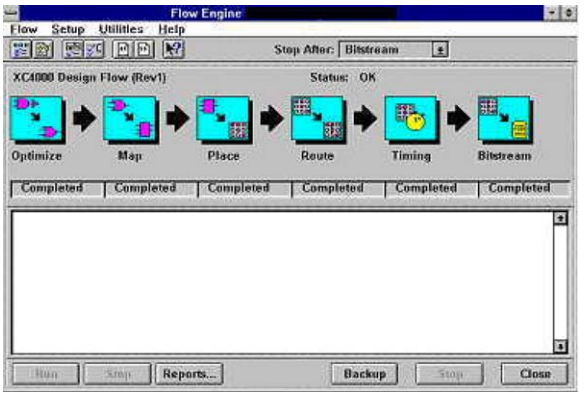

Fig. 8. Flow-engine panel of the adopted design implementation.

3.2.3. The digital apparatus

The chosen FPGA device is the XILINX 4010EPC84-4™. It presents a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). Loading configuration data into its internal memory cells customises the device. The XILINX 4010EPC84-4™ can either actively read its configuration data from an external PROM, or the configuration data can be transferred from an external device. In particular, the FPGA device has been mounted on a Demonstration Board and connected to a personal computer by means of the Xchecher cable.

The characteristics of the XILINX 4010EPC84-4™ are reported in Table 2.

Design stages are performed in the advanced design environment ACTIVE-CAD™. It provides

Table 2
XILINX 4010EPC84-4™ characteristics

Logic cells	Max logic gates	Max. RAM bits	Typical gate range	CLB matrix	Total CLBs	No. of flip-flops	Max. user I/O
950	10,000	12,800	7000–20,000	20×20	400	1120	61

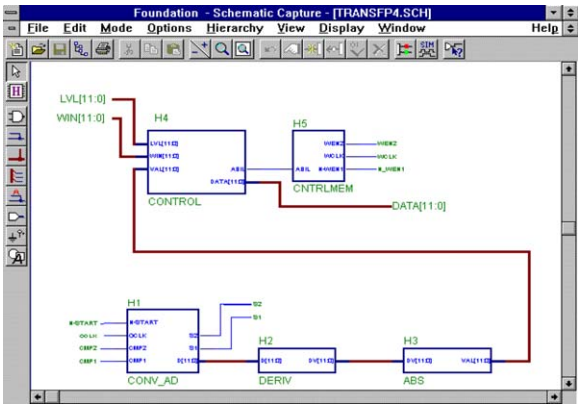

Fig. 9. The schematic of the proposed FPGA apparatus.

front-to-back electronic automation tools for: design entry (either schematic or VHDL), design verification and logic synthesis. The *Project Manager* of the ACTIVE-CAD™ governs the whole design process. It keeps track of design revision levels; the last one will automatically be loaded for customising the FPGA device.

Four fundamental blocks have been designed and implemented in the FPGA device: (a) the digital part of the *A/D conversion*, (b) the *Derivative*, (c) the *Absolute value*, (d) the *Inequality*, and (e) the *Memory control*. The developed schematic is shown in Fig. 9.

With regard both to the *A/D conversion* and *Memory control*, more detailed information has to be provided.

The A/D conversion section is based on a 12 bits SAR A/D converter which consists of (i) a digital part implemented in the FPGA device, and (ii) an

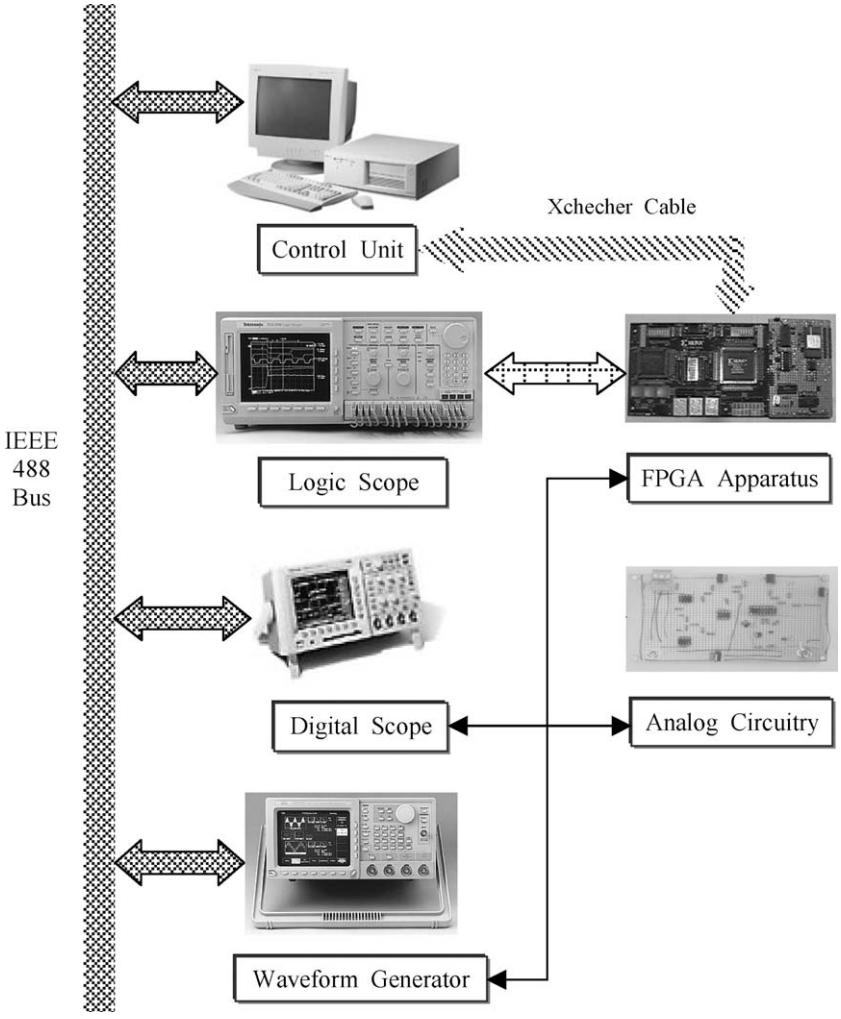

Fig. 10. The measurement apparatus.

external part containing a D/A converter and two comparators.

As for memory banks, the storage capability of a logic scope has been exploited in order to reduce design complexity.

4. Performance verification

4.1. The measurement station

To assess the performance of both solutions, an automatic measurement station has properly been set up. It consists of (i) a control and processing unit, namely a personal computer, (ii) an arbitrary waveform generator, (iii) a logic scope, and (iv) a digital scope. They all are connected by means of a IEEE-488 interface system.

The arbitrary waveform generator is mandated to generate test signals with known characteristics. Each signal consists of a basic stationary waveform on which a transient phenomenon is superimposed. The generated signal is routed to the analog circuitry, the FPGA apparatus, and the digital scope. The digital scope receives the impulse voltage provided by the analog circuitry on its second input channel; the impulse acts like a trigger signal for its acquisition to start. The control unit retrieves the acquisition results produced by both the analog circuitry and FPGA apparatus from the digital scope and the logic scope, respectively. Fig. 10 clearly shows the whole measurement apparatus.

Several test signals have been enlisted for different shapes (sinusoidal, square, triangular) and frequencies of the stationary waveform, and different amplitudes, frequencies and locations inside the stationary waveform cycle of the transients. For the sake of brevity, only some results related to a sinusoidal stationary waveform characterised by a frequency value equal to 50 Hz are presented in the following.

As an alternative pair, both solutions force the acquisition process to collect significant samples only at the occurrence of transient phenomena.

To this aim, the FPGA apparatus has been designed according to the relation (4); in particular, the value of β_1 has been fixed to 2583 V/s taking into account (i) the sinusoidal shape of the stationary waveform, (ii) its frequency value (50 Hz), (iii) the input range of the apparatus (±2.5 V), and (iv) its sampling period (60 μs). With regard to the analog solution, the performance of the hardware prototype previously described in Fig. 5 has been verified.

Figs. 11 and 12 show two significant cases of transients occurring on the sinusoidal waveform; Fig. 11 is related to a voltage dip and Fig. 12 to an oscillatory transient.

Fig. 11 upper and Fig. 12 upper show the acquisition results as displayed by the digital scope. It is worth noting the detection capability of the analog circuitry; a voltage impulse is provided for each transient. In particular, the voltage impulse occurs a bit later with respect to the beginning of the transient; this delay amount, estimated equal about 1 ms, can be compensated by fixing a sufficient pretrigger on the data acquisition system.

Fig. 11 lower and Fig. 12 lower, on the other hand, displays the data collected by the logic scope under the control of the FPGA apparatus; a small pretrigger has been adopted in order to better denote that the acquisition starts at the beginning of the transient.

Many tests have confirmed that each occurrence of transients satisfying the relations (1) and (4) is correctly detected and makes both acquisitions

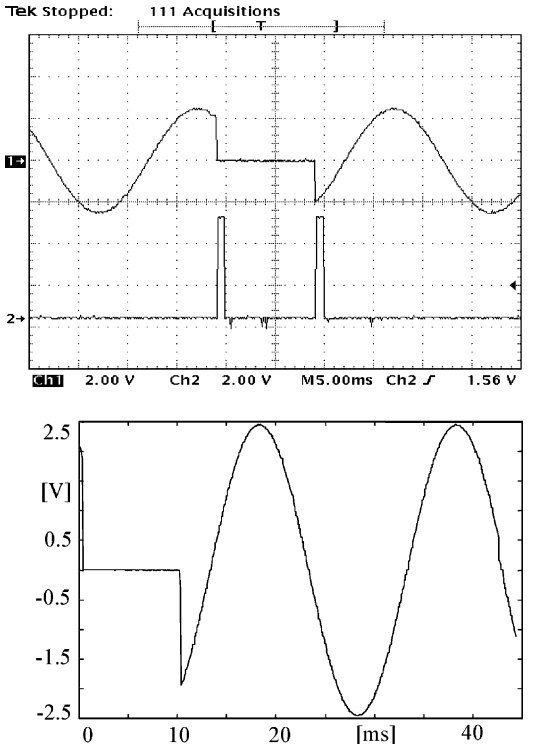

Fig. 11. Acquisition results as displayed by the digital scope (upper) and collected by the logic scope (lower) in the case of a voltage dip.

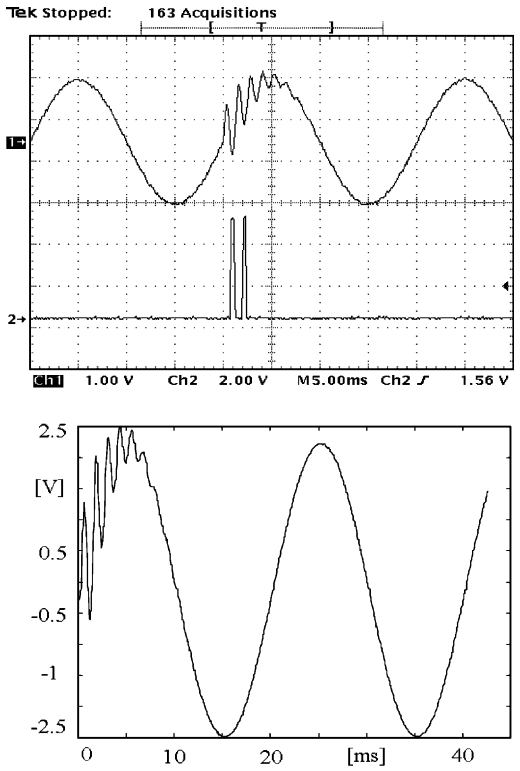

Fig. 12. Acquisition results as displayed by the digital scope (upper) and collected by the logic scope (lower) in the case of an oscillatory transient.

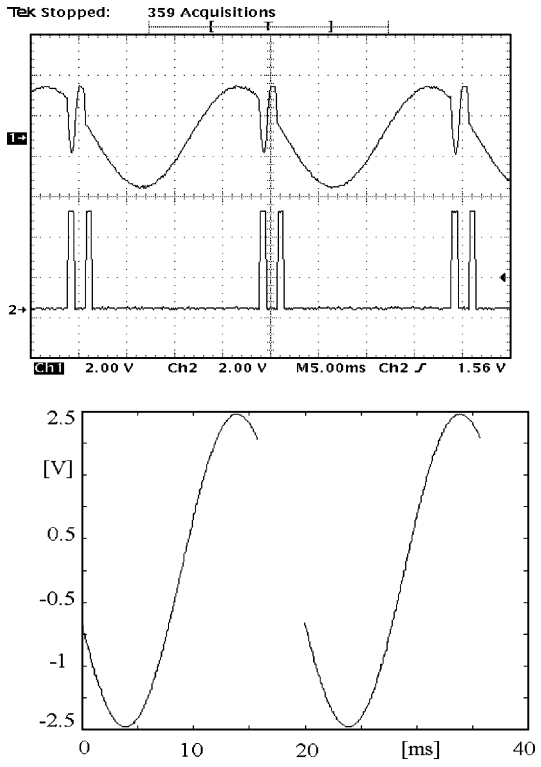

Fig. 13. Acquisition results as displayed by the digital scope (upper) and collected by the logic scope (lower) in the presence of a periodical notch.

start. The performance of both solutions is quite the same.

4.2. Complementary pair

As a complementary pair, each solution has been addressed to a specific task. The analog circuitry plays the same role described in the previous section. The FPGA apparatus, in contrast, manages the acquisition process avoiding those parts of the input signal affected by transients. To this aim, the FPGA device has been customised according to the relation (5); the input range, the sampling period, and the value of β_2 are just the same as before. When the aforementioned relation is not satisfied (as an example, at the occurrence of a transient), a fixed time window of the input signal is discarded. The extent of the time window can be established by the user; its value is equal to 5 ms for the example given below.

A notable case is presented in Fig. 13. A periodical transient phenomenon (notch) has been superimposed on the sinusoidal waveform in order to better highlight the performance of the FPGA apparatus.

Fig. 13 upper shows the acquisition results as displayed by the digital scope; the analog circuitry outputs a voltage impulse whenever the notch occurs. Fig. 13 lower, on the other hand, displays the data collected by the logic scope under the control of the FPGA apparatus. It is worth noting that only the samples belonging to the unaffected portions of the monitored signal have been collected.

The same performance has been experimented in many other tests related to transients the characteristics of which satisfy the relations (1) and (5).

5. Conclusions

Two solutions able to confer intelligent triggering capabilities to traditional data acquisition systems have been proposed. The first solution is completely analog and specialised for detecting transient phenomena superimposed on the stationary waveform under analysis; in particular, an impulse voltage, outputted at the occurrence of the transient, can act as a trigger signal for the acquisition to start. The second solution can initiate the acquisition

process according to a specific value assumed by the current, absolute value of the derivative of the signal being monitored.

Many experiments have been conducted by analysing signals with known characteristics; the obtained performance has been quite good for both solutions.

The on-going activity is oriented to (i) assess the performance of the two solutions both in noisy environment and on actual signals, and (ii) enlarge the set of intelligent trigger conditions.

Referring to this last case, the attention is mostly paid on solutions capable of generating a trigger signal at the occurrence of any variation both of load and harmonic level in electrical power systems. These solutions could be developed taking advantage from more and more powerful FPGA devices, also in analog version.

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