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Adaptive Display Frequency Control for Power Savings

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Abstract:

This publication describes systems and techniques directed at adaptive display frequency control for power savings. In aspects, a display manager can adjust a base frequency and/or a driving frequency of display panel circuitry based on determining a number of operating conditions, including an ambient light condition, a current base frequency and driving frequency, a user interaction with the display, and/or a display brightness. Responsive to determining one or more of these conditions, the display manager can implement a base frequency and a driving frequency that can reduce power consumption and eliminate display artifacts commonly associated with automatic driving frequency transition.

Keywords:

Display panel, active-matrix organic light-emitting diode (AMOLED), active-matrix organic diode, organic light-emitting diode (OLED), display driver integrated circuit (DDIC), frame rate, refresh rate, pixel, pixel array, variable frequency, dynamic frequency, dynamic refresh, self-refresh frequency, power consumption, clock frequency, driving frequency, base frequency

Background:

Many electronic devices (e.g., smartphones) include displays having tens of thousands of pixels. Display panel drivers (e.g., scan drivers, gate drivers, emission-control drivers) in these displays directly control the timing, the luminance, and the color of individual pixels to generate

an image. Such displays may utilize organic light-emitting diode (OLED) technology to provide variable refresh rates and reduced display response times. These features make OLED displays well-suited for electronic devices and are, thus, highly valued by users.

However, under certain operating conditions, displays, including OLED displays, can consume a considerable amount of power. In fact, displays often serve as one of the leading sources of power expenditure in electronic devices. As a result, power-conscious users often operate displays in such a way to reduce power consumption (e.g., low brightness, low refresh rates). For instance, a user of an electronic device may configure an OLED display to be driven at a low refresh rate. Although, such a technique can minimize power expenditure, it may contribute to the presentation of certain display artifacts, including static flicker. In some cases, for example in a low-battery mode, electronic devices are configured to drive displays in such a way to reduce power consumption. For example, an electronic device may be configured to save power by dynamically altering a display refresh rate. Such a device configuration may save power, but this too may result in the presentation of annoying display artifacts, including transitional flickers.

Description:

This publication describes systems and techniques directed at adaptive display frequency control for power savings. In aspects, a display manager can adjust a base frequency and/or a driving frequency of display panel circuitry based on determining a number of operating conditions, including an ambient light condition, a current base frequency and driving frequency, a user interaction with the display, and/or a display brightness. Responsive to determining one or more of these conditions, the display manager can implement a base frequency and a driving

frequency that can reduce power consumption and eliminate display artifacts commonly associated with automatic driving frequency transition (e.g., dynamically adjusting display driving frequencies).

Figure 1 illustrates an example electronic device in which systems and techniques directed at adaptive display frequency control for power savings can be implemented.

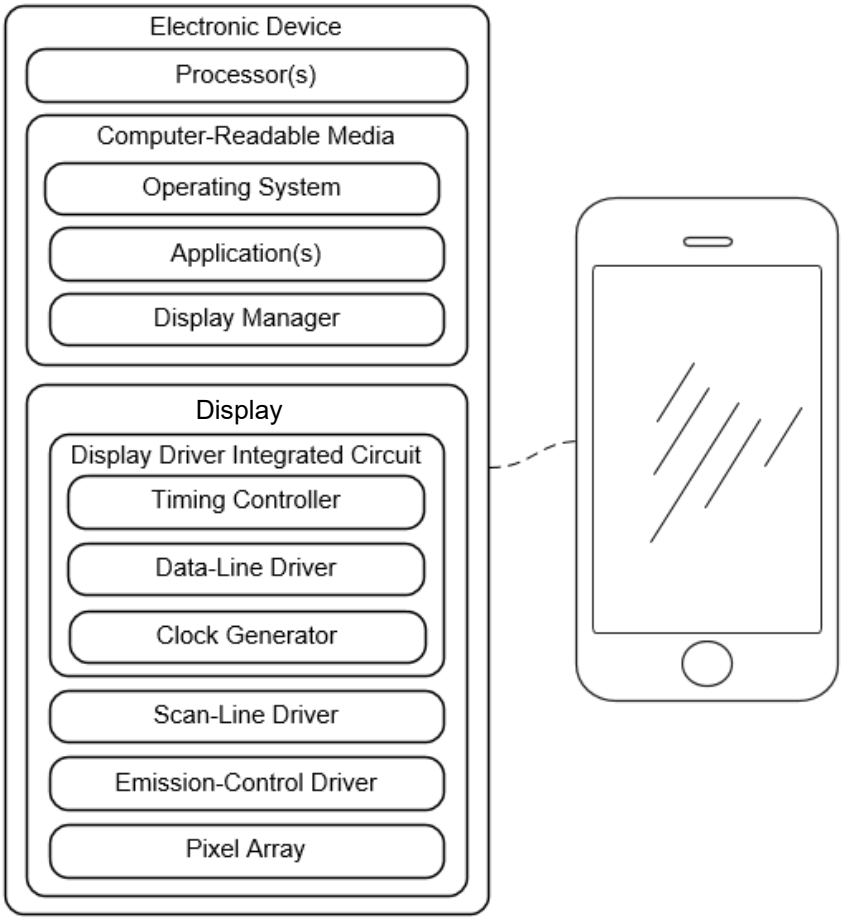

Figure 1

As illustrated in Figure 1, the electronic device is a smartphone. The electronic device may include one or more processors. The processor(s) may be configured to execute instructions or commands stored within a computer-readable media to implement an operating system, application(s), and a display manager (e.g., an algorithm implemented as a set of computer-readable instructions directed at display driving logic). For example, the processor(s)

may execute instructions of the operating system to implement a display refresh rate of 120 Hz. In another example, the processor(s) may execute instructions of the operating system to alter a display brightness. The computer-readable storage media may include one or more non-transitory storage devices suitable for storing electronic instructions, each coupled with a computer system bus.

The electronic device may further include a display (e.g., an organic light-emitting diode (OLED) display). The display may include display panel circuitry having a display driver integrated circuit (DDIC), one or more drivers, and a pixel array of pixel circuits. The DDIC may include a timing controller (e.g., a TCON board) and a data-line driver. The timing controller may provide interfacing functionality between the processor(s) and the drivers (e.g., data-line driver, scan-line driver, emission-control driver). For example, the timing controller can accept commands and data from the processor(s) and generate signals with appropriate voltage, current, timing, and demultiplexing. The timing controller can then pass the signals to the drivers. The drivers may be operably coupled to pixel circuits via driver lines.

As an example, the timing controller may receive display data from a processor (e.g., graphics processing unit) and separate the display data into input signals (e.g., image data, control signals). The timing controller may then pass the input signals to a data-line driver, a scan-line driver, and an emission-control driver. In response, the drivers may pass time-variant and amplitude-variant signals (e.g., voltage signals, current signals) to control the pixel array. The data-line driver may pass data-line signals containing voltage data to the pixel array to control the luminance of an organic light-emitting diode. The scan-line driver may pass a scan-line signal to enable or disable an organic light-emitting diode to receive the data voltage from the data-line

driver. The emission-control driver may supply an emission-control signal to the pixel array. Together, the drivers can control the pixel array to generate light to create an image on the display.

In a configuration, the electronic device may include a DDIC separate from the display. In still other configurations, the electronic device may include a timing controller separate from the DDIC and the display. Additional implementations and components may be configured to control the pixel array and still implement the techniques described herein.

The DDIC may further include a clock generator (e.g., clock circuit, internal oscillator, crystal oscillator), that may produce a constant clock signal oscillating between a high and a low state (e.g., pulses). For example, the clock signal may be in a form of a square wave with a 50% duty cycle. The clock generator may synchronize different parts of the display panel circuitry, including the pixel circuits, via a transmitted clock signal. In at least some implementations, the clock generator may be integral to the timing controller. In additional implementations, the clock generator may be operatively coupled to the timing controller.

In such a configuration, the DDIC can adjust a refresh rate of the display, for example, via the timing controller and/or the clock generator. The display manager, executing on the one or more processors, can instruct the DDIC to implement a specific base frequency. For example, the DDIC can direct the clock generator to produce a clock signal at 60 hertz (Hz), 120 Hz, 144 Hz, and the like. The electronic device operating the DDIC at a higher clock signal frequency may be referred to herein as a “high-speed mode,” whereas a lower clock signal frequency may be referred to herein as a “normal-speed mode.”

The display manager can also be configured to instruct the DDIC to set a driving frequency, for example, by ignoring a pulse of a clock signal (e.g., periodic pulse skipping). In implementations, the driving frequency is a mathematical factor of the base frequency. In one

example, if the base frequency is 60 Hz, then the driving frequency, under the direction of display manager, can be implemented as 30 Hz, 20 Hz, 10 Hz, 1 Hz, and the like.

Experimental data has shown that operating display panel circuitry at lower base frequencies (e.g., the normal-speed mode) and lower driving frequencies result in significant power saving. However, operating a display at these lower frequencies, or even just transitioning a display between high and low frequencies, can result in undesirable display artifacts, including lag, static flickers, transitional flickers, and so on.

To this end, the display manager is configured to provide intelligent, adaptive display frequency control which can reduce power expenditure and minimize undesirable display artifacts. In aspects, the display manager (e.g., via the DDIC) can adjust a base frequency and/or a driving frequency based on determining a number of operating conditions, including an ambient light condition (e.g., from an ambient light sensor), a current base frequency and driving frequency, a user interaction with the display, and/or a display brightness (e.g., a pulse width modulation (PWM) setting). Responsive to determining one or more of these conditions, the display manager can implement a base frequency and a driving frequency that can reduce power consumption and eliminate display artifacts commonly associated with automatic driving frequency transition.

Figure 2 illustrates a logical flowchart depicting example decision logic with which the display manager can determine a base frequency and a driving frequency to reduce power expenditure and eliminate display artifacts.

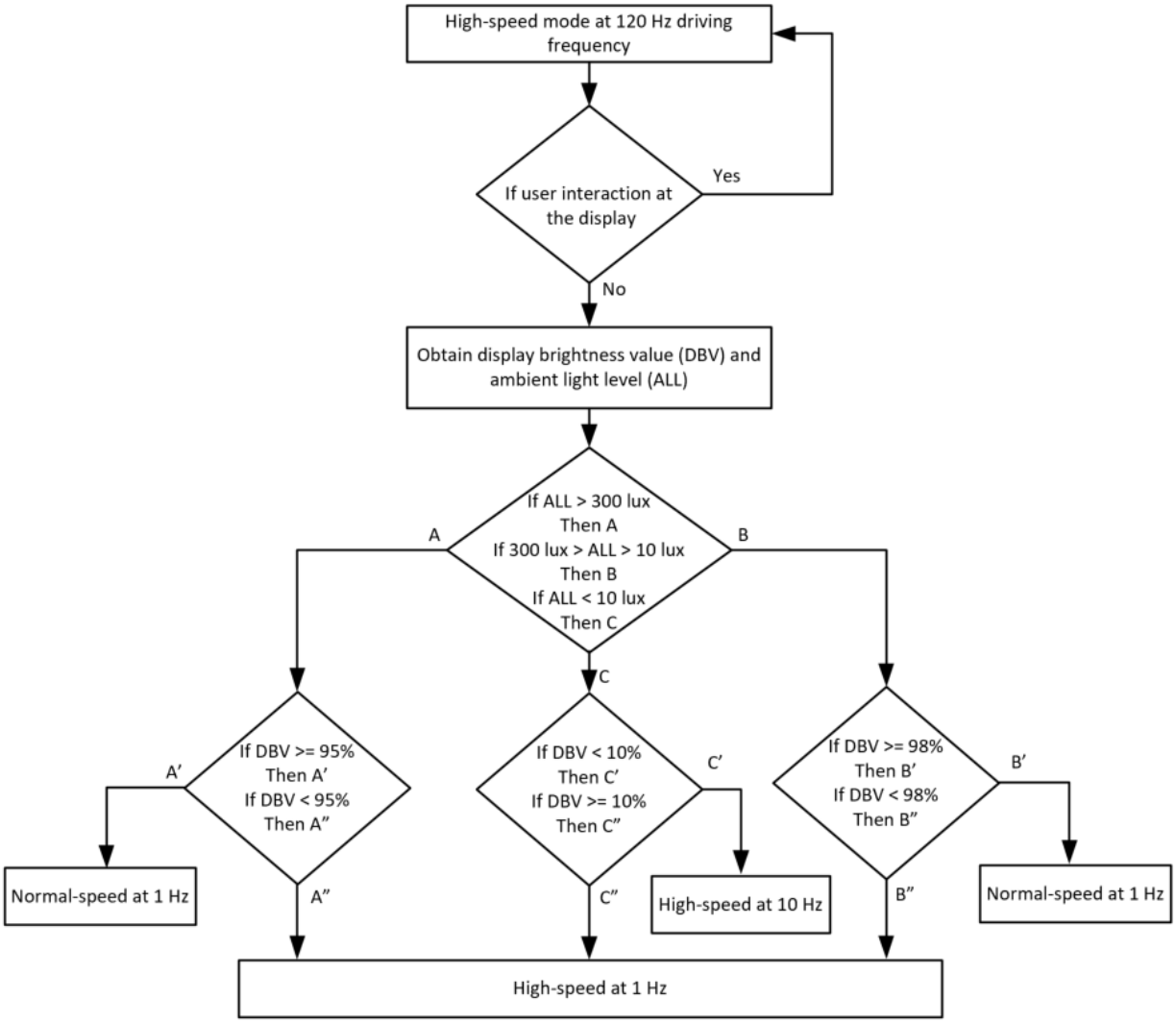

Figure 2

As illustrated, the display manager is configured to operate the display at a high-speed ("HS") mode with a 120 Hz driving frequency. Although this example decision logic presumes a high-speed mode implemented with a 120 Hz base frequency, it should be understood to those skilled in the art that the high-speed mode may be implemented with a 144 Hz, 240 Hz, etc. base frequency. In additional implementations, the driving frequency may be implemented with 144 Hz, 90 Hz, 60 Hz, etc. In implementations, the high-speed mode at the 120 Hz driving frequency may be a default setting, such that at any point when a user interacts with the display (e.g., provides

a scrolling gesture) the display manager may direct the DDIC to implement the high-speed mode with the 120 Hz driving frequency. In this way, a user may not experience a lag when interacting with, for example, a touch-sensitive display. In additional implementations, a timeout feature may be provided to determine a duration since a last user interaction at the display was received.

Further illustrated, if a user interaction at the display is not received, then the display manager may obtain a display brightness value (DBV) and an ambient light level (ALL). At any point during the next steps of the example decision logic, the display manager may obtain an updated DBV and an updated ALL and repeat some or all steps. Further, at any point during the next steps of the example decision logic, the display manager may perform an early exit if user interaction is received.

In aspects, the display manager may be configured to determine if an ALL is greater than, less than, or between a range of values. Example values and percentages are provided in Figure 2 for illustrative purposes and should not be construed as limiting. For instance, if the display manager determines that the ALL is greater than 300 lux (e.g., which may be indicative of an outdoor luminance) then the display manager can determine if the current DBV is greater than or equal to, or less than 95%. Based on the determination, the display manager can then implement a normal-speed ("NS") mode with a 1 Hz driving frequency or a high-speed mode with a 1 Hz driving frequency, respectively. Both of these implementations reduce power expenditure and minimize display artifacts commonly associated with their given operating context. For instance, a display artifact commonly associated with a display operating under normal-speed mode is static flicker. However, this display artifact most frequently manifests when the display brightness is lower than, for example, 95%. As result of the example decision logic, the display manager avoids

the display artifacts and still saves power by implementing normal-speed mode at 1 Hz when the DBV is greater than or equal to 95%.

Likewise, the display manager may be configured to determine if the ALL is less than 300 lux but greater than 10 lux (e.g., between a range of values). If this condition is true, then the display manager can determine if the current DBV is less than, or greater than or equal to, 10%. Based on the determination, the display manager can then implement a high-speed mode with a 10 Hz driving frequency or high-speed mode with a 1 Hz driving frequency, respectively.

Further, the display manager may be configured to determine if the ALL is less than 10 lux. If this condition is true, then the display manager can determine if the current DBV is greater than or equal to, or less than, 98%. Based on the determination, the display manager can then implement a normal-speed mode with a 1 Hz driving frequency or high-speed mode with a 1 Hz driving frequency, respectively.

Based on such decision logic, the display manager can implement a base frequency and a driving frequency to reduce power expenditure and eliminate display artifacts. Such an implementation can result in greater than 30% percent power-savings than conventional techniques.

Figure 3 illustrates a graphical representation of the decision logic that the display manager may utilize to implement adaptive display frequency control for power savings.

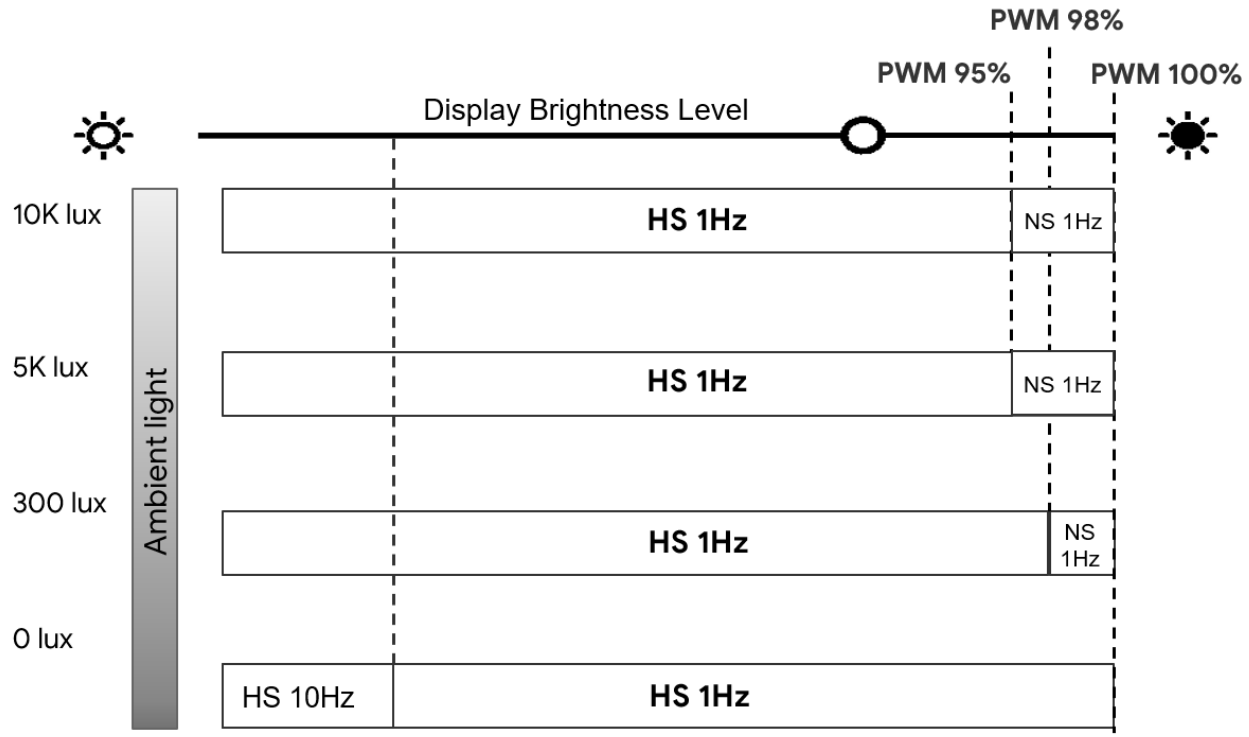

Figure 3

As illustrated, the graphical representation of the decision logic corresponds to the logical flowchart of Figure 2. Again, the values and percentage provided herein are for illustrative purposes and should not be construed as limiting.

The systems and techniques described herein enable adaptive display frequency control for enhanced power savings. In aspects, the display manager, via the DDIC, can adjust a base frequency and/or a driving frequency based on determining a number of operating conditions, including an ambient light condition, a current base frequency and driving frequency, a user interaction with the display, and/or a display brightness. Responsive to determining one or more of these conditions, the display manager can implement a base frequency and a driving frequency that can reduce power expenditure and eliminate display artifacts commonly associated with automatic driving frequency transition.

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