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PIXEL-BASED CONVERSION GAIN SELECTION FOR QUAD-CELL CMOS IMAGE SENSORS WITH IMAGE CALIBRATION AND EXTENDED DYNAMIC RANGE

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ABSTRACT

A Quad Bayer pixel structure is the current driving technology in developing high resolution image sensors with smaller pixel pitch. However, by reducing the pixel size the signal-to-noise ratio (SNR) and the dynamic range (DR) of an image sensor will be compromised. One of the means to improve the SNR and DR for a quad-cell image sensor or other type of complementary metal-oxide semiconductor (CMOS) image sensor with tiny pixels is to use a dual conversion gain (DCG) approach in a pixel structure where the conversion gain (CG) selection is adaptive with scene illumination and enhances the SNR and DR. However, current DCG image sensors use the same CG for all of the pixels within one frame (or one image) to obviate nonuniformity pattern artifacts that would appear within an image (because of the pixel dark offset values and also the light response that may be changed with a CG). To address the challenge that was described above, techniques are presented herein that support two-pixel readout mechanisms and image calibration means for a full resolution (i.e., remosaicing) mode of quad-cell image sensors that enable each individual pixel's gain to be selected independently from the remaining pixels. Such unique readout mechanisms sense the exposure level of each pixel, set the conversion gain of each pixel individually in real-time, and extend analog-to-digital convertor (ADC) bit depth by adding gain bits to achieve the highest DR and SNR. Further, each pixel may be characterized by a unique dark and flat field calibration for each CG setting. Still further, dark and flat field calibrations may be applied to correct any nonuniformity pattern image artifacts that may result from the use of multiple CGs within a single image. Aspects of the presented techniques support image calibration and correction activities. Importantly, the presented techniques may be extended for all types of image sensors.

DETAILED DESCRIPTION

Two of the main image quality requirements for a high-resolution image sensor are a high signal-to-noise ratio (SNR) and a high dynamic range (DR) throughout the whole illumination range. SNR is the ratio of the image signal to combined noise and is a critical to quality parameter for all imaging systems. A DR refers to the difference between the darkest region of an image and the brightest region of that image that may be captured simultaneously. The greater that difference, the better that one may record the faint scene of an image without saturating or clipping the bright highlights.

There is a tradeoff for a higher conversion gain (CG) and a full well capacity of each pixel of a complementary metal-oxide semiconductor (CMOS) array sensor. The well capacity of a pixel limits the total amount of charge that a pixel may hold. A larger well capacity means that a CMOS sensor can image a brighter scene without saturation. The DR is proportional to well capacity and it is defined as the ratio of a full well capacity divided by the read noise. CG is the charge-to-voltage conversion within a pixel and it is defined as the change of a pixel's output voltage with respect to the generation of new charges (V/e-).

In a Quad Bayer structure, there are four adjacent green, red, and blue color filters as depicted in Figure 1, below.

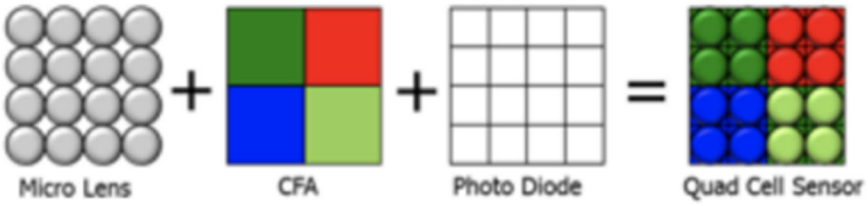


Figure 1: Exemplary Quad Pixel Sensor

A quadrant (or quad) cell image sensor (i.e., a quad-cell image sensor) may be read in either a full resolution (or remosaicing) mode or in a demosiacing mode (that sums the pixel output of the four adjacent pixels within the same color filter). Figures 2a and 2b, below, illustrate such approaches.

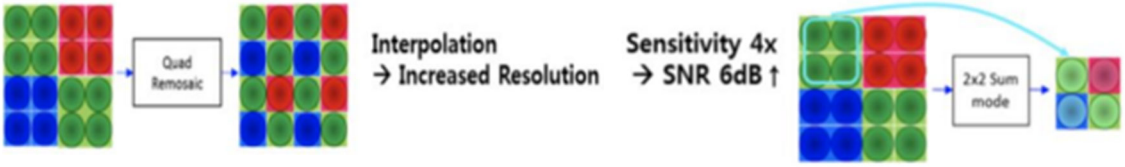
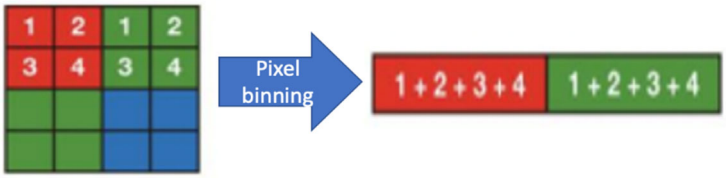


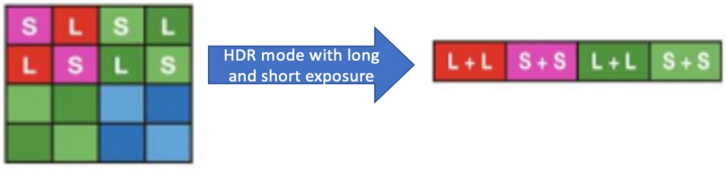
Figure 2a: Full Resolution Mode *Figure 2a: Half Resolution Mode*

Figure 2a, above, depicts a remosaic mode that is consistent with, for example, high illumination. Figure 2b, above, depicts a sum mode that is consistent with, for example, low illumination.

High resolution image sensors with four cells have smaller pixel sizes, with the tinier pixels having a smaller SNR and DR. To overcome this in quad-cell image sensors, four adjacent pixels with the same color filters may be binned to improve SNR and DR. High DR (HDR) may also be achieved by employing a double exposure (comprising a combination of low and high exposures) as illustrated in Figures 3a and 3b, below.



(a) Normal 2x2 Binning



(b) HDR mode of binning

Figure 3: Different Binning modes

Figure 3a, above, depicts a normal mode with 2x2 binning while Figure 3b, above, depicts an HDR mode with 2x2 binning. The 2x2 binning of quad-cells provides a higher SNR and DR for normal and HDR modes, respectively. The penalty that is paid is a loss of image resolution. To prevent image resolution loss, and obtain a higher SNR and DR, the concept of a dual conversion gain (DCG) pixel was introduced for quad-cells.

For a DCG pixel, there is an additional transistor in a pixel structure that can switch or change the CG of a pixel. Figures 4a through 4c, below, illustrate such an approach.

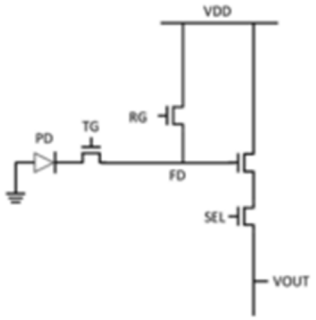


Figure 4a: Single CG

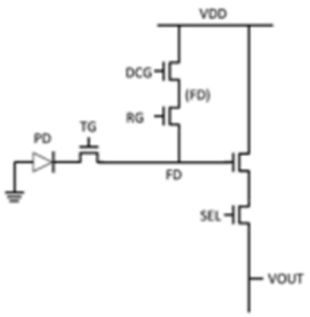


Figure 4b: Dual CG

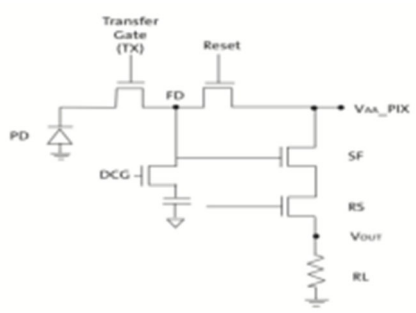


Figure 4c: Alternative Dual CG

Figure 4a, above, presents an exemplary arrangement of a single CG pixel. In contrast, Figures 4b and 4c, above, present two exemplary arrangements for a DCG pixel.

In general, a higher CG yields an improved SNR and a smaller full well pixel capacity. It is important to note that the current DCG approaches that have been developed for quad-cells do not allow for individual pixel gain changes independently from other pixels. In other words, the CGs for all of the pixels of a single frame are the same and HDR is achieved by blending a low CG image with a high CG image. There are approaches to achieve high SNR and extended DR, but they are not fully dynamic or real-time and they suffer from spatial and temporal resolution loss and nonlinearity.

Referring to Figures 4a through 4c, above, the CG in a CMOS sensor is equal to the inverse of the capacitance that is observed from the gate of a source follower (SF). The gate of an SF may be connected to a floating diffusion (FD) element and by switching a DCG transistor, the CG of an image sensor may be changed between low gain and high gain.

A greater CG results in a smaller read noise and therefore a higher SNR. However, a larger CG results in a smaller full well capacity of a pixel. Since the full well is smaller for a higher CG, the DR will be smaller and the sensor may reach its saturation at a lower exposure.

The above pixel approach is currently implemented in the design of CMOS image sensors by a number of image sensor suppliers. However, the current design of a DCG does

not allow for some pixels within one frame to have a lower CG and other pixels to have a higher CG. In other words, the pixels of the entire frame must have the same CG.

To address the limitation that was described above, techniques are presented herein that support novel pixel readout mechanisms and image calibration means through two different methods. Each of the methods will first be briefly introduced and then described and illustrated, in detail, below.

A first method encompasses allowing a single frame to contain pixels with a different CG (unlike existing solutions that use one CG for an entire frame) and correct the image non-uniformity artifacts through image calibration. A second method adds a 'gain bit' or 'gain bits' to the output of an analog-to-digital converter (ADC) which increases the quantization resolution (i.e., yields a higher bit depth) and extends the DR of an ADC.

Regarding the first method (which supports CG selection through a comparator circuit), Figures 5a and 5b, below, illustrate elements of an adaptive DCG control circuit with pixel intensity and an ADC gain bit and depict a comparator circuit which compares a pixel's output with a threshold.

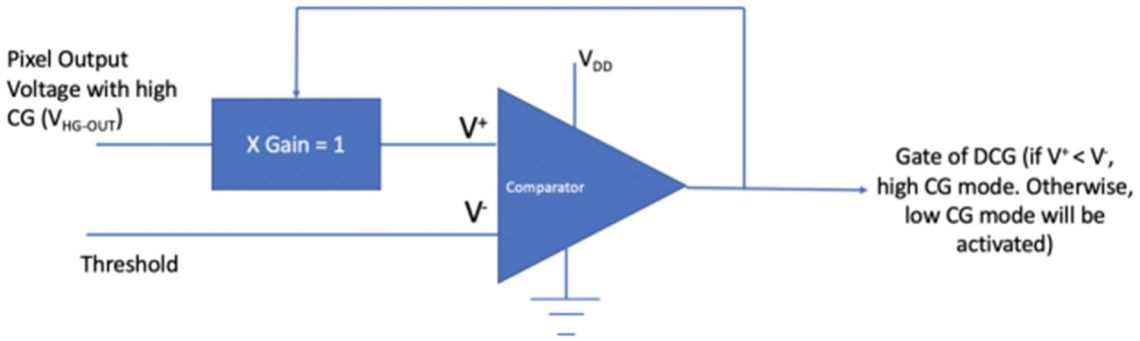


Figure 5a: Pixel Outputs with High CG

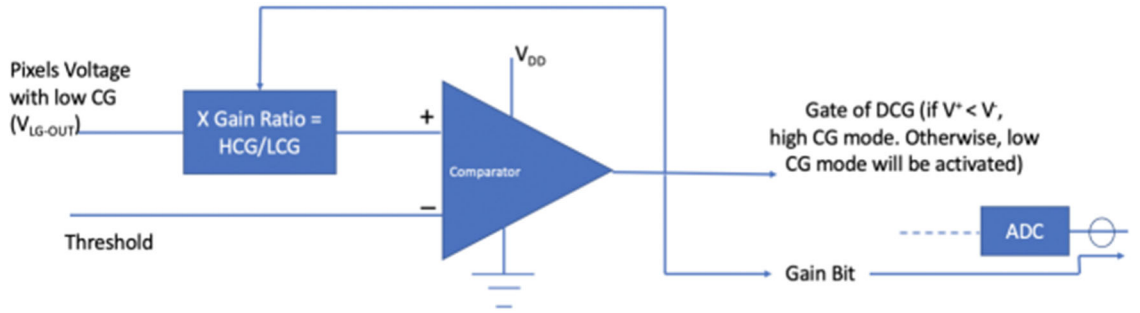


Figure 5b: Pixel Outputs with Low CG

As depicted in Figures 5a and 5b, above, if the DGT is off (referring back to Figure 4c, above) and a pixel is in a high CG mode, the ‘x Gain Ratio’ or ‘times Gain ratio’ in Figure 5a, above, is equal to one. Under such a condition, the non-inverting input voltage of a comparator is equal to the pixel output voltage. When the light exposure increases, the pixel output voltage will also increase. A threshold voltage (representing the proximity of a saturation limit for a high CG) may be connected to the inverting input of the comparator.

When the V+ exceeds the threshold of the V- (approaching the saturation limit for a high CG), the output of comparator will be high and this will activate the gate of a DGT (as shown in Figure 4c, above) and the transistor will be turned on. Under such a condition, the pixel is in a low CG mode (as depicted in Figure 5b, above) and the output voltage of the pixel will be multiplied by a gain ratio which is equal to the ratio of the high CG to the low CG. That is:

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Gain Ratio = High CG / Low CG
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The gain ratio multiplication with pixel intensities occurs only for pixels with a low CG. For instance, if a high CG is equal to 120μV/e and a low CG is 30μV/e, the gain ratio will be equal to four. In a low CG mode (e.g., Figure 5b, above), the output voltage of a pixel will be multiplied by a gain ratio (four in the above example) and then compared with the threshold voltage. If the voltage in a non-inverting input of a comparator becomes less than an inverting input, a DGT will be turned off and the pixel will be switched again to a high gain mode (as shown in Figure 5a, above).

To extend the dynamic range and quantization resolution of an imager, a gain bit may be added to the most significant bits (MSBs) of an ADC during a low CG mode as shown in Figure 5b, above. For example, with a 10-bit ADC and a gain ratio of four, for a low CG the bit depth will be 12 bits and the overall image senor bit resolution will be 12 bits.

Figure 6, below, illustrates the overall block diagram of a CMOS image sensor according to aspects of the techniques presented herein and reflective of the above discussion.

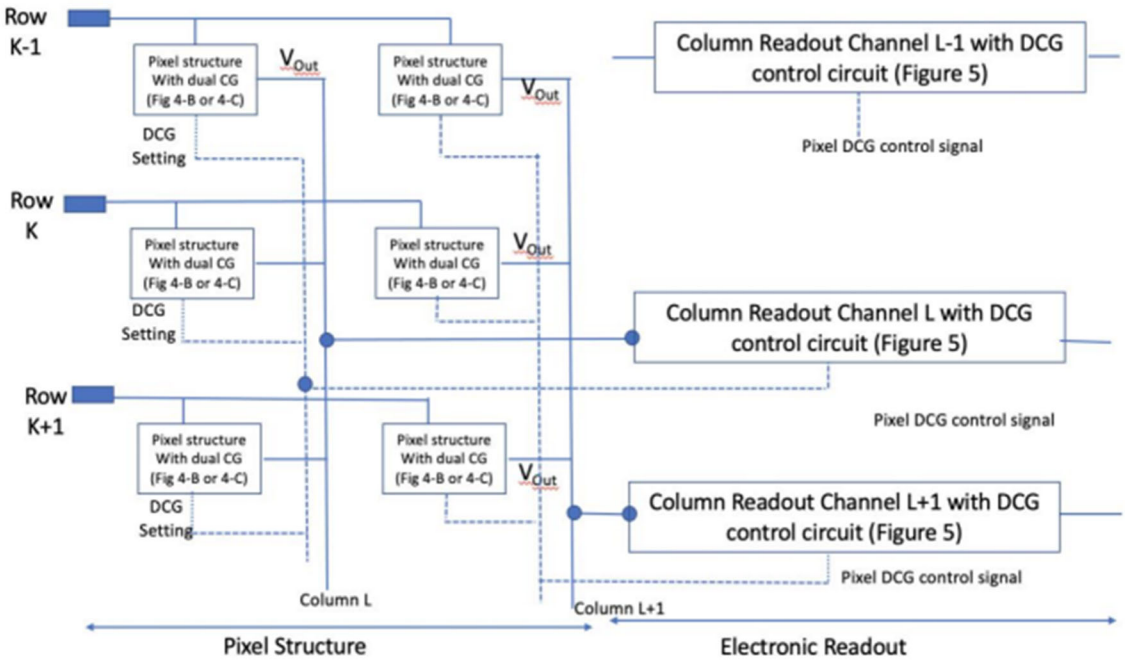

Figure 6: Block Diagram of CMOS Image Sensor with DCG Control Circuits

As depicted in Figure 6, above, the sensor contains two sections of pixel structures and readout circuitries. The pixel structure may be based on the five-transistor (5T) design that was shown in Figures 4b or 4c, above, or, alternatively, it may be based on any pixel design with DCG options. Once a specific row is selected, the pixel output of that row will pass through the column readout that incorporates the DCG control circuits as were depicted in Figures 5a and 5b, above. Depending upon the pixel output (or pixel intensity), a suitable CG may be selected and the DCG transistor within the pixel structure may be switched on or off based on the selected CG (which depends upon the light intensities). The new CG setting may then be applied for the next frame.

Such a design allows each pixel's gain to be selected individually (which is adaptive with scene light intensity) and extends the dynamic range and bit depth while at the same time delivering a higher SNR for low exposure (using a high CG mode). However, a single frame that contains pixels with different gain settings will exhibit nonuniformity pattern artifacts that will need to be corrected through image calibration (as will be described below in connection with a discussion of pixel calibration and correction).

Under the second method (which supports CG selection through dual readout), there is no need for the comparator circuit that was depicted in Figures 5a and 5b, above.

Instead, a frame may be read out twice. Under such an approach, the accumulated signal by a pixel may be read twice – once with a high CG and then with a low CG. Note that there will be no reset of an FD between two the readouts. In other words, the Reset transistor that was show in Figure 4c, above, or the RG transistor that was shown in Figure 4b, above, will not be activated to reset the FD between the two readouts. Under such an approach, a frame data size will be twice that of a conventional frame. The reset of an FD may happen after the two readouts by a high CG and a low CG.

In a dual readout mode, the CG selection decision may be made by the downstream image processing. The image processing may analyze each pixel's output (with a high CG and a low CG) and determine the best CG to be used for each pixel. The advantage of this method, as compared to first method (involving CG selection by a comparator) that was described above, is that there is no need for comparator circuits. However, a disadvantage is the loss of temporal resolution since the frame data size will be doubled.

It is important to note that a difference between the second method and some existing solutions in which two images may be captured (one with low CG and the other one with high CG) and then blended into one image is that only one image (or one frame) is captured (i.e., the frame size data is only doubled) and there will be no temporal artifacts that may be associated with other the techniques.

Under the second method, the gain bit and the extension of an ADC's output by a gain bit (which may be equal to the gain ratio of a high CG and a low CG) will be the same as the first method. Additionally, with this method a single image may contain pixels with different CG values that will appear as nonuniformity artifacts that need to be corrected by image calibration (as will be discussed below).

As noted previously, pixel calibrations are required to correct any nonuniformity artifacts due to different CGs that may have been used in a single frame. Corrections may be completed for a raw image and before applying any remosaicing by an Image Signal Processing (ISP) as illustrated in Figure 7, below.

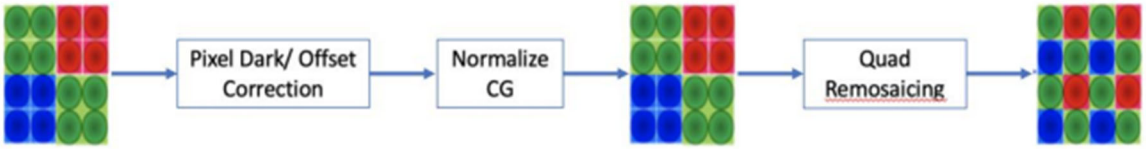

Figure 7: Pixel Calibration Before Remosaicing

Since each frame may contain pixels with a different CG, there may be a need to correct the different dark offset values of pixels due to different CGs. Note that by changing the CG of each pixel its dark offset value will also be changed. To correct this, a dark or offset correction is required. Additionally, there may also be a need to normalize the different pixel CG values that are used in a single frame. This will compensate the different CG values that are used in a single image and homogenize the image.

Under a dark field calibration or offset correction, an electronic offset may be calculated and/or measured for each CG under different camera operating conditions (such as integration time, analog gain, temperature, etc.). The electronic offset of a pixel may be subtracted from the pixel values of a captured image. The shielded pixels of an image sensor may also be used to determine the offset value for each CG.

For a flat field correction, a CG may be computed and/or measured for each CG and a gain ratio (i.e., the ratio of a high CG toa low CG) may be developed. Such a gain ratio may be utilized to normalize the pixel intensities within the same frame and to compensate for the different gain values of the pixels. A CG may be computed by determining the capacitance of a pixel FD for a DCG that is “on” and “off;” or measured by using a photon transfer curve (PTC) or a photon counting histogram (PCH) during image sensor characterization; or computed using image analysis by capturing two images (one at a low CG and another one at a high CG) with the same light intensity & profile and then applying the formula:

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Gain ratio of each pixel =
 (pixel intensity at high CG after dark field calibration) /
 (pixel intensity at low GC after dark field calibration)
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In summary, and as described and illustrated in the above narrative, techniques have been presented herein that support two novel readout mechanisms that enable a dual gain quad-cell CMOS image sensor to select different CGs in a single frame or image. The CG of each pixel may be adaptive with scene light intensity and selected automatically in real time. For darker pixels (such as a shading area), a high CG may be utilized to enhance SNR. For brighter pixels, a low CG may be selected to increase the full well of a pixel, to avoid premature saturation, and therefore increase the DR. Additionally, the bit depth of an ADC

may be extended by gain bits that are determined through the gain ratio of CGs. Since a single image (or frame) may include pixels with different CGs, aspects of the presented techniques encompass image calibration procedures that correct the different dark offset values and normalize the light sensitivities of pixels with a different CG.