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Sistema de Polarização Pulsado para Caracterização de Transístores de Potência de RF

Bias-Point Pulsing System for RF Power Transistors' Characterization

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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Doutor Luís Carlos Cótimos Nunes, Investigador do Instituto de Telecomunicações e Doutor Pedro Miguel da Silva Cabral, Professor Auxiliar do Departamento de Eletrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Palavras-chave

Amplificador de Potência de RF, Caracterização, Transístor de RF, GaN HEMT, Colapso de Corrente, Medidas I/V pulsadas, Sistemas de Medição Pulsados, Técnica do Duplo Pulso, Constantes de Tempo

Resumo

Com a evolução exponencial das redes móveis, é exigido aos sistemas que, não só, operem com mais potência e que sejam mais eficientes, mas também que operem a frequências mais altas e com maior largura de banda. Para isto, a comunidade científica está dedicada a tentar obter o melhor desempenho possível para as estações base das redes móveis.

O componente que domina o rendimento destas estações base é o amplificador de potência RF, composto por um transístor capaz de amplificar o sinal que se deseja transmitir. Hoje em dia, os dispositivos mais usados são os GaN HEMT (do inglês, *Gallium Nitride High Electron Mobility Transistor*), que permitem atingir grandes densidades de potência e grande largura de banda. Mas, estes dispositivos sofrem de diversos fenómenos dinâmicos que causam o colapso da corrente e, consequentemente, a diminuição da capacidade de entrega de potência. De modo a que se consiga prever e tentar compensar estes comportamentos dinâmicos, é necessário caracterizar os transístores num estado onde estes fenómenos sejam conhecidos, o que significa obter medidas isodinâmicas.

Este trabalho foca-se em construir um sistema que permita efetuar medidas pulsadas num transístor e evitar que efeitos de temperatura e de outros fenómenos dispersivos inerentes da tecnologia mencionada (conhecidos como *trapping*, do inglês) apareçam. Para tal, foram desenvolvidos dois circuitos: um para porta do transístor, cuja gama de tensões é de $-10\,\mathrm{V}$ a $2\,\mathrm{V}$, a corrente máxima é de $2\,\mathrm{A}$ e o tempo de estabelecimento é de $500\,\mathrm{ns}$, e outro para o dreno do transístor, cuja tensão máxima é de $160\,\mathrm{V}$, a corrente é de, pelo menos, $15\,\mathrm{A}$ e o tempo de estabelecimento é de $4\,\mu\mathrm{s}$. Com este sistema, foi possível analisar o impacto da temperatura nas medidas, através do estudo da variação da largura de pulso e do *duty-cycle*, e estudar o efeito do *trapping*, aplicando a técnica do duplo pulso. Como o *trapping* é um fenómeno dinâmico, existem constantes de tempo associadas que devem ser conhecidas, para que se possa estudar a natureza da dinâmica presente nos dispositivos.

Finalmente, para comprovar que o sistema pode ser usado para testar diversos dispositivos, foram caracterizados transístores GaN HEMT de diferentes potências. No fim, foi possível obter as suas curvas I/V isodinâmicas pulsadas, assim como os valores das constantes de tempo associadas ao efeito de *trapping*. Com todos os resultados obtidos, foi possível comprovar que o sistema é capaz de efetuar as medidas desejadas para a caracterização dos dispositivos, e que a dinâmica dos efeitos mencionados é dependente de cada transístor e deve ser sempre cuidadosamente analisada.

Keywords RF Power Amplifier, Characterization, RF Transistor, GaN HEMT, Current Collapse, Pulsed I/V Measurements, Pulsed Measurement Systems, Double Pulse Technique, Time Constants

Abstract

With the exponential evolution of mobile networks, the systems are demanded, not only to work at high power levels and to be more efficient, but also to operate at higher frequencies and with more bandwidth. For that, the scientific community is always trying to obtain the best performance possible for the mobile networks base stations.

The efficiency limiting component of these base stations is the RF power amplifier, that is composed by a transistor capable of amplifying the signal that is wanted to transmit. Nowadays, the most used devices are the GaN HEMT (Gallium Nitride High Electron Mobility Transistor), that allow operations with high power density and high bandwidth. However, these devices suffer from several dynamic phenomena that cause the current to collapse and, consequently, the reduction of the power delivery capability. To predict and try to compensate these dynamic behaviours, it is necessary to characterize the transistors in a state where these phenomena are known, which means that isodynamic measurements should be obtained.

This work focuses on designing a system that allows to perform pulsed measurements on a transistor and that avoids temperature effects and other dispersive phenomena characteristic of the mentioned technology (known as trapping). For that, two circuits were developed: one for the transistor gate, with a voltage range from $-10\,\mathrm{V}$ to $2\,\mathrm{V}$, a maximum current of $2\,\mathrm{A}$ and a settling time of $500\,\mathrm{ns}$, and another for the transistor drain, with a maximum voltage of $160\,\mathrm{V}$, a current of, at least, $15\,\mathrm{A}$ and a settling time of $4\,\mu\mathrm{s}$.

With this system, it was possible to analyse the impact of the temperature on the measurements, through the study of the pulse width and duty-cycle variation, and it was also possible to study the impact of the trapping, by applying the double pulse technique. As the trapping is a dynamic phenomenon, there are associated time constants that should be known, so it is possible to study the dynamic nature of the devices.

Finally, to prove that the system could be used to characterize several devices, GaN HEMT transistors rated for different power values were characterized. In the end, it was possible to obtain their pulsed isodynamic I/V curves, as well as the time constants associated with the trapping effect. With all the obtained results, it was possible to conclude that the system is capable of performing the desired measurements needed to characterize a device, and that the dynamic of the mentioned effects is characteristic of each device, so it should always be carefully analysed.

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List of Acronyms

R_{on} *On-resistance.*

g_{ds} *Output conductance.*

g_m *Transconductance.*

i_C *Collector current.*

i_{DS} *Drain-to-Source current.*

v_{BE} *Base-to-Emitter voltage.*

v_{CE} *Collector-to-Emitter voltage.*

v_{DS} *Drain-to-Source voltage.*

v_{GS} *Gate-to-Source voltage.*

2-DEG *2-Dimensional Electron Gas.*

ADS *Advanced Design System.*

AlGaN *Aluminium Gallium Nitride.*

AWG *Arbitrary Waveform Generator.*

BJT *Bipolar Junction Transistor.*

CW *Continuous Wave.*

DUT *Device Under Test.*

GaAs *Gallium Arsenide.*

GaN *Gallium Nitride.*

HEMT *High Electron Mobility Transistor.*

I/V *Current/Voltage.*

MESFET *Metal Semiconductor Field Effect Transistor.*

MOSFET *Metal Oxide Semiconductor Field Effect Transistor*.

NMSE Normalized Mean Square Error.

OpAmp *Operational Amplifier*.

PA *Power Amplifier*.

PAPR Peak to Average Power Ratio.

PCB *Printed Circuit Board*.

RF *Radio Frequency*.

Si *Silicon*.

SiC *Silicon Carbide*.

SMD *Surface Mount Device*.

Chapter 1

Introduction

1.1 Motivation and Context

Nowadays, with the exponential evolution of mobile networks, that demand more power and efficiency as well as higher operation frequencies and bandwidth, the *Radio Frequency* (RF) research field is being forced to improve its systems to obtain the best performances. This way, it is possible to communicate for larger distances with better quality, i.e. to guarantee that the high data rate exchanged by the users is properly transmitted and received around the globe. This leads to the need of having amplification stages that amplify the low power signals in the base stations of these networks. Otherwise, it would be very difficult to detect and correctly extract the information that is circulating between users. This amplification process is usually possible through the use of *Power Amplifier*s (PAs).

A PA is mainly composed by an active device, i.e. a transistor, capable of delivering output power according to its input power and gain profile, and considering also appropriated input and output matching networks to do that [1]. Due to power, linearity and efficiency reasons, they are the key element of these systems, limiting their performance. This leads to the extreme need of having measurement systems capable of extracting precise measurements in the complete operation range of these active devices, so accurate models that encompass all their characteristics are created to help the PA designer in its work.

Unfortunately, for the high power active devices required for the wireless networks currently in use, it is not possible to characterize their full operation range with *Continuous Wave* (CW) excitation or DC *Current/Voltage* (I/V), because that will lead to high heat dissipation. To do that characterization, it is imperative to use high power pulsed waveforms with an extremely low duty-cycle and, to generate them, it is necessary to use pulsed measurement systems.

In this chapter, an overview of the challenges in the technology of transistors that integrate PAs is going to be made, as well as of the state of the art pulsers. Lastly, the objectives and outline of this work are presented.

1.2 Challenges in the Transistors Technology

Output power and efficiency are two of the main goals when designing a PA. When the input power of a PA is increased, the output delivered power starts to increase as well, until it saturates due to the amplifier gain compression. This saturation phenomenon can be seen

in all power amplifiers and is caused by strongly non-linear effects that arise at high power levels [1]. At those power levels, the efficiency is usually higher. So, with these metrics, or others, the PA designer can choose what is the main goal of its amplifier: if the purpose is to maximize the efficiency or if the level of output power is the priority, for example. Since it is very difficult to obtain all the ideal characteristics for the power amplifier operation, devices made of new technologies are considered and taken to their limits.

With the evolution of technologies, that require more efficient and powerful systems, it is necessary to correctly choose the type of transistors to be integrated in the power amplifiers, so the best performance can be achieved. The *Silicon* (Si) devices being used for years are still the most common and least expensive transistors in the industry [2]. These devices can be used in specific applications, such as space or military industries, but now they have been outran by other semiconductors that have better intrinsic properties [3] [4]. Since Si transistors have considerable losses and low power density [2], the high power transistors that are being used more and more are, for example, *Gallium Arsenide* (GaAs) *Metal Semiconductor Field Effect Transistor*s (MESFETs) or *Silicon Carbide* (SiC) *Gallium Nitride* (GaN) *High Electron Mobility Transistor*s (HEMTs) [5] [6].

GaAs devices began as very popular devices to replace the Si ones, enabling a higher power and higher frequency operation [7]. With GaAs MESFETs, it was possible to achieve those power levels because of their great electron mobility and reduced parasitic capacitance. Having the MESFETs reached to their limits in terms of operation frequency, power and noise, new devices that answer the demands of the technology evolution had to be considered [5]. To have higher electron mobility, the HEMT structure is a better choice. In terms of semiconductors, researchers became aware of the great advantages of GaN that, due to its material higher energy bandgap, enables higher breakdown voltages and, consequently, higher power [6].

By combining the great properties of the GaN material and the structure of HEMT devices, GaN HEMTs are the preferred devices for high power amplifiers. They can achieve higher power densities with the same size as other devices, meaning that they have a smaller intrinsic capacitance and less losses and, finally, have more bandwidth. Since these devices can operate at high temperatures, it is important to choose a substrate that gives mechanical support and that spreads the dissipated heat. Thus, a substrate that has a very good thermal conductivity, the SiC substrate, is commonly used, contributing to an improvement on the performance of these devices [6].

Because of all the reasons described before, the GaN HEMT-based PAs are one of the preferred options for the cellular base stations being used today [8].

But, despite all the mentioned advantages, these devices suffer from inherent dynamic effects that limit their performance and that need to be taken into account so their accurate behaviour is known.

1.3 Dynamic Effects in GaN Devices

As mentioned before, the attractiveness of GaN devices, specially GaN HEMTs, carries a big disadvantage related to dispersive effects, that can be seen as memory in the devices or, in other words, as dynamic effects. As with many other phenomena that occur in the RF world, they should be understood so the correct compensations can be done [9].

Besides temperature effects that can arise, the most relevant phenomena occurring in

these devices are the trapping effects (drain lag and gate lag), that are commonly observed as current collapse, and result in a reduction of the output power [8].

When the devices are fabricated, some impurities and contaminations might be created in their structure, leading to imperfections that negatively affect their performance [8]. This leads to the phenomenon known as drain trapping effect (drain lag), which is considered as the dominant dispersive effect in GaN HEMT devices. The current collapse is mainly due to this drain trapping effect, that causes the output current of the devices to drop as a result of charges trapped in the device's heterojunction (buffer traps), when a high *Drain-to-Source voltage* (v_{DS}) is applied [10]. With this, the overall efficiency and output delivered power of the RF PAs where the devices are integrated is reduced. Another known phenomenon related to the output current drop in these devices is the knee walkout, also named as dynamic *On-resistance* (R_{on}), where an increase in the knee voltage (or change in the device's R_{on}) is felt in the transistor [10].

The gate-lag is caused by very negative voltages applied to the gate that create trapping effects at the surface of the device structure (surface traps). This implies the formation of a virtual gate and can be seen as a delayed response of the current in the channel to the gate voltage modulation. It was shown that the use of passivation dielectrics reduces this phenomenon, so it will not be considered as a relevant aspect in this work [11].

The understanding of all these dispersive effects is a very important aspect for the RF community that, as said before, is constantly trying to obtain the best performances for their systems. To help them, it is important to have accurate device models, that can be obtained through three main methods. One of the methods relies on the knowledge of the actual physical structure of the devices (physics-based modeling), that leads to very complex models and Industrial Property exposure. Other method is the use of behaviour models, where only the input and output signals of the system are known. Sometimes, a mixture of the two modeling methods is used, allowing a compromise between accuracy and complexity. Being the last two the preferred solutions, the correct measurements have to be performed to excite all different behaviours in the device and include the dispersive effects mentioned before in the models.

To perform these measurements, the I/V curves of *Drain-to-Source current* (i_{DS}) as function of *Gate-to-Source voltage* (v_{GS}) and as function of v_{DS} are extracted and analysed. As the power involved in these experiments is high and the devices are working close to their limits, pulsed measurements are required. With these pulsed measurements, the trapping effects arise and the double pulse technique, a technique that uses a set of two pulses to set the traps at a known state, and that is going to be explained later in detail, has to be used. This technique can be illustrated in Figure 1.1.

1.4 Pulsed Measurement Systems

A pulsed measurement system is characterized by being able to put at its output the desired voltage to apply to the *Device Under Test* (DUT), and deliver the pulsed current that is required by it. To obtain the correct I/V measurements, these pulses have to be of a very narrow width and very low duty-cycle, allowing the device being characterized to maintain its mean dissipated power at low and secure levels.

Over the years, pulsed measurement systems have been developed and improved to answer the needs of the devices being created. Transistors are becoming more powerful and complex,

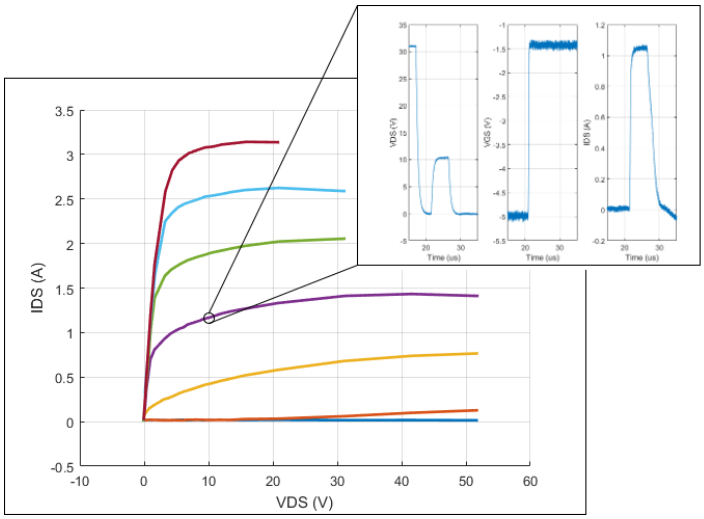

Figure 1.1 – I/V curves obtained with the double pulse technique.

demanding the systems that help with its characterization to become faster, capable of deliver more power and more accurate.

As the scope of this work is the creation of a pulsed measurement system, a summary of the different solutions proposed by several companies and that are available on the market is presented, as well as the previous pulsed measurement system developed in University of Aveiro.

AMCAD Engineering has two series of pulsed measurement systems. The *AM3100*, where voltages up to 120 V and currents of 30 A can be achieved [12], and the *AM3200*, where voltages up to 250 V and currents of 30 A are delivered [13]. The former is a more general system, used in different applications to substitute complex architectures, and the latter is a more powerful and flexible system.

Focus Microwaves Group has a set of pulser heads named *Auriga's 5th generation AU-5 Pulsed IV/RF Characterization System*, where it is possible to have systems capable of delivering a maximum of 100 V and 2 A, up to very powerful systems working at a maximum of 2000 V and 100 A, all of them with rise and fall times of tens of nanoseconds [14]. These systems are based on two pulser heads, one for the drain (higher power) and another for the gate (lower power), where their voltage levels are set using two pairs of external voltage sources, and are used for applications where high voltage and precise current pulses are necessary.

In 2016, a low cost pulsed measurement system was developed under a master degree work, where voltages up to 120 V and a maximum current of 45 A could be achieved in settling times from 300 ns to 800 ns. The two main differences between this system and the ones available on the market are the fact that it is low cost and more versatile, being possible to apply different pulsed waveforms to the devices [15].

In 2020, the latest commercial pulser head solution was created by Focus Microwaves Group, known as the *Tri-State Pulsed I-V*. This solution is capable of delivering 220 V and 10 A for very narrow width pulses of 200 ns, and is presented in Figure 1.2. What distinguishes this system from the others mentioned before is the fact that it is capable of applying the pre-pulse technique, which is essential to characterize the trapping effects in the devices,

using for that three pairs of power supplies to allow the setting of different trapping states, in comparison with the two pairs used by the ones described before. All the time settings of this system are adjustable, giving the users a lot of freedom degrees to adapt the setup to their needs [16].

Figure 1.2 – Tri-State Pulsed I-V system from Focus Microwave Group [16].

1.5 Objectives

The scope of this work is to perform accurate measurements on devices, that can be used later to create their models. Since the previously described commercial systems are expensive and not flexible, there is room to design and build a system from scratch, like the one in this work.

With the need of having transistors working at more and more high power and as the previous system developed in Aveiro is limited in terms of operating voltage range, this work is essential to provide a low cost and more powerful pulsed measurement system so it is possible to characterize several high and low power devices with different techniques that are going to be explained later in this dissertation.

So, the main objective of this work is to build two pulser heads, one for the drain and another for the gate of the DUT. The drain pulser head should be a high power circuit, that allows to bias the devices at high power conditions, and the gate pulser head should be a low power circuit, allowing to characterize transistors with very negative threshold voltages.

The first step of this work is to design and simulate the circuits in *Advanced Design System* (ADS) and then implement them in a *Printed Circuit Board* (PCB). To validate the circuits, several tests under different loads and pulse shape configurations are going to be performed in each one of them, separately. Finally, the overall system is going to be assembled and several measurements on different devices are going to be performed, where I/V curves and the dominant time constants of the dynamic behaviour are going to be obtained, allowing to understand the trapping phenomenon that these type of devices suffer.

To achieve this main objective, the following goals were defined:

- The drain pulser should work in a voltage range from 0 V to 160 V, and deliver, at least, 15 A to test the available devices.
- The gate pulser should have a voltage range from −10 V to 2 V and should be able to deliver, at least, 2 A. This way, it will be possible, not only to charge the devices input capacitance, but also, with positive voltages from 0 V to 12 V, to use it as a drain pulser for smaller transistors.
- The circuits should be fast enough to obtain isodynamic measurements, with settling times of 1 µs for the drain pulser and 300 ns for the gate pulser.

1.6 Outline

As described before, this chapter presents the scope of the work, highlighting the pulsed measurement systems, the power transistors technologies and some of their inherent problems and, finally, the objectives of the dissertation.

In Chapter 2, the developed circuits are discussed. The chapter starts with the explanation of theoretical concepts regarding the choice of the circuit topology. Then, the design and implementation of the drain pulser circuit and the gate pulser circuit are described. Finally, tests to validate their performance are presented and analysed.

In Chapter 3, a study about the drain trapping effect in GaN HEMT devices is presented. Here, a theoretical explanation is provided, the pre-pulse technique is explained and applied to the DUT and, finally, the extraction of the time constants is performed. Also, the I/V curves and time constants of two other devices are presented, demonstrating that the developed system has the capability and versatility to characterize high and low power devices.

In Chapter 4, the work done in this dissertation is summarized, where the qualities and flaws of the system are presented, and an overall analysis of the achievements is made.

In Chapter 5, some suggestions for future work are included.

Finally, the Appendices are presented.

Chapter 2

Pulsed Measurement System Design and Implementation

As mentioned in the previous chapter, the main objective of this work is to design a pulsed measurement system, where two pulser heads are developed: one for the drain of the DUT and another for its gate.

The system should be versatile, so both pulsers have at their input a low voltage signal supplied by an *Arbitrary Waveform Generator* (AWG), with the desired waveform shape, to be amplified.

In terms of architecture, two different topologies were analysed. On one hand, it could be a system that would switch between the necessary voltages and, with high voltage storage capacitors, present a pulsed waveform at its output, such as the concept of the Tri-State Pulsed I-V system developed by Focus Microwaves Group [16] [17]. On the other hand, it could be a topology based on a voltage amplifier followed by an output stage with feedback [15]. Due to simplicity reasons, the voltage-series feedback topology was chosen for both pulsers and the correspondent block diagram can be found in Figure 2.1.

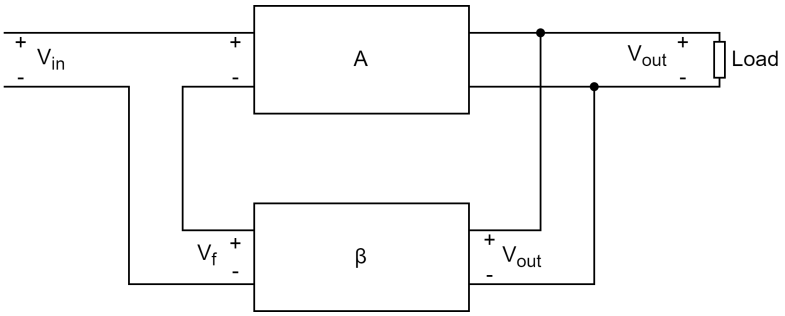

Figure 2.1 – Block diagram of the voltage-series feedback topology.

The closed loop gain equation [7] that corresponds to the presented block diagram can be found in (2.1).

$$A_F = \frac{A}{1 + \beta A} \tag{2.1}$$

where A is the open loop gain and β is the feedback factor.

Through (2.1), it is possible to analyse several advantages that a circuit with negative feedback has, such as bandwidth extension, gain desensitivity, and others [7].

Considering that the amplifier has only one pole, the bandwidth extension is proved by (2.2) [7].

$$\omega_F = \omega \cdot (1 + \beta A) \tag{2.2}$$

where ω_F is the closed loop cut-off frequency and ω is the amplifier cut-off frequency.

The property of gain desensitivity explains that the circuit becomes less sensible to variations in component values, so the output is always adjusted to the desired point [7]. This can be proved through equations (2.3) to (2.5), where a perturbation felt in the closed loop gain due to one in the open loop gain is very small.

$$\frac{\partial A_F}{\partial A} = \frac{1}{(1 + \beta A)^2} \tag{2.3}$$

$$\iff \frac{\partial A_F}{\partial A} = \frac{A_F}{A} \cdot \frac{1}{1 + \beta A} \tag{2.4}$$

$$\iff \frac{\partial A_F}{A_F} = \frac{\partial A}{A} \cdot \frac{1}{1 + \beta A} \tag{2.5}$$

Having the topology chosen, a detailed explanation regarding each section of the circuits is provided throughout this chapter.

2.1 Drain Pulser Circuit

The drain pulser must be composed by a voltage amplification stage followed by an output stage, so the circuit can deliver higher power to loads [15]. The output stage is a very important part of an amplification circuit because it gives the circuit the ability of delivering current without losing voltage gain. This is possible because it is a circuit in the common drain configuration, so it has a voltage gain approximately equal to the unity [7].

To have the best rise and fall times possible in the circuit, *Operational Amplifier*s (OpAmps) with very high slew rate and that could support the voltages specified for this work have to be used. Besides that, the output stage should be composed by *Metal Oxide Semiconductor Field Effect Transistor*s (MOSFETs) capable of handling high voltages and capable of delivering high current to loads. Since this output stage will be a high power one, it will need enough current to be driven with, so fast response times are obtained.

Since OpAmps that operate fast, that deal with high voltages and that deliver enough output current to drive a high capacitive load (as the power MOSFET is) do not exist, another output stage was added between the two previously mentioned stages. This way, it is possible to deliver the necessary current to the power output stage and maintain the fast response times of the overall circuit.

The block diagram of the drain pulser circuit is presented in Figure 2.2, where it is possible to visualize the sections of the circuit and how they are connected.

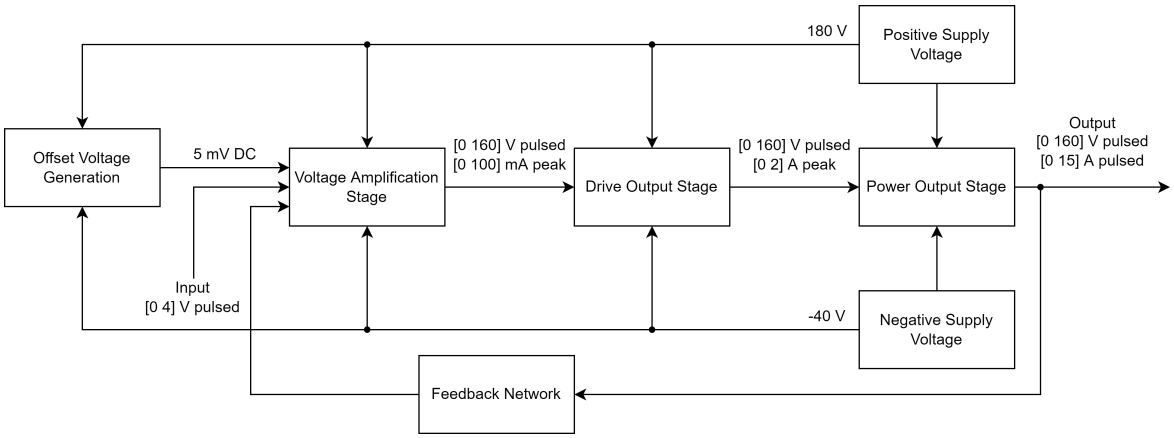

Figure 2.2 – Drain pulser block diagram.

2.1.1 Design of the Circuit

Following the block diagram, a more detailed explanation regarding the different parts of the circuit is provided.

The positive supply voltage of 180 V was chosen taking into account the maximum output voltage of the circuit (the 160 V), and the negative supply voltage of -40 V was chosen to respect the common mode input voltage range of the circuit [18] and to allow current sinking for the circuit. Also, bypassing capacitors were added to stabilize these supply voltages at the input of the circuit.

The circuit only has one stage of voltage amplification, where a high voltage and high speed OpAmp from Apex Microtechnology Inc., the PA194, is responsible for amplifying the input voltage from the AWG to the maximum of 160 V, with a maximum slew rate of 2100 V/µs in the best operating conditions. Also, to protect the PA194, its output current was limited using a current limiting resistor of 3.9 Ω [18]. Considering that the input voltage of the AWG used in this work could be up to 10 V, the gain was set to a lower value to allow the circuit to be more stable, given that, in that case, the combination between the feedback resistor and the parasitic elements in the feedback line will not be very relevant [19]. The circuit corresponding to this part of the system is presented in Figure 2.3 and the value for the gain of this non-inverting configuration is given by (2.6).

$$G = 1 + \frac{R4}{R1 + R2 + R3} = 1 + \frac{27000}{100 + 510 + 22} = 42.7\,\text{V/V} \tag{2.6}$$

For this gain value, an input voltage up to 4 V could be used, making it possible to reach the desired maximum of 160 V at the output of the circuit.

To have the circuit output always adjusted to the desired value, the feedback network should encompass the complete circuit. Despite that, there may be a offset voltage at the output of the circuit that needs to be adjusted. To compensate that, a DC voltage was generated, using a voltage divider adjusted by a potentiometer, and added at the circuit input.

The offset voltage generation block was designed considering that the output voltage could be affected by an offset of hundreds of mV. Considering the gain value of the circuit, it is possible to apply a few mV at the input of the circuit, that are then amplified, to compensate

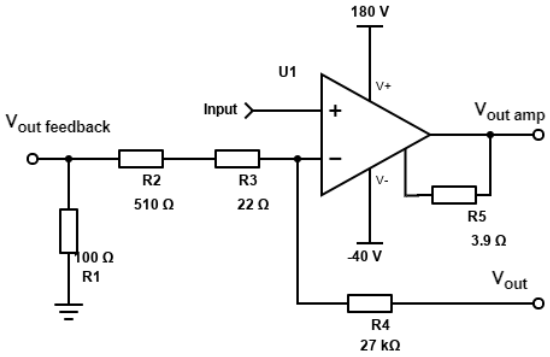

Figure 2.3 – Voltage amplification stage circuit.

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the output DC offset voltage. So, that was the reference voltage used to design the voltage divider. In Figure 2.4, it is possible to see the offset voltage generation circuit.

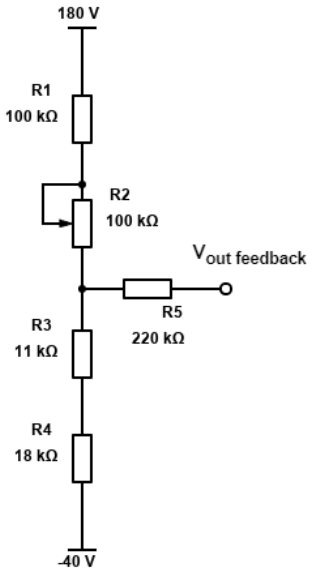


Figure 2.4 – Offset voltage generation circuit.

To reduce the load effect and have $V_{out\ feedback}$ equal to a few mV, it was considered that $R5 = 220\,\text{k}\Omega$ and that the output voltage of the voltage divider, $V_{out\ divider}$, was equal to $-11\,\text{V}$. Thus, the voltage divider resistors are given by (2.7) for the set $R1$ and $R2$ and by (2.8) for the set $R3$ and $R4$, when a reference current of $1\,\text{mA}$ is considered.

$$R_{offset\ 1} = \frac{V_{CC} - V_{out\ divider}}{I_{reference}} = \frac{180 - (-11)}{0.001} = 191\,\text{k}\Omega\ (100\,\text{k}\Omega + 91\,\text{k}\Omega) \tag{2.7}$$

$$R_{offset\ 2} = \frac{V_{out\ divider} - V_{EE}}{I_{reference}} = \frac{-11 - (-40)}{0.001} = 29\,\text{k}\Omega\ (18\,\text{k}\Omega + 11\,\text{k}\Omega) \tag{2.8}$$

As explained before, the PA194 can not deliver the necessary current to drive the power output stage, so the drive output stage is the block responsible for that. Its schematic is presented in Figure 2.5. For its design, it is important to highlight that the PA194 is capable of delivering a continuous current of 100 mA (and a peak current of 200 mA) [18], so the MOSFETs that integrate it should have an input capacitance that can be charged by this current in a short period of time, allowing fast rise times.

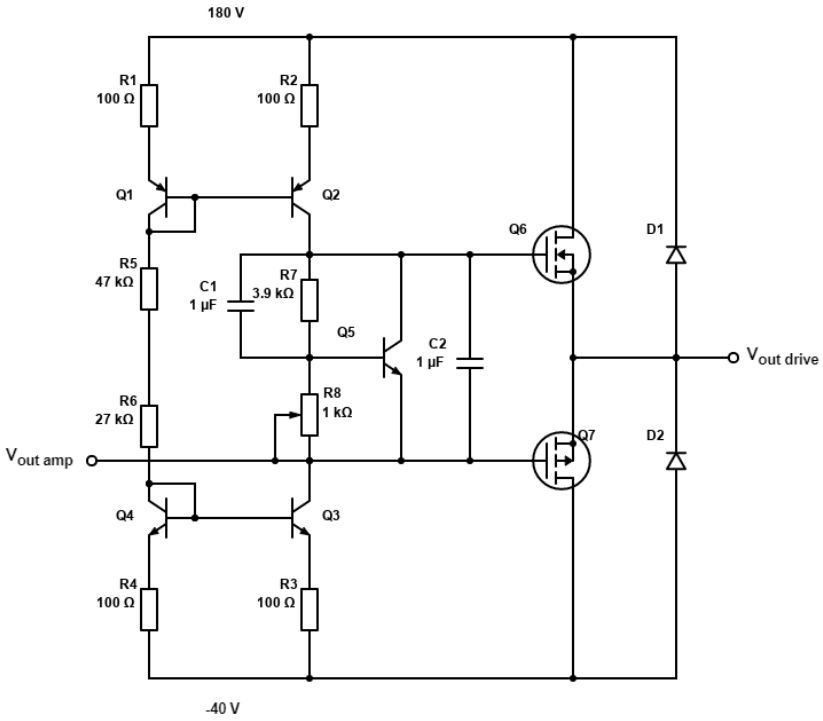


Figure 2.5 – Drive output stage circuit.

Considering this current value and rise times of around 1 µs, the mentioned MOSFETs should have a small input capacitance and operate at around 200 V. For the chosen N-type MOSFET, which is the one that delivers current to the output, the applied DC v_{DS} voltage is 180 V and its input capacitance is 140 pF [20]. For the P-type MOSFET, that does the current sinking, the applied DC v_{DS} voltage is -40 V and the input capacitance is 190 pF [21]. The necessary current to charge them is given by (2.9) and it is possible to conclude that the amplifier output current can charge this output stage in times around the one considered.

$$i = C_N \cdot \frac{dv}{dt} + C_P \cdot \frac{dv}{dt} = 140 \cdot 10^{-12} \cdot \frac{180}{1 \cdot 10^{-6}} + 190 \cdot 10^{-12} \cdot \frac{40}{1 \cdot 10^{-6}} = 32.8\,\text{mA} \qquad (2.9)$$

The drive output stage is biased in class AB, so it is very fast and capable of maintaining the very low rise and fall times that the amplification stage will have. The class AB is known for reducing the crossover distortion that is inherent in class B, where the transistors conduct alternately. To overcome the problem of class B, transistors are previously biased at a small bias current, so they are conducting more than half a cycle, in class AB [7]. To adjust the correspondent bias voltage, a *Base-to-Emitter voltage* (v_{BE}) multiplier is used.

The bias voltage, i.e. the *Collector-to-Emitter voltage* (v_{CE}) of the v_{BE} multiplier *Bipolar Junction Transistor* (BJT), equals to the sum of both MOSFETs v_{GS} at the conduction threshold, as is presented in Figure 2.6. Here, it is important to note that, as the drive output stage is not controlled by the feedback loop, its operation will only rely on the adjustments made at the output of the circuit, which can be a disadvantage of this architecture.

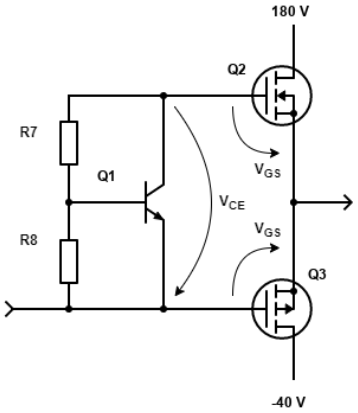
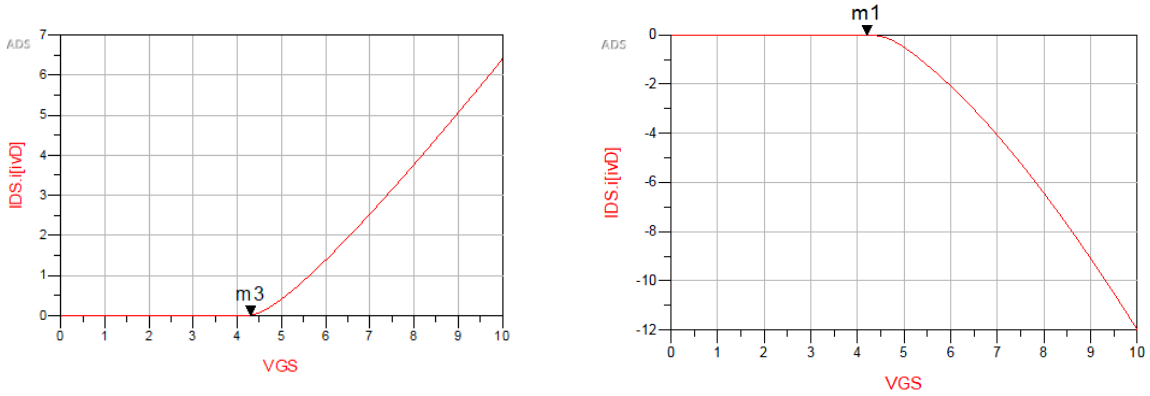


Figure 2.6 – Output stage biasing.

The v_{GS} values for the drive output stage bias voltage can be extracted from the v_{GS} (in V) versus i_{DS} (in A) curves of each MOSFET, simulated in ADS, as can be seen in Figure 2.7 (the marker m3 identifies the chosen bias current of $i_{DS} = 6\,\text{mA}$, which corresponds to $v_{GS} = 4.3\,\text{V}$, and the marker m1 identifies the chosen bias current of $i_{DS} = -7\,\text{mA}$, which corresponds to $v_{GS} = 4.2\,\text{V}$).



(a) v_{GS} versus i_{DS} curve for a v_{DS} of 180 V.

(b) v_{GS} versus i_{DS} curve for a v_{DS} of $-40\,\text{V}$.

Figure 2.7 – v_{GS} values for the N-type MOSFET (left) and P-type MOSFET (right) for the bias of the drive output stage.

To bias the v_{BE} multiplier, it is necessary to design a current source. So, a current mirror with a passive load, capable of delivering 3 mA, was designed: 2 mA are destined for the voltage divider, $I_{divider}$, and 1 mA is used to bias the BJT in the v_{BE} multiplier. To know the v_{BE} of the complementary BJTs in the current mirror, the v_{BE} (in V) versus *Collector*

current (i_C) (in A) curve for one of the transistors is presented in Figure 2.8 (the marker m3 identifies the $v_{BE} = 0.8\,\text{V}$ for 1 mA).

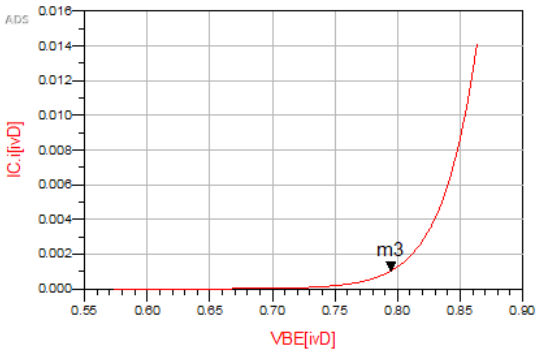


Figure 2.8 – v_{BE} versus i_C curve for a v_{CE} of 8.5 V.

So, considering the BJT base current negligible and with $v_{CE} = 4.3 + 4.2 = 8.5\,\text{V}$, the resistors R7 and R8 can be calculated through (2.10) and (2.11).

$$R7 = \frac{v_{CE} - v_{BE}}{I_{divider}} = \frac{8.5 - 0.8}{0.002} = 3850\,\Omega \rightarrow 3.9\,\text{k}\Omega \tag{2.10}$$

$$R8 = \frac{v_{BE}}{I_{divider}} = \frac{0.8}{0.002} = 400\,\Omega \tag{2.11}$$

Another important aspect regarding the v_{BE} multiplier is the presence of bypassing capacitors. Since pulses of a very short width are being applied, the bypassing capacitors have the fundamental role of maintaining the voltages between the MOSFETs gates, and allow the signal to pass smoothly.

Finally, the calculations for the current source are presented. To have low dissipated power with the reference current of 3 mA, 100 Ω resistors were chosen for the passive load. With this reference current, it is possible to calculate the resistors R5 and R6, $R_{reference}$, following the expression in (2.12) and considering the v_{BE} of the current source BJTs equal to 1 V [22].

$$I_{reference} = \frac{V_{CC} - V_{EE} - 2 \cdot v_{BE}}{R_{reference} + 2 \cdot R1} \iff R_{reference} = 72.7\,\text{k}\Omega\ (47\,\text{k}\Omega + 27\,\text{k}\Omega) \tag{2.12}$$

Regarding the power output stage, its design is very similar to the drive output stage, but here the power output MOSFETs need to be more powerful. So, the most important step was to choose MOSFETs that could deliver high current pulses and peaks to the active devices (that have an output capacitance and are seen as having a low variable resistance at their outputs). The schematic can be seen in Figure 2.9.

Following the expression presented in (2.9), the current that the MOSFETs need to receive, considering the same 1 µs, can be again given by the sum of the currents to charge each MOSFET. For the N-type power MOSFET, the applied DC v_{DS} voltage is 180 V and the input capacitance is 3590 pF [23]. For the P-type power MOSFET, the applied DC v_{DS}

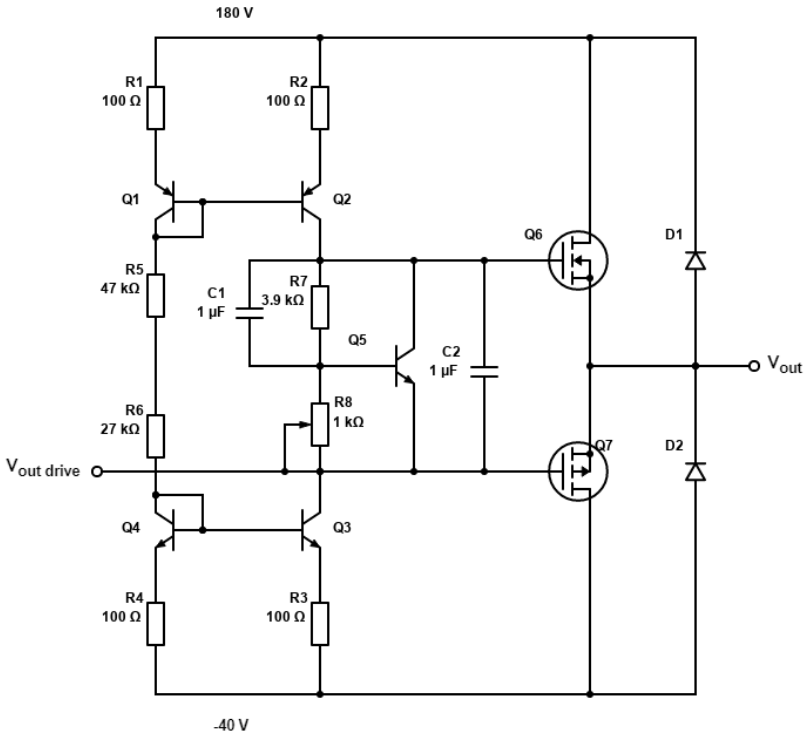


Figure 2.9 – Power output stage circuit.

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voltage is $-40\,\mathrm{V}$ and the input capacitance is $910\,\mathrm{pF}$ [24]. The total current needed to charge this output stage is presented in (2.13).

$$i = C_N \cdot \frac{dv}{dt} + C_P \cdot \frac{dv}{dt} = 3590 \cdot 10^{-12} \cdot \frac{180}{1 \cdot 10^{-6}} + 910 \cdot 10^{-12} \cdot \frac{40}{1 \cdot 10^{-6}} = 0.7\,\mathrm{A} \tag{2.13}$$

Since the N-type MOSFET from the previous output stage can deliver a peak of $6.3\,\mathrm{A}$ [20], it is possible to conclude that this stage will also be quickly charged.

This power output stage is also biased in class AB to take benefit of the advantages described before, and the v_{GS} value for the threshold of conduction is known in the same way as before, according to Figure 2.10 (the marker m1 identifies the chosen bias current of $i_{DS} = 48\,\mathrm{mA}$, which corresponds to $v_{GS} = 4.3\,\mathrm{V}$, and the marker m4 identifies the chosen bias current of $i_{DS} = -13\,\mathrm{mA}$, which corresponds to $v_{GS} = 4.5\,\mathrm{V}$).

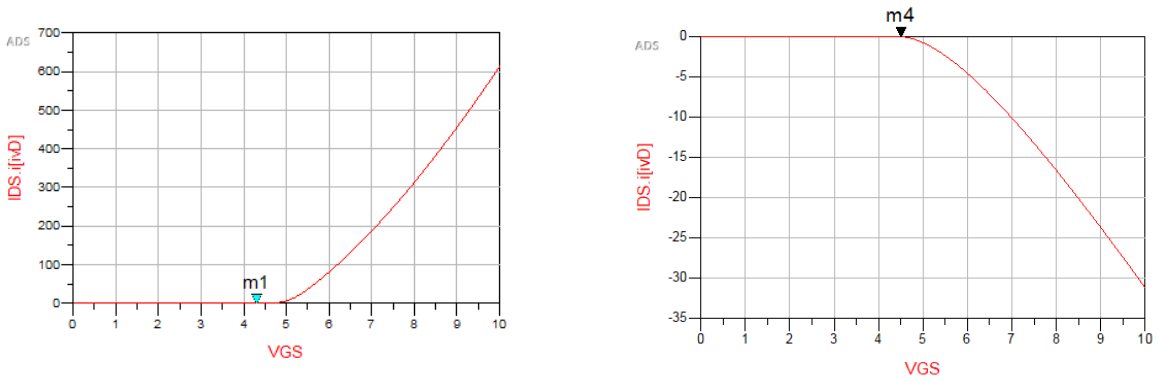
So, considering the BJT base current negligible and with $v_{CE} = 4.3 + 4.5 = 8.8\,\mathrm{V}$, which is a value very similar to the previous output stage bias voltage, it is possible to conclude that the v_{BE} multiplier and current source resistors for this output stage will have the same values.

In the end, diodes were added at the output of each output stage to protect the load from transients that could occur in the circuit.

Finally, the complete schematic of the drain pulser is presented in Figure 2.11.

Moreover, the drain pulser main components are presented in Table 2.1.

To conclude the drain pulser design and have a reference for the expected behaviour of the complete circuit, simulations with a capacitor of $100\,\mathrm{pF}$ and a resistor of $3\,\Omega$ as loads, carried



(a) v_{GS} versus i_{DS} curve for a v_{DS} of 180 V. **(b)** v_{GS} versus i_{DS} curve for a v_{DS} of −40 V.

Figure 2.10 – Power output stage v_{GS} values for the N-type MOSFET (left) and P-type MOSFET (right).

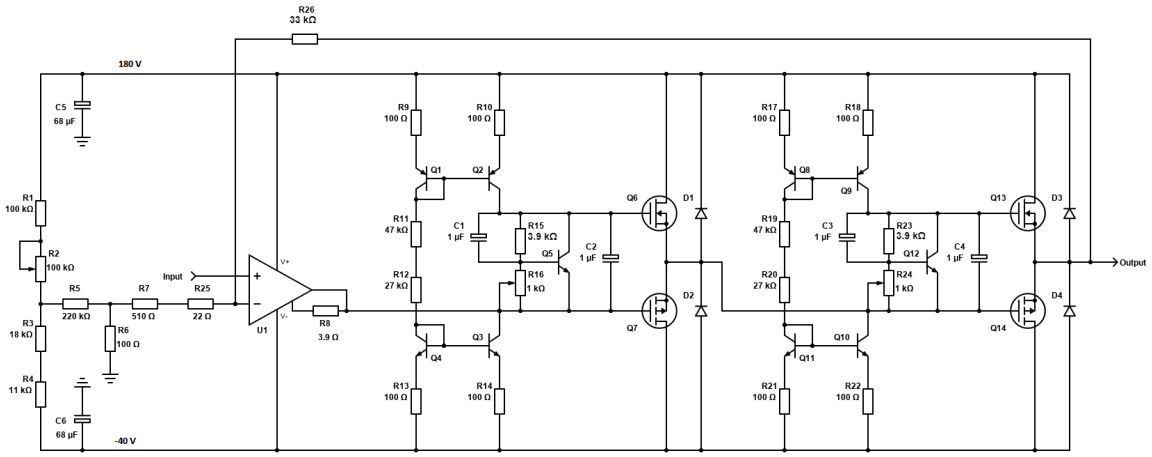


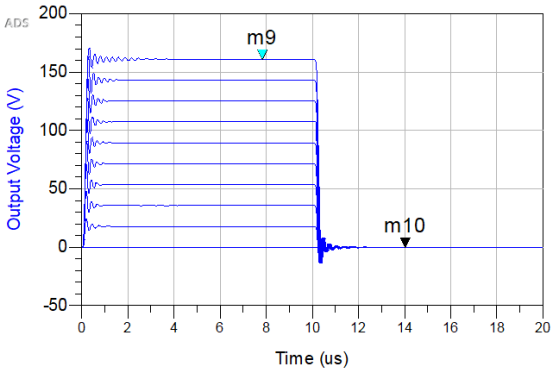
Figure 2.11 – Drain pulser complete schematic.

Table 2.1 – Drain pulser main components.

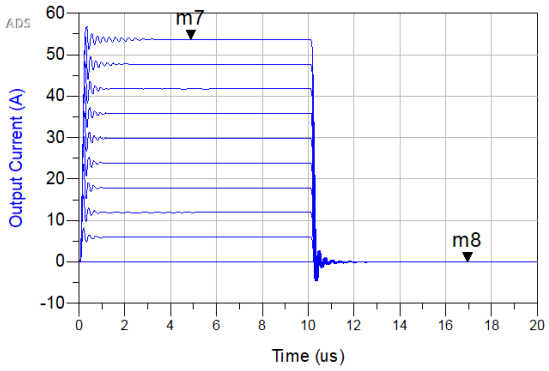
Identification	Component
High Voltage Amplifier (U1)	PA194
High Voltage PNP (Q1, Q2, Q8 and Q9)	MJE15033
High Voltage NPN (Q3, Q4, Q10 and Q11)	MJE15032
V_{BE} Multiplier NPN (Q5 and Q12)	2N3053
Drive N-type MOSFET (Q6)	IRFL214
Drive P-type MOSFET (Q7)	FQT2P25
Power N-Type MOSFET (Q13)	FDA59N30
Power P-type MOSFET (Q14)	FQP9P25

out in ADS, are presented in Figure 2.12, with a voltage sweep for all the pulser operation range. The markers in Figure 2.12a identify the maximum voltage of 160 V that can be achieved and the DC offset voltage of −30 mV, and the markers in Figure 2.12b identify the maximum current, for this load, of 54 A and the DC current of −10 mA.

It is also important to note that the simulation predicts a settling time of around 1 µs, which is the expected theoretical value considered in the design. But, the practical settling time value could be different (is usually slower) due to implementation uncertainties and compensations that are needed to be done in order to try to have the smallest transients possible in the pulsed waveform. Nevertheless, the simulation allows to conclude that the circuit is designed in the correct way, as the results fulfil the goals for this work.



(a) Voltage pulses at the the drain pulser output.



(b) Current pulses at the drain pulser output.

Figure 2.12 – Simulation results for the drain pulser.

After simulating the circuit with several loads to guarantee its correct operation and know what to expect, the implementation of the circuit in a PCB was done.

2.1.2 Implementation

To implement the circuit, a PCB was designed in Eagle. To avoid several problems that could arise, care had to be taken when designing the board.

To make the debugging easier, the components were placed in sections, according to the function of each part of the circuit. Then, the high power components were placed on one side of the board to make possible their connection to the heatsink, that should be grounded to avoid oscillations. The *Surface Mount Device* (SMD) components that dissipate a significant amount of power were also considered and extra copper was added to make the dissipation area larger. Finally, knowing where high currents would flow, the traces width and spacing was taken into account, and the feedback line was made as short as possible to avoid inductive type oscillation problems coming from there.

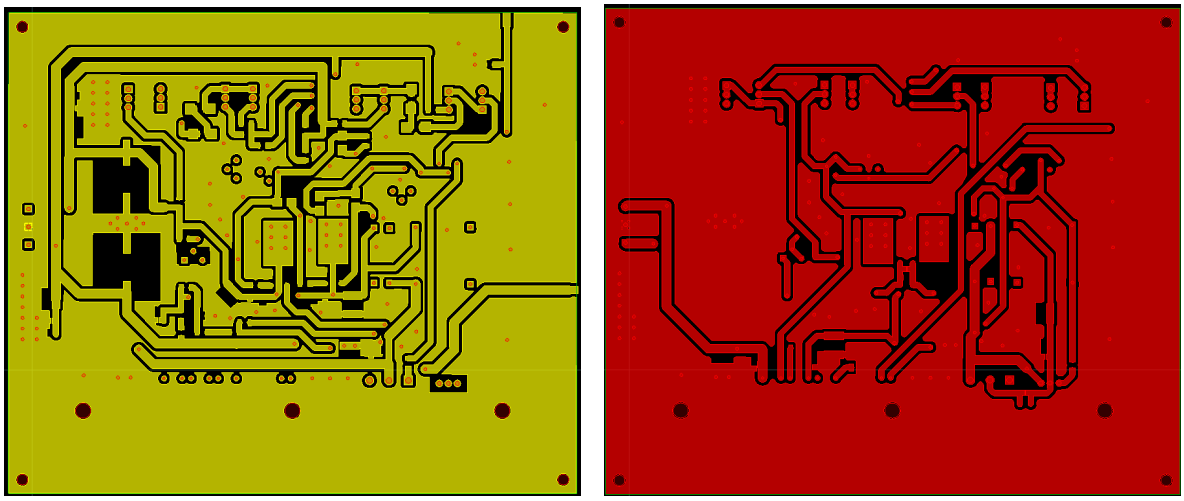
Since this type of circuit is prone to oscillate, several additions and modifications to the circuit were made until all the oscillations were solved.

As was said before, bypassing capacitors were added on the voltage supply rails at the input of the circuit to stabilize the voltages, with high value ones doing the low frequency bypassing (in the order of µF), and smaller ones doing the high frequency bypassing. Since the bypassing capacitors have the function of maintaining the voltages stable even when current

is being pulled from the source, several capacitors in each decade from nF to µF should be added on each supply pin of the PA194 and MOSFETs. This way, the stability of the circuit can be improved [25]. Also, to stabilize the offset voltage being applied at the input of the circuit and since there aren't OpAmps that handle the involved high voltages to operate as buffers, more capacitors were added at the output node of the voltage divider.

Then, since the circuit oscillated at higher voltages and with low resistive loads, compensation techniques were applied. First, there is the possibility of placing a compensation capacitor in the PA194, since it has a designated pin for that. With this capacitor, the dominant pole technique is applied and the circuit becomes slower, i.e. with higher rise times. As this reduces the bandwidth of the circuit, another technique was tried, to have the circuit compensated but with lower rise times. Therefore, a capacitor was also added in parallel with the resistor at the feedback network of the circuit, to compensate the feedback factor (β) [25] [26]. To try to have the best compromise between the effects of these capacitors in the circuit, their values were chosen by trial and error, where the compensation capacitor ended up with a value of 200 pF, and the feedback capacitor of 18 pF. Also, small value resistors were added at the gates of each MOSFET, limiting the current that flows there and improving, once again, the stability.

In Figure 2.13, the top and bottom layers of the PCB are presented.



(a) Top layer of the drain pulser PCB.

(b) Bottom layer of the drain pulser PCB.

Figure 2.13 – Drain pulser PCB.

Finally, the board is shown in Figure 2.14.

2.1.3 Validation and Tests

To see if the response of the circuit is the same as the simulated one, different loads were tested and the results were extracted and validated for the pulser complete operation range.

For these tests, the input signal is a pulse or a set of pulses, so MATLAB code was developed to create pulsed waveforms with the desired voltages to apply at the input of the circuit. The detailed explanation of the code can be found in Appendix A.

The first test to perform in the drain pulser is the analysis of its response with no load. The voltage at the output of the circuit is presented in Figure 2.15. In Figure 2.15a, it is

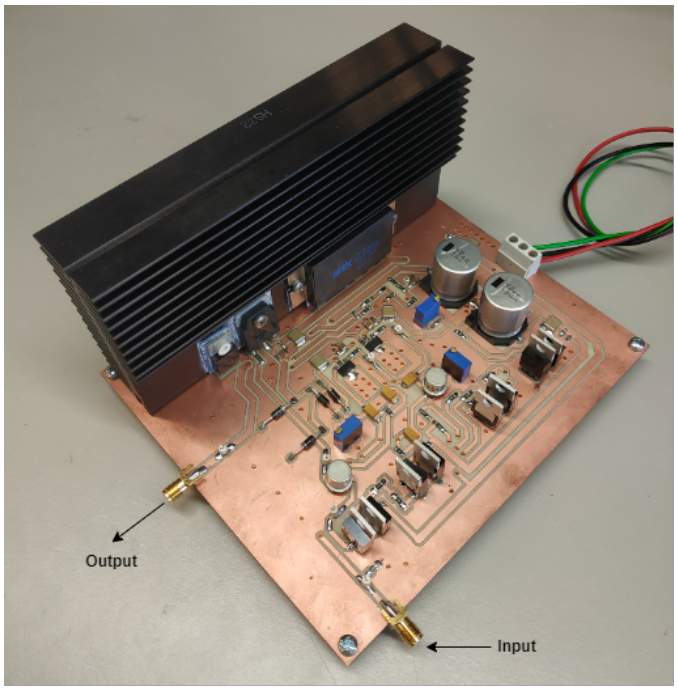


Figure 2.14 – Drain pulser board.

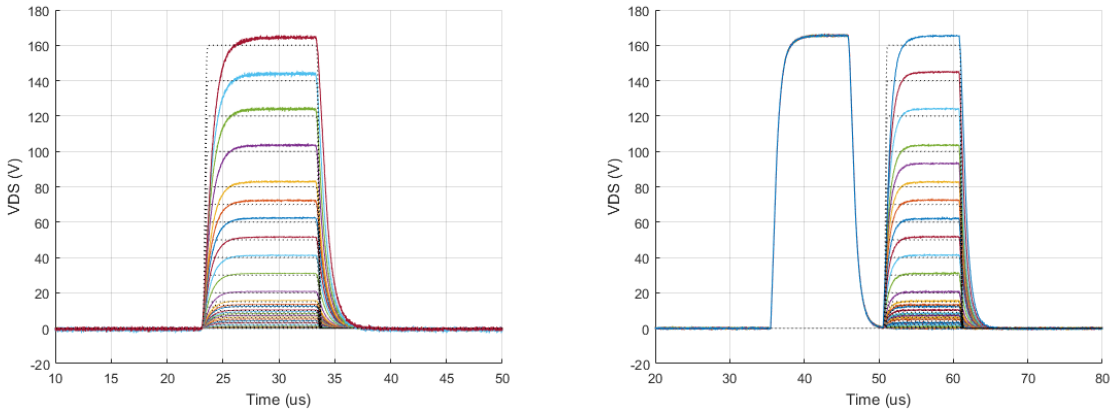
possible to observe the response to a pulse with a duration of 10 µs and the correspondent theoretical curves in black. In Figure 2.15b, the response to a set of two pulses, each one with a duration of 10 µs, is presented, creating the pre-pulse configuration (that it is going to be explained later).

Through Figure 2.15, it is possible to see that the drain pulser response is the expected one. Since the pulses cover the entire operation voltage range and the theoretical values correspond to the practical ones despite the small gain difference that is felt in the complete voltage range (and that can be compensated by adjusting the feedback resistor), it is considered that the circuit operates correctly with an open load. The settling time is, in the worst case, of around 4 µs, which is reasonable, giving the theoretical expected value of 1 µs and all the compensations that were done to make the circuit more stable. Finally, the application of different configurations of pulses is demonstrated to be possible with this circuit.

As the aim of the circuit is to characterize active devices, it is important to test the pulser with capacitive and low resistive loads.

So, a capacitive load of 680 pF and three resistive loads of 1 Ω, 3 Ω and 47 Ω were applied at the output of the circuit. The output voltage and the output current of the circuit for the different loads can be seen in Figure 2.16. Since the low resistance values are only going to occur at smaller v_{DS}, those tests were made for lower pulsed voltages.

The pulses presented in Figure 2.16 still demonstrate the correct operation of the circuit in around the same or even less settling time values. It is possible to state that, the smaller the resistive load is, more overshoot the pulse will have. This is accepted because it is clear that, after 3 µs or 4 µs, the pulse is stable, so the measurement can be done. As is going to be demonstrated later, it is very important to make the measurements in the pulse as soon as possible and to guarantee that the maximum voltage of the pulse is never higher than the pre-pulse to avoid dynamic effects. But, if the overshoot is not wanted, pulse shaping could



(a) Drain pulser output voltage for an open load, from 0 V to 160 V.

(b) Drain pulser output voltage with a pre-pulse for an open load, from 0 V to 160 V.

Figure 2.15 – Drain pulser output pulsed voltage for an open load, with the correspondent theoretical waveforms in black.

be done to reduce it.

To confirm that the gain is constant all over the circuit voltage range and that it has the expected value of 42.7 V/V, its value for an open load and for the different types of mentioned loads is presented in Figure 2.17. Despite the higher gain value that is felt in all measurements, it is considered that the results are satisfactory because the voltage true value will always be measured and the maximum voltage is within the pulser operating limits. As the gain is even higher for low v_{DS}, it might not be possible to accurately measure very low voltage pulses.

Then, it is possible to consider that the circuit will be able to generate high and low power pulses to loads, meaning that the characterization of active devices is going to be correctly made.

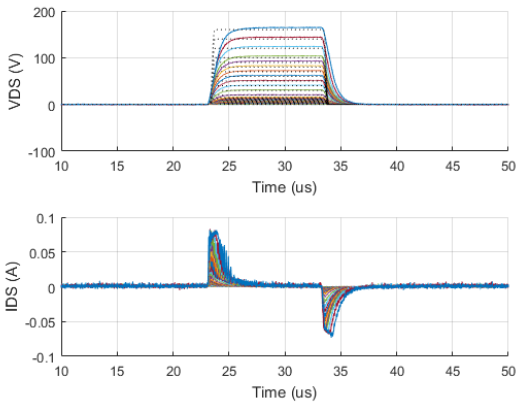
2.2 Gate Pulser

As was explained in the beginning of the chapter, the gate pulser also has a voltage-series feedback topology. Since it should work at lower voltages, the major concern about its design was to guarantee the low response times of the circuit. To do that, high speed operational amplifiers were chosen.

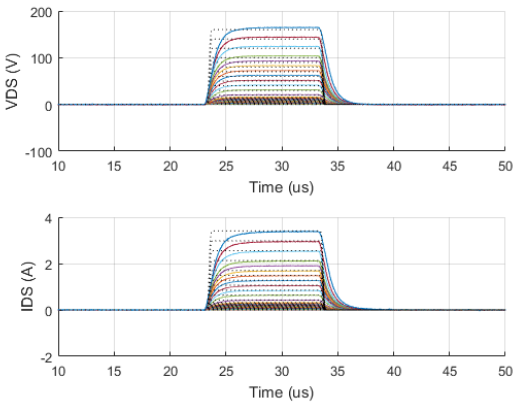
This circuit is based on a differential amplifier configuration where, in one branch, the input signal from 0 V to 1 V is amplified to the range of 0 V to 12 V, and in the other branch, an offset voltage of 10 V is generated through a voltage divider to be subtracted and obtain the desired range of negative and positive voltages at the output of the circuit.

Since different transistors have different threshold voltages, it is possible to change the output voltage range of the circuit by adjusting the offset voltage value. With this functionality, it is even possible to use the circuit as a drain pulser to pulse smaller devices. To allow that, an output stage was added to give the circuit the capability of delivering current.

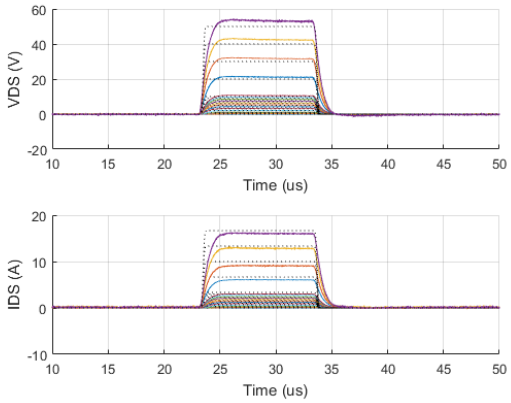
The block diagram of the gate pulser circuit is presented in Figure 2.18, where it is possible to understand how the different sections of the circuit are connected.



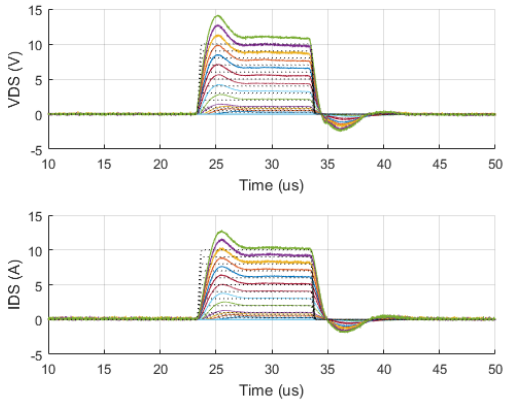
(a) Drain pulser output voltage and output current with a capacitive load, from 0 V to 160 V.



(b) Drain pulser output voltage and output current with a 47 Ω load, from 0 V to 160 V.



(c) Drain pulser output voltage and output current with a 3 Ω load, from 0 V to 50 V.



(d) Drain pulser output voltage and output current with a 1 Ω load, from 0 V to 10 V.

Figure 2.16 – Drain pulser output voltage and output current for several loads, with the correspondent theoretical waveforms in black.

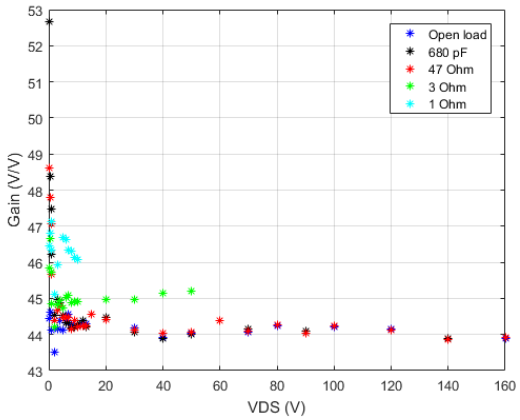


Figure 2.17 – Drain pulser gain for several loads.

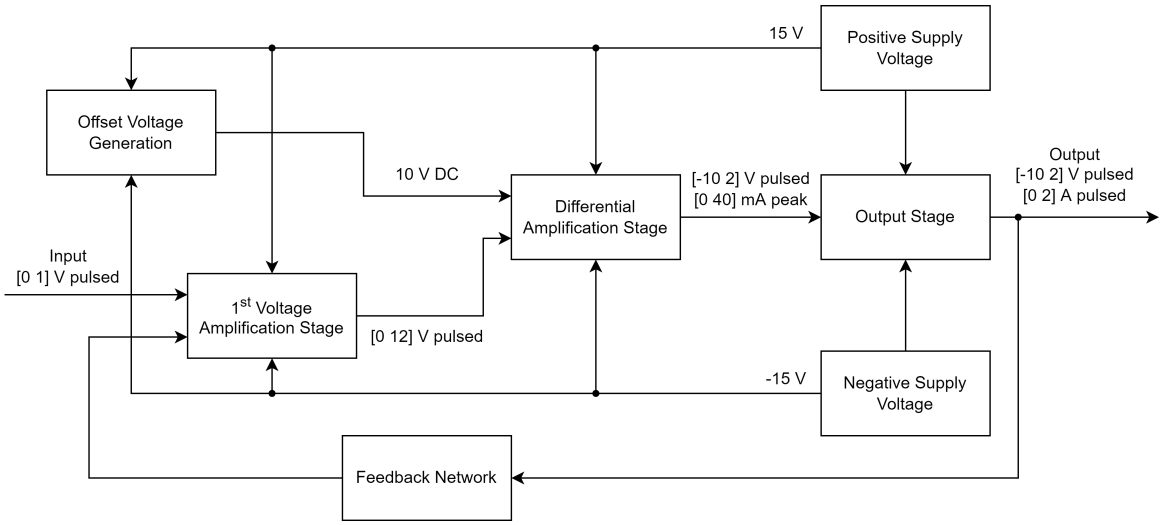


Figure 2.18 – Gate pulser block diagram.

2.2.1 Design of the Circuit

Following the block diagram, a more detailed explanation regarding the different sections of the circuit is provided.

The voltage supply values were chosen having in mind the desired output voltage range. So, symmetric voltage supplies of 15 V were selected for the amplifiers and the output stage components. Here, bypassing capacitors were also added at the input of the circuit.

Considering the input voltage from the AWG with a maximum value of 1 V, the first amplifier should have 12 V at its output. Considering a non-inverting configuration and the input voltage range, the schematic of the 1st voltage amplification stage is presented in Figure 2.19 and the gain is given by equation (2.14).

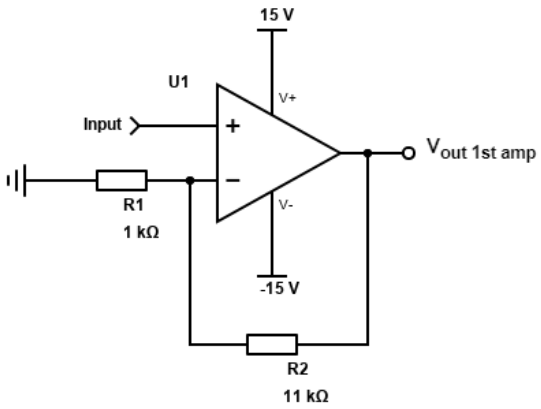


Figure 2.19 – 1st voltage amplification stage circuit.

$$G = 1 + \frac{R2}{R1} = 1 + \frac{11000}{1000} = 12\,\mathrm{V/V} \tag{2.14}$$

The 10 V offset voltage was obtained using a voltage divider, as is demonstrated in Figure 2.20. Through equations (2.15) and (2.16), and considering a reference current of 1 mA, the resistor values can be calculated.

$$R_{offset\ 1} = \frac{V_{CC} - V_{out\ offset}}{I_{reference}} = \frac{15 - 10}{0.001} = 5\,\text{k}\Omega \tag{2.15}$$

$$R_{offset\ 2} = \frac{V_{out\ offset} - V_{EE}}{I_{reference}} = \frac{10 - (-15)}{0.001} = 25\,\text{k}\Omega\ (12\,\text{k}\Omega + 13\,\text{k}\Omega) \tag{2.16}$$

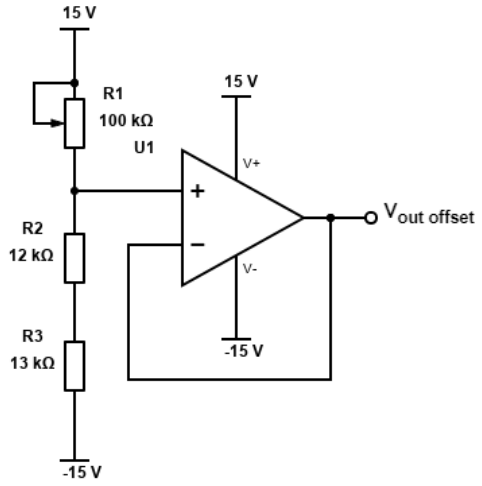


Figure 2.20 – Offset voltage generation circuit.

The gate pulser has a dynamic range of 12 V that can be adjusted to obtain the desired voltage range to pulse a device. By adjusting the offset to obtain only positive output voltages, the gate pulser can be used as a drain pulser for smaller devices, i.e. for devices with operation voltages and currents in this range and low output capacitances. So, the 5 kΩ resistor was replaced by a 100 kΩ potentiometer. Then, the offset voltage was stabilized using an OpAmp in the buffer configuration.

To obtain the final output voltage, these voltages were subtracted by adding another OpAmp in the differential configuration with unitary gain. As in the case of the drain pulser, the feedback of this amplifier encompasses its output stage, directly controlling the output voltage. This differential amplification stage with unitary gain can be found in Figure 2.21. In the end, to compensate the overshoot that the pulses had with this circuit, a small value isolation resistor was placed between the amplification stage and the output stage [27], and a capacitor was placed in the feedback network to reduce the gain at high frequencies. Both values were chosen by trial and error.

Regarding the output stage, it was once again designed to operate in the class AB bias condition, introducing the already mentioned advantages. So, the MOSFETs should always be conducting a small bias current to guarantee faster response times. These MOSFETs should safely operate in the circuit voltage range and have a capacitance that could be quickly charged with the current supplied by the previous OpAmp. The schematic for the output stage is presented in Figure 2.22.

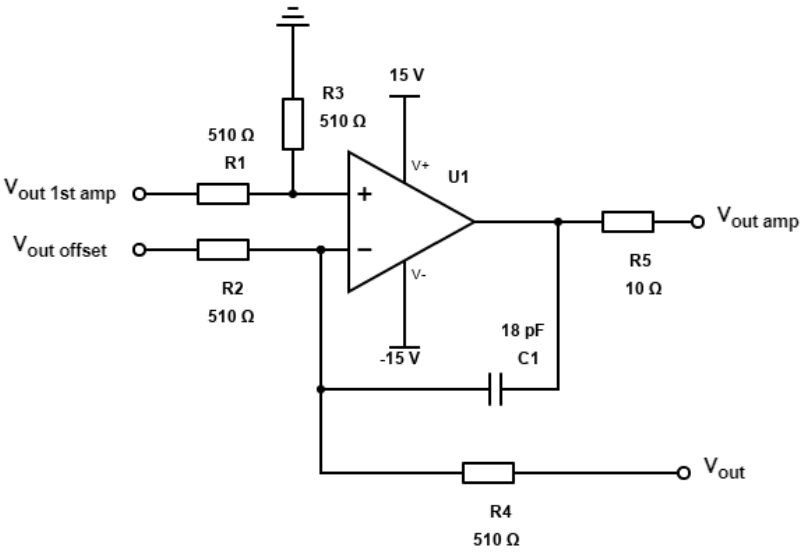


Figure 2.21 – Differential amplification stage circuit.

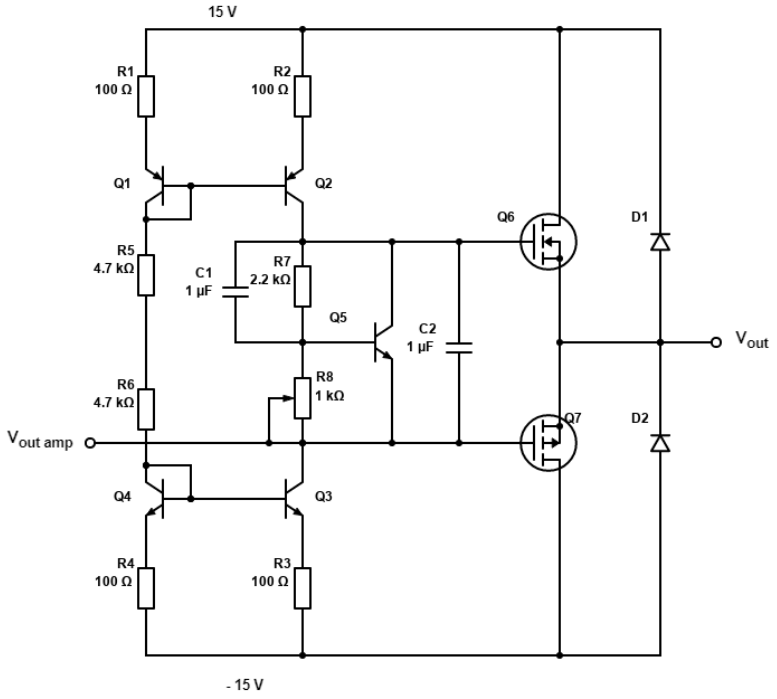
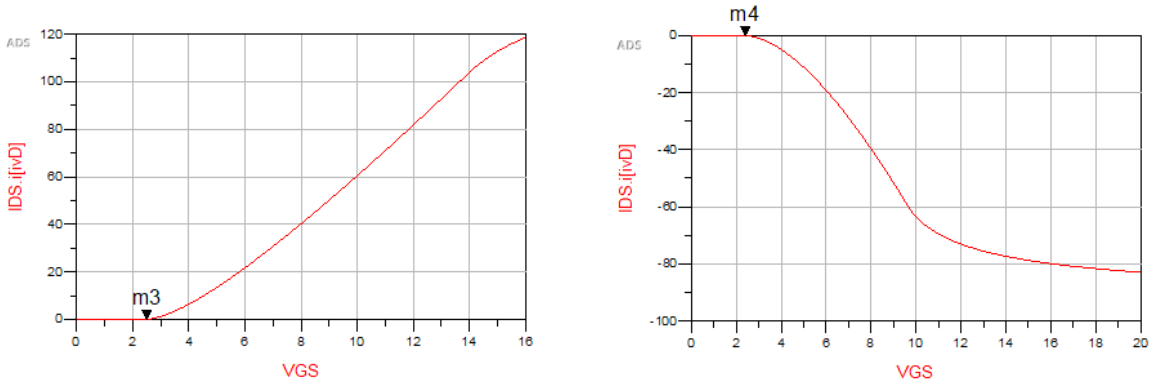


Figure 2.22 – Output stage circuit.

Considering rise times in the order of 300 ns, for the best case, and that the LM7171 can deliver 100 mA, the current needed to supply the two MOSFETs can be calculated as was done for the drain pulser. The input capacitance of the N-type MOSFET is 400 pF [28] and the applied DC v_{DS} voltage is 15 V. For the P-type MOSFET, the input capacitance is 365 pF [29] and the applied DC v_{DS} voltage is -15 V. The current can then be given by (2.17) and it is possible to conclude that the amplifier can drive the output stage in times around the one considered.

$$i = C_N \cdot \frac{dv}{dt} + C_P \cdot \frac{dv}{dt} = 400 \cdot 10^{-12} \cdot \frac{15}{300 \cdot 10^{-9}} + 365 \cdot 10^{-12} \cdot \frac{15}{300 \cdot 10^{-9}} = 38\,\text{mA} \quad (2.17)$$

According to Figure 2.6, the v_{CE} for the bias voltage of the output stage can be extracted from the simulated v_{GS} (in V) versus i_{DS} (in A) curves of each MOSFET, as can be seen in Figure 2.23 (the marker m3 identifies the bias current of $i_{DS} = 46$ mA, which corresponds to $v_{GS} = 2.5$ V, and the marker m4 identifies the bias current of $i_{DS} = -41$ mA, which corresponds to $v_{GS} = 2.4$ V).



(a) v_{GS} versus i_{DS} curve for a v_{DS} of 15 V.

(b) v_{GS} versus i_{DS} curve for a v_{DS} of 15 V.

Figure 2.23 – Output stage v_{GS} values for the N-type MOSFET (left) and P-type MOSFET (right).

From Figure 2.23, it is possible to extract the v_{CE}, that is given by the sum of each MOSFET v_{GS}, which is $v_{CE} = 2.5 + 2.4 = 4.9$ V.

The v_{BE} multiplier biasing is done with a current mirror, as was done in the drain pulser. Being the v_{BE} multiplier BJT the same as in the drain pulser circuit, its bias current can be considered the same, i.e. 1 mA, and the resistors R7 and R8 can be calculated through (2.18) and (2.19) with a reference current of 2 mA.

$$R7 = \frac{v_{GS} - v_{BE}}{I_{DIV}} = \frac{4.9 - 0.8}{0.002} = 2050\,\Omega \rightarrow 2.2\,\text{k}\Omega \quad (2.18)$$

$$R8 = \frac{v_{BE}}{I_{DIV}} = \frac{0.8}{0.002} = 400\,\Omega \quad (2.19)$$

Again, it is necessary to add bypassing capacitors to the v_{BE} multiplier so the pulsed signal can pass smoothly.

Finally, the calculations for the current source are presented. The 100 Ω resistors were also chosen for this circuit, so low power is dissipated with the considered reference current. This reference current allows the calculation of the resistors R5 and R6, $R_{reference}$, following the expression in (2.20) and considering the v_{BE} of the current source BJTs equal to 0.6 V [30].

$$I_{reference} = \frac{V_{CC} - V_{EE} - 2 \cdot v_{BE}}{R_{reference} + 2 \cdot R1} \iff R_{reference} = 9.4\,\text{k}\Omega\ (4.7\,\text{k}\Omega + 4.7\,\text{k}\Omega) \tag{2.20}$$

In the end, diodes were also added at the output of the circuit to protect the load from transients.

The complete schematic of the gate pulser is shown in Figure 2.24.

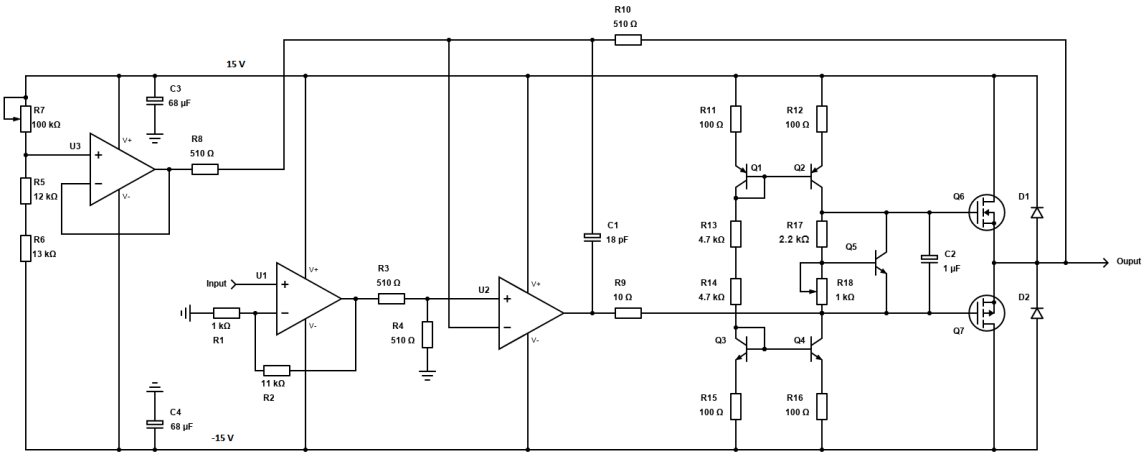


Figure 2.24 – Gate pulser schematic.

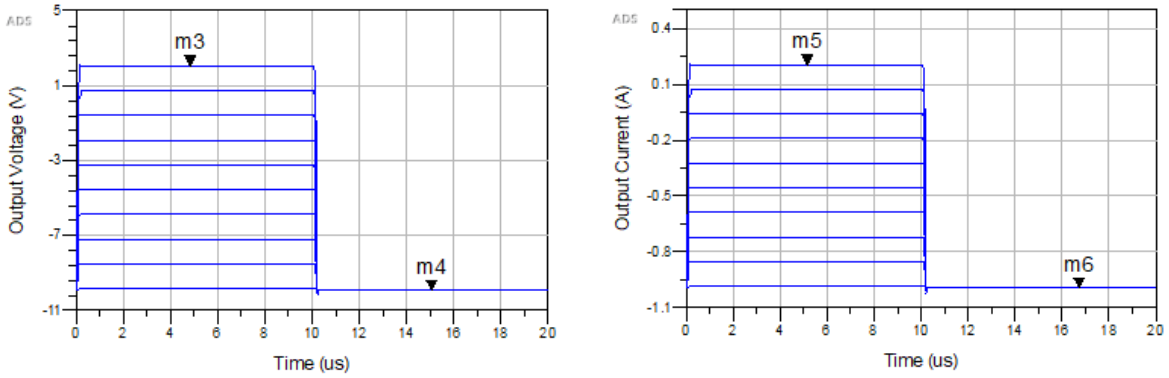
Moreover, the gate pulser main components are presented in Table 2.2.

Table 2.2 – Gate pulser main components.

Identification	Component
Operational Amplifier (U1, U2 and U3)	LM7171
Bipolar Transistor PNP (Q1 and Q2)	2SA2125
Bipolar Transistor NPN (Q3 and Q4)	2SC5964
V_{BE} Multiplier NPN (Q5)	2N3053
N-type MOSFET (Q6)	IRLL014
P-type MOSFET (Q7)	BSP171P

To conclude the gate pulser design and have a reference for its expected behaviour, simulations with a capacitor of 100 pF and a resistor of 10 Ω as loads, carried out in ADS, are presented in Figure 2.25, with a voltage sweep for all the pulser operation range. The markers on Figure 2.25a identify the maximum voltage of 2 V that can be achieved and the DC voltage of −10 V, and the markers on Figure 2.25b identify the maximum current, for this load, of 200 mA and the DC current of −1 A.

It is also important to note that the simulation predicts a rise time of hundreds of ns, which is the expected theoretical value considered in the design but, once again, the circuit can become slower due to implementation uncertainties. Regardless, the simulation shows that the circuit should produce the desired results.



(a) Voltage pulses at the gate pulser output.

(b) Current pulses at the gate pulser output.

Figure 2.25 – Simulation results for the gate pulser.

After simulating the circuit with several loads to guarantee its correct operation and know what to expect, the circuit was implemented in a PCB.

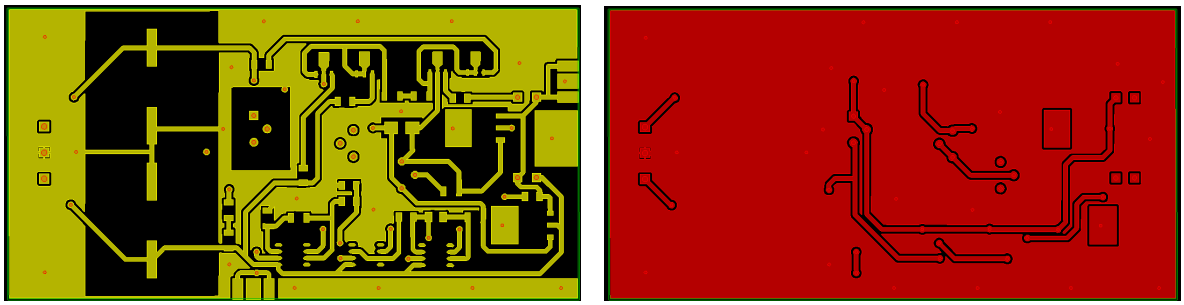
2.2.2 Implementation

To implement the circuit, a PCB was designed in Eagle.

Since there were not traces with very different current values, the PCB design was made considering only the components placement in sections, according to the function of each part of the circuit.

Being the gate pulser a simpler circuit, that deals with lower power levels than the drain pulser, all the extra care taken to stabilize the latter was not very important in this case. So, it was possible to obtain the expected results with no additional compensations.

In Figure 2.26, it is possible to see the top and bottom layer of the PCB, respectively.



(a) Top layer of the gate pulser PCB.

(b) Bottom layer of the gate pulser PCB.

Figure 2.26 – Gate pulser PCB.

Finally, the board is shown in Figure 2.27.

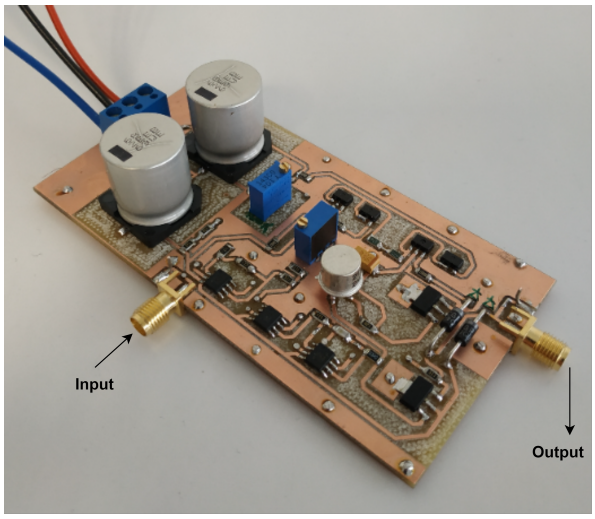


Figure 2.27 – Gate pulser board.

2.2.3 Validation and Tests

To see if the response of the circuit is the expected one, different loads were tested and the results were validated for the pulser complete operation range.

For these tests, MATLAB code was also developed to create pulsed waveforms with the desired voltages to apply at the input of the circuit. This code follows the same logic as the one described for the drain pulser tests and can be found in Appendix A.

The first test made to the circuit was the measurement of its response to a pulse with no load. The voltage at the output of the circuit is presented in Figure 2.28, for a pulse with a duration of 10 µs.

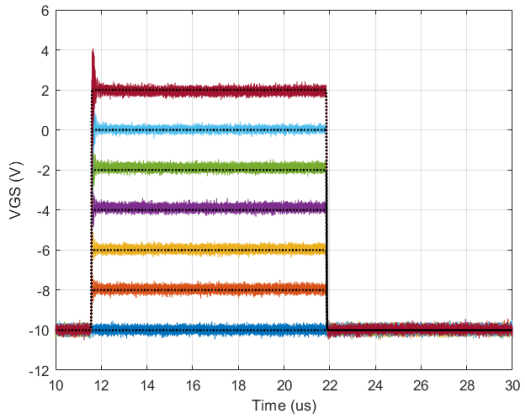
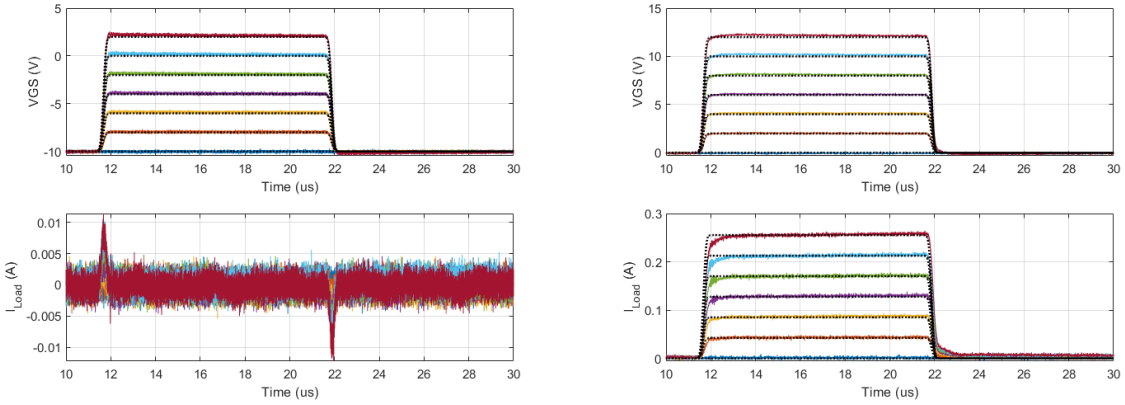


Figure 2.28 – Gate pulser output voltage for an open load, from −10 V to 2 V, with the correspondent theoretical curve in black.

Through Figure 2.28, it is possible to see that the gate pulser response is the expected one, as the measured curves overlap the theoretical ones. The pulses cover the entire operation range and the settling time is, in the worst case, of 500 ns, which is close to the expected theoretical value.

To demonstrate the circuit capability to handle different types of loads, tests with a capacitive load of 150 pF and a resistive load of 47 Ω were made. For the 47 Ω resistor, the measurements were only performed for the range of 0 V to 12 V, because it is the case when the circuit is operating as a drain pulser and will have to deliver pulsed current. The results are presented in Figure 2.29.



(a) Gate pulser output voltage and output current with a capacitive load, from −10 V to 2 V.

(b) Gate pulser output voltage and output current with a resistive load, from 0 V to 12 V.

Figure 2.29 – Gate pulser output voltage and utput current for two different types of loads, with the correspondent theoretical curve in black.

The pulses presented in Figure 2.29 still demonstrate the correct operation of the circuit in the expected settling times. It is possible to see that the circuit has a smoother response in terms of overshoot when connected to loads. Since there will always be a load in the tests to be performed, the overshoot observed in the test with an open load is not a concern.

To confirm that the gain is constant all over the circuit operation range and that it has the expected value of 12 V/V, its value for an open load and for the different types of mentioned loads is presented in Figure 2.30. As can be seen, the gain is very close to the theoretical value.

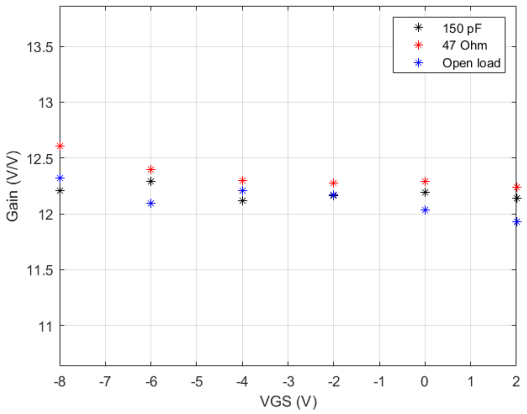


Figure 2.30 – Gate pulser gain for several loads.

With all the obtained results, it was possible to validate the design of the circuit, concluding that it operates as expected and that the results that are going to be obtained when testing active devices are going to be accurate.

2.3 Measurements in an Active Device

After all the tests performed in each pulser, the first pulsed I/V measurements were done in an active device. The device for these tests is the CGH40010F transistor from Wolfspeed, that is a 10 W RF Power GaN HEMT.

To do that, the MATLAB code developed for the previous tests was adapted to do a sweep of v_{DS} values for several v_{GS} values (and can be found in Appendix B), the complete measurement system was set up and the I/V curves were extracted. The block diagram of the complete system is presented in Figure 2.31 and the setup is shown in Figure 2.32.

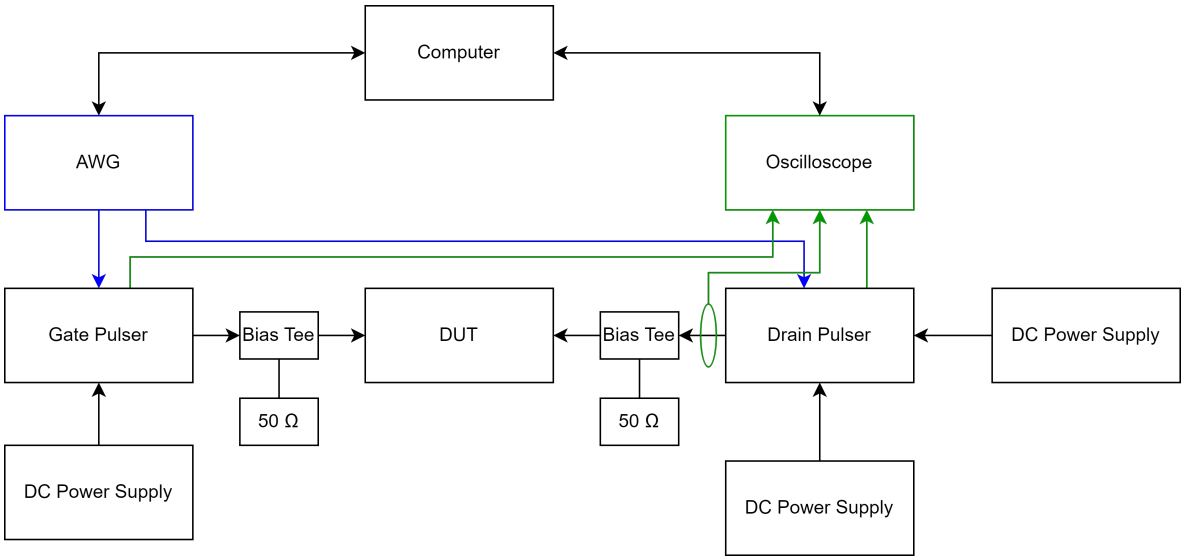


Figure 2.31 – Pulsed measurement setup block diagram.

To have the system ready to perform measurements, it is important to follow some steps to correctly switch it on and avoid getting the devices damaged. Since the transistors to be tested have negative threshold voltages, if a v_{DS} is applied when the gate pulser is off, i.e. when the v_{GS} equals 0 V, the transistor will start to conduct and can even burn. So, the gate pulser must first set a negative voltage at the gate of the device to put it in the cut-off region, and then, the drain pulser can be switched on.

Since the device is being tested with pulses, its operation conditions can be pushed to the limit, namely its instantaneous dissipated power, that is allowed to be higher than the DC limit specified in the datasheet. So, for a duty-cycle of 0.5 % and a pulse width of 6.6 µs, the instantaneous dissipated power in the device was limited to 52.5 W, and the I/V curves for a v_{GS} from −3.5 V to 1.5 V were measured, as can be seen in Figure 2.33.

With the obtained I/V curves, it is possible to see that the transistor has a maximum drain current of around 3.5 A and a threshold voltage of around −2.8 V, which is in agreement with the expected theoretical values.

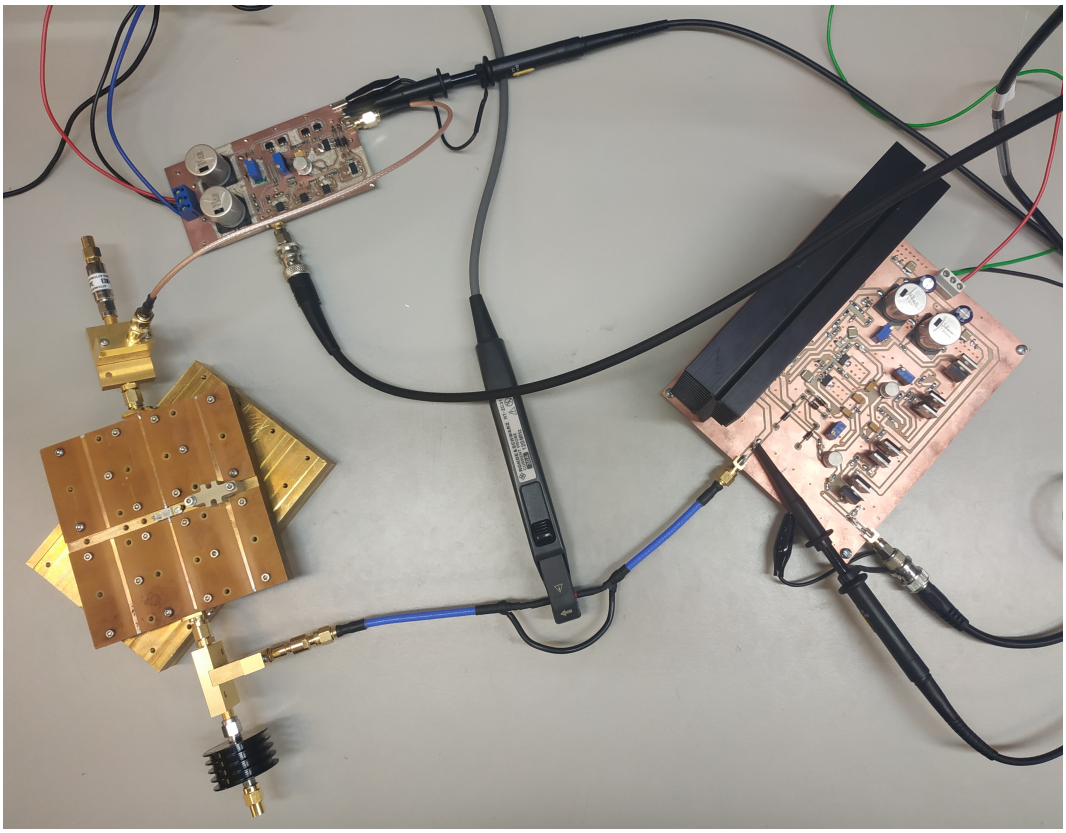
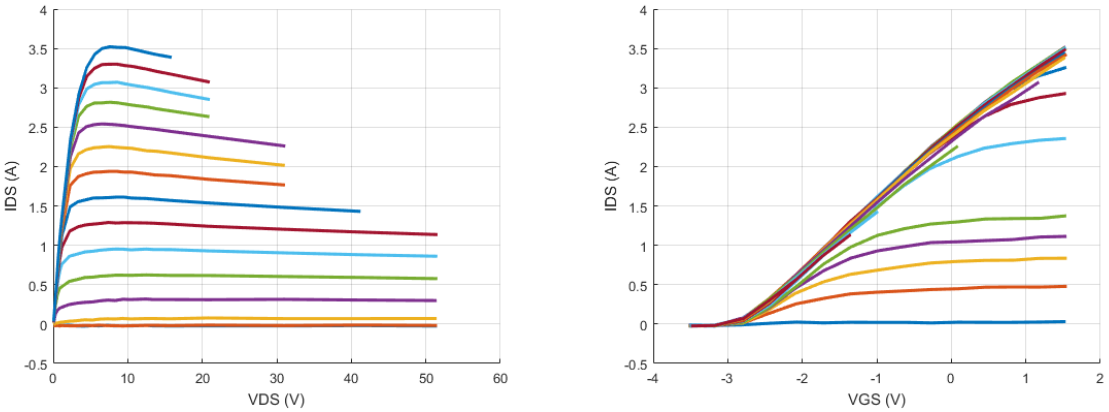


Figure 2.32 – Pulsed measurement setup.



(a) v_{DS} versus i_{DS} curves.

(b) v_{GS} versus i_{DS} curves.

Figure 2.33 – I/V curves for the CGH40010F transistor.

To plot these I/V curves, it is necessary to choose samples from the voltage and current pulses obtained at the output of the device. So, a set of the measured voltage and current pulses is presented in Figure 2.34, where, in red, the part of the pulse that is sampled and used for the I/V curves is showed.

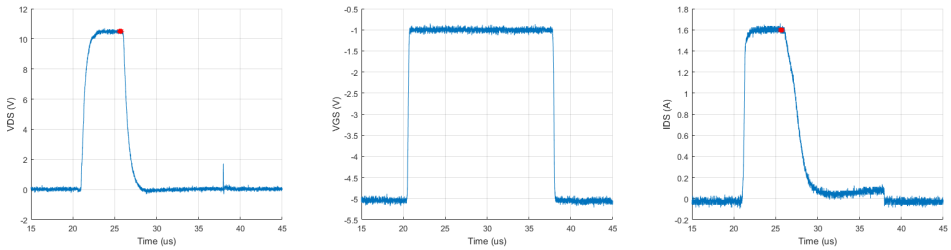
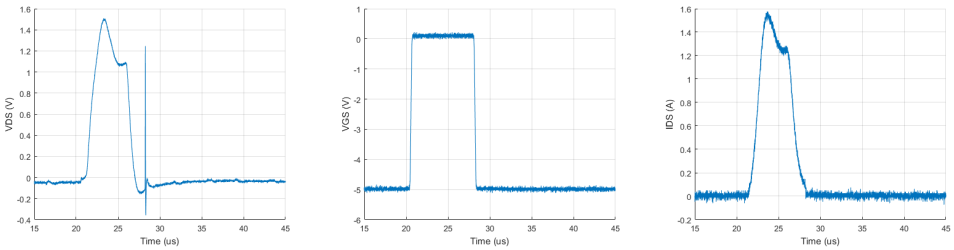
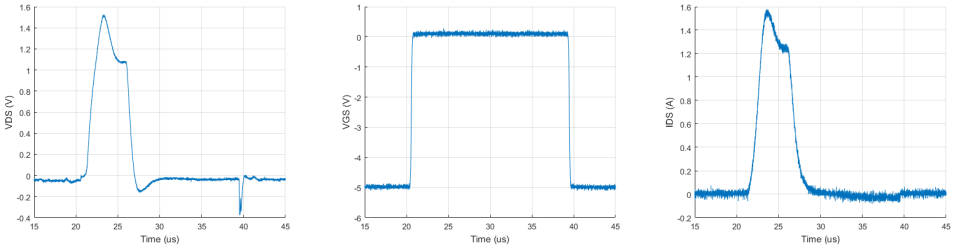


Figure 2.34 – Measured pulses for a v_{DS} of 10 V and a v_{GS} of −1 V.

Besides that, it is important to note that if the transistor is suddenly cut-off when there is current flowing, there would be a voltage spike in the bias tee inductance that can damage the DUT (or even change the trapping state, as is going to be seen in the next chapter). Therefore, to avoid this problem, the transistor should be cut-off after all the current is reduced to zero [31]. The comparison between the voltage spikes obtained when the v_{GS} of 0 V is set to −5 V right after the v_{DS} of 1 V, or after 20 µs, is presented in Figure 2.35.



(a) Measured pulses for a 10 µs v_{GS} width.



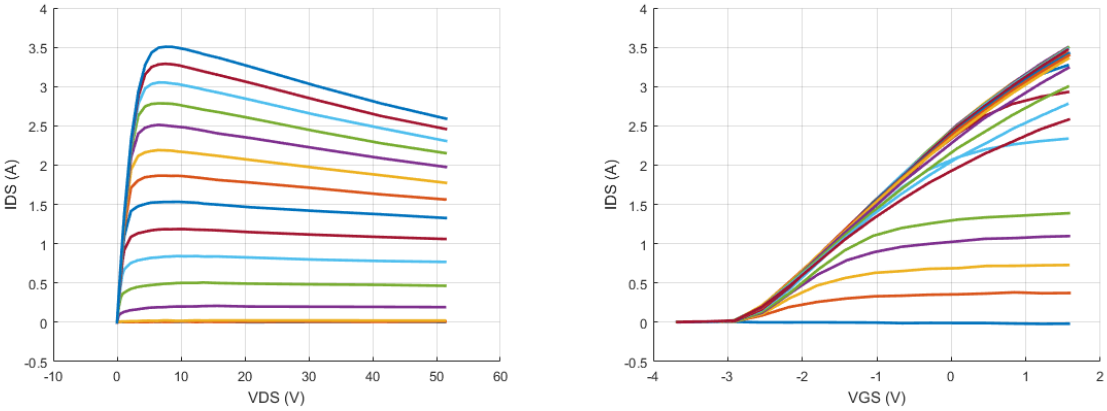
(b) Measured pulses for a 25 µs v_{GS} width.

Figure 2.35 – Measured pulses for two different v_{GS} widths.

As was explained before, when performing measurements in a GaN device, dispersive effects will occur. The dynamic behaviour associated with these effects arises from the temperature increase that the device can suffer or from the trapping effects that occur. Both phenomena cause the device current to drop, so they should be carefully analysed to try to achieve isodynamic measurements. In this section, besides presenting the transistor I/V curves, an analysis about the temperature effect in the measurements will be made. After

understanding the conditions to obtain isothermal measurements, the trapping effect can be studied.

In Figure 2.36 (and in Figure 2.33 too), it is possible to see the consequence of these dynamic effects in the I/V curves of the transistor, that clearly cause the output current of the device to drop, for the same measurement conditions of Figure 2.33, but now achieving a pulsed power of almost 150 W.



(a) v_{DS} versus i_{DS} curves.

(b) v_{GS} versus i_{DS} curves.

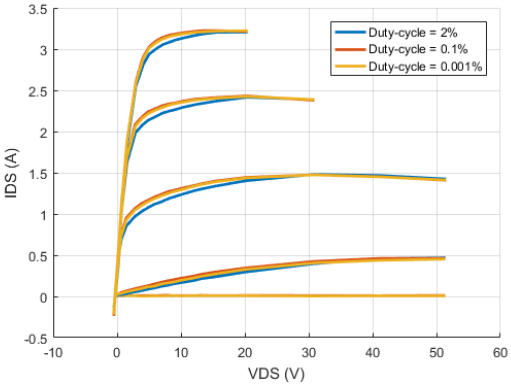
Figure 2.36 – I/V curves for the CGH40010F transistor, up to 150 W pulsed power.

There are two ways in which the temperature effect in a device can be analysed.

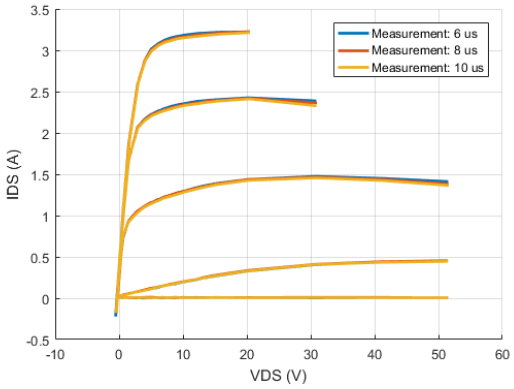
The temperature of the device is mainly given by its average dissipated power. So, to reduce it, the device should have a small duty-cycle, that makes the temperature raise negligible, but that keeps the measurement period acceptable [15]. So, a study about the impact of the duty-cycle variation in the measured I/V curves, for the same transistor, was made and is presented in Figure 2.37a. Here, the measurement of the pulse was always done in the same place to avoid other sources of temperature variation. From the obtained results, it is possible to see that for the highest duty-cycle, the current is reduced in average, so the duty-cycle should be smaller to avoid this temperature rise. The results obtained with a duty-cycle of 0.1 % and 0.001 % are similar, which can be explained by the device thermal constant being slow, making the impact of these duty-cycle values negligible. Nevertheless, the thermal constant is different for each device and that duty-cycle variation can have an impact on other transistors, despite not being relevant in this case. So, the minimum value should always be used to avoid heat dissipation.

But the reduced duty-cycle is not enough to obtain isothermal measurements. Another source of thermal effects arises from the excessive power being dissipated inside the pulse. This means that the pulse might be too wide and that the samples are extracted in a region where the device already started to dissipate. To avoid this, the samples extraction must be done as soon as possible, i.e. in the beginning of the pulse, but after any transient that can occur. With this, even if the temperature of the device rises throughout the pulse, it is not felt in the measurements. Besides this, the pulse should have the smallest width possible so the measurement period is reduced. In Figure 2.37b, the DUT I/V curves for different sampling sections in a 20 µs pulse and with a 0.001 % duty-cycle are presented. It is possible to confirm that as soon the sampling is done, less temperature effects the measurements will

feel (because the current drop is reduced), contributing to achieve isothermal measurements.



(a) Measured I/V curves for different duty-cycles.



(b) Measured I/V curves for different sampling parts of the pulse.

Figure 2.37 – I/V curves for the CGH40010F transistor with a quiescent voltage of 50 V.

Having achieved isothermal measurements, it is now necessary to understand the impact of the trapping effect.

Chapter 3

Drain Trapping Effect

The goal of the drain trapping effect study is to understand the phenomenon, so it can be possible to design a system capable of performing isodynamic measurements. This means that, besides the temperature, the trapping state has to be the same for all the measured pulses.

But, before analysing the trapping in GaN HEMT devices, a brief summary about their structure is presented, so it is easier to understand what happens during these dispersive effects. In Figure 3.1, it is possible to see the device typical structure.

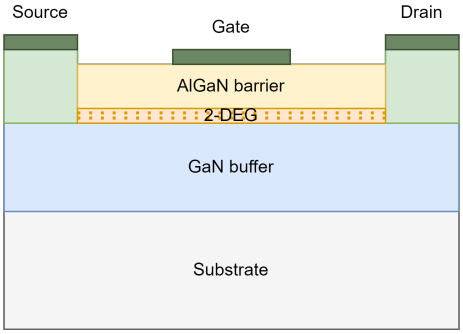


Figure 3.1 – Basic GaN HEMT schematic.

Besides the gate, drain and source terminals, the GaN HEMT is composed by 4 typical layers: the *Aluminium Gallium Nitride* (AlGaN) barrier, the *2-Dimensional Electron Gas* (2-DEG) GaN channel, the GaN buffer and the substrate. In short, the AlGaN barrier isolates the gate from the channel, so the current does not flow there, the 2-DEG is the channel where the charges flow with a very high mobility (achieving high currents), the GaN buffer is where the traps are, so it is responsible for confining the charges movement to the channel, and the substrate, usually SiC, is used to support all of these layers and spread the dissipated heat [4]. With this structure, it is possible to achieve high quality performances.

3.1 Drain Trapping Effect Analysis

As was briefly introduced before, the drain trapping effect is a dispersive phenomenon that has to be carefully taken into account when measuring GaN HEMTs. Otherwise, their real behaviour can not be fully captured.

When a high v_{DS} pulse is applied to the transistor, the current flows in the buffer in a disperse way, which is not wanted. So, besides the traps that are created in the devices due to imperfections in the fabrication process, the traps that exist under the channel, in the buffer, will capture these charges and decrease the available current. As the v_{DS} is higher, more charges will be trapped and even less current will flow [8].

This phenomenon can be seen as a potential applied to the channel that varies with the state of the trapping. As long as it is above the threshold voltage, the v_{GS} applied to a transistor will allow current to flow. But, with the trapping, that current will be reduced, so it will be as if a more negative potential is being applied to the channel. Since the v_{GS} is fixed, the only way for this potential to change with the trapping is through the changing of the potential under the channel, where the trapping occurs. So, when capturing electrons, the traps will become negatively charged and, as if there is another gate, a negative potential is created, that is added to the applied v_{GS} [10]. Furthermore, it can also be seen as if the device threshold voltage increased, for the same value of current. In Figure 3.2, a schematic of the applied voltages is presented.

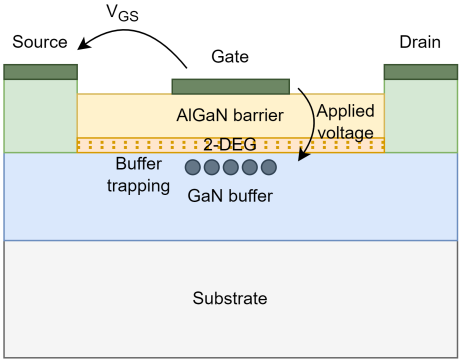


Figure 3.2 – Basic GaN HEMT schematic where charges are trapped in the buffer.

Additionally, there is one mathematical analysis that can be made in order to try to obtain isodynamic measurements. As the system can be used to extract S-parameters (small signal analysis) [15], the capacitances and inductances from the transistor can be known. With this information and with the DC pulsed measurements, a large signal model can be obtained and allow the extraction of the transistor *Transconductance* (g_m) and *Output conductance* (g_{ds}). With this, one can conclude if the obtained measurements are isodynamic through (3.1) and (3.2) [7]. If the measurements are isodynamic, the i_{DS} should be the same if a v_{GS} sweep is made for each v_{DS} or vice-versa.

$$g_m = \frac{\partial\, i_{DS}}{\partial\, v_{GS}} \Rightarrow i_{DS} = \int g_m \, d\, v_{GS} \tag{3.1}$$

$$g_{ds} = \frac{\partial\, i_{DS}}{\partial\, v_{DS}} \Rightarrow i_{DS} = \int g_{ds} \, d\, v_{DS} \tag{3.2}$$

For the same device used in the previous tests, the comparison between the I/V curves obtained with (in orange) and without (in blue) the trapping at a known state is presented in Figure 3.3. As can be seen, besides the current drop that is felt for the same v_{DS} and v_{GS} values, the knee voltage also changes, leading to a very different behaviour of the device that depends significantly on the trapping state.

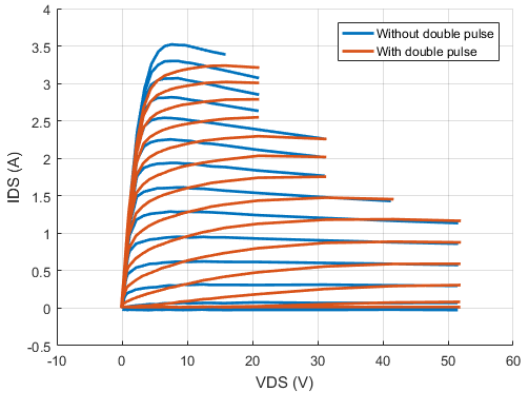


Figure 3.3 – Comparison between the I/V curves obtained with and without the trapping at a known state.

As the trapping is a dynamic phenomenon, it means that there are time constants associated with it. It has been proved that the time the traps take to capture all the free charges, i.e. the capture time constant, is very short (shorter than the pulse width of the state of the art pulsers), and that the time the charges take to be completely released, i.e. the emission time constant, is very long (reaching dozens of seconds, depending on the device) [31]. An illustration of what is expected when the trapping occurs is presented in Figure 3.4.

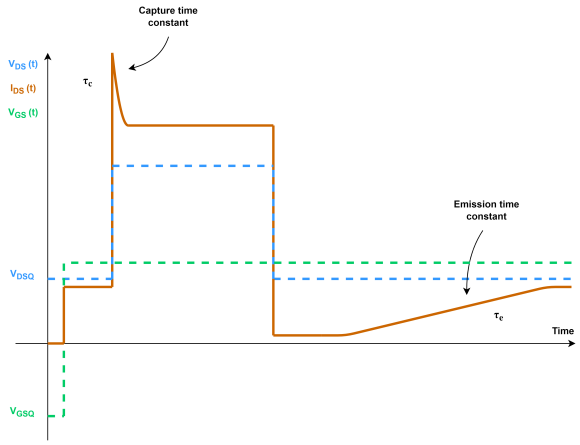
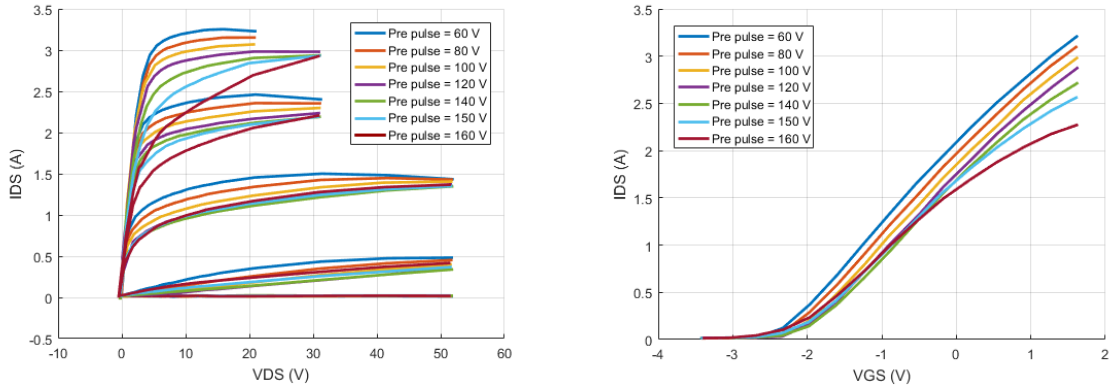


Figure 3.4 – v_{DS}, v_{GS} and i_{DS} waveforms representing what happens in the trapping effect.

To have the phenomenon at a known state, and since it is not possible to measure high v_{DS} voltages before the traps charging, two pulses can be applied to the transistor: the first pulse sets the trapping state and the second one is a voltage sweep that allows to perform I/V measurements. This technique is known as the double pulse technique and uses the fact that the capture time constant is much faster than the emission one, so the measurements can be performed in a known trapping state, right after the first pulse.

Another important fact is that the pre-pulse always has to be higher than the v_{DS} pulse. Otherwise, more charges will be captured when the measurement is performed and the trapping state will change. Since the transistor is cut-off during the pre pulse, there will be no heat dissipation and the obtained I/V curves will still be isothermal. In Figure 3.5, it is

possible to see the effect of the pre-pulse voltage on the drain current (left), and the threshold voltage variation, with $v_{DS} = 10\,\text{V}$, (right) for the CGH40010F transistor.



(a) I/V curves variation.

(b) Threshold voltage variation.

Figure 3.5 – CGH40010F I/V curves for different pre-pulse voltages.

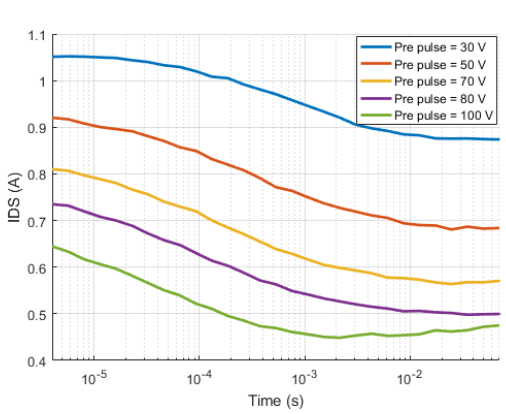
As can be seen, the higher the applied pre-pulse voltage is, the less current will flow in the transistor due to the high level of trapped charges. Also, the transistor threshold voltage becomes higher, as is expected.

Besides setting the trapping state at a known level, the pre-pulse technique allows to perform a set of measurements to obtain the capture and emission time constants of a device. As the telecommunication signals used today have a high Peak to Average Power Ratio (PAPR), the trapping can be activated in the PA and degrade the efficiency and linearity of the devices [31]. Thus, it is extremely important to characterize the capture and emission time constants of the devices and understand the dynamic nature associated with them.

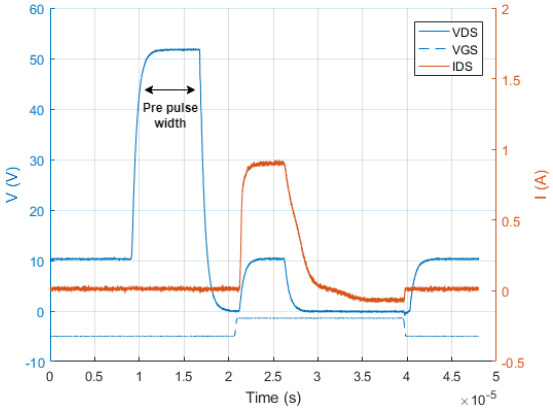
Because the time constants are associated with the time taken between the trapping and detrapping states, these measurements are performed at different trapping states. This way, to assign the current variation only to the trapping effect, it is essential to obtain them at the same temperature [31].

As the trapping state is imposed by the pre-pulse, the steady state of this effect, after the charges capture process, can be obtained if a sufficiently long pre-pulse is applied. The first measurement is performed with no pre-pulse, where the maximum possible current is obtained. Then, the pre-pulse width is varied from 0 ms to 100 ms and the current is measured for each case, until all the charges are captured. To guarantee that the charges capture is always done in the same way, it is imperative that seconds, or even dozens of seconds, are waited between the measurements with a quiescent voltage equal to the measured v_{DS}. In Figure 3.6, it is possible to observe the current variation for different pre pulses, with a v_{DS} of 10 V and a v_{GS} of $-1.5\,\text{V}$ (left) and a set of pulses used to perform this measurement (right).

From the measured curves, it is possible to see that the capture is completed after 10 ms because the current is stable after that. Since the measured v_{DS} is always the same and the first value of current presented in the graph decreases for each pre-pulse value, it is possible to conclude that there is a fast capture process at the beginning (between the measurements with no pre-pulse, where the current is maximum and equal to all pre-pulses, and the measurements with the narrowest pre-pulse) that then becomes slower until the steady state is achieved. This indicates that there are different time constants associated with this capture phenomenon,



(a) Current evolution for the charges capture process, with different pre-pulse voltages.



(b) Set of pulses demonstrating how the capture time constant can be obtained.

Figure 3.6 – Capture time constant of the CGH40010F transistor.

but only the dominant one will be calculated.

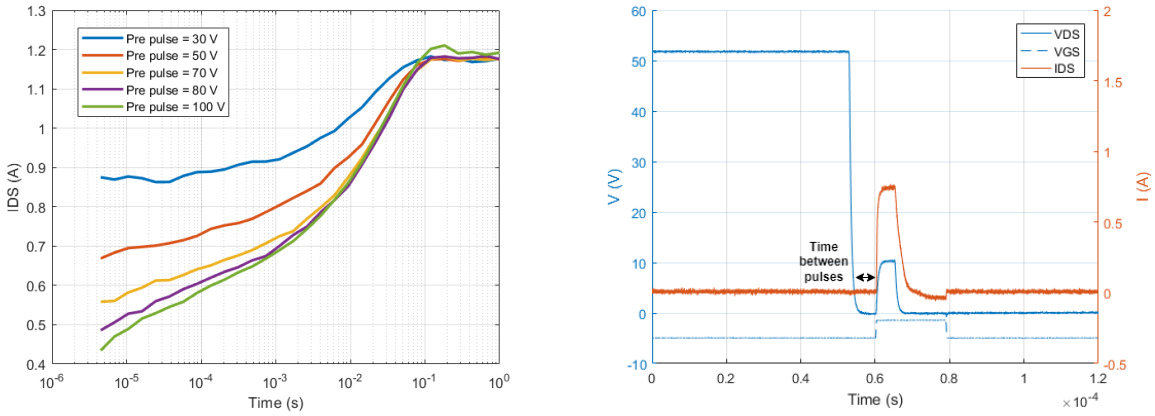
The dominant capture time constant can be obtained by the time constant value that corresponds to the maximum derivative of the current as a function of the pre-pulse width. Since the current waveform follows a decreasing exponential function, several time constants (τ) were tested to try to obtain the best fit possible between the theoretical equation and the measured current. The detailed explanation regarding the algorithm used to obtain the capture time constant values can be found in Appendix C. For the DUT, the values for the capture time constants for each pre-pulse are shown in Table 3.1. The values show a decreasing trend with the increase of the pre-pulse voltage, proving that, in the presence of more charges, the capture process of the majority of them will be faster.

Table 3.1 – Capture time constants for different pre-pulses, in the of the CGH40010F device.

Pre-pulse voltage	Capture time constant
30 V	1.1 ms
50 V	0.48 ms
70 V	0.28 ms
80 V	0.22 ms
100 V	0.062 ms

To obtain the emission time constant, it is necessary to first set the trapping at a steady state with a pre-pulse width longer than the time taken to capture all the charges of the device. Since the pre-pulse is sufficiently long, the trapping state is imposed by it and there is no need to use a quiescent voltage equal to the v_{DS}. Then, it is necessary to measure the current when the charges are being released. To do that, the time between the pre-pulse and the pulse is varied from 4.5 µs to 1 s, and the current is measured until all the charges are emitted. In Figure 3.7, it is possible to observe the current variation for different pre-pulses, with a v_{DS} of 10 V and a v_{GS} of −1.5 V (left) and a set of pulses used to perform this measurement (right).

Once again, for different pre-pulses (which correspond to different trapping states), the



(a) Current evolution for the charges emission process, with different pre-pulse voltages.

(b) Set of pulses demonstrating how the emission time constant can be obtained.

Figure 3.7 – Emission time constant of the CGH40010F transistor.

Table 3.2 – Emission time constants for different pre-pulses, in the of the CGH40010F device.

Pre-pulse voltage	Emission time constant
30 V	16 ms
50 V	21 ms
70 V	23 ms
80 V	27 ms
100 V	32 ms

current will have different values. As is expected, when all the charges are emitted, the current returns to the initial value, independently of the previous trapping state. From the measured curves, it is possible to see that the emission is finished after 100 ms.

Figure 3.7a indicates that there are different time constants associated with the charges emission process, but only the dominant one will be acquired. So, the dominant emission time constant can be obtained by the time constant value that corresponds to the absolute value of the maximum derivative of the current as a function of the time between pulses. Since the current waveform now follows an increasing exponential function, several time constants (τ) were tested to try to obtain the best fit possible. The detailed explanation regarding the algorithm used to obtain the emission time constant values can also be found in Appendix C. For the DUT, the time constant values are shown in Table 3.2. Now, the values show an increasing trend with the increase of the pre-pulse voltage, proving that the emission process is slower as more charges are trapped in the device.

To conclude, besides the current being stable at the end of the capture process and at the beginning of the emission process, those values should match, so one can confirm if the capture and emission process were done in the correct way. If the values do not match, specially if the first value of current in the emission process is not the same as the last value of current in the capture process, it is because there was some emission due to the time between the end of the pre-pulse and the measurement in the pulse. Through Figure 3.6a and Figure 3.7a, it is possible to conclude that there was already some emission, specially for the cases where the pre-pulse is higher, but it is thought that they are approximately equal. To solve this, the

pre-pulse and the pulse should have less time between each other but, due to the waveforms settling times and transients, it was considered that it was safer to wait for the pre-pulse to reach 0 V, then apply the v_{GS} and finally apply the v_{DS}.

With the measurements performed in this section, it was possible to obtain isodynamic measurements and understand the trapping time constants involved in this dispersive phenomenon. To completely validate the system, several devices with different characteristics are tested in the next section.

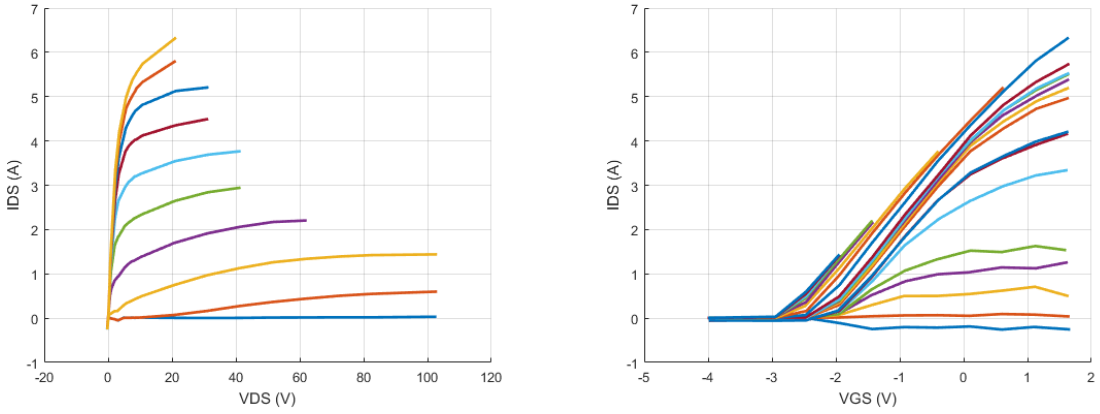
3.2 Drain Trapping Effect Characterization

Despite being possible to validate the system with the previous measurements, it is important to test several devices that can achieve higher currents and, consequently, higher power. This way, the current delivering capability of the system will be confirmed with real devices and not only with resistive loads. Also, the variability of the devices dynamic can be studied.

The previous device is rated with a DC power of 10 W, and can achieve a maximum current of around 3.5 A. So, to achieve more current, a device rated with a DC power of 50 W and another device rated with a DC power of 100 W are tested.

In this section, the I/V curves of each device are presented and the capture and emission time constants of the 50 W transistor are calculated.

Starting with the 50 W GaN HEMT, the double pulse technique was applied and the I/V curves were obtained. For a pre-pulse voltage of 160 V with 100 µs of duration, and a v_{GS} from −3 V to 1.5 V, the I/V curves are presented in Figure 3.8. As depicted in Figure 3.8, a maximum current of 6.5 A is achieved with this transistor and its threshold voltage is in the range of −3 V to −2 V.

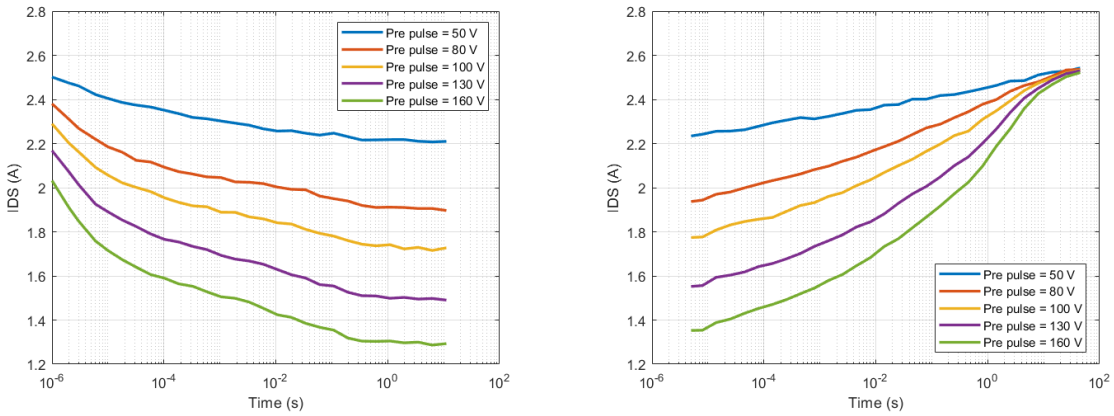


(a) v_{DS} versus i_{DS} curves. **(b)** v_{GS} versus i_{DS} curves.

Figure 3.8 – I/V curves for the 50 W GaN HEMT.

In Figure 3.9, the evolution of the current for the charge capture process (left) and the charge emission process (right), due to the trapping effect happening in the device, is presented, for different pre-pulse voltages, with a v_{GS} of −1.5 V and a v_{DS} of 20 V. For the characterization of the capture process, the pre-pulse width was varied from 0 s to 20 s and, for the emission process, the time between the pre-pulse and the pulse was varied from 4.5 µs to 80 s. Through Figure 3.9a and Figure 3.9b, it is possible to conclude that the capture and

emission process were done in the correct way because the current values at the end of the capture and at the beginning of the emission match. It is also possible to see that, for this transistor, the capture is completed after 10 s and the initial value of current is achieved after 80 s, demonstrating that the dynamics here is slower, in comparison with the CGH40010F transistor.



(a) Current evolution for the charges capture process, with different pre-pulse voltages, in a 50 W transistor.

(b) Current evolution for the charges emission process, with different pre-pulse voltages, in a 50 W transistor.

Figure 3.9 – Trapping effect time constants in a 50 W device.

Furthermore, the values of the capture time constants are presented in Table 3.3a and the values of the emission time constants are presented in Table 3.3b.

(a) Capture time constants for different pre-pulses, in a 50 W.

Pre-pulse voltage	Capture time constant
50 V	201 µs
80 V	201 µs
100 V	101 µs
130 V	101 µs
160 V	101 µs

(b) Emission time constants for different pre-pulses, in a 50 W transistor.

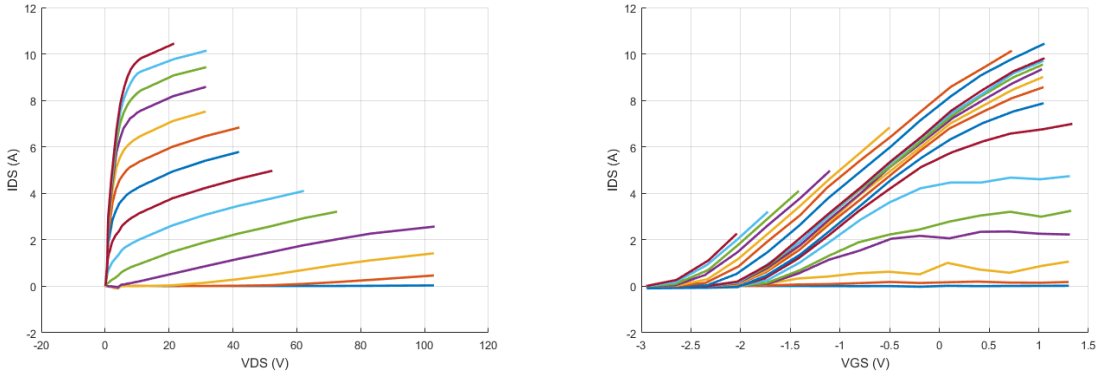
Pre-pulse voltage	Emission time constant
50 V	86 ms
80 V	94 ms
100 V	134 ms
130 V	232 ms
160 V	324 ms

Table 3.3 – Time constants values for a 50 W device.

To conclude these tests, the I/V curves of the 100 W GaN HEMT were obtained. For a pre-pulse voltage of 160 V with 100 µs of duration, and a v_{GS} from −3 V to 1.2 V, the I/V curves are presented in Figure 3.10. As can be seen, a maximum current of 10.5 A is achieved with this transistor and its threshold voltage is in the range of −3 V to −1.7 V.

For the other devices, the correspondent time constants were obtained to prove that the trapping effect has different characteristics and should be carefully analysed in each case. With this, it is possible to conclude that some devices, when subject to some signals, can activate the trapping very quickly but be in a trapping steady state for a long time, and others not.

Furthermore, a comparison between the tested transistors can be made. From the I/V



(a) v_{DS} versus i_{DS} curves.

(b) v_{GS} versus i_{DS} curves.

Figure 3.10 – I/V curves for the 100 W GaN HEMT.

curves of each transistor, it is possible to conclude that the 100 W device is able to operate at higher power than the others, as is expected by its DC rated power. And, through the values of the capture time constants obtained for the two transistors, it can be seen that the 50 W transistor has a faster capture process in terms of the dominant time constant, but takes longer to complete the process, and a slower emission process, either in terms of the dominant time constant or of finishing the complete process. As mentioned before, this demonstrates that the trapping dynamics depends largely on the device.

Finally, with the obtained results and with the performed analysis, it is possible to draw some conclusions about the work developed in this dissertation.

Chapter 4

Conclusion

The aim of this work was to build two versatile and low cost pulser heads from scratch, one for the drain and another for the gate of a transistor. This system should be able to perform accurate pulsed measurements of different devices and obtain information that could be used to model them.

The drain pulser was a high power circuit, that allowed to achieve voltages up to 160 V and a current of, at least, 15 A. To accomplish this goal, a PCB was designed and then tested with several loads so its response could be evaluated.

The first difficulty faced when designing this circuit was the components selection. Since the goal of the circuit is to have very high power pulses with the lowest settling time possible at its output, only few components met the requirements. These components led to a circuit that requires high current and high voltage at some points, making it prone to achieve instability. As the simulation did not include these behaviours, it was very difficult to predict what could happen. The three main instability reasons, that were only possible to observe after the PCB implementation, were: incorrect compensation of the circuit, incorrect bypassing in some nodes and thermal runaway that occurred in the output stages. To solve these problems, several capacitors were added in the circuit critical nodes to stabilize it and the dissipation area was increased to try to have a more efficient dissipation. To obtain the best results, several boards were designed until most of the good practices of PCB design were fulfilled. The most important ones are:

- The feedback line should be as short as possible to avoid inductive type oscillations.
- The traces width should be carefully considered according to the current flowing in it.
- The components should be placed in the board according to its function, so simpler connections are possible.
- The board ground should be of a very high quality, with several vias connecting both sides.
- The bypassing capacitors should be placed as close as possible to the components pins.

As the drain can be seen as a variable resistor with a capacitance connected from the drain to the source and to the gate (the device output capacitance), the most important analysis was to study the circuit behaviour with different resistor values and a capacitor as loads.

Despite the gain being higher than the theoretical value, it is considered that the results are still valid because the true voltage value will always be measured. Furthermore, the circuit guarantees a settling time of around 4 µs in the worst case. This happens when it is with high voltages and with a high impedance load, or when there is a low resistive load seen by the pulser, that creates a transient in the pulse. The goal was to obtain settling times in the order of 1 µs, but it is considered that the ones obtained are reasonable because it is possible to have isothermal measurements. Thus, it is possible to conclude that the circuit works as expected.

The gate pulser was a low power circuit, that allowed voltages from −10 V to 2 V and a current up to 2 A. To fulfil the objective, another PCB was assembled and several tests with loads were performed to validate the circuit response. Being the gate pulser a low power circuit, it was much easier to achieve the desired results because there were no problems regarding the stability of the circuit and the knowledge acquired when designing the drain pulser board was already applied in this case. As the gate will see the input capacitance of the device (its gate), it is imperative that the circuit is tested with a capacitor as load and, since the circuit should deliver some current, it was also tested with a resistive load. Here, the gain follows the expected value, making the measured pulses to match the theoretical ones and allowing to conclude that the results are the expected ones. The settling times are in the order of 500 ns, which is close to the expected value, because the circuit does not need to be stabilized, as before. Once again, it is considered that the circuit works as expected.

After confirming the correct operation of the developed circuits, it was time to use them to obtain pulsed measurements from the transistors. To do that, the dominant dynamic effects that are present in the devices were studied to know their impact on the measurements. First, the temperature effect was analysed in terms of the measurement duty-cycle and power dissipation inside the pulse. For that, I/V curves measured in different places of the pulse and with different duty-cycles were obtained and compared. Through these tests, it was possible to conclude that the measurements should be performed with the smallest duty-cycle possible and as soon as there is a stable region in the pulse, so thermal effects don't appear and isothermal measurements can be obtained.

Finally, a study about the trapping effect on these devices was performed, so the desired isodynamic measurements could be obtained. First, a study about the aplication of the double pulse technique with different pre-pulse voltages allowed to understand how the trapping level varies with the applied voltage. It was possible to conclude that the higher the pre-pulse voltage is, the more traps are captured, which causes the current to drop and the threshold voltage to increase. Furthermore, the time constants of the phenomenon were obtained, leading to the conclusion that the capture process becomes faster and the emission process becomes slower as the pre-pulse voltage increases, and that the capture process is faster than the emission one.

To conclude the analysis, a 50 W and a 100 W transistor were tested, proving that the system can be applied to more powerful transistors. Moreover, the capture process in the 50 W transistor was faster and the emission process slower than in the CGH40010F transistor. This demonstrates the variability of the drain trapping effect on devices.

In short, it was possible to design a drain and gate pulser circuit that fulfilled the goals specified in the beginning of this dissertation. Then, several devices were measured and tested, leading to the conclusion that the circuit can test several devices successfully and can be used to obtain measurements to model devices.

Chapter 5

Future Work

With this work, it was possible to develop a complete prototype for a pulsed measurement system and to perform measurements to characterize transistors. However, it is always important to continue the work and improve it. In this chapter, an analysis of the improvements that can be made to the system is presented.

Since the main challenge of this dissertation was solving the instability of the drain pulser circuit, most of the suggestions are related to its design.

As mentioned before, this topology faced several problems that were not completely solved, such as settling times higher than the desired goals and thermal runaway. To have faster settling times, the solution could be to use a topology that would not suffer from the stability issues that the used one did. For example, for low voltages, a voltage-series feedback topology could still be used because, as was seen for the low voltage components of the gate pulser, there were no major stability problems. Then, for higher voltages, a topology like the Tri-State Pulsed I-V system [16] could be used. Regarding the thermal runaway, thermal coupling between the MOSFETs and the BJTs should be applied in the output stages, a temperature compensation circuit could be used or even a new topology that avoids these problems by itself could be implemented [32]. Also, to protect the output stages from excessive current, it would be important to add a current limit circuit.

Another issue regarding the drain pulser circuit is the fact that, as the circuit should be supplied with very high voltages, there are not always power supplies available in the laboratories that can deliver these voltage values. So, instead of connecting different power supply channels or even connecting more than one power supply, a booster type voltage regulator could be added. This way, the circuit is supplied with lower voltages and then the booster would do the voltage step up to the desired values.

Furthermore, this circuit could be improved to operate at higher voltages by replacing the output stage MOSFETs with GaN devices (and adding more output stages to drive it). Since the GaN transistors would be inside the feedback loop and the emission of the trapping effect is very slow, the feedback would compensate the current drop and the correct values of current would still be obtained.

Finally, to measure the devices drain current, a current probe was used. These current probes are usually dependent on the used oscilloscope, which means that the same current probe can not be used with all oscilloscopes. To overcome this inconvenience, a current sense circuit could be designed to facilitate the current measurement.

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Appendix A

MATLAB code description for pulse generation

To evaluate the developed circuits response to several loads, pulsed waveforms have to be created to test them. Since the used equipment, i.e. the AWG and the oscilloscope, had not been programmed yet, it was necessary to develop MATLAB code to control them. To start, a script to send one v_{DS} and one v_{GS} pulse to the AWG was created, so the drain and gate pulsers could be tested separately. At the end, the data from the oscilloscope was saved and presented in Chapter 2.

In Figure A.1, a flowchart of the mentioned script is presented. This code can be used for either generate the v_{DS} pulses or the v_{GS} pulses, being the only difference the variable used in the code decision block.

Finally, an example of the code used to convert the waveforms to bytes is presented.

```
function [V_wave_bytes, V_Offset, V_Scale] = num2byte(handle_AWG, Wave, Source
    )
    base = 2^13;
    offset = 2^13-1;

    % Create and send waveforms
    if (max(Wave) - min(Wave) ~= 0 )
        V_Offset = (max((Wave))+min((Wave)))/2;
        V_Scale = 2/(max((Wave))-min((Wave)));
    else
        V_Offset = 0;
        if (max(Wave) == 0)
            V_Scale = 2000;
        else
            V_Scale = 1/max(Wave);
        end
    end

    V_wave_scaled = ((Wave)-V_Offset)*V_Scale;
    V_wave = round(base + offset*V_wave_scaled);

    % Extract the bytes
    V_wave_bytes = zeros(1,length(V_wave)*2);
    V_wave_bytes(1:2:length(V_wave_bytes)) = floor(V_wave/256);
    V_wave_bytes(2:2:length(V_wave_bytes)) = V_wave - floor(V_wave/256)*256;
end
```

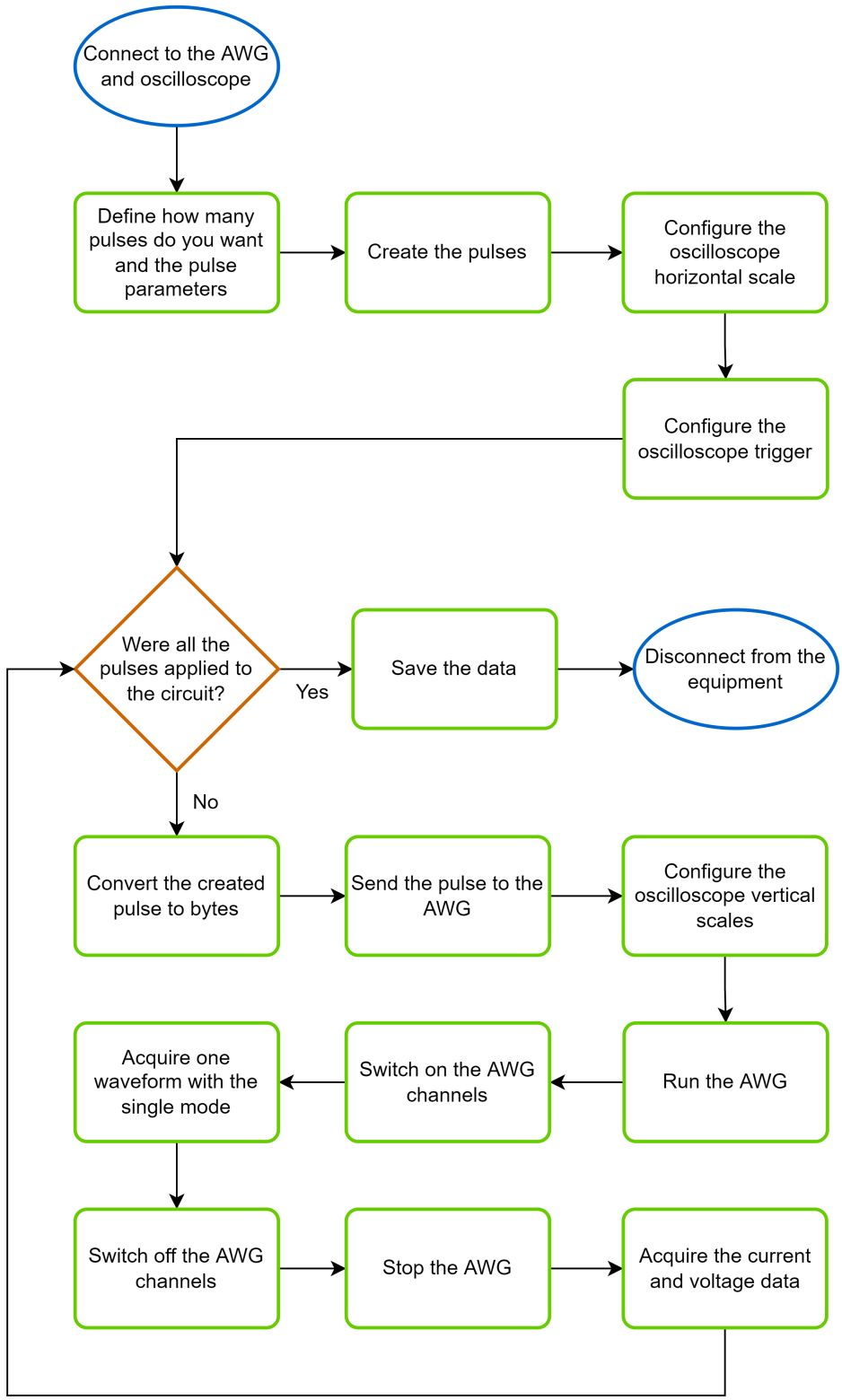

Figure A.1 – Flowchart of the code used to create one pulse, send it to the AWG and save the result from the oscilloscope.

Appendix B

MATLAB code description for double-pulse waveform generation

Furthermore, the previous code was adapted so the double-pulse configuration could be used. To apply the pulses to a transistor, it is now important to maintain a low duty-cycle, for example, the 0.001 % duty-cycle that was mentioned in Chapter 2. This means that, for a pulse of 6.6 µs, a period of 660 ms has to be set for the measurement (and a waveform of 660 ms would have to be sent to the AWG). The equipment has a certain memory so it is not possible to send a very long waveform. To have it, a short segment is sent to the AWG and it is repeated a certain number of times until the desired duration is achieved.

In Figure B.1, a flowchart of the mentioned developed script is presented.

Finally, an example of the code used to create and send one segment to the AWG is presented.

```
fprintf(handle_AWG, 'SEQuence:LENGth 2');

VDS_DC = zeros(1,1000);
VDS_DC_Name = 'VDS_DC';

[VDS_DC_bytes, VDS_Offset, VDS_Scale] = num2byte(handle_AWG, VDS_DC,
    VDS_DC_Name);

fprintf(handle_AWG, 'SEQuence:ELEM1:MARKer:STATE 1');

load_waveform(handle_AWG, VDS_DC_bytes, 2, VDS_DC_Name, 2, 2) % load the
    waveform in source 2 and segment 2

fprintf(handle_AWG, 'SEQuence:ELEM2:GOTO:STATe 1');
fprintf(handle_AWG, 'SEQuence:ELEM2:GOTO:INDex 1'); % after element 2, return
    to element 1

rep_DC = X.Trep/(1000*(X.Ts)); % X.Trep: measurement period
fprintf(handle_AWG, sprintf('SEQuence:ELEM2:LOOP:COUNt %d', rep_DC)); % repeat
     the DC segment rep_DC times
```

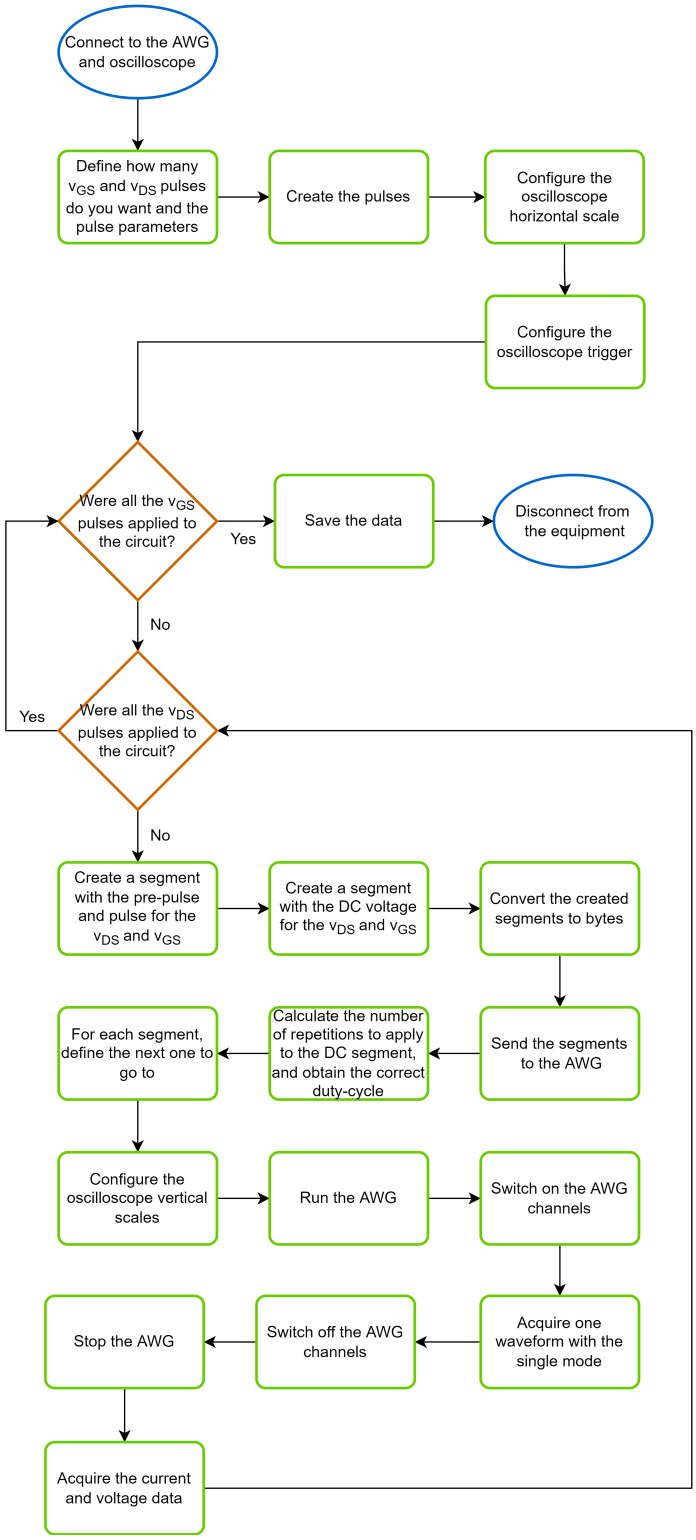

Figure B.1 – Flowchart of the code used to create the double pulse configuration, send it to the AWG and save the result from the oscilloscope.

Appendix C

MATLAB code description for time constants extraction

After extracting the i_{DS} values for different pre-pulse widths (for the capture process) and different times between pulses (for the emission process), it was necessary to extract the dominant time constant for each case. As explained in Chapter 3, the dominant time constant is given by the time constant value that corresponds to the maximum derivative of the current as a function of the pre-pulse width (for the capture process) or as function of the time between pulses (for the emission process).

So, an algorithm to calculate the time constant value was developed in MATLAB. For the capture process, the current follows a decreasing exponential function, that can be given by (C.1).

$$i_f = i_0 \cdot e^{-t/\tau} \tag{C.1}$$

where i_f is the final value of current, i_0 is the initial value of current, t is the time vector and τ is the time constant.

The code then tries to fit the exponential equation in the measured curve by trying several time constants (τ) in it. To verify if the best fit was obtained, the Normalized Mean Square Error (NMSE) between the theoretical and measured curves is calculated for each τ and the τ that corresponds to the lowest NMSE is chosen.

The pseudo code of the capture time constant calculation is presented in Algorithm 1.

Regarding the emission process, the measured current follows an increasing exponential function, that can be given by (C.2).

$$i_f = i_0 \cdot (1 - e^{-t/\tau}) \tag{C.2}$$

The evaluation of the fitting between the theoretical and measured curve is done in the same way as before.

The pseudo code of the emission time constant calculation is presented in Algorithm 2.

However, it is important to note that the measured curves are approximately exponential, which means that there are times when the theoretical exponential equation and the measured curve do not fit correctly. The region where the maximum slope of the curves occurs is what matters so, in those cases, the initial value of current used for the theoretical expression was adjusted until the theoretical curve slope overlapped the measured one. An example of the mentioned case can be found in Figure C.1.

Algorithm 1 Calculation of the capture time constant

```
function (tau) = capture(width, i_DS)
    t ← width
    i_0 ← i_DS(1) − i_DS(end)
    tau ← [1 · 10^−6 ... 1]
     for i = 1 : length(tau) do
        i_f(i) = discharge_equation(i_DS, t, tau(i), i_0)
        nmse(i) = nmse_equation(i_DS, i_f)
     end
    % Obtain the time constant
    [nmse, idx] = min(nmse)
    tau = tau(idx)
```

Algorithm 2 Calculation of the emission time constant

```
function (tau) = emission(time, i_DS)
    t ← time
    i_0 ← i_DS(1) − i_DS(end)
    tau ← [4.5 · 10^−6 ... 10]
     for i = 1 : length(tau) do
        i_f(i) = discharge_equation(i_DS, t, tau(i), i_0)
        nmse(i) = nmse_equation(i_DS, i_f)
     end
    % Obtain the time constant
    [nmse, idx] = min(nmse)
    tau = tau(idx)
```

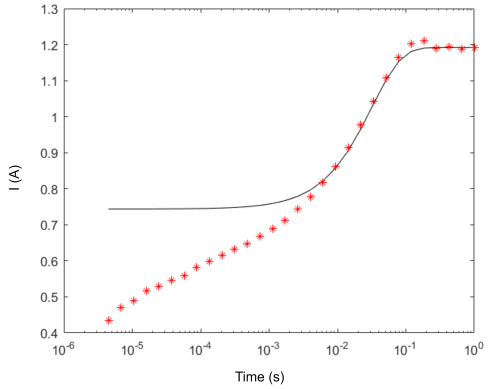

Figure C.1 – Example of the fit between the theoretical and measured curves.

Finally, the flowchart of the current evolution measurement procedure for the charges capture process is presented in Figure C.2. For the charges emission process, instead of sweeping the pre-pulse width, the time between pulses is varied.

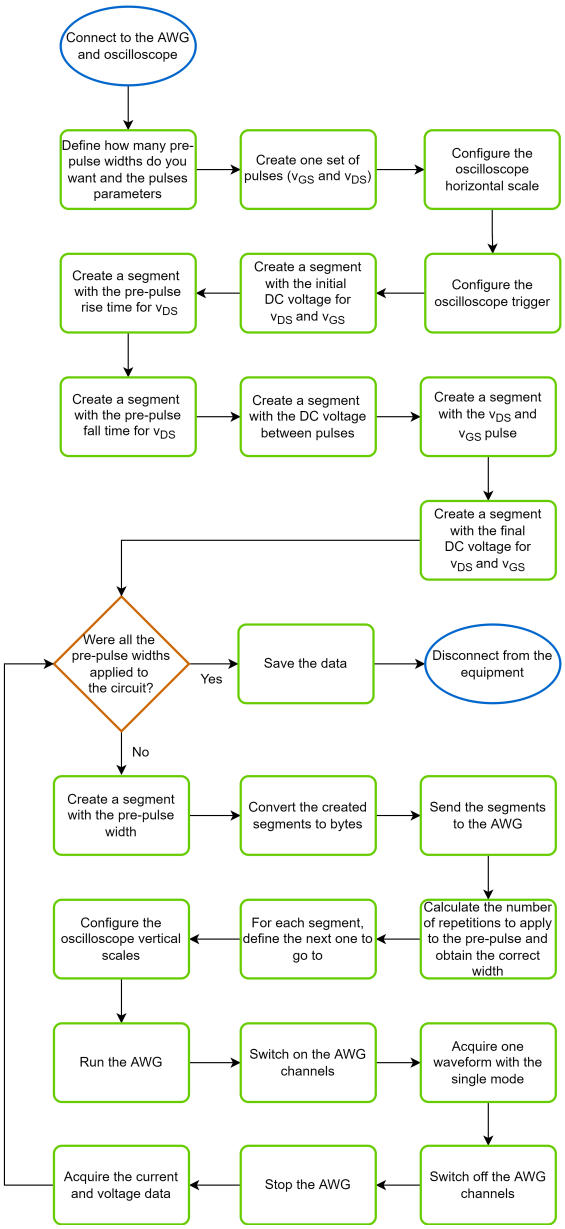

Figure C.2 – Flowchart of the code used to measure the current evolution for the charges capture process.