VOL. 20, NO. 2-2, 2021, 93-97
www.elektrika.utm.my
ISSN 0128-4428

ELEKTRIKA
Journal of Electrical Engineering

Electrical Characterization of N-MOS and P-MOS Junctionless Gate-All-Around (GAA) Mosfet for an Inverter Application

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Abstract: This paper presents a numerical simulation to examine the electrical performance of a Junctionless Gate-All-Around (JGAA) Field Effect Transistor (FET) as an inverter. The advantages of the device offer smaller threshold voltage, lower leakage current, better electrostatic control, better device performance and can operate at a high speed. Thus, to examine the potential of the device for an inverter application, the characterization of the Junctionless GAA MOSFET is performed to identify the critical device parameters in optimizing the device performance. Besides, the optimization of the device is aimed to be used to meet IRDS standard, particularly for a low power application. The characterization of electrical properties conducted based on carrier concentration, radius, gate length and drain voltage. It is found that the drain voltage and gate length give a significant impact on the threshold voltage and on-state current of the Junctionless GAA MOSFET but the minimum impact on its leakage current. However, the device parameters such as carrier concentration and radius of the channel contributed significant impact on the threshold voltage, on-state current and leakage current. The simulated result of the optimized device for N-MOS and P-MOS indicates that its electrical properties enhanced significantly. For N-MOS, the threshold voltage, current-ratio and subthreshold and drain induced barrier lowering were calculated as 0.350V, 1.606, 60 mV and 40.04 mV/dec, respectively, meanwhile for P-MOS, the threshold voltage, current-ratio and subthreshold and drain induced barrier lowering were obtained as 0.355V, 4.132, 60 mV and 60.6 mV/dec, accordingly. These results revealed that the Junctionless GAA MOSFET could meet the requirement set by IRDS for a low power application which can offer minimum leakage current and suitable to be used for an inverter application.

Keywords: Junctionless GAA MOSFET, Inverter.

Article History: received 25 May 2021; accepted 12 June 2021; published 15 September 2021.

1. INTRODUCTION

Technology roadmaps become the pillar of the semiconductor industry for many years. The first roadmap was Moore's law, which started as an empirical observation that competitive forces then turned into a prediction that became an industry roadmap. Then, the International technology roadmap semiconductor (ITRS) roadmap was developed and used by leading-edge semiconductor producers to drive the new technology needed. The recent roadmap is known as the International Roadmap Device Semiconductor (IRDS) roadmap, which provides the guideline in semiconductor end-user requirements and develops a technology roadmap based on those requirements [1]. The International Roadmap for Devices and Semiconductors (IRDS) provides a guideline to simplify research coordination, manufacturing supply and academic relating to the development and implementation of electronic systems and devices. In the past, simple shrinks of critical dimensions for CMOS logic devices offer an improvement in their performance. Advancements in patterning technology directly gave improved devices. However, as device dimensions got smaller and smaller, electrical factors such as current leakage forced innovation in device design based on material or architecture [2-5]. In 2011, the Fin-FET was introduced to manufacturing, where the gate was redesigned into a vertical structure to improve leakage performance and give better performance. Fin-FETs are expected to be replaced by Lateral Gate-All-Around structures (LGAA), then by Vertical Gate-All-Around structures (VGAA), which will then scale in 3D instead of shrinking further. Junctionless Field Effect Transistor is introduced in IRDS as an alternative device that can be implemented for a low power application.

Junctionless GAA MOSFETs are introduced to overcome the uncontrollable leakage current in conventional GAA MOSFET which susceptible to the changes in the radius of the channel. For a Junctionless

GAA, the main prerequisite of the device is the source, drain and channel region must be heavily doped. The advantages of the Junctionless GAA offers a lower leakage current and smaller threshold voltage which causes the devices operates faster at higher performances. Besides, the fabrication process also much simpler compared to the conventional structures. Most of the existing works related to the Junctionless GAA MOSFETs reported on the analysis related to their physical and electrical characteristic [4-7]. Moreover, there are fewer findings emphasized on the crucial device parameter that assisting in the optimization and application as an inverter. Thus, in this work, the characterization of the Junctionless GAA MOSFET is performed to identify the critical device parameters in optimizing the device performance. The characterized device is further continued for an inverter application and their electrical performance are compared with IRDS standard and other published works for a low power application.

2. METHODOLOGY

A Junctionless GAA MOSFET is built by using TCAD tools as shown in Figure 1[8]. Firstly, all the device parameters should be decided. Then, the idea is executed by designing the proposed device using the TCAD tool. To achieve a smaller leakage current, the thickness of the channel is recommended to be narrow and thin to allow the device to operate in depletion modes. The most important consideration in designing Junctionless MOSFET is the doping level for source, drain and channel must be heavily doped with uniform concentration to ensure the device operated under accumulation mode for both n-type or p-type. The process used to develop a Junctionless GAA MOSFET started by constructing the substrate layer followed by depositing the oxide layer and gate layer where polysilicon material is used as a gate material. Then, the source, drain, gate and channel regions are assigned accordingly before performing the electrical characterization.

Table 1. Device parameter used for N-MOS and PMOS

Device parameters	N-MOS	P-MOS
Doping (cm^{-3})	$1.5x10^{19}$	$1.0x10^{19}$
Length of source and drain (nm)	5.10	5.10
Gate length (nm)	1000	1000
Oxide thickness (nm)	6.00	6.00
Radius (nm)	2.50	5.00
V_{DS} (V)	0.01	0.01
Gate thickness (nm)	3.00	3.00
Mobility (cm^2/Vs)	90	45
Doping cm^{-3}	$1.5x10^{19}$	$1.0x10^{19}$

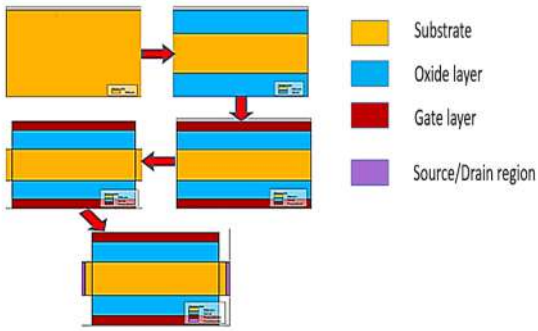

Figure 1. Process to build the Junctionless GAA MOSFET.

3. RESUTLS AND DISCUSSION

In this section, validation of the device parameters is performed by comparing its electrical behaviour with published data meanwhile characterization of the developed device will be further discussed based on drain voltage, radius, gate length and doping concentration.

3.1 Validation

Table 1 shows the device parameters used to characterize the device performance of the Junctionless Gate- All-Around MOSFET. Meanwhile, Table 2 indicates the device parameters used to validate the device parameter used in this work with published data. From Figure 2, it should be noticed that the value of device parameters used is in lined with published work where the discrepancy is estimated as less than 5%. Thus, the device parameters used in this work in the acceptable range.

Table 2. Validation of developed device with published data.

Device parameters	Our work	Published data [9]
Doping (cm^{-3})	$2.5x10^{18}$	$1x10^{19}$
Work function (V)	4.67	-
Length of source & drain (nm)	5.10	-
Gate length (nm)	1000	1000
Oxide thickness (nm)	6.00	5.00
Radius (nm)	5.00	5.00
V_{DS} (V)	1.00	1.00
Gate thickness (nm)	3.00	-
Mobility (cm^2/Vs)	90	100

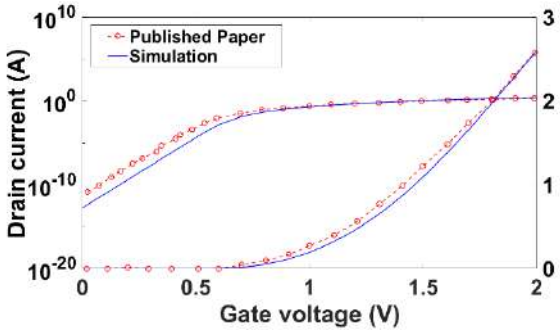

Figure 2. A comparison between simulated and published data.

3.2 Variation of drain current versus gate voltage (I_{ds}-V_{gs}) graph analysis

Figure 3 depicts the variation of drain current against the gate voltage for various drain voltages, gate lengths, channel radii, and carrier concentrations. In general, the variation of those parameters can give a direct impact on its electrical properties as indicated by the changes in the I_{ds}-V_{gs} for both P-MOS and N-MOS. The drain voltage and gate length give a significant effect on the threshold and on-state current as shown in Figure 3(a-b) but less impact on its leakage current. However, the device parameters such as carrier concentration and radius of the channel contributed to the changes of the threshold voltage, on-state current and leakage current as seen in Figure 3(c-d).

From these results, the changes of the radius and carrier concentration are the critical parameters need to be considered when optimizing the device performance. The changes of simulated results based on drain voltages, gate length, radius, and doping is aligned with reported data in [10-11].

3.3 Device Optimization and benchmarking.

Figure 4 shows the I_{ds}-V_{gs} for P-MOS and N-MOS Junctionless GAA MOSFET. The electrical parameters of the device were extracted and tabulated in Table 3. According to the latest IRDS prediction (2018), the targeted threshold voltage, current ratio and subthreshold swing for low power or high-density application are reported as 363 mV, 1.271×10^7 and 75mV/dec respectively. For DIBL, the targeted value is less than 100 mV/V. In overall, the behaviour of the developed device exhibited much better electrical performance in comparison to other published work in term of its threshold voltage, current ratio and subthreshold swing. Despite higher the drain induced barrier lowering, the values are still considered in the ideal range. Thus, the electrical performance of the developed device summarized in Table 2 indicates that the developed device is suitable to be used for a low power application since the device could offer minimum leakage current [9].

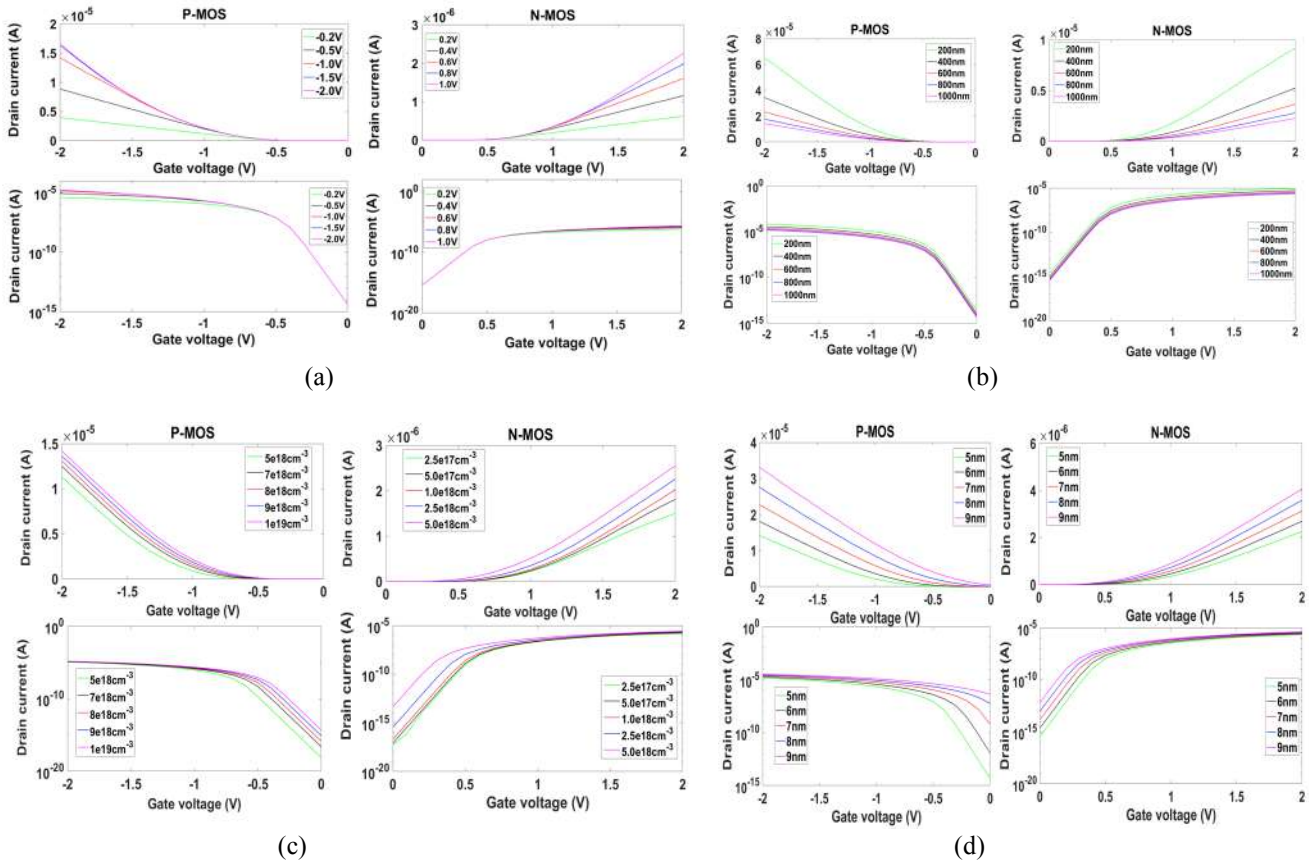

Figure 3. Variation of drain current versus gate voltage (I_{ds}-V_{gs}) for different (a) drain voltage, (b) gate length, (c) carrier concentration and (d) radius of the channel.

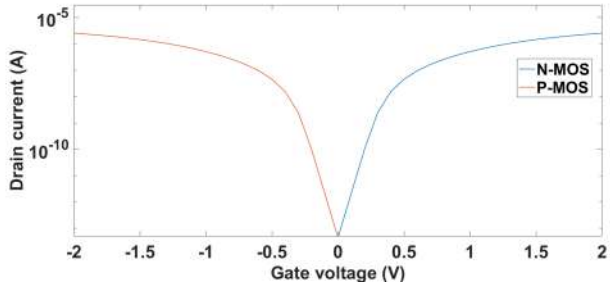

Figure 4. The drain current versus gate voltage for P-MOS and N-MOS Junctionless GAA MOSFETs.

Table 3. Validation of developed device with published data.

Device type	V_{th} (mV)	$I_{on}/I_{off}(10^7)$	SS (mV/dec)	DIBL (mV/V)	**refs**
Junctionless GAA MOSFET (N-MOS)	350	1.606	60	40.404	This work
Junctionless GAA MOSFET (P-MOS)	-355	4.132	60	60.606	This work
GAA MOSFET	394	0.1	113.891	-	[12]
Junctionless GAA MOSFET	-	0.0714	73	13	[13]
Junctionless Double Gate MOSFET	350	-	110	65	[14]

4. CONCLUSION

In this work, a Junctionless GAA MOSFET structure is created and its electrical characteristics were simulated using the TCAD tool. The Junctionless type of GAA MOSFET is achieved by applying homogenous doping at the source, drain and channel regions and the doping must be heavily doped. The drain voltage and gate length have a significant impact on the threshold voltage and on-state current of the Junctionless GAA MOSFET but less impact on its leakage current. Nevertheless, the device parameters such as carrier concentration and radius of the channel contributed to the changes of the threshold voltage, on-state current and leakage current. The electrical performance of the optimized device revealed that the Junctionless GAA MOSFET can meet the requirement set by IRDS for a low power application that can offer minimum leakage current. The junctionless device also can be implemented as a basic circuit like an inverter and therefore could be used for a complex application such as a memory application that needs high performance with minimum leakage current.

ACKNOWLEDGMENT

The authors would like to acknowledge the support from the Unversiti Teknologi Malaysia for providing an excellent research environment to make this work possible.

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