Soft-Switching Solid-State Transformer (S4T) with Reduced Conduction Loss

Liran Zheng, *Student Member, IEEE*, Rajendra Prasad Kandula, *Member, IEEE*, and Deepak Divan, *Life Fellow, IEEE*

***Abstract*—Solid-state transformers (SSTs) are a promising solution for photovoltaic (PV), wind, traction, data center, battery energy storage system (BESS), and fast charging electric vehicle (EV) applications. Traditional SSTs are typically three-stage, i.e., hard-switching cascaded multilevel rectifiers and inverters with dual active bridge (DAB) converters, which leads to bulky passives, low efficiency, and high EMI. This paper proposes a new soft-switching solid-state transformer (S4T). The S4T has full-range zero-voltage switching (ZVS), electrolytic capacitor-less dc-link, and controlled dv/dt which reduces EMI. The S4T comprises two reverse-blocking current-source inverter (CSI) bridges, auxiliary branches for ZVS, and transformer magnetizing inductor as reduced dc-link with 60% ripple. Compared to the prior S4T, an effective change on the leakage inductance diode is made to reduce the number of the devices on the main power path by 20% for significant conduction loss saving and retain the same functionality of damping the resonance between the leakage and resonant capacitors and recycling trapped leakage energy. The conduction loss saving is crucial, being the dominating loss mechanism in SSTs. Importantly, the proposed single-stage SST not only holds the potential for high power density and high efficiency, but also has full functionality, e.g., multiport DC loads integration, voltage regulation, reactive power compensation, unlike traditional single-stage matrix SST. The S4T can achieve single-stage isolated bidirectional DC-DC, AC-DC, DC-AC, or AC-AC conversion. It can also be configured input-series output-parallel (ISOP) in a modular way for medium-voltage (MV) grids. Hence, the S4T is a promising candidate of the SST. The full functionality, e.g., voltage buck-boost, multiport, etc. and the universality of the S4T for DC-DC, DC-AC, and AC-AC conversion are verified through simulations and experiments of two-port and three-port MV prototypes based on 3.3 kV SiC MOSFETs in DC-DC, DC-AC, and AC-AC modes at 2 kV.**

Keywords—Solid-state transformer (SST), power electronic transformer (PET), high-frequency link (HFL), soft-switching solid-state transformer (S4T), dc transformer (DCT), current-source converter (CSC), MVDC, smart grid, distributed renewable energy resource (DER).

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I. INTRODUCTION

SOLID-STATE transformers (SSTs) are a promising solution in the future grid as a replacement for conventional line-frequency transformer in distribution grid [1]-[4], data center [5]-[7], renewable energy sources and energy storage integration [8], traction [9], and other applications [10]-[12]. As the key power conversion component to integrate energy sources and loads into the smart grids, it is desirable for the SST to have the following features: (1) high efficiency, (2) high power density, (3) capability of integrating AC or DC resources with four-quadrant power flow and buck-boost voltage conversion ratio, (4) low EMI, (5) high reliability, and (6) reasonable cost.

The state-of-the-art SST topology typically consists of three-stage power conversion: a hard-switching inverter, an isolated bidirectional DC-DC converter like dual active bridge converter (DAB) [13]-[14], and a hard-switching cascaded multilevel rectifier [15]-[18]. Such circuit configuration has advantages including well-established sub-circuit topologies and controls, capability to integrate various DC/AC loads and sources with bidirectional power flow, and modularity for redundancy and high reliability. However, the state-of-the-art topology does have some limitations. First, the hard-switching inverter and rectifier should be designed for lower switching frequency than the soft-switching converters to limit the switching loss, e.g., 300-400 Hz with Si devices in [19]-[20] and 3 kHz with SiC devices in [3], which means bigger passives. Second, for MV converter, normally SiC devices are preferred thanks to its higher blocking voltage ratings and lower losses, which results in >50kV/μs dv/dt and hence EMI issue [3], [15]. Third, the DAB can only achieve ZVS and controlled dv/dt within a certain range, which translates to reduced efficiency and higher EMI for non-ZVS region in voltage buck-boost and full load-range operation [13]-[14].

In existing literature, single-stage converters like matrix converter or its variants adapted as SSTs can potentially achieve better trade-off between efficiency and power density [15], [21]-[24]. However, the functionality is limited due to the lack of dc-link and the lack of buck-boost capability, which is one of the major disadvantages preventing the matrix converter's industry adoption. Moreover, when leakage inductance is non-negligible in MV converters due to high isolation requirement, voltage spikes during commutation can occur [21]-[24].

Another class of the single-stage SST is derived from current-source converter, which has current-source dc-link and

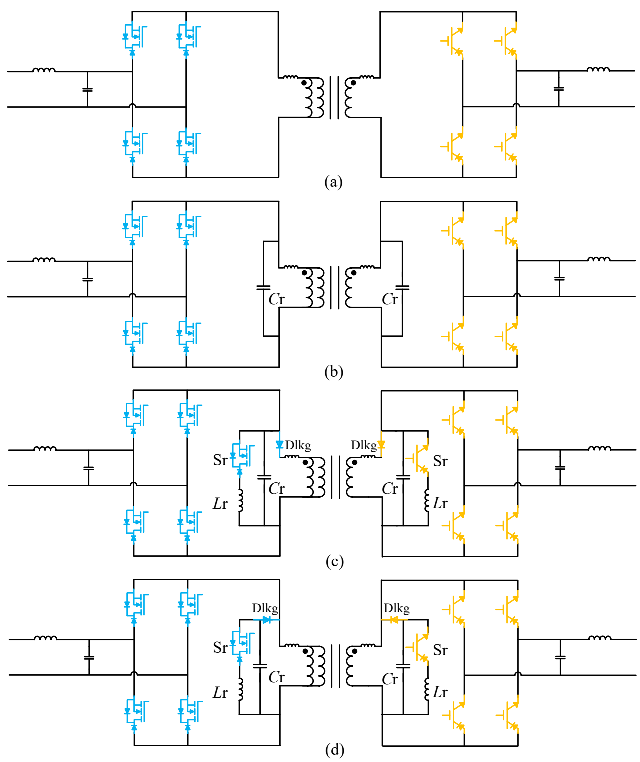


Fig. 1. Basic circuits of the single-stage solid-state transformer (SST). Circuit schematics are shown for MV DC to LV DC conversion but the same concept can be extended for all other configurations such as AC-DC, AC-AC, etc. (a) Dynamic-current converter (Dyna-C) [25]. (b) ZVS isolated HF-Link converter [26]. (c) The prior soft-switching solid-state transformer (S4T) [27]-[28]. (d) The proposed S4T with reduced conduction loss.

therefore can achieve the same full functionality as three-stage SSTs, e.g., buck-boost operation, reactive power compensation, multiport dc resources integration, etc. Existing circuits in this class include Dyna-C converter [25], ZVS isolated HF-Link converter [26], and soft-switching solid-state transformer (S4T) [27]-[28] as shown in Fig. 1. Circuit schematics are shown for MV DC to LV DC conversion but the same concept can be extended for other configurations such as AC-DC, AC-AC, etc. The Dyna-C converter in Fig. 1 (a) has a simple circuit topology. However, as the Dyna-C is a hard-switching converter, the switching loss can be large which can compromise the trade-off between efficiency and power density and the EMI issue can be severe. In [26], a ZVS isolated HF-Link converter in Fig. 1 (b) is proposed, where ZVS is enabled by the resonant capacitors (C_{r}). However, the resonant time, i.e., the lost duty cycle is large because the resonant capacitors resonate with the transformer magnetizing inductance in each switching cycle for ZVS. Moreover, it operates in nearly critical conduction mode with large transformer-winding current ripple. Hence, the efficiency can potentially be limited. With short resonant time thanks to the resonant inductors (L_{r}), the S4T in Fig. 1 (c) has unique benign features and potential to achieve full-range ZVS, full functionality the same as three-stage SSTs, and reduced EMI compared to the hard-switching counterpart. However, one major issue that limits the efficiency is the leakage diodes ($\mathrm{D_{lkg}}$) in the main power path to manage the interaction between the leakage inductance and the resonant capacitors [27]-[29]. It ends up with five devices (two switches and three diodes) in the main current conduction path. The additional leakage diodes can increase the number of devices on the main current path by 25% from four to five and lead to significant conduction loss penalty.

It should be noted that generally the conduction loss, especially from LV devices, is the major loss mechanism in the state-of-the-art SST prototypes and the efficiency of the SST is one of the major challenges that impede its industry adoption [30]. Two state-of-the-art prototypes are used as examples. In [5], the semiconductor conduction loss accounts for more than 50% of the total loss of the DC-DC SST at full power. In [10], more than 60% of the total loss in the AC-AC SST at full power is attributed to the devices. With SiC diodes, line-frequency unfolders, and the ZVS technique applied to SiC MOSFETs [31], most of the device loss should be conduction loss in [10]. Moreover, the transformer loss is mainly limited by the magnetic material and therefore cannot be improved significantly [5]. Therefore, to further improve the efficiency of the S4T, it is critical and effective to avoid the additional conduction drop from the leakage diodes in the S4T circuit to achieve a minimal conduction path of four devices instead of five in the prior S4T.

To summarize, existing topologies cannot achieve all the desirable features of the SST as mentioned in the beginning of this section. This paper proposes a new S4T with reduced conduction loss in Fig. 1 (d) to address all the above issues. To be exact, the proposed converter has potential to achieve the following desirable features of the SST: (1) high efficiency thanks to the minimal conduction path (compared to [27]-[28]) and full-range ZVS, (2) high power density thanks to its single-stage power conversion and its reduced dc-link by tolerating higher ripple on its dc-link, (3) unlike matrix converter, *full* functionality the same as the three-stage SST of integrating AC or DC resources with four-quadrant power flow and buck-boost voltage conversion ratio, (4) reduced EMI thanks to the controlled dv/dt, (5) high reliability with redundant modules and no usage of dc-link capacitors in the topology. Compared to the prior S4T in [27]-[28], an effective change is made to achieve 20% fewer devices on the main current path for significant conduction loss saving. As mentioned, the conduction loss is the major loss mechanism and hence the conduction loss saving is critical. It will be shown in Section II that the leakage management diodes can be moved from the main power path to the resonant branch and retain the functionality of managing interactions between the leakage inductance and the resonant capacitor and recycling trapped leakage energy. In addition, this change enables a desirable feature of preventing ZVS failure. C_{r} energy will not be dumped into the switch when ZVS is not achieved under wrong command from controller or other non-ideal cases.

The paper is organized as follows. The basic operation principle is introduced in Section II. Section III presents key design equations and parameters for a 25 kVA 600V - 2.5 kV converter prototype. An electric drive simulation is provided in Section IV to verify the capability of the proposed S4T for

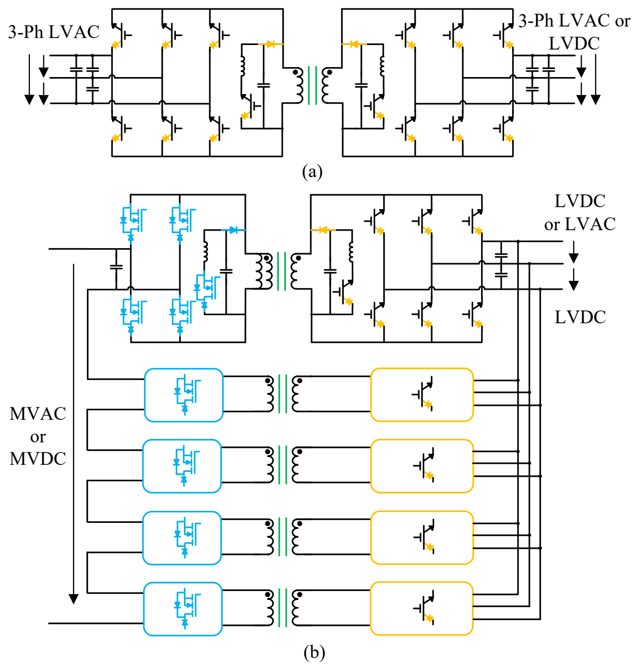


Fig. 2. The proposed soft-switching solid-state transformer (S4T) is universal and can be configured to convert three-phase AC, single-phase AC, or DC to three-phase AC, single-phase AC, or DC. Some of the possible configurations: (a) LV application, and (b) MV stacked application. A modular approach is applied for scalability to high-voltage and/or high-power applications.

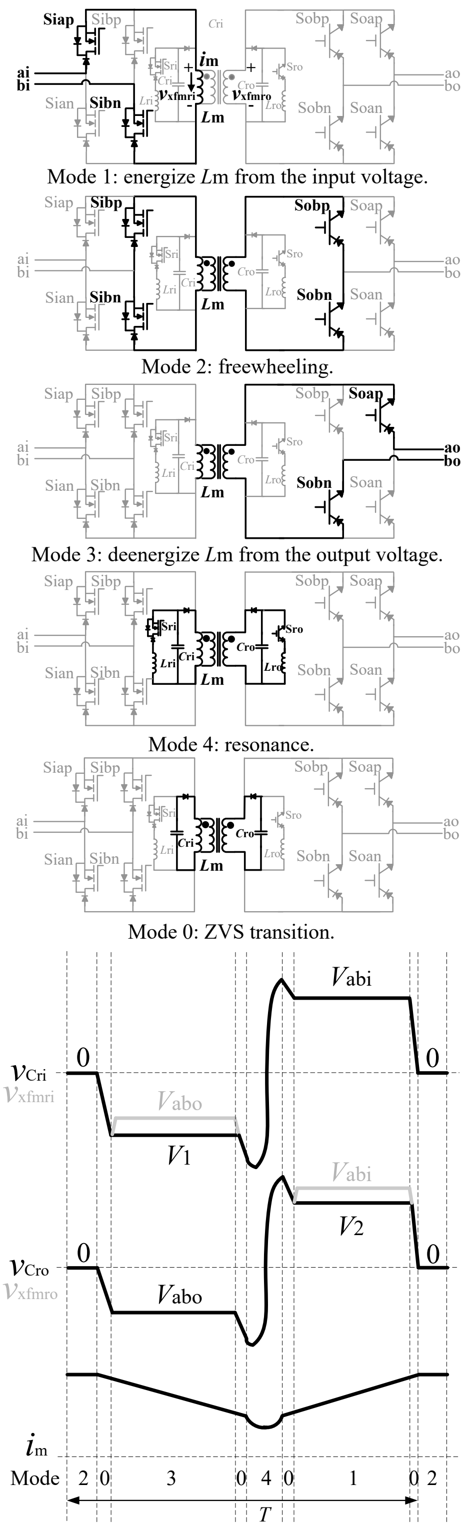


Fig. 3. Conceptual operation waveforms of the proposed soft-switching solid-state transformer (S4T) with reduced conduction loss. Energy is transferred from the input to the magnetizing inductance in mode 1. Then, the energy is released to the output from the magnetizing inductance in mode 3. Mode 0 and mode 4 are for the ZVS. The magnetizing inductance (L_m) is the dc-link inductor of this current-source based converter. Most of the time in a switching cycle, v_{xfmri} and v_{xfmro} are equal to and overlap v_{Cri} and v_{Cro}, respectively. $V_2 < V_{abi}$ and $V_1 < V_{abo}$ are due to the leakage inductance and the leakage management diode.

LVAC conversion to deliver high-quality voltages and currents with variable output frequency and inductive load. In Section V, 2 kV experimental results verify the S4T for MVDC and MVAC multiport conversion with voltage buck-boost capability and further prove the universality of the S4T for single-stage DC-DC, AC-DC, and AC-AC conversion. A comparison between the proposed S4T and existing topologies are presented in Section VI. Section VII concludes the paper.

II. Possible Configurations, Operation Principle, and Key Commutation Analysis of the Proposed Soft-Switching Solid-State Transformer (S4T)

The proposed S4T with reduced conduction loss is able to accommodate various bidirectional or four-quadrant isolated power conversion applications. Such a universal module can interface AC or DC, single-phase or multi-phase loads or sources. Some possible configurations are shown in Fig. 2 (a)-(b) for LV applications and MV applications, respectively. As shown in Fig. 2, converter modules can be connected in series or parallel for scalability to high-voltage and/or high-power applications [4], [11]. Moreover, two bidirectional DC sources/loads can be integrated as shown in Fig. 2 (b). The number of phase legs can be increased for more than two DC sources/loads. Here, the LV sources or loads include but are not limited to motor drives, EV chargers, PV, and energy storage. Filter capacitors of the S4T need to be sized to fulfill specific ripple or stability requirements of the interfaced source or load to reduce the switching-frequency or double line-frequency ripple.

The basic operation principle of the proposed S4T with reduced conduction loss is shown in Fig. 3. For simplicity, a two-leg variant is described, while the same principle can be applied to multi-leg configuration in Fig. 2. Each switching cycle of the S4T can have two or more active vectors, which depends on the number of input and output and the number of phases of the input and the output. During the charging active vector, or mode 1 in Fig. 3, the voltage across the transformer is positive and energy is delivered from the source to the magnetizing inductance (L_{m}) to increase the magnetizing current (i_{m}). During the discharging active vector, or mode 3 in Fig. 3, the voltage across the transformer is negative and energy is transferred from the magnetizing inductance to the load. Between these active vectors, the ZVS transition state or mode 0 is inserted to achieve the ZVS, during which the resonant capacitor (C_{r}) voltages are discharged by the magnetizing current. The switches corresponding to the incoming active vectors can be turned on when the voltage across them which is the voltage difference between the filter capacitor and the resonant capacitor is zero. On the other hand, the resonant state, mode 4 is used to flip the resonant capacitor voltages so that the active vectors sorted from the highest voltage level to the lowest voltage level can achieve the ZVS sequentially. Note that as shown in Fig. 3, the ZVS transition state, i.e., mode 0 can be inserted before the resonant state, i.e., mode 4 to ensure the resonant capacitor (C_{r}) voltages are negative enough before mode 4 so that the resonant capacitor voltages will be higher than V_{abi} after the resonant state to ensure the full-range ZVS. Freewheeling state, mode 2, is inserted when necessary to ensure a constant switching frequency.

The detailed commutation process of the ZVS and the leakage inductance management are shown in Fig. 4. Assume that now the converter is in mode 2, the freewheeling state in Fig. 3, and v_{Cro} is at essentially zero voltage. Then, $\mathrm{S_{ibp}}$, $\mathrm{S_{ibn}}$, $\mathrm{S_{obp}}$, and $\mathrm{S_{obn}}$ can be turned off. Subsequently, the converter enters mode 0 and the two resonant capacitors are discharged as shown in Fig. 4 (a). Once v_{Cro} is discharged to the same voltage level of V_{abo}, switches $\mathrm{S_{oap}}$ and $\mathrm{S_{obn}}$, i.e., the two switches in Fig. 4 (a), can be turned on with zero voltage across them and hence the ZVS is achieved. Then, the converter goes into mode 3. In mode 3, the leakage management diodes ($\mathrm{D_{lkg}}$) in Fig. 4 (b) and (c), corresponding to the proposed S4T and the prior S4T respectively can damp the resonance between C_{ri} and the leakage inductance (L_{lkg}). In the phase-plane diagram in Fig. 4 (d), during the resonance between L_{lkg} and C_{ri}, i_1 decreases and v_{Cri} increases as the energy of the leakage inductance is gradually recycled into C_{ri}. When i_1 approaches zero, the resonance ends because $\mathrm{D_{lkg}}$ snaps off and prevents i_1 from becoming negative. Due to the existence of the main devices' diodes in Fig. 4 (b) and (c), $\mathrm{D_{lkg}}$ can be moved from the main power path to the auxiliary branches to save significant amount of conduction loss. With this change, the resonance still ends when i_1 approaches zero and the energy trapped in the leakage is recycled to C_{ri}. This explains the derivation of the proposed S4T from the prior version. After $\mathrm{D_{lkg}}$ snaps off and starts to block the voltage difference between v_{xfmri} and v_{Cri}, the voltage across the transformer (v_{xfmri} in Fig. 3) is equal to the filter capacitor voltage (V_{abo}) which is impressed on L_{m} from the other side of the transformer. As can be observed in Fig. 3, v_{Cri} and v_{xfmri} have the same peak voltage stress for this bidirectional converter, which the main devices see in the prior S4T and the proposed S4T, respectively. The current flowing through the main devices synthesizes load current and is determined by the load current requirement, which remains the same between the prior S4T and the proposed S4T. Therefore, the proposed S4T retains all the advantages of the prior S4T with the same main-device rating and achieves minimal conduction path with reduced leakage-diode current rating by moving the auxiliary diodes away from the main current path for large conduction loss savings. Importantly, the proposed S4T basically only has advantages and no disadvantages compared to the prior S4T, to the authors' best knowledge.

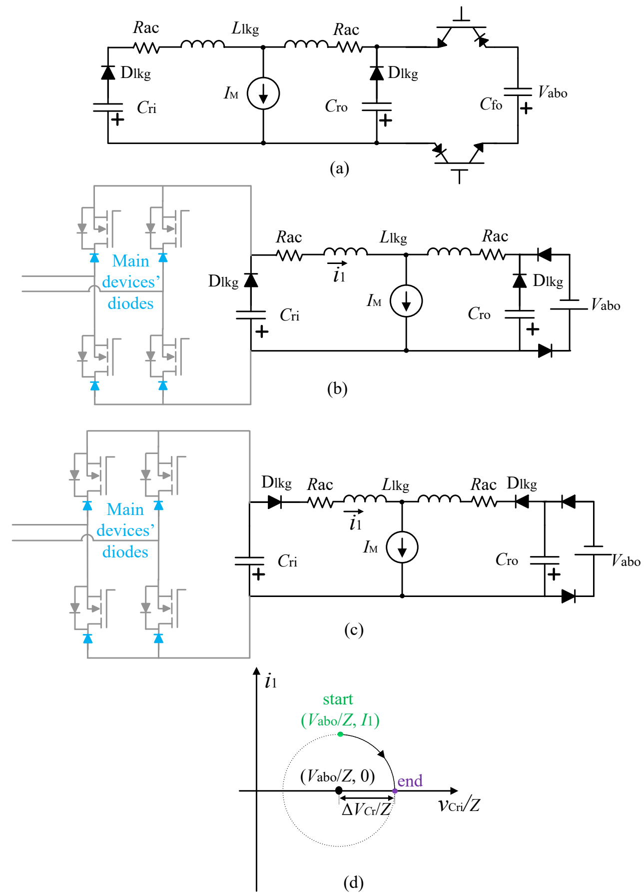


Fig. 4. (a) Equivalent circuit of the proposed soft-switching solid-state transformer (S4T) in mode 0 immediately after mode 2 in Fig. 3. (b) Commutation equivalent circuit of the proposed S4T during the resonance between L_{lkg} and C_{ri} at the beginning of mode 3. (c) Commutation equivalent circuit of the prior S4T in [27]-[28]. (d) Phase-plane diagram of the resonance between L_{lkg} and C_{ri} when $v_{\mathrm{Cri}(t=0)} = V_{\mathrm{abo}}$. $Z = \sqrt{L_{\mathrm{lkg}}/C_{\mathrm{ri}}}$. The main devices' diodes enable moving the leakage diodes from the main power path in (c) to the auxiliary path in (b) to achieve significant conduction loss saving while retaining all the advantages and not inducing any disadvantages compared to the prior S4T.

From the phase-plane diagram and the mathematic description of the commutation process in (1)-(3), the voltage difference between C_{ri} and C_{ro} at the end of the commutation can be derived in (4) for the operating point in Fig. 4. Assumptions are that the winding resistance (R_{ac}) is neglected for the worst-case scenario and the magnetizing current is constant during the commutation. Equation (4) also explains the voltage difference between the two resonant capacitors in Fig. 3, e.g., the difference between V_1 and V_{abo}.

$$\begin{cases} V_{\mathrm{abo}} = L_{\mathrm{lkg}}\dfrac{di_1}{dt} + v_{\mathrm{Cri}} \\ i_1 = C_{\mathrm{ri}}\dfrac{dv_{\mathrm{Cri}}}{dt} \end{cases} \quad (1)$$

$$\begin{cases} i_{1(t=0)} = I_1 \\ v_{\mathrm{Cri}(t=0)} = V_{\mathrm{Cri}} \end{cases} \quad (2)$$

$$\begin{cases} v_{\mathrm{Cri}} = K\sin\left(\dfrac{t}{\sqrt{L_{\mathrm{lkg}}C_{\mathrm{ri}}}} + \varphi\right) + V_{\mathrm{abo}} \\ i_1 = K\sqrt{\dfrac{C_{\mathrm{ri}}}{L_{\mathrm{lkg}}}}\cos\left(\dfrac{t}{\sqrt{L_{\mathrm{lkg}}C_{\mathrm{ri}}}} + \varphi\right) \\ K = \sqrt{(V_{\mathrm{Cri}} - V_{\mathrm{abo}})^2 + L_{\mathrm{lkg}}/C_{\mathrm{ri}} \cdot I_1^2} \\ \varphi = \arctan((V_{\mathrm{Cri}} - V_{\mathrm{abo}})/(\sqrt{L_{\mathrm{lkg}}/C_{\mathrm{ri}}} \cdot I_1)) \end{cases} \quad (3)$$

$$\Delta V_{Cr} = \sqrt{(V_{\mathrm{Cri}} - V_{\mathrm{abo}})^2 + L_{\mathrm{lkg}}/C_{\mathrm{ri}} \cdot I_1^2} + (V_{\mathrm{abo}} - V_{\mathrm{Cri}}) \quad (4)$$

III. Parameter Design of the Proposed Soft-Switching Solid-State Transformer (S4T)

The key design equations of the proposed S4T with reduced conduction loss are presented in this section. The design example in this paper is a 25 kVA MV-LV prototype that can interface DC voltage or AC voltage. The prototype has a rated voltage of 2.5 kV-600 V for DC-DC conversion and 2.5 kV-480 V for AC-AC conversion. High-frequency transformer's turns ratio is selected to be 4:1 to match the nominal DC-DC voltage conversion ratio. The auxiliary resonant circuits on both sides of the transformer (L_{r} and C_{r}) conform to the transformer turns ratio. In the equations below, all quantities are referred to the HV side. V_{pk} and I_{pk} stand for the rated voltage and current of the prototype, respectively. The transformer peak-to-peak ripple current can be approximately calculated with (5) to size the transformer magnetizing inductance. The filter capacitor peak-to-peak ripple voltage can be calculated as shown in (6) to size the filter capacitance.

$$\Delta I_{\mathrm{m}} = \frac{V_{\mathrm{pk}}}{L_{\mathrm{m}}}\frac{D_{\mathrm{eff}}}{2}T_{\mathrm{sw}} \quad (5)$$

$$\Delta V_{\mathrm{f}} = \frac{I_{\mathrm{pk}}}{C_{\mathrm{f}}}\left(1 - \frac{D_{\mathrm{eff}}}{2}\right)T_{\mathrm{sw}} \quad (6)$$

The dv/dt of the active devices can be calculated as shown in (7) to size the resonant capacitors. It should be noted that the theoretical voltage stress calculation in [29] considers the worst case. A simulation can be performed for a final decision if a less conservative solution is desired.

$$\frac{dv}{dt} = \frac{I_{\mathrm{M}}}{2C_{\mathrm{r}}} \quad (7)$$

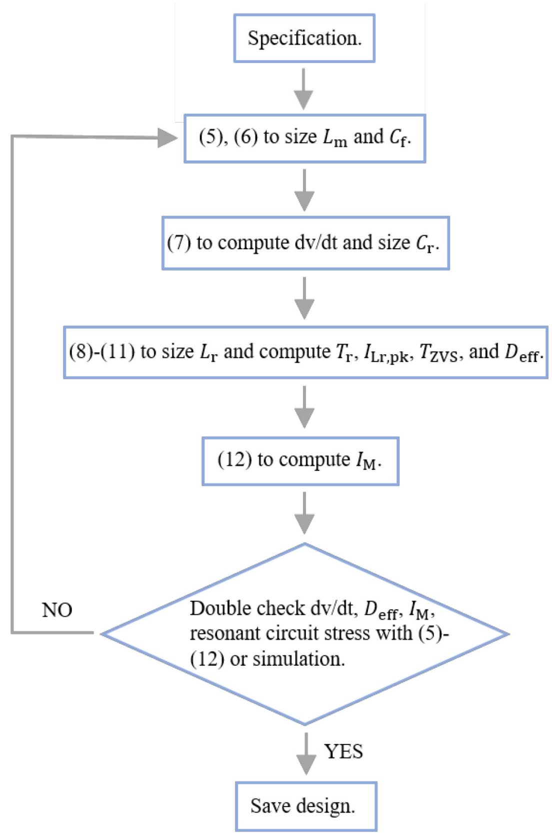


Fig. 5. Design flow chart of the proposed soft-switching solid-state transformer (S4T).

Table I. Parameters of the MV-LV 25 kVA soft-switching solid-state transformer (S4T) prototype in experiments.

Parameter	Symbol	Value
Magnetizing inductor	$L_{\mathrm{m\_HV}}$	4.32 mH
Leakage inductor	$L_{\mathrm{lkg\_HV}}$	5.49 μH
HV resonant inductor	$L_{\mathrm{r\_HV}}$	80 μH
HV resonant capacitor	$C_{\mathrm{r\_HV}}$	6.25 nF
LV resonant inductor	$L_{\mathrm{r\_LV}}$	5 μH
LV resonant capacitor	$C_{\mathrm{r\_LV}}$	100 nF
HV filter capacitor	$C_{\mathrm{f\_HV}}$	4.9 μF
LV filter capacitor	$C_{\mathrm{f\_LV}}$	60.0 μF

The resonant inductor can be sized according to the resonant time in (8). The peak current in the resonant inductor in (9) and the rms current are generally not a concern since the resonance is only activated once per switching cycle.

$$T_{\mathrm{r}} = \sqrt{L_{\mathrm{r}}C_{r}}\left(2\pi - \mathrm{asin}\left(\frac{\sqrt{I_{\mathrm{M}}{}^2 V_{\mathrm{pk}}{}^2 C_{\mathrm{r}}/L_{\mathrm{r}}}}{I_{\mathrm{M}}{}^2/4 + V_{\mathrm{pk}}{}^2 C_{\mathrm{r}}/L_{\mathrm{r}}}\right)\right) \quad (8)$$

$$I_{\mathrm{Lr,pk}} = I_{\mathrm{M}}/2 + \sqrt{I_{\mathrm{M}}{}^2/4 + V_{\mathrm{pk}}{}^2 C_{\mathrm{r}}/L_{\mathrm{r}}} \quad (9)$$

Then, effective duty cycle of the converter can be calculated according to (10). Ideally, lost duty cycle is expected to be small (< 10%) for small circulating reactive power and hence high-efficiency power conversion. If the effective duty cycle is not large enough, either smaller resonant inductance or resonant capacitance is needed to drive down the resonant time or the

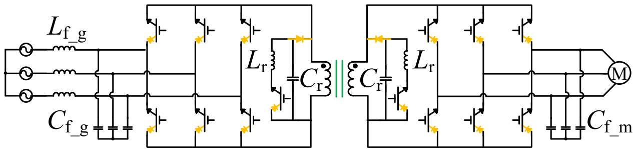


Fig. 6. Circuit schematic of the proposed LV-LV soft-switching solid-state transformer (S4T) in the electric drive simulation.

Table II. Parameters of the simulated 10 kVA 208 V soft-switching solid-state transformer (S4T) drive and the 9 HP 208 V induction motor.

Parameter	Symbol	Value
Magnetizing inductor	L_m	200 µH
Leakage inductor	L_{lkg}	2 µH
Resonant inductor	L_r	8 µH
Resonant capacitor	C_r	400 nF
Grid-side filter inductor	L_{f_g}	220 µH
Grid-side filter capacitor	C_{f_g}	192 µF
Motor-side filter capacitor	C_{f_m}	192 µF
Motor rated speed	ω_m	1725 rpm
Motor pole number	P	4

ZVS transition time in (11). Lastly, the magnetizing current, i.e., dc-link current of this current-source SST can be calculated with (12).

$$D_{\text{eff}} = 1 - (T_r + T_{\text{ZVS}})/T_{\text{sw}} \tag{10}$$

$$T_{\text{ZVS}} = \frac{2V_{\text{pk}}}{dv/dt} \tag{11}$$

$$I_M = \frac{2I_{\text{pk}}}{D_{\text{eff}}} \tag{12}$$

Using an iterative process in Fig. 5, the final design parameters obtained are shown in Table I. The final dv/dt designed is roughly 2 kV/µs on the HV side and 0.5 kV/µs on the LV side with 4:1 transformer turns ratio. The resonant time is approximately 3.5 µs and the effective duty cycle is around 90% with a switching frequency of 16 kHz to avoid audible acoustic noise. If the dv/dt constraint is relaxed, a higher effective duty cycle can be achieved, which is basically a trade-off between the EMI and the effective duty cycle.

For device selection of the 25 kVA MV-LV prototype, devices with low conduction drop should be adopted to minimize the conduction loss, which is the dominant loss mechanism. Due to the limited availability of reverse-blocking modules on the market, customized modules from manufacturers are needed or discrete devices are connected in parallel. On the HV side, a customized Cree 3.3 kV 45 A reverse-blocking module with SiC MOSFETs and SiC diodes is used, which packages all the main devices and the auxiliary-branch devices [32]. Customized 3.3 kV 45 A diodes are also provided by Cree as HV leakage diodes. These SiC MOSFETs and SiC diodes are used for their superior performance compared to the HV Si IGBTs and diodes. On the LV side, two 1.2 kV Si IGBTs IGW60T120 are in parallel as LV main and resonant switches, and two 1.2 kV SiC diodes GP2D050A120B are in parallel as LV main and resonant diodes. The same 1.2 kV SiC diodes is used as LV leakage diodes but no paralleled devices are needed because the leakage diodes in the proposed S4T only conducts during mode 0 in Fig. 3 to discharge the small

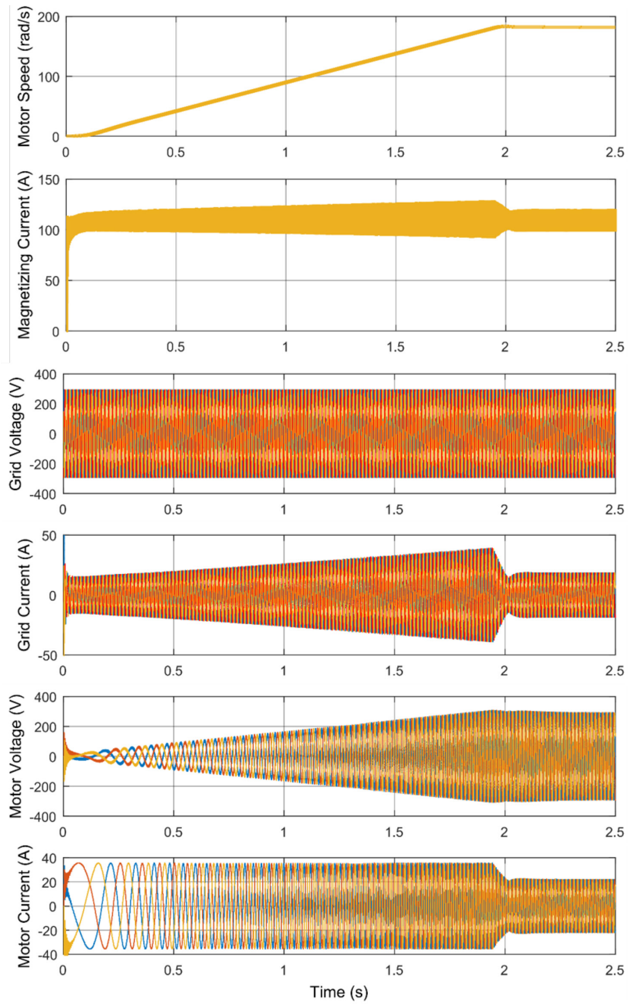
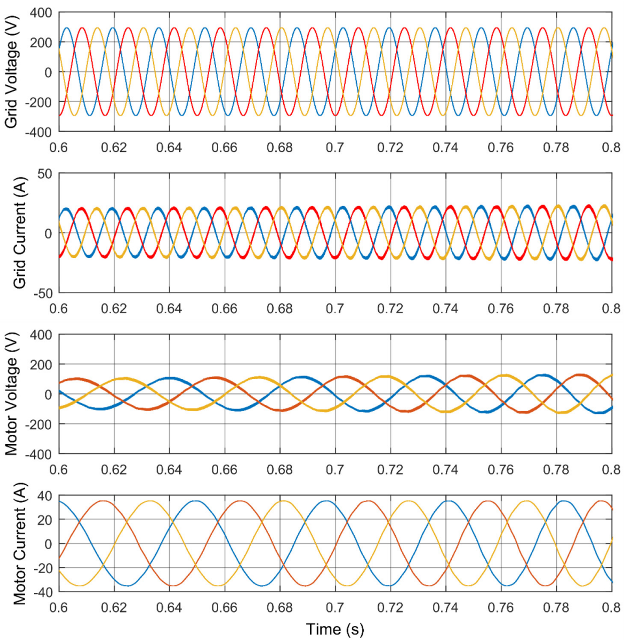


Fig. 7. Simulation waveforms of the proposed soft-switching solid-state transformer (S4T) for LVAC-LVAC conversion in electric drive application.

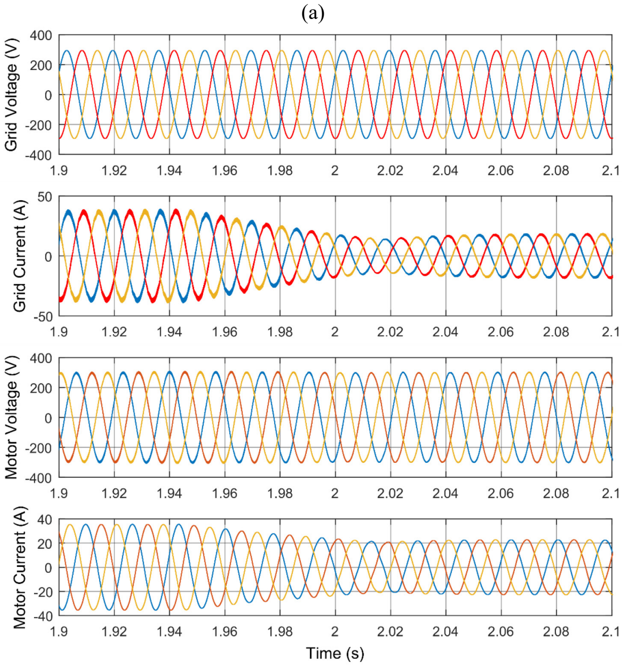
resonant capacitors. These LV SiC diodes are used for no reverse recovery and reduced loss and LV Si IGBTs are used due to reasonably low conduction drop and low cost. Certainly, LV SiC MOSFETs can replace the LV Si IGBTs to achieve highest possible efficiency. In the future, SiC reverse-blocking devices can be used if available instead of connecting a switch and a diode in series.

IV. Simulation Results of the Proposed Soft-Switching Solid-State Transformer (S4T)

The simulation section is devoted to verify the LV-LV configuration in Fig. 2 (a), while the MV-LV configuration in Fig. 2 (b) is validated using the MV experimental prototypes. For the LV S4T in Fig. 6, the simulation scenario is selected to be electric drive to demonstrate the capability of the S4T to supply inductive loads and provide sinusoidal outputs at variable frequency different from the input frequency. Note that the LV S4T's application is not limited to LV electric drive. Other applications like EV charging, UPS, etc. are also possible. The parameters of the S4T with 1:1 high-frequency transformer and

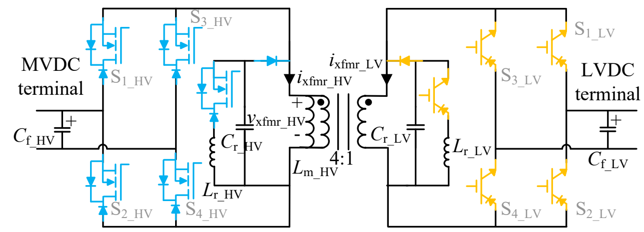


(a)

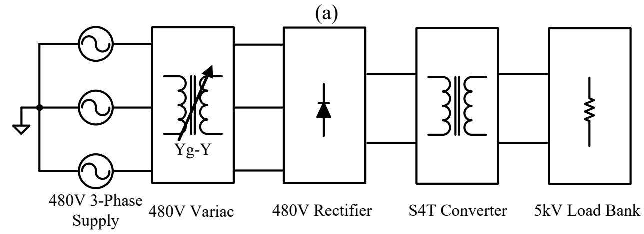


(b)

Fig. 8. Zoomed simulation waveforms of the proposed soft-switching solid-state transformer (S4T) drive (a) during the acceleration and (b) when the speed nearly reaches the full speed. The waveforms show the dynamic characteristics and the capability of supplying inductive loads with sinusoidal variable-frequency output voltage.

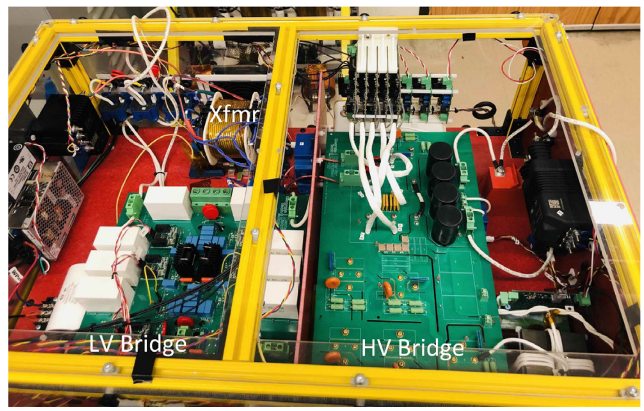


(a)

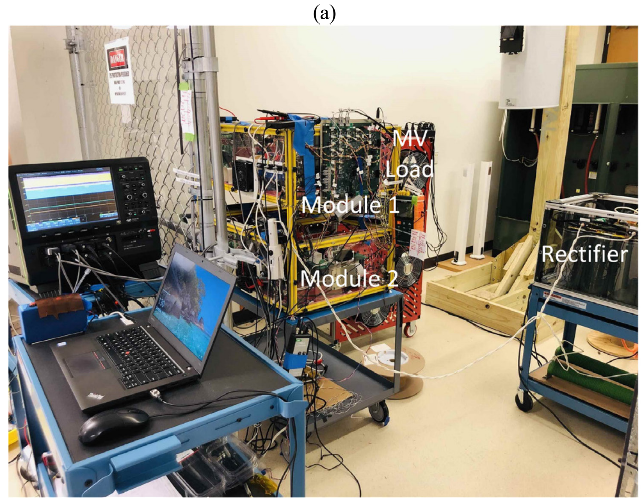


(b)

Fig. 9. (a) Circuit schematic of the proposed soft-switching solid-state transformer (S4T) prototype for DC-DC conversion. (b) Test setup with a LV source and a HV load for the prototype.



(a)

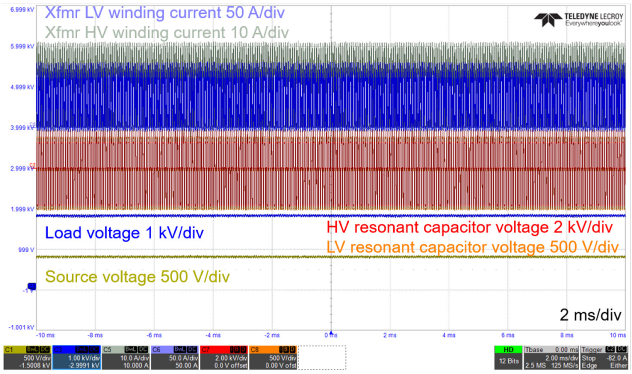


(b)

Fig. 10. (a) A 25 kVA 600 V-2.5 kV proposed soft-switching solid-state transformer (S4T) module. (b) Experimental setup of the modular 50 kVA 600 V-5 kV S4T. Single module is under test in this paper.

the motor are summarized in Table II. An indirect field-oriented control method with dual-loop PI regulators in [33] is applied.

Fig. 7 illustrates the operation of the S4T drive to accelerate the motor smoothly from zero-speed to full-speed with all the state variables stably controlled, which proves the dynamic characteristics of the proposed S4T. The zoomed dynamic waveforms are shown in Fig. 8 (a) during the acceleration and Fig. 8 (b) when the motor speed nearly reaches the full speed. In Fig. 8, the grid-side and the motor-side currents and voltages are high-quality sine waves, which verifies the capability of the S4T to supply the inductive load and produce variable-frequency output voltage different from the input frequency.



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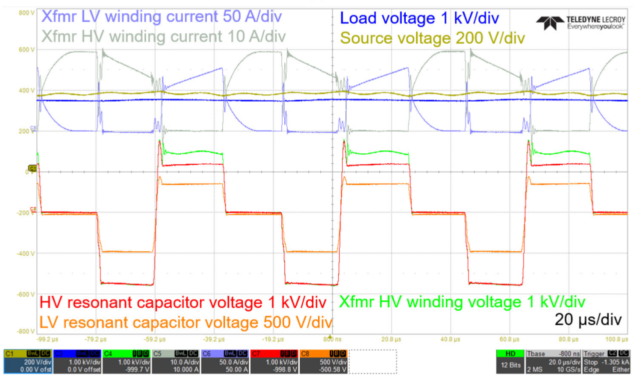
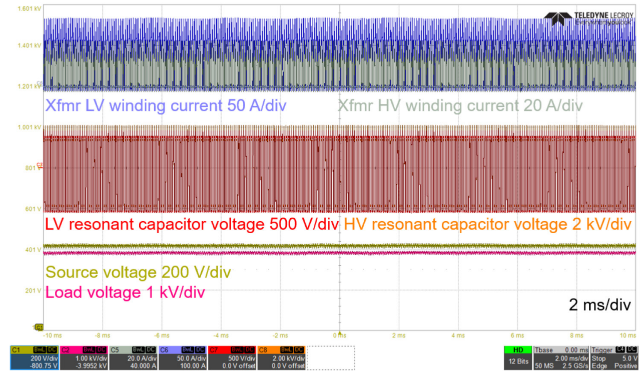
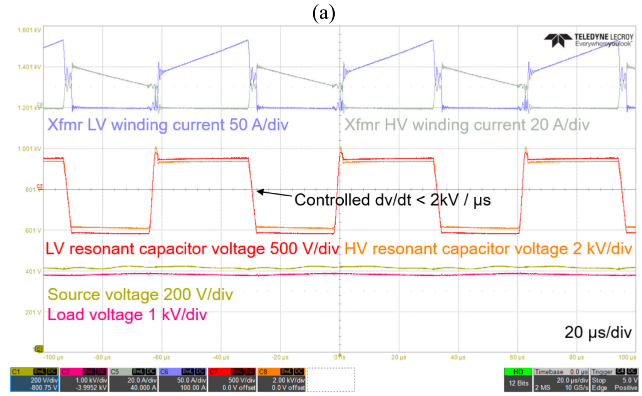


(b)

Fig. 11. (a) Experimental waveforms of the proposed soft-switching solid-state transformer (S4T) at about 10 kW 400 V-2 kV DC-DC conversion. (b) Zoomed waveforms illustrate switching-cycle operation of the S4T.



(a)



(b)

Fig. 12. (a) Experimental waveforms of the proposed soft-switching solid-state transformer (S4T) at about 13 kW 400 V-2 kV DC-DC conversion. (b) Zoomed waveforms illustrate switching-cycle operation of the S4T.

V. Experimental Results of the Proposed Soft-Switching Solid-State Transformer (S4T)

A 25 kVA 600 V-2.5 kV experimental prototype of the proposed S4T with reduced conduction loss is built. As shown in the circuit schematic in Fig. 9 (a), each switch in the converter prototype has an IGBT or a MOSFET in series with a diode for reverse-blocking capability. Therefore, the prototype can be used for DC-DC or AC-AC conversion without device change. For the experimental results here, the converter is used for DC-DC conversion with a LV rectifier source and a HV load bank for LV to HV power flow direction as shown in Fig. 9 (b). The experimental prototype and the experimental setup are shown in Fig. 10.

The 10 kW 400 V-2 kV DC-DC conversion results are shown in Fig. 11, where the model predictive priority-shifting (MPPS) control method is used [34]. The MPPS directly controls the magnetizing current every switching cycle to avoid large transient on the dc-link current, which is measured by summing up the transformer primary and secondary windings' current sensor measurements with a scaling factor of the 4:1 turns ratio. The nomenclature used hereinafter in the experimental waveforms is clarified. Load voltage and source voltage refer to the voltages of $C_{\mathrm{f\_HV}}$ and $C_{\mathrm{f\_LV}}$ in Fig. 9 (a), respectively. HV resonant capacitor voltage and LV resonant capacitor voltage refer to the voltages of $C_{\mathrm{r\_HV}}$ and $C_{\mathrm{r\_LV}}$, respectively. Xfmr LV winding current and xfmr HV winding current refer to $i_{\mathrm{xfmr\_LV}}$ and $i_{\mathrm{xfmr\_HV}}$ in Fig. 9 (a), respectively. In Fig. 11 (a), it can be observed that the load-bank voltage and the magnetizing current, i.e., the dc-link current are smooth and steady. The envelopes of the LV and the HV resonant capacitor voltages are well controlled within the device voltage rating, i.e., within 2 kV on the HV side.

Fig. 11 (b) shows the zoomed waveforms to verify the effectiveness of the proposed circuit to manage the interaction between the resonant capacitors and the leakage inductance, where xfmr HV winding voltage refers to $v_{\mathrm{xfmr\_HV}}$ in Fig. 9 (a). The magnetizing current in Fig. 11 (b), i.e., the dc-link current, increases to store energy from the source when the voltage across the HV winding of the transformer is positive and decreases with negative voltage across the transformer to release the energy to the load. The freewheeling state is inserted in between for a constant switching frequency, during which the magnetizing current fully commutates to the HV winding since the on-state voltage drop of the 3.3 kV SiC devices referred to the LV side is much smaller than that of the 1.2 kV devices. After the resonant state when the resonant capacitors' voltages are flipped from negative to positive due to the resonance with the resonant inductors, the converter enters mode 0 in Fig. 3 and both the resonant capacitors on the LV side and the HV side are discharged until the LV-side resonant capacitor is discharged to the voltage level of the LV source. During this ZVS transition state, the transformer voltages on both the LV and the HV side should be the same as the LV and the HV resonant capacitor

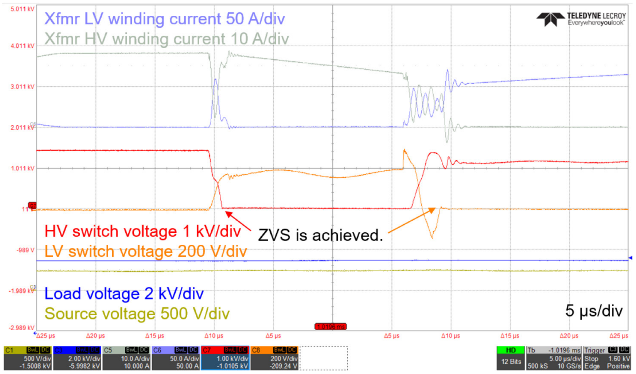


Fig. 13. Zoomed experimental waveforms of the proposed soft-switching solid-state transformer (S4T) to verify the ZVS and the controlled dv/dt.

voltages because the leakage management diodes are conducting. The equivalent circuit during the transition is similar to what is depicted in Fig. 4 (a). Once the LV resonant capacitor is discharged to the LV source voltage level, the converter enters mode 1 in Fig. 3 when the energy is delivered from the source and get stored in the magnetizing inductance. Then, the resonance between the leakage inductance and the HV resonant capacitor starts. It ends when the current through the leakage management diode on the HV side resonates to zero, as is described in Fig. 4 (b) and (d). After the current through the HV leakage management diode reaches zero, the diode will be commutated to the blocking state to block the voltage difference between the HV transformer winding voltage and the HV resonant capacitor voltage, as shown in Fig. 11 (b). To summarize, as can be verified in Fig. 11 (b), the HV transformer winding voltage should be the same as the HV resonant capacitor voltage, unless the HV leakage management diode is in the blocking state and stops the resonance between the leakage and the HV resonant capacitor when the converter is in mode 1.

Fig. 12 shows the experimental results at another operating point, i.e., 2 kV 13 kW. In Fig. 12 (a), the HV load voltage is steady with very low ripple and the resonant capacitor voltages are within the safe limits of the device rating. Moreover, the controlled dv/dt (< 2 kV/µs on the HV side, < 500 V/µs on the LV side) is achieved during the ZVS transition state in Fig. 12 (b). In Fig. 12 (b), the ZVS are achieved. The IGBT or the MOSFET for the incoming vector can be turned on at the beginning of the ZVS transition state (while the diode in series with the switch is blocking) and the diode will be automatically commutated on when the voltage of the resonant capacitor is discharged until the load/source voltage. The freewheeling duration in this waveform sets are tuned to nearly zero. Therefore, there is no zero-voltage vector in the waveforms of the resonant capacitor voltage.

Fig. 13 verifies the ZVS feature and the controlled dv/dt feature. The HV switch in Fig. 13 refers to S_{3_HV} and the LV switch refers to S_{1_LV} in Fig. 9. Under hard-switching conditions, the dv/dt across devices can be as large as 100 kV/µs for MV SiC MOSFETs [3] and ~10 kV/µs for LV Si IGBTs. In

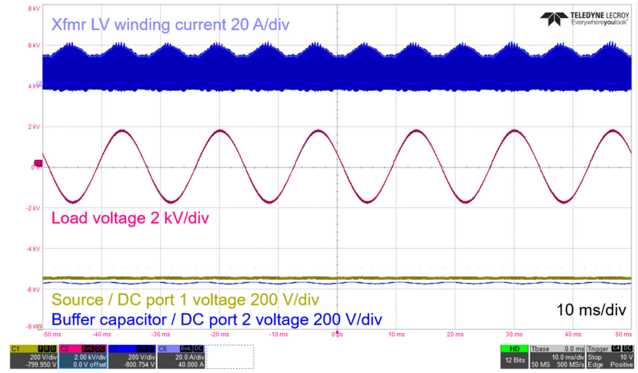
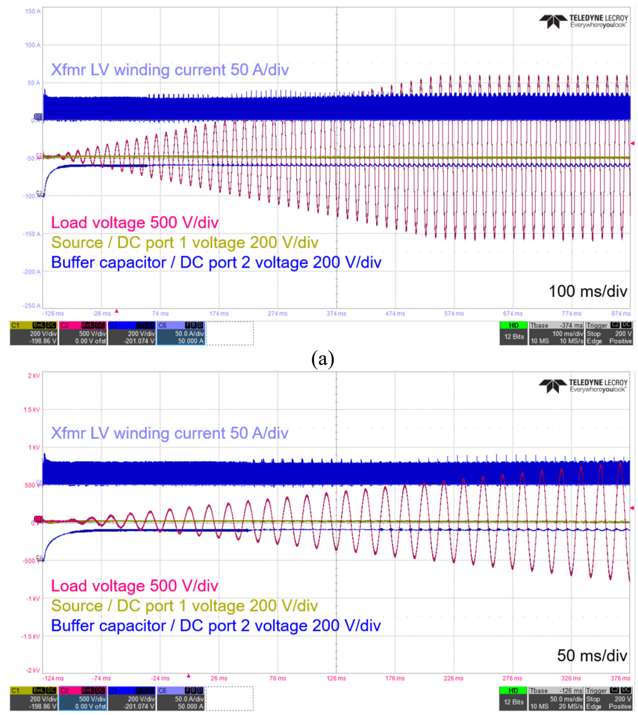


Fig. 14. Experimental waveforms of the proposed soft-switching solid-state transformer (S4T) at 2kV peak MV AC.



(a)

(b)

Fig. 15. (a) Experimental waveforms of the proposed soft-switching solid-state transformer (S4T) during dynamic voltage ramp-up. The staircase-like shape on the load-voltage waveform is due to the oscilloscope resolution, which is in fact smooth as shown in the zoomed version. (b) Zoomed waveforms illustrate sinusoidal output voltage of the S4T even at low output-voltage level.

this prototype, the dv/dt on the MV side is controlled to be < 2 kV/µs and the dv/dt on the LV side is controlled to be < 500 V/µs with the resonant capacitors. Therefore, if the switch is turned on under hard switching condition, the dv/dt across the devices will be much larger [32]. As can be observed in Fig. 13, the dv/dt is always controlled and there is no hard switching in the waveform. Here, probes are not installed to measure the current through the switches due to the circuit layout for low parasitic inductance. At the falling edge of the HV switch voltage in Fig. 13, the dv/dt first decreases and then increases. The reason is that the transformer HV-winding current in Fig. 13, which flows through C_{r_HV} to determine the dv/dt, first decreases and then increases during the ZVS transition state.

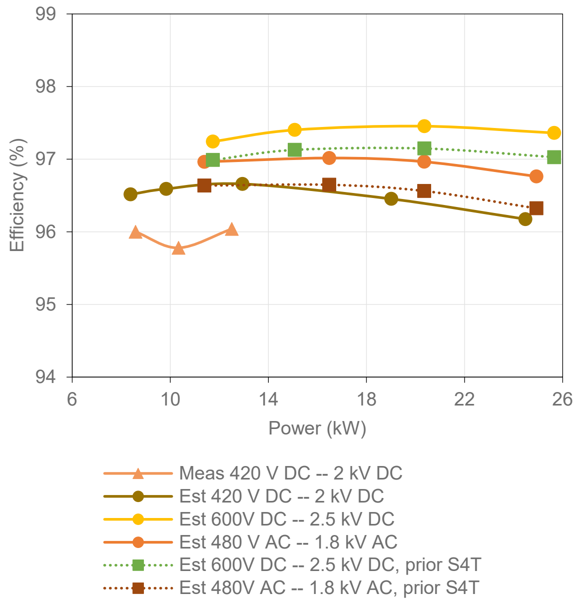


Fig. 16. The S4T prototype efficiency measurement and estimation. Meas. stands for measured efficiency and est. stands for estimated efficiency. The proposed S4T is compared against the prior S4T in [27] to show efficiency improvement. The peak estimated efficiency of 1.8 kV-480 V AC-AC conversion is about 97.0%.

The proposed S4T topology can be used to interface AC or DC inputs or outputs, thanks to the reverse-blocking switches. Moreover, multiport configuration is also possible. To further validate this concept, experimental results are shown in Fig. 14 from single converter module of the prototype in [4] based on the proposed S4T in Fig. 2 (b) with the same customized 3.3 kV Cree reverse-blocking module and a 6:1 transformer. The experiment is at 250 V DC-2 kV peak AC with the same rectifier as a LV source and the load bank as a MV load in Fig. 10. In this experiment, the DC port 2 is a buffer capacitor bank controlled to absorb the 120 Hz ripple power from the single-phase MVAC load. In Fig. 14, the load voltage is sinusoidal with very low distortion. The envelope of the HV winding current has 120 Hz component because the dc-link current has varying switching ripple across a line cycle as the power processed by the dc-link and the converter has 120 Hz component. Fig. 15 verifies the high-quality sinusoidal output voltage of the S4T even at low-output-voltage level and during the dynamic voltage ramp-up. The load voltage trace is clean and smooth with very low distortion. Importantly, Figs. 14-15 prove the buck-boost capability and the multiport capability of the proposed S4T, which are not achieved with the conventional single-stage matrix SST.

The measured and the estimated efficiency for the implemented prototype in Fig. 10 for DC-DC conversion and AC-AC conversion are shown in Fig. 16. It should be noted that the prototype has full reverse-blocking devices and hence can be used for AC-AC conversion without any topology or device module change. The efficiency is measured with a Yokogawa power analyzer WT 1806E at about 420 V-2 kV DC-DC conversion. The efficiency estimation is done in the following

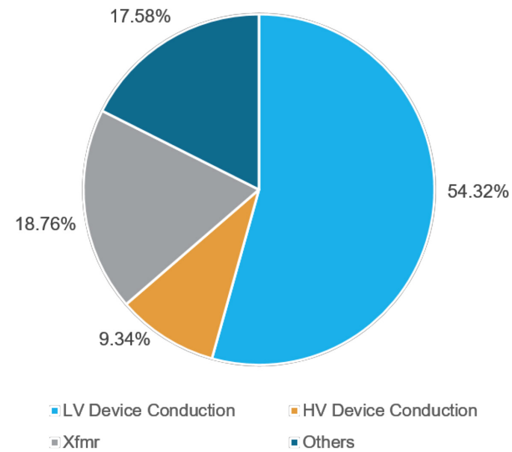


Fig. 17. The estimated proposed S4T prototype's loss breakdown at 25 kW 600 V-2.5 kV. The device conduction loss, especially the LV device is the main loss mechanism, which justifies the necessity of the proposed S4T to move the leakage diode away from the main power path for significant conduction loss savings.

way. Simulations, which include device forward-voltage or resistance model from manufacturers' datasheets and transformer resistance from experimental measurements, are performed to replicate and record each operating point's DC, AC, and rms currents of the devices and the windings of the magnetic components. With the manufacturers' datasheets and the recorded currents, the conduction loss of the MOSFETs, the IGBTs, and the diodes can be computed using (13)-(15).

$$P_{\mathrm{MOS,cond}} = I_{\mathrm{MOS,rms}}^2 R_{\mathrm{MOS}} \tag{13}$$

$$P_{\mathrm{IGBT,cond}} = I_{\mathrm{IGBT,dc}} V_{\mathrm{ce}} + I_{\mathrm{IGBT,rms}}^2 R_{\mathrm{IGBT}} \tag{14}$$

$$P_{\mathrm{D,cond}} = I_{\mathrm{D,dc}} V_{\mathrm{f}} + I_{\mathrm{D,rms}}^2 R_{\mathrm{D}} \tag{15}$$

The transformer and the resonant inductor winding loss is estimated with the measured resistance of the transformer used in the prototype and the current measurements from the simulation. The transformer and the resonant inductor core loss is calculated with the Steinmetz equations in [11]. In Fig. 16, for DC-DC conversion, the difference between the calculated efficiency and the measured efficiency could be attributed to the equipment measurement error and underestimates of loss terms or parasitic losses like PCB trace conduction loss, etc. The peak estimated efficiency of the proposed converter prototype for AC-AC conversion is ~97.0% and for DC-DC conversion is ~97.5%. The estimated converter loss breakdown is shown in Fig. 17. It can be observed that the device conduction loss, especially the LV device, is the dominating loss mechanism. More discrete devices can be paralleled to reduce the LV device conduction loss as high-current-rating 1.2 kV reverse-blocking modules are not commercially available. If the 1.2 kV Si IGBTs in the converter are replaced by 1.2 kV SiC MOSFETs, even more improvements are expected.

As is illustrated in Fig. 16, the prior version of the S4T in [27] has lower efficiency than the proposed S4T. For example, at 25 kVA full power for 480 V to 1.8 kV AC-AC conversion,

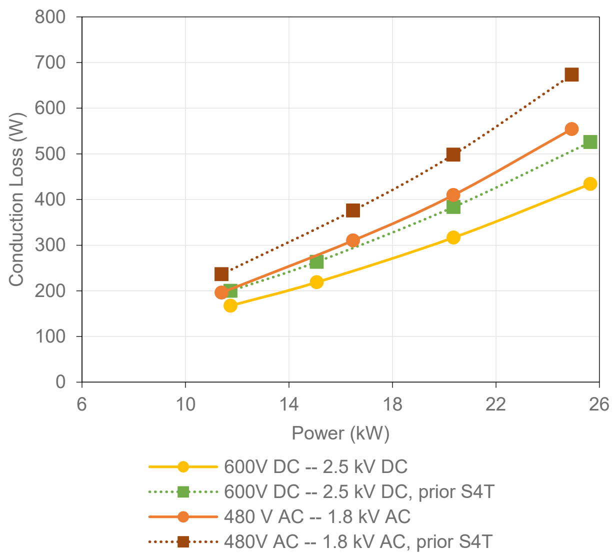


Fig. 18. Conduction loss comparison between the proposed S4T and the prior S4T in [27]. The S4T in [27] has ~21% higher conduction loss in the operating points shown.

the total loss of the prior S4T is ~15% higher than the proposed S4T. To further verify the conduction loss savings, the total device conduction losses including the resonant branch are compared in Fig. 18, where the S4T in [27] generally has ~21% higher conduction loss than the proposed S4T. For example, at 20 kW 480 V AC-1.8 kV AC conversion in Fig. 18, the prior S4T has roughly 500 W conduction loss, while the proposed S4T only has around 400 W conduction loss which is approximately 20% conduction loss saving. It should be noted that in this comparison, two SiC diodes GP2D050A120B in parallel are used as LV leakage management diodes, which are located in the main conduction path for the S4T in [27]. However, for the proposed S4T, the leakage management diode is not in the conduction path and hence one GP2D050A120B is enough. If only one leakage diode is used for the prior S4T in [27], the conduction loss difference will be even larger. Moreover, it should be noted that the conduction loss savings highly depend on the best device available in the specific voltage class. At 1.2 kV class, Si IGBT (Infineon IGW60T120, 1.9 V at 60A, 25°C) has generally higher voltage drop compared to similar rating SiC diode (Global Power GP2D050A120B, 1.7 V at 60A, 25°C). However, if the LV voltage is 240 V, 650 V device can be used. 650 V Si IGBT (Infineon IKW75N65EL5, 1.1 V at 75A, 25°C) can have much lower voltage drop than 650 V SiC diode (GeneSiC GC50MPS06-247, 1.75 V at 75A, 25°C) and hence the conduction savings will be higher. Generally, the proposed S4T has four device drops versus five device drops in [27], which means the number of device drops reduces by 20%.

It is worth mentioning that the proposed S4T with the leakage diode in the auxiliary branch can also prevent ZVS failure. If the resonant capacitor voltage is smaller than the corresponding active state's filter capacitor voltage and the main switches are turned on by mistake due to sensor measurement error or controller fault, the resonant capacitor will be immediately charged up through the main switches in the prior S4T. This can result in additional loss and heat in the main switch. However, the same will not happen in the proposed S4T as the leakage diode will block the voltage difference and prevent the capacitive energy dump into the main switches turned on by error under non-ideal conditions.

To summarize, the experimental results show stable operation of the proposed converter under both MVDC and MVAC voltage, the controlled dv/dt, the ZVS capability, the buck-boost voltage conversion capability, the multiport DC-load integration functionality, and clean commutation waveforms of the leakage diode, which verifies the concepts in the previous sections.

VI. Comparison and Discussion

The ideal requirements for a SST as discussed in Section I include (1) high efficiency, (2) high power density, (3) capability of integrating AC or DC resources with four-quadrant power flow and buck-boost voltage transfer ratio, (4) low EMI, (5) high reliability, and (6) reasonable cost. The cost is largely influenced by the HV SiC modules and is not discussed there.

A comparison between the proposed S4T with reduced conduction loss and existing state-of-the-art solutions is presented in Table III. The proposed S4T is compared against the prior version of the S4T in [27], the traditional three-stage SST in [15]-[16], and the traditional single-stage matrix SST in [16]. From the number of conversion stages point of view, the proposed S4T, the S4T in [27], and the matrix SST enjoys single-stage conversion, which eliminates the bulky dc-link capacitor. In fact, the dc-link capacitor is one of the largest parts in the converter hardware in [35]. In [17], Huang also claims that the dc-link capacitor can occupy significant space.

From auxiliary devices point of view, the prior version of the S4T in [27] has leakage diodes in addition to main switches on the main current path, while the proposed circuit moves the leakage diodes away from the main current path and achieves significant conduction loss reduction. The traditional three-stage solution and single-stage solution also have minimal conduction path as no auxiliary devices are on the main current path.

As to soft-switching capability, the proposed circuit has full-range ZVS, which is better than traditional solutions with no ZVS or only limited-range ZVS within the DAB [13]-[14]. MV MOSFETs can achieve significantly reduced switching loss for improved converter efficiency under ZVS compared to the hard-switching condition [31], [35].

For functionality, a dc-link is generally required to reject disturbance and prevent it propagating from one side to the other [15]-[16]. Commutation challenge is another problem for the traditional single-stage solution [21]-[24]. As the proposed circuit uses the transformer magnetizing inductance as its inductive dc-link, the proposed S4T has full functionality the same as the traditional three-stage SSTs. As verified in the simulations, the S4T can deliver variable-frequency output under non-unity power factor for electric drives. With these

Table III. Comparison between the proposed S4T and other SSTs. The proposed S4T can achieve the same full functionality as three-stage SSTs within a single conversion stage, while conventional single-stage SSTs only have limited functionality.

	Proposed S4T in this Paper	Previous Version of the S4T [27]	Traditional Three-Stage SST [15], [16]	Traditional Single-Stage Matrix SST [16]
Number of Conversion Stages	1	1	3	1
Bulky DC-Link Capacitor	No	No	Yes	No
Auxiliary Device on the Main Power Path	No	Yes. 5 devices conduct main current instead of 4 in this paper.	No	No
Soft Switching Capability	ZVS	ZVS	DAB: Limited-range ZVS. AC/DC & DC/AC: Hard-switching.	No
Voltage Regulation Capability	Yes	Yes	Yes	Limited buck-boost range
Reactive Power Capability	Yes	Yes	Yes	Difficult
Variable Output Frequency	Yes	Yes	Yes	No. Not suitable for AC drives.
Multiport DC Load	Yes	Yes	Yes	No
Dv/dt	~2kV/µs, controlled by *Cr*	~2kV/µs, controlled by *Cr*	>50kV/µs for SiC, uncontrolled	>50kV/µs for SiC, uncontrolled
Modularity for ISOP	Yes	Yes	Yes	Yes

functionalities, the S4T can also achieve voltage regulation or reactive power compensation for utility applications. Moreover, the proposed S4T allows multiport configuration and integrate DC loads as shown in Fig. 14. Therefore, the proposed circuit can achieve full SST functionality, similar to the conventional three-stage solution.

For EMI, the proposed circuit can benefit from the ZVS to achieve controlled dv/dt to reduce the common-mode current flowing into the ground. The dv/dt of MV SiC devices can be as high as 100 kV/µs [3], while the dv/dt in the S4T is controlled to be less than 2kV/µs. As is pointed out in [35]-[37], the much lower dv/dt can significantly reduce the EMI. Regarding reliability, all the solutions have potential to achieve a modular redundant structure for high reliability.

The reader may wonder if a single-stage SST can improve the trade-off between efficiency and power density and whether a direct quantitative comparison is possible. The authors agree with Akagi *et al.* [38] that weight, size, and power density of most of the academic prototypes cannot be directly compared because most of the prototypes are not optimized to the extent of manufacturer's product and space for probing and measurement is required. Moreover, device module characteristics can have a significant impact on the efficiency and the power density according to the data in [17], [38]. As devices of different current and voltage ratings are used in different prototypes, a direct quantitative comparison cannot justify a conclusion on the performance of the topology but would be in favor of prototypes with the newest generation HV SiC devices. Generally, the authors agree with Huang *et al.* [10], [15] and Barbi *et al.* [37] that the single-stage SST can potentially have a better trade-off between the efficiency and the power density. Actually, [10] claims direct AC-AC conversion can lead to possibly low cost and light weight and [15] states higher efficiency is achievable with one power conversion stage. The authors think that the traditional three-stage solution has to design the hard-switching AC/DC and DC/AC stage with lower switching frequency for lower switching loss and hence has larger passives, e.g., the bulky dc-link capacitor [17]. In the future, a comprehensive quantitative comparison is needed with similar devices and optimal design to further justify the potential advantage of single-stage SSTs in terms of the trade-off between the efficiency and the power density.

To summarize, the traditional three-stage solution can achieve full functionality but the efficiency and the power density are regarded not as good as the single-stage solution [10], [15], [37]. However, the traditional single-stage solution can only achieve limited functionality [16]. With significant conduction loss improvement from the prior version of the S4T, the proposed S4T holds the potential of high efficiency and power density due to its single-stage structure and achieves full functionality thanks to the transformer magnetizing inductance as its dc-link.

VII. CONCLUSION

This paper proposes a single-stage SST topology, the soft-switching solid-state transformer (S4T) with reduced conduction loss. The proposed S4T has minimal conduction path, full-range ZVS for low switching loss, small passives from its single-stage structure, and reduced EMI with controlled dv/dt. Compared to the prior S4T, the proposed S4T significantly reduces the conduction loss, retains all the advantages, and has no disadvantages. This paper has demonstrated the universality of the proposed S4T in DC-DC, DC-AC, and AC-AC modes and the full functionality including multiport load integration, reactive power capability, buck-boost voltage regulation, and variable output frequency through simulation and experimental results of 3.3kV-SiC-based MV-LV experimental prototypes at 2 kV, 13 kW. The current-source solid-state transformer and the S4T are experimentally verified for the first time at medium voltage (MV). The peak measured efficiency at MV is ~96% and the peak estimated efficiency for AC-AC conversion is ~97%. With the potential of high efficiency and power density and the full functionality, the proposed S4T can be considered as a promising candidate of the SST for applications including renewable energy integration, data center, EV fast charging, etc.

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