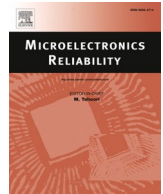




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Unclamped inductive stressing of GaN and SiC Cascode power devices to failure at elevated temperatures

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ABSTRACT

In this paper, the ruggedness performance of GaN HEMT and SiC JFET devices in cascode configuration with a low voltage silicon power MOSFET has been evaluated experimentally. The impact of the bus voltage on the drain current and avalanche energy are investigated as well as the temperature sweep to enable analysis of the alternation of these parameters on the Unclamped Inductive Switching (UIS) ruggedness of cascode devices. The experimental measurements show that the GaN cascode devices have lower avalanche energy rating when compared with the closely rated SiC cascode devices just before the failure. SiC cascode devices can also withstand higher bus voltage in comparison to GaN cascode devices when under electrothermal stress by unclamped inductive switching. The analysis of transfer characteristics and leakage current of SiC JFET & GaN HEMT cascode structures following UIS stress have also been performed together with Computed Tomography (CT) Scan imaging to determine the per-area avalanche energy density.

1. Introduction

Gallium Nitride (GaN) and Silicon Carbide (SiC) are the most promising wide-bandgap materials in comparison with traditional narrow-bandgap Silicon for fabrication of power semiconductor devices. This is due to their superior characteristics, including higher critical electric field and electronic saturation velocity which lead to higher efficiency with faster switching and higher power density. It also enables lower on-state resistances, and higher temperature operations [1]. The energy conversion in power electronics converters is also improved with SiC power devices due to their fast-switching capability at higher temperatures together with better avalanche capability than the traditional Silicon-based devices. The reasons for this are the high critical electric field and wide-bandgap, therefore more energy is required to create hole-electron pairs by the impact ionization process [2–4]. Nevertheless, with respect to the reliability of the SiC MOSFETs, threshold voltage instability and gate oxide reliability are important concerns that still need to be addressed despite the significant developments in the new generation of devices. The SiC JFETs are commercialized in 2006 [5] and as normally-on devices were not attractive for power electronics

applications. However, the interest in the SiC cascode devices is increased due to the gate oxide reliability issue in SiC MOSFETs [6].

SiC JFET device as well as GaN HEMT device connected in series together with a low voltage (LV) Silicon MOSFET were tested in this study. The LV Silicon MOSFET provides an enhancement mode device with negative voltage subject to the gate of the HEMT and JFET device in the cascode structure. Due to the absence of the p-n junction in GaN HEMT structure, the GaN HEMTs has small avalanche capability. Some studies shows that it can stand the avalanche energy with charge of the internal capacitances [7,8].

In this paper, the UIS performance of the GaN and SiC cascode devices at close ratings have been discussed. Their drain current and avalanche energy capabilities are demonstrated and the transfer characteristics and leakage current of the devices after increasing avalanche energy with fixed bus voltages have been captured and shown, as well as the CT-Scan imaging of the devices after failure by avalanche.

2. Experimental set-up

The power devices with high switching rates are suitable for power

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electronics applications. The application of these devices in power electronics that ensue very fast switching can lead to electrothermal stress. As a matter of fact, the switching speed of cascode devices can be very fast especially during the turn-off, and this can lead to serious overvoltage even with small parasitic inductance in the circuit. This is due to the changes of the current through the inductor that abruptly increases, leading the inductor creating electromagnetic force that will be subjected to the device. When this overvoltage reaches the breakdown limit, the power device will be enforced into the so-called avalanche process.

The UIS test is the standard method to measure the ruggedness of power devices under electrothermal stress. In the measurements of this paper, 650 V GaN cascode (TPH3212PS) and 650 V SiC cascode devices (UJ3C065080T3S) have been compared with each other, while the 900 V GaN cascode device (TPH90H180PS) have also been compared with 1200 V SiC cascode devices (UJ3C120150K3S) regarding to their avalanche capability. The 900 V device is the highest voltage rating of GaN Cascodes that is commercially available at the time of writing, and hence is used to be compared with 1200 V device as the highest rating of SiC Cascodes available. In understanding the measurement results, the difference in voltage ratings of devices must be considered.

The schematic circuit view of the UIS test board and the test rig used in the experimental measurements are illustrated in Fig. 1. The pulse length is fixed to 30 μ s and 60 μ s and a free-wheeling inductor inductance of 0.65 mH is used. The bus voltage is increased until avalanche breakdown occurs. Furthermore, the temperature is also increased to observe its effect on the stored avalanche energy and avalanche current.

Fig. 2 shows the cross-section areas of the GaN HEMT and SiC JFET. It can be seen that the SiC JFET is normally-on device and requires connection to enhancement-mode MOSFET to be able to normally-off. The HEMT device shown in Fig. 2 is normally-off, thanks to the P-GaN layer under the gate which has bended the fermi level at the 2DEG layer, while the GaN HEMTs used in cascodes are normally-on devices.

Fig. 3 demonstrates the typical results of the UIS test for power devices with a single pulse. As it is illustrated, the UIS waveforms are same

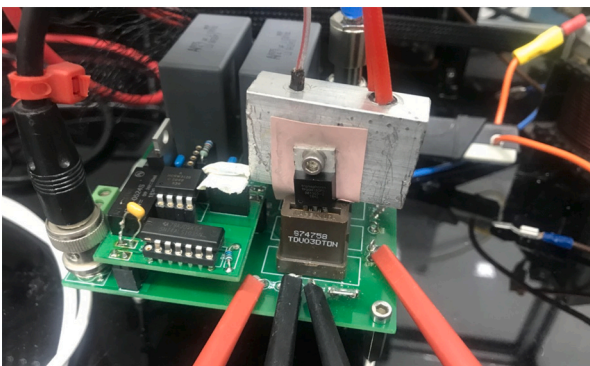
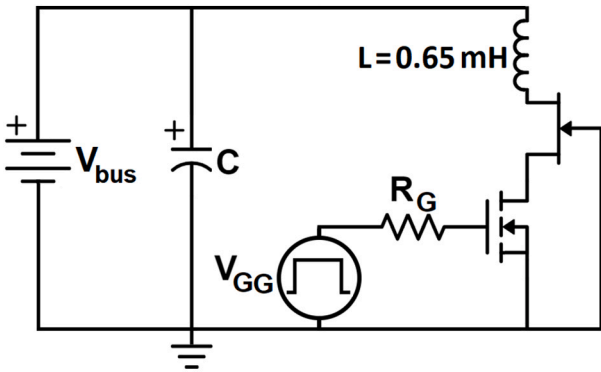


Fig. 1. The schematic circuit view of the UIS test and the test rig that is used in the experiments.

as to that of the traditional Silicon based devices. At the beginning of the process, the device under test (DUT) is in the turn-off mode, followed by a period that the cascode device is switched on by an adjusted single pulse. The duration of this pulse determines the magnitude of current through the load inductor and the DUT just before the avalanche state. The slope of the current in turn-on phase can be calculated by:

$$\frac{dI_{DS(on)}}{dt} = \frac{V_{bus}}{L_{load}} \quad (1)$$

The current in the load inductor cannot be decreased sharply, therefore the EMF in the inductor drives the cascode device into avalanche state where the avalanche energy is dissipated at the drain terminal of the DUT. The induced voltage at this terminal is effectively the avalanche voltage applied to the device. The voltage magnitude across the inductor is based on the bus voltage and inductor, thus the slope of the current can be calculated by:

$$\frac{dI_{DS(off)}}{dt} = \frac{V_{bus} - V_{avalanche}}{L_{load}} \quad (2)$$

The avalanche period can be predicted by:

$$t_{avalanche} = \frac{I_{avalanche} \cdot L_{load}}{V_{avalanche} - V_{bus}} \quad (3)$$

As a result, the avalanche energy that is the dissipated energy in the device in the period of avalanche process can be calculated by:

$$E_{av} = \frac{V_{avalanche}}{V_{avalanche} - V_{bus}} \cdot \frac{1}{2} I_{avalanche}^2 L_{load} \quad (4)$$

The device failure is relied on three main factors; the avalanche energy, the rate of power dissipation of the device and the peak of the voltage at UIS applied to the device [9]. The gate of high voltage device can also be subject to significant avalanche current and this can also be a secondary failure mechanism. Avalanche process is inherently an electrothermal process, which coupled with excessive peak voltage that rises above the rating of the devices, and in turn above the critical electric field of the device, could lead to failure. Should failure not to occur, the process is usually reversible, though some degradation in device performance can be observed.

3. Results and discussion

In the measurements of this paper, the bus voltage is increased step by step until failure occurs and the drain current and drain voltage waveforms of each device has been captured, enabling calculation of the avalanche energy. As seen in Fig. 4, for the 650 V GaN cascode device, it is failed with almost 13 A drain current at DC bus voltage of 220 V and avalanche voltage of 700, whereas the SiC has experienced over the 20 A of drain current under the DC bus voltage of 360 V and avalanche voltage of 760 V, both at 175 °C. The result shows that the durability of the SiC cascode device is much larger than the GaN cascode device if considering the avalanche ruggedness as the comparing factor.

The output capacitor of the DUT charges and discharges over the UIS test cycles which comprises the drain current. During the UIS test, the conventional devices are failed with displacement current in power devices. The avalanche ruggedness can increase the hole density that can trigger the displacement current in traditional MOSFETs. Therefore, the holes must be extracted immediately to enable the device to have a better avalanche capability. The likelihood of the BJT latch-up in the silicon MOSFET at very high dV/dt cannot be ignored as the displacement current may lead to its unwanted activation, leading to significant current coinciding with DC voltage, and thermal runaway, although this is relatively well suppressed and in most modern devices UIS can only be attributed to voltage. With respect to high rated GaN and SiC cascode devices at 900 V & 1200 V, respectively, As seen in Fig. 5 the GaN device failed with almost 13 A drain current at DC bus voltage of 200 V but at higher avalanche voltage of 1050 V, whereas the SiC has over the 20 A of

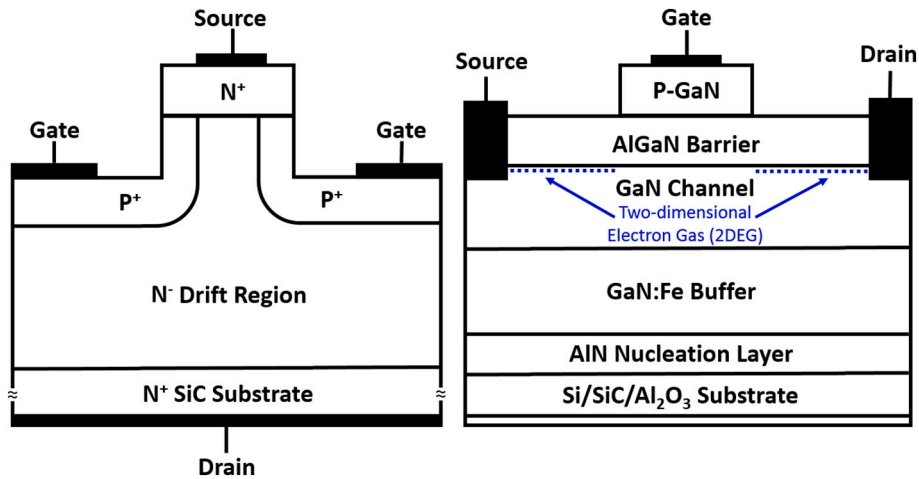


Fig. 2. The cross-sectional view of the (left) SiC JFET and (right) GaN eHEMT.

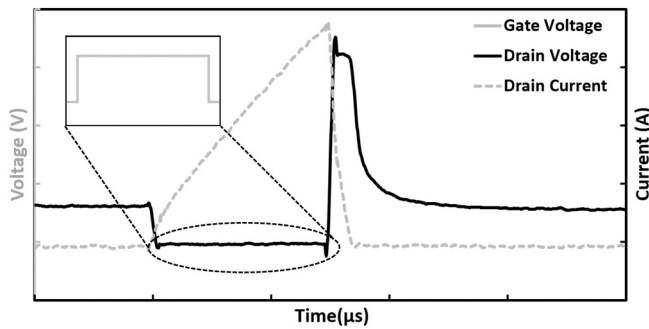


Fig. 3. Typical avalanche current and voltage waveforms for UIS test together with the applied gate voltage.

drain current under the DC bus voltage of 340 V and a higher avalanche voltage of 1920 V compared with the low voltage device, both at 175 °C. The high voltage will lead to a higher avalanche energy, and as expected, can be translated into higher electrothermal ruggedness in higher voltage devices.

Following stressing of the GaN and SiC cascode devices with a single 60 μs pulse avalanche stress with increasing bus voltage in steps of 20 V at room temperature, the 650 V-rated GaN cascode device is failed with 1440 V avalanche voltage and 7 A avalanche current, while the avalanche voltage in SiC cascode device is saturated at around 600 V and the avalanche current is reached 31.4 A as shown in Fig. 6. As for 650 V-rated cascode devices at high temperature, the avalanche current and voltage of them is almost the same as to their avalanche capabilities at room temperature as highlighted in Fig. 7. Looking in details, the slope of the drain current for the 650 V SiC cascode device at high temperature just before the failure, is not as sharp as that at room temperature, as significant degradation may have already occurred, and failing with higher voltage.

With respect to the higher rated GaN and SiC cascode devices after a single 60 μs pulse at room temperature, the avalanche currents of them when avalanche happens are 23.6 A and 27.2 A, while the avalanche voltages are 2140 V and 1380 V, respectively, as it is shown in Fig. 8. During the UIS test, the GaN cascode device exhibits significant oscillations due to its high switching speed and in the end of this experiment, 900 V GaN cascode devices have been exploded due to avalanche energy. Concerning the high temperatures, both high rated cascode devices have been failed at earlier bus voltages as shown in Fig. 9.

The drain current of the four devices at failure have been compared with each other. The 1200 V SiC cascode device has the largest

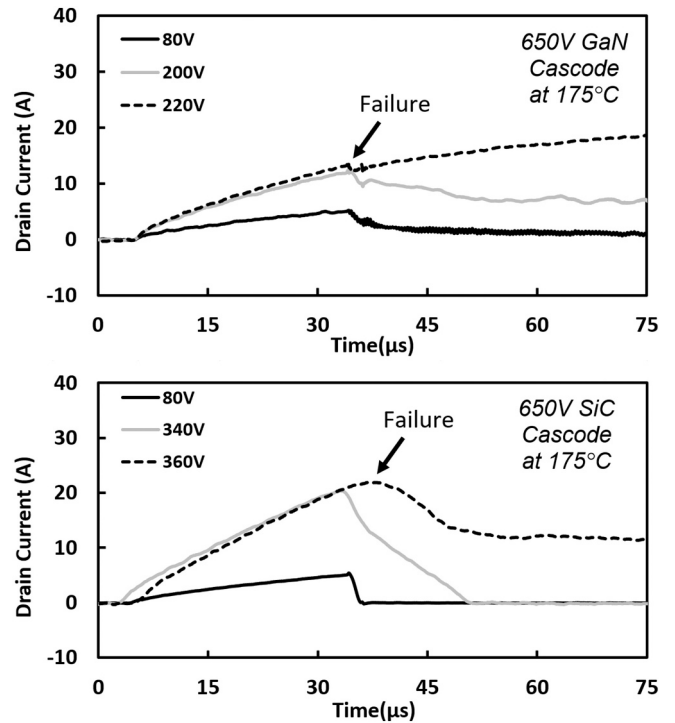


Fig. 4. The drain currents of the 650 V-rated GaN and SiC cascodes at different voltage levels with 30 μs single pulse, with highest voltage being the avalanche voltage at 175 °C.

avalanche current compared to other devices with almost 30 A after failure at 175 °C as it is shown in Fig. 10. The current peaks of the devices after failure with their bus voltage values are illustrated in Fig. 11 at 25 °C and 175 °C for low and high rated GaN and SiC cascode devices. As it is seen in this figure, 1200 V SiC cascode device has the highest avalanche current at room temperature as well as at higher temperature.

Regarding to the avalanche energy of the four devices, as shown in Fig. 12, SiC cascode devices have the highest stored avalanche energy just before their failure with approximately 130 mJ and 55 mJ, respectively, even at lower bus voltages, while the GaN cascode devices have lower avalanche energy by around 20–30 % of that of the SiC devices. In GaN HEMT structure, the holes are extracted from the gate to drain or substrate to drain, however the hole extraction from gate is not readily done for the conventional GaN HEMT structure. Furthermore, in

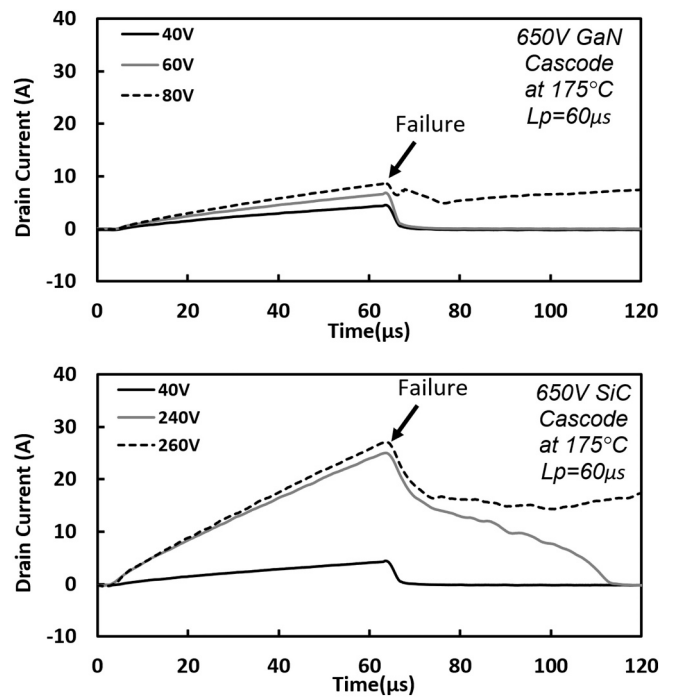
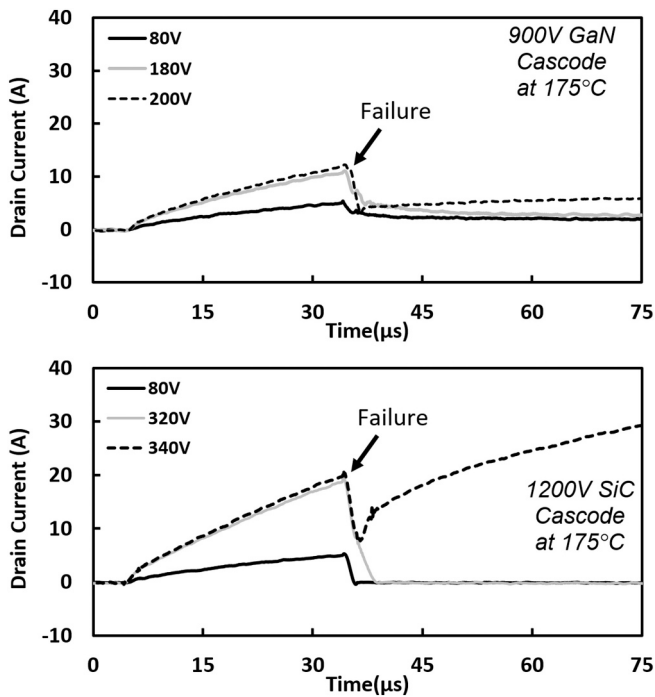


Fig. 5. The drain currents of the higher-rated GaN and SiC cascodes at different voltage levels with 30 μ s single pulse, with highest voltage being the avalanche voltage at 175 $^{\circ}$ C.

Fig. 7. The drain currents of the 650 V-rated GaN and SiC cascodes at different voltage levels with 60 μ s single pulse, with highest voltage being the avalanche voltage at 175 $^{\circ}$ C.

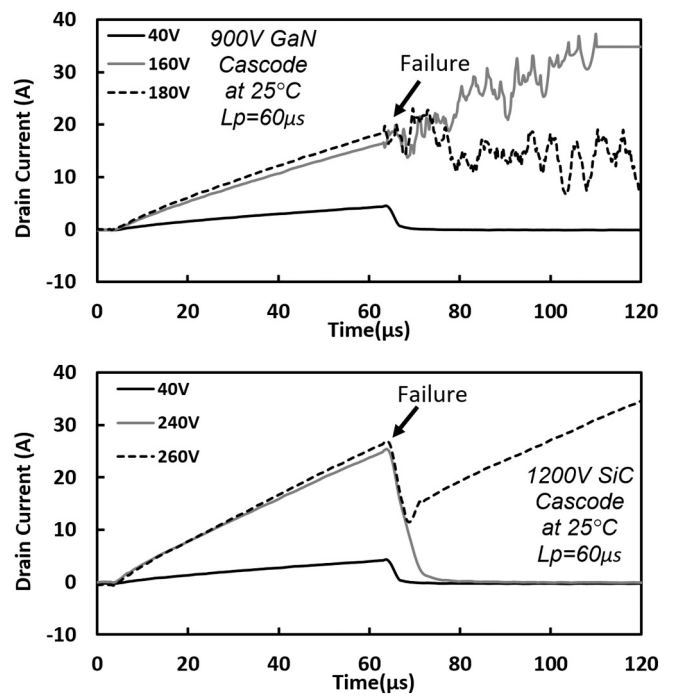
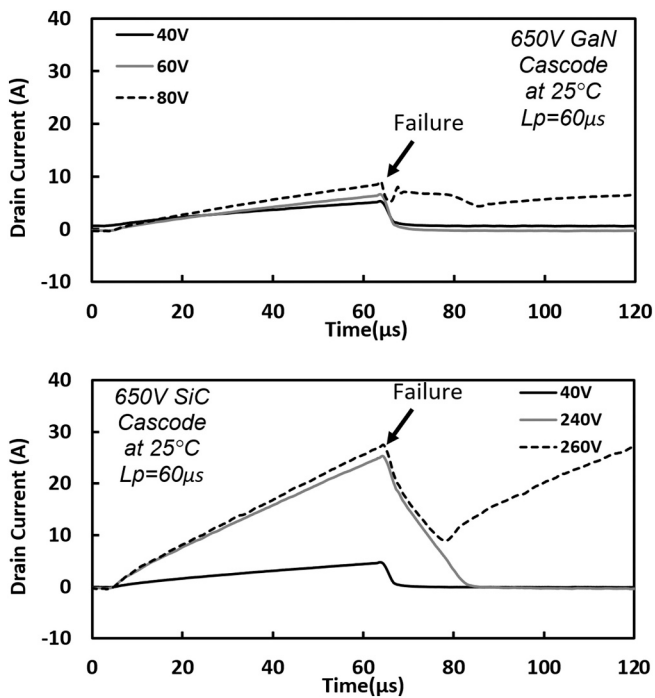


Fig. 6. The drain currents of the 650 V-rated GaN and SiC cascodes at different voltage levels with 60 μ s single pulse, with highest voltage being the avalanche voltage at 25 $^{\circ}$ C.

Fig. 8. The drain currents of the high rated GaN and SiC cascodes at different voltage levels with 60 μ s single pulse, with highest voltage being the avalanche voltage at 175 $^{\circ}$ C.

the period of voltage clamping, the gate voltage is not sufficient to turn-on the device and the drain current is much higher than the rating of the device. Thus, the drain current includes the displacement current from output capacitor of the device and the avalanche current. In this case, the avalanche energy not only includes the charging energy of the output capacitance, but also includes the dissipated energy by the

avalanche current and clamped drain voltage. During the avalanche breakdown the created electrons move through the drain, whereas the holes move to the gate and source terminals. Due to the potential barrier at the heterointerface of the GaN HEMT structure, the created holes are trapped under the gate layer that leads to increase of the electric field under the gate. These trapped holes can increase with impact ionization

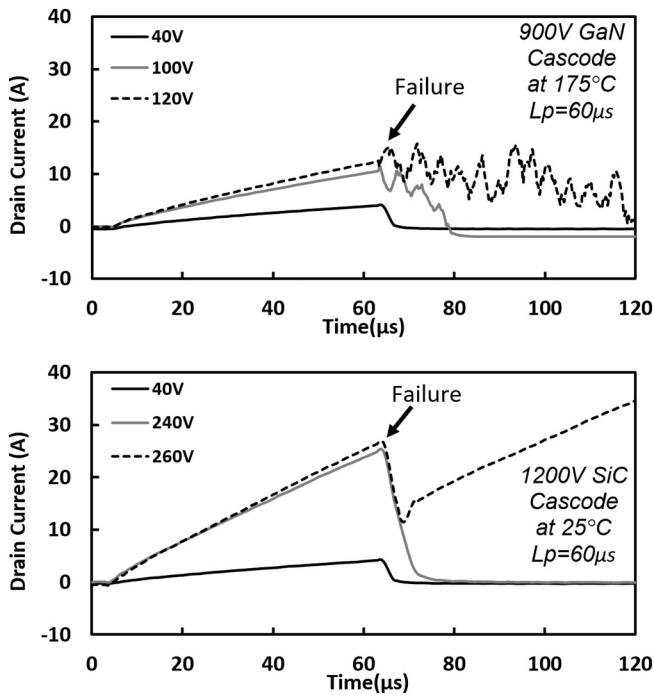


Fig. 9. The drain currents of the high rated GaN and SiC cascodes at different voltage levels with 60 μ s single pulse, with highest voltage being the avalanche voltage at 175 $^{\circ}$ C.

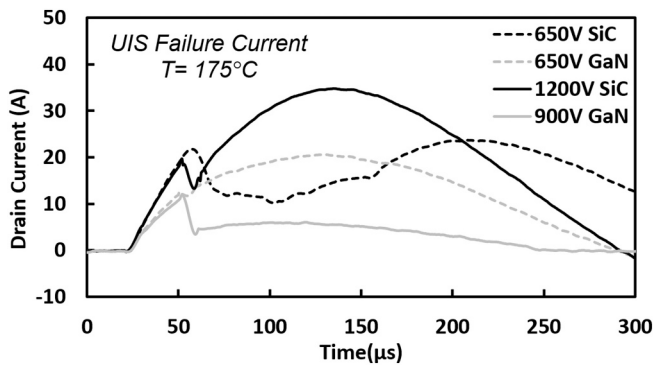


Fig. 10. Drain current of the GaN and SiC cascode devices at avalanche failure with 30 μ s single pulse at 175 $^{\circ}$ C.

and accelerating the device failure at avalanche. The potential at the heterointerface in the GaN structure can be decreased with a negative voltage to the gate of the HEMT which is connected to the source terminal of the LV Silicon MOSFET. This can help the hole extraction of the GaN HEMT structure, reducing the field stress.

Measurements are done with increased periods of pulse to analyse the avalanche energy with doubled period of the single pulse for four devices. It is also seen that the 650 V SiC cascode device withstands against a significant avalanche energy, at 230 mJ, while the similarly-rated GaN cascode device exhibits lower avalanche energy with only 10 mJ. The same level of difference in avalanche rating can also be seen with higher rating devices, and also when the voltage or temperature is increased.

To enable analyzing the avalanche energy density of the devices, the failed devices have been CT-Scanned using a Nikon[®] XT H 225 ST CT-Scanner at the XTM Facility, Palaeobiology Research Group, University of Bristol and have been analyzed using the Dragonfly[®] software for the precise determination of the active area, necessary to calculate the energy density. The results are shown in Fig. 13 together with a

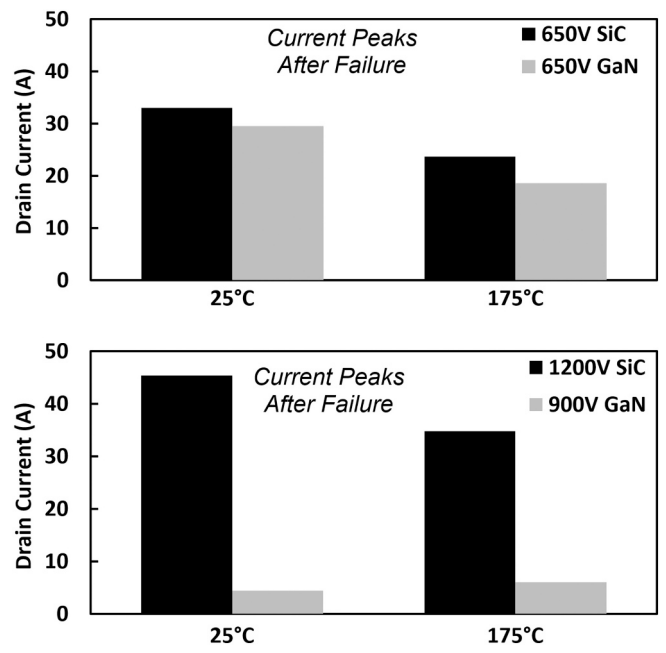


Fig. 11. Current peaks in drain currents of the GaN and SiC cascodes after the avalanche at 25 $^{\circ}$ C and 175 $^{\circ}$ C at the peak with 30 μ s single pulse, as shown in Fig. 10.

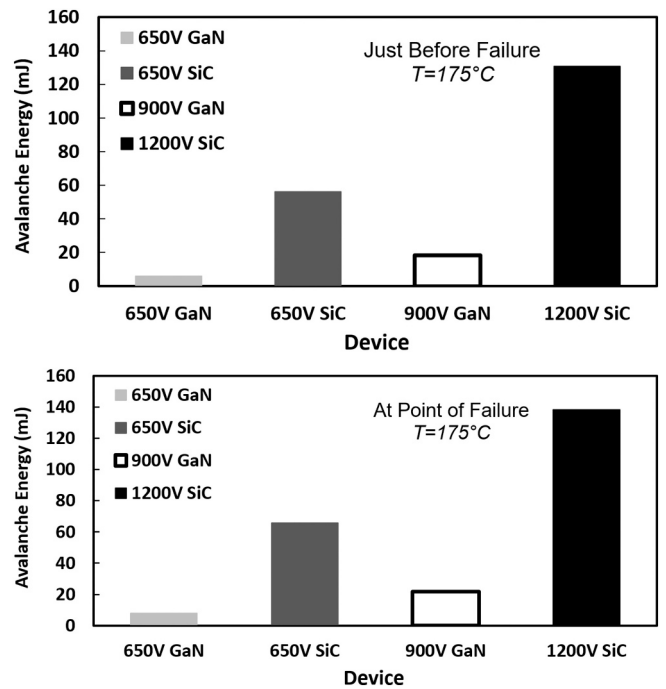


Fig. 12. The avalanche energy of the GaN and SiC cascode devices at point of failure and just before failure when switched with a 30 μ s single pulse at 175 $^{\circ}$ C.

screenshot of the interconnection between the die and direct-bond-copper (DBC) of the decapsulated 900 V GaN cascode device seen under microscope following UIS failure. It can be seen that the size of the GaN device is in fact larger than that of the SiC device, despite its lower avalanche energy, leading to smaller rating per die area (mm^2) as avalanche energy density. Nevertheless, the thickness of the bond wires in the GaN cascode devices are a lot higher than the SiC cascode device (which is about 180 μ m). This has led to a very clear observation of the bond wires in the GaN cascodes, while observation for the SiC device

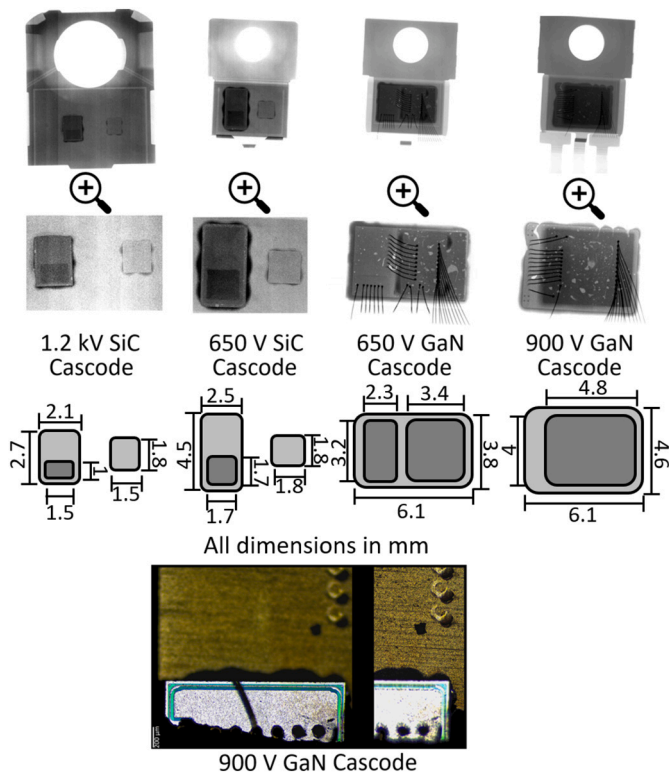


Fig. 13. The failed cascode devices after UIS and view of the exploded 900 V GaN cascode device under microscope. The size of all dies is measured by readings of software in millimeters shown with magnification factor of 19.5 times.

requires deeper zooming with a highly clear contrast. The bond-wire material used by the two manufacturers appears to be different as well. Observation of the dies in the SiC device were particularly difficult since they caused a lot of scatter around the die. The contrast was also difficult to control which could be caused by the resin packaging and thickness of the die. The microscopic view of the 900 V GaN device shows burnout on the die while the impact on substrate has happened during decapsulation of residuals of the package following device explosion at the UIS test.

The measurements shown in Fig. 13 are used to determine the avalanche energy density (mJ/mm^2) of the devices. It is seen in Fig. 14 that given the smaller avalanche energy of the GaN devices, and its dimensions, the avalanche rating per area of the device in GaN is significantly smaller than the SiC device. This is expected, given the lower thermal conductivity of GaN compared with SiC, and is despite using thicker wire-bonds for packaging of the dies in the GaN Cascode structure as shown in Fig. 13. This trend is the same for case of plotting the avalanche energy density just before failure and at the point of failure for both the low voltage and high voltage devices.

Fig. 15 demonstrates the leakage current of the GaN Cascode as opposed to the SiC Cascode and its impact by the UIS avalanche cycles. It can be seen that although the measured leakage current in the GaN device is significantly smaller than that of the SiC device [10–12], it exhibits a clear increase after being subject to avalanche energy after each UIS cycle, especially in the case of the 900 V GaN cascode device. Regarding SiC cascode, the leakage current is higher than that of the GaN devices, but it is almost invariant despite the UIS cycles at higher voltages.

Figs. 16 & 17 show the transfer characteristics of the cascode devices, repeated after each cycle of electrothermal stress by the UIS avalanche energy. It can be seen that the impact of UIS cycles on transfer characteristics on GaN devices is significantly more pronounced than the SiC

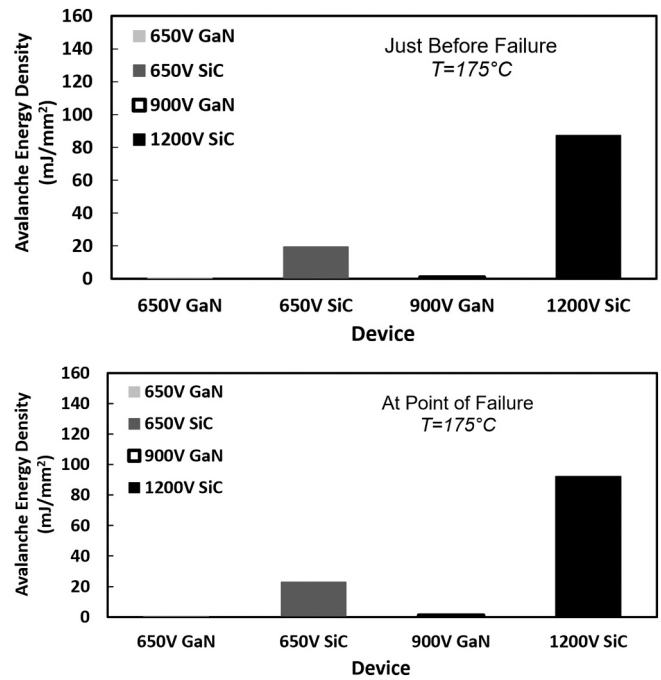


Fig. 14. The avalanche energy per die area (mm^2) of the GaN and SiC cascodes during the avalanche breakdown and just before the failure with $30 \mu\text{s}$ single pulse at 175°C .

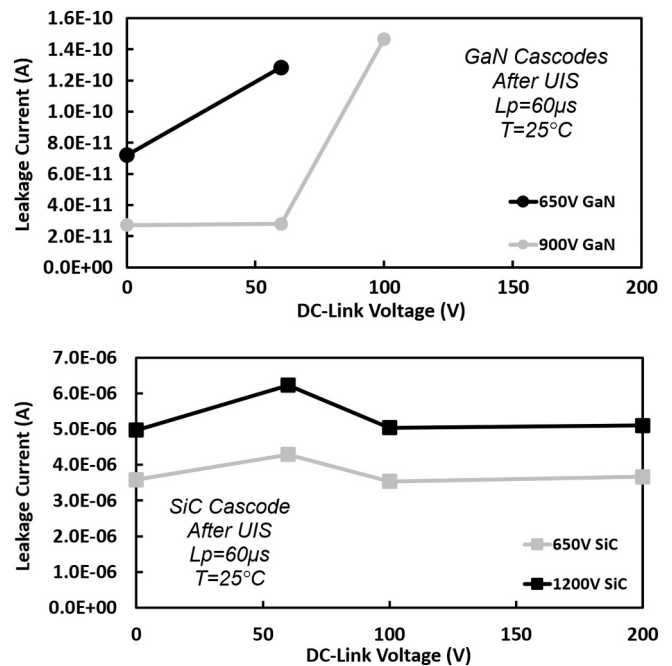


Fig. 15. The leakage currents of the GaN and SiC cascode devices after each electrothermal stress with increasing DC-link voltage and $60 \mu\text{s}$ single pulse at 25°C .

devices, a reason for which is the longer heat dissipation of GaN and the lower threshold voltage in GaN device.

4. Conclusion

This paper demonstrates the avalanche performance of wide-bandgap GaN and SiC cascode devices with close ratings. The UIS test is performed at different voltages, temperatures and pulse lengths to

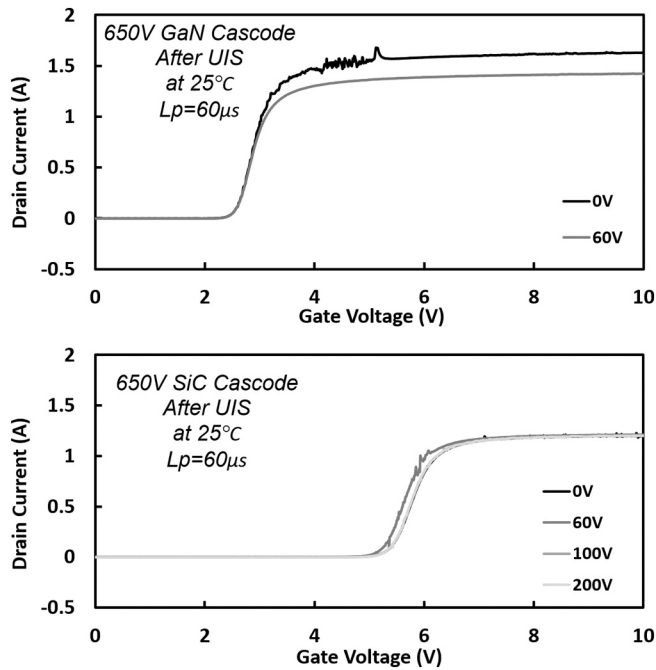


Fig. 16. The transfer characteristics of the low rated GaN and SiC cascode devices after each electrothermal stress with increasing DC voltage and 60 μ s single pulse at 25 °C.

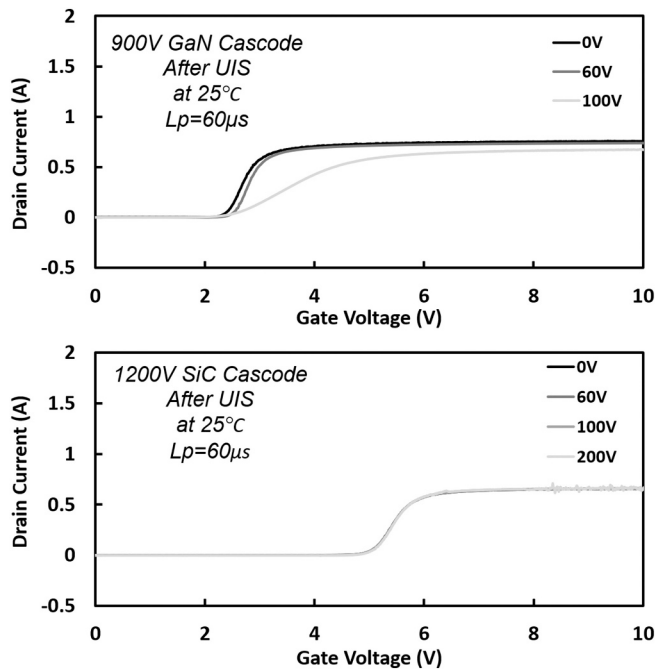


Fig. 17. The transfer characteristics of the high rated GaN and SiC cascode devices after each electrothermal stress with increasing DC voltage and 60 μ s single pulse at 25 °C.

observe the avalanche capability of the cascode devices. The results illustrates that the SiC cascode has higher avalanche energy capability

than the GaN device. The SiC device also has a higher avalanche energy density per area than the GaN Cascode. The current capability in GaN is almost half of that of the SiC device while the SiC cascode can withstand larger bus voltages.

CRediT authorship contribution statement

Yasin Gunaydin: Conceptualization; Investigation; Writing - Original Draft

Saeed Jahdi: Conceptualization; Methodology; Writing - Review & Editing

Phil Mellor: Writing - Review & Editing

Renze Yu: Investigation

Sai Priya Munagala: *Investigation*

Andrew Hopkins: *Investigation*

Nick Simpson: *Investigation*

Mana Hosseinzadehlsh: *Investigation*

Olayiwola Alatisè: Methodology; Writing - Review & Editing

Jose Angel Ortiz-Gonzalez: Methodology; Writing - Review & Editing

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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References

- [1] K. Zhong, Avalanche capability of 650-V normally-off GaN/SiC cascode power device, in: 33rd IEEE Int. Sym. on Power Semi. Dev. and ICs (ISPSD), May 2021, pp. 223–226.
- [2] B. Pushpakaran, et al., Evaluation of SiC JFET performance during repetitive pulsed switching into unclamped inductive load, *IEEE Trans. Plas. Sci.* 42 (10) (Oct. 2014) 2968–2973.
- [3] B.N. Pushpakaran, et al., High temperature unclamped inductive switching mode evaluation of SiC JFET, *IEEE Electron Device Lett.* 34 (4) (April 2013) 526–528.
- [4] J. Ortiz Gonzalez, et al., 'Dynamic characterization of SiC and GaN devices with BTI stresses', in *microelectronics reliability*, Volumes 100–101 (2019), 113389.
- [5] X. She, et al., Review of sic power devices & the applications, *IEEE Trans. Ind. Electron.* 64 (10) (2017) 8193–8205.
- [6] S.N. Agbo, et al., UIS performance and ruggedness of stand-alone and cascode SiC JFETs, *Microelectron. Reliab.* 114 (2020), 113803.
- [7] R. Zhang, et al., Surge-energy & overvoltage ruggedness of P-gate GaN HEMT, *IEEE Trans. Power Electron.* 35, 12 (2020) 13409.
- [8] R. Zhang, et al., Surge energy robustness of GaN gate injection transistors, *IEEE Int. Rel. Phy. Sym. (IRPS)* (Apr 2020) 7.
- [9] L. Yang, Characterization of high-voltage SiC MOSFETs under UIS avalanche stress, in: 7th IET Int. Conf. on Power Electronics, Machines & Drive - PEMD, 2014, pp. 1–5.
- [10] Q. Song, et al., Robustness of cascode GaN HEMTs in unclamped inductive switching, *IEEE Trans. Power Electron.* 37 (4) (April 2022) 4148–4160.
- [11] S. Li, et al., Comparison investigations on unclamped-inductive-switching Behaviour's of GaN switching devices, *IEEE Trans. Ind. Electron.* 69 (5) (May 2022) 5041–5049.
- [12] Y. Gunaydin, et al., Performance of wide-bandgap discrete and module cascodes at sub-1 kV: GaN vs. SiC, *Microelectron. Reliab.* 125 (2021), 114362.