Impact of threshold voltage shifting on junction temperature sensing in GaN HEMTs

Burhan Etoz[1], Jose Ortiz Gonzalez[1], Arkadeep Deb[1], Saeed Jahdi[2] and Olayiwola Alatise[1]
[1]SCHOOL OF ENGINEERING, UNIVERSITY OF WARWICK
Coventry, United Kingdom
[2]FACULTY OF ENGINEERING, UNIVERSITY OF BRISTOL
Bristol, United Kingdom
Tel.: +44(0)247 615 1437
E-Mail: burhan.etoz@warwick.ac.uk, J.A.Ortiz-Gonzalez@warwick.ac.uk,
Arkadeep.deb@warwick.ac.uk, saeed.jahdi@bristol.ac.uk, O.Alatise@warwick.ac.uk

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Keywords

«Gallium Nitride (GaN)», «HEMT», «Leakage Current», «Condition Monitoring», «Junction Temperature»

Abstract

Junction temperature sensing in GaN HEMTs has been identified as a critical challenge for condition monitoring especially under power cycling conditions. The use of temperature sensitive electrical parameters has been widely studied. In GaN devices, the ON-state resistance and gate leakage currents have been identified as TSEPs as both are junction temperature sensitive. Circuits capable of measuring the gate leakage currents in commercially available GaN HEMTs have previously been presented, however, the impact of variability in the threshold voltage on junction temperature sensing requires further investigation. In this paper, junction temperature measurements are implemented using the gate current as a TSEP and are compared with the junction temperature inferred from the ON-state resistance. The measured junction temperatures were verified against electrothermal simulations using manufacturer provided thermal networks. Threshold shift from charge trapping in Schottky GaN HEMTs has been shown to impact the temperature dependence of the gate leakage currents and ON-state resistance. It is important to account for these changes when using them as temperature sensitive electric parameters for real time junction temperature estimation in GaN HEMTs.

1. Introduction

GaN HEMTs are capable of very high switching frequencies while maintaining high energy conversion efficiency [1]. This is due to the very low switching losses compared to comparatively rated SiC MOSFETs and IGBTs. Carrier confinement in the AlGaN/GaN hetero-interface means very high electron mobility since carriers are shielded from scattering mechanisms (like acoustic phonon, surface roughness or ionized dopants) that reduce carrier mobility. This high carrier mobility means low conduction losses and low specific ON-state resistance which can be traded for reduced parasitic capacitances by die shrinkage. Hence GaN devices have the lowest switching energy compared to all other comparatively rated technologies including SiC MOSFETs.

GaN HEMTs, due to spontaneous charge polarization and carrier confinement in quantum wells at the AlGaN/GaN interfaces, are normally ON. However, GaN e-HEMTs have been made normally OFF using advanced gate technologies. The two commercially available variants of GaN HEMTs are the Schottky gated GaN HEMTs (from GaN Systems) [2] and Ohmic gated GaN HEMTs (from Infineon) [3]. Both devices comprise of reverse biased PN junctions to deplete the 2DEG of carriers in the OFF

state. Fig. 1 shows a simple schematic of the gate structure [4] of the Schottky gated GaN HEMT with the back-to-back diode arrangement that enables normally OFF operation. To turn the Schottky gated GaN HEMT ON, the breakdown voltage of the reverse bias Schottky diode must be exceeded and the GaN/AlGaN diode must be forward biased for hole injection into the AlGaN layer. For charge neutrality, electrons must diffuse from the AlGaN layer into the p-GaN gate. This means that unlike MOS gated devices, like MOSFETs and IGBTs, there is significant gate current (µA to mA depending on the gate technology and temperature) during steady state ON operation of GaN e-HEMTs. In MOSFETs and IGBTs, gate leakage currents are on the order of nanoamperes due to the fact that leakage currents are generated from carriers scaling the oxide interface as a result of thermal energy and high electric fields. Furthermore, at the nominal gate driving voltage the increase with temperature of the gate leakage currents [5] is very low in MOS devices, which result in measurement challenges.

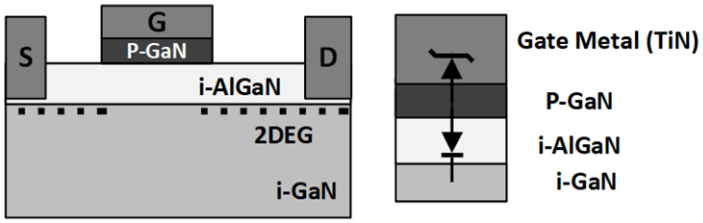


Fig. 1. Schottky gated GaN HEMT showing gate design

When power cycling GaN HEMTs, it is a requirement to have accurate measurements of the junction temperature [6]. This is to enable control of the power cycling system especially as the device packaging degrades and the thermal impedance of the package changes with the number of cycles. The gate leakage current in GaN HEMTs have previously been identified as TSEP for junction temperature estimation for both Schottky Gate and Ohmic Gate HEMTs [7, 8]. The gate leakage current in GaN e-HEMTs shows a very high temperature dependency, as shown in [9, 10] for Schottky gate GaN HEMTs. Modified gate driver circuits with diodes for sensing gate leakage currents have been developed for real-time junction temperature sensing in GaN devices and were presented in [8, 11]. The HEMT ON-state resistance has also been identified as a TSEP since it increases with temperature, with a temperature coefficient higher than SiC MOSFETs and silicon IGBTs [12]. However, the stability of TSEPs is important to investigate since unstable TSEPs can cause inaccurate junction temperature estimation, as shown in [13] for SiC MOSFETs. One of the device parameters that can influence the use of TSEPs in GaN is the threshold voltage. Threshold voltage (V_{TH}) shifting under gate voltage stress in GaN devices has been reported by various researchers, with both positive and negative shifts in V_{TH} reported depending on the magnitude of the gate voltage stress, the stress time and the stress temperature [2, 9, 14-16]. At low V_{GS} stress voltages, positive V_{TH} shifts have been reported due to negative charge trapping in the p-GaN gate. At higher V_{GS} stress, negative V_{TH} shifts have been reported to positive charge injection in the AlGaN layer. In this paper, V_{GS} stressing is combined with gate leakage current measurements to investigate the consistency of the gate leakage currents and ON-state resistance as TSEPs, similar to the studies done with SiC MOSFETs and the impact of V_{TH} shifts in TSEPs [13, 17]. Section 2 of the paper describes the experimental set-up for gate leakage current measurement and junction temperature estimation. Section 3 analysis the experimental measurements while section 4 discusses the impact of threshold voltage shifting.

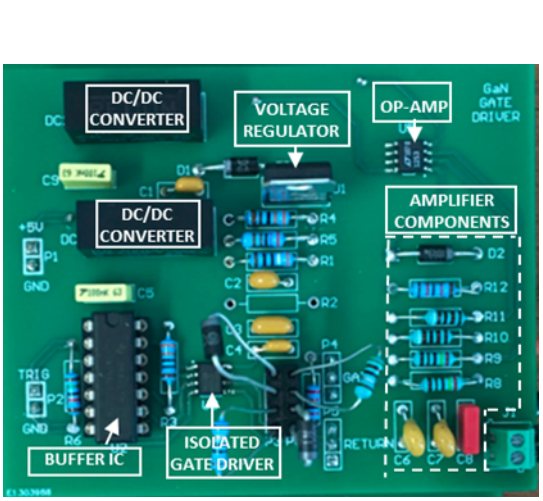
2. Experimental Measurement of Gate Leakage as TSEP

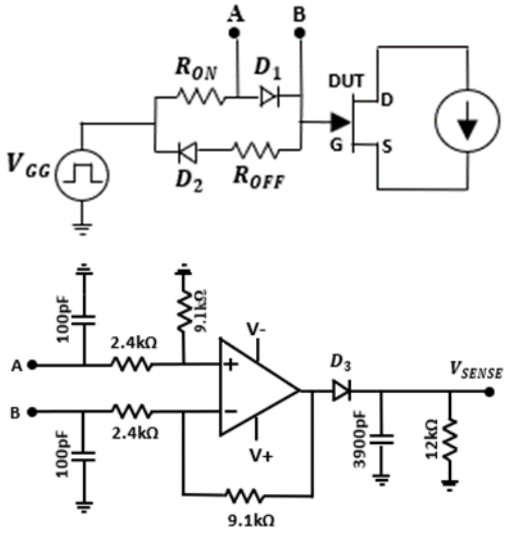
a. Gate Driver for Junction Temperature Sensing

To evaluate the effectiveness of the gate leakage current as a TSEP, the gate driver circuit of the GaN HEMT has been modified to include the leakage current sensing diode. In this paper, commercially available normally-OFF 650V/30A GaN HEMTs from GaN Systems with datasheet references GS65508T have been evaluated. The gate driver has two isolated DC/DC converters: one with datasheet reference RP-0509S for providing the required voltage to an adjustable voltage regulator that defines the gate driver supply voltage and another DC/DC converter with datasheet reference RP-0512D, which

provides the dual voltage required for powering an operational amplifier. The PCB prototype designed for testing GaN HEMTs, and sensing voltage measurement is shown in Fig. 2(a). The circuit schematic of the experimental set-up and further details of the temperature sensing circuit are shown in Fig. 2(b). When the device is ON, the gate leakage current forward biases the diode D_1 in series with the gate resistance R_{ON}, as shown in Fig. 2(b). Since the leakage current increases with the temperature, this causes an increase of the voltage across the diode. The diode type used for this study is pn rectifier diode with datasheet reference of 1N4007. A differential amplifier circuit is used to indicate the sensing voltage by amplifying the voltage difference between anode and cathode terminals of the pn rectifier diode, V_{AB}. The sensing voltage is proportional with the resistors used in the amplifier input. The relationship between V_{SENSE} and V_{AB} is given by (1).

$$V_{SENSE} = \frac{R_2}{R_1} V_{AB} \tag{1}$$





(a) (b)

Fig. 2 (a) GaN Gate driver circuit and GaN HEMT with connections, (b) Circuit schematic of GaN HEMT and gate driver with current sensing diode and differential amplifier

In the diode voltage sensing circuit, R_1 and R_3 are 2.4 kΩ, and R_2 and R_4 are 9.1 kΩ. The differential amplifier's main component is a operational amplifier with the reference LT1253, and the op-amp works with -12V/+12V supplied by the RP-0512D. In addition, a passive low-pass filter was used at the output of the circuit to suppress unwanted frequencies and transmit signals at the desired frequencies. The cut-off frequency for the filter is selected as 3.4 kHz. The schematic of the gate driver with diode voltage sensing circuit is shown in Fig. 2(b). To measure the current across the diode in the turn-ON branch, the effective gate voltage (V_{GEFF}) of the Device Under Test (DUT) is measured after triggering the circuit with the voltage of 5 V. The gate leakage current causes a voltage drop on R_{ON} and D_1, influencing the effective gate voltage. The current across the diode depends on the applied gate voltage, voltage drop between gate and source, effective gate voltage and the value of turn-ON resistance. The value of the current can be calculated by using equation (2)

$$i_{leak} = \frac{V_{GG} - V_{D1} - V_{GEFF}}{R_{ON}} \tag{2}$$

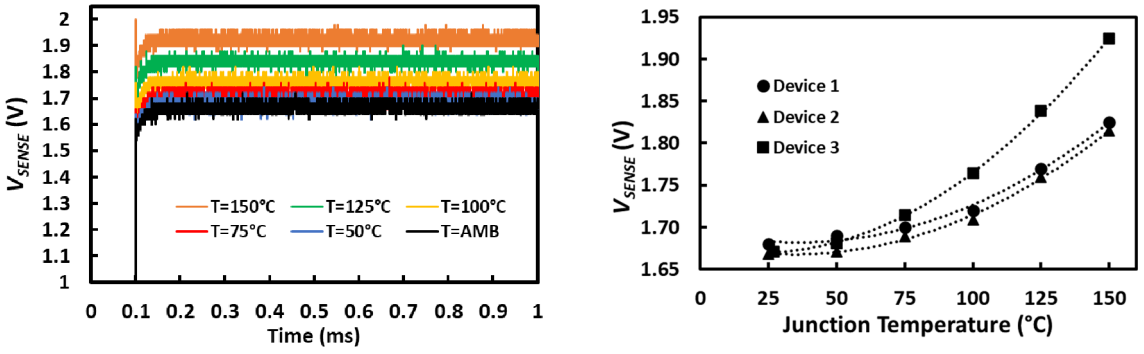
b. Temperature Calibration Curves

For the calibration test, three GaN devices were characterized at different junction temperatures ranging from ambient temperature (T_{AMB}) to high temperature (150°C). The case temperature (T_C) was set using a small DC electric heater and sufficient time was allowed for the junction temperature (T_J) to reach thermal equilibrium with the case temperature. Table I shows the measured sensing voltage (V_{SENSE}) as

a function of the case/junction temperature. The measurements of V_{SENSE} were performed using an oscilloscope (model TDS5054B from Tektronix). Fig. 3(a) shows the plot of the measured sensing voltage during a calibration pulse for one of the GaN HEMTs as a function of time. It can be seen from Fig. 3(a) that when the gate is triggered there is a short transient (less than 50 µs long) before V_{SENSE} reaches its steady state value. Fig. 3(b) shows the measured steady-state V_{SENSE} for 3 different GaN devices as a function of junction temperature set by the electric heater. It can be seen from Fig. 3(b), that the temperature dependence of the gate leakage current varies from device to device, hence, normalization techniques are required to make temperature extraction device invariant.

Table I: Sensing voltage at different temperatures

Case Temp (°C)	V_{SENSE} (V)		
	Device 1	***Device 2***	***Device 3***
T_{AMB}	1.680	1.668	1.669
50	1.690	1.671	1.681
75	1.700	1.689	1.715
100	1.720	1.709	1.763
125	1.770	1.760	1.839
150	1.825	1.815	1.927



(a) (b)

Fig. 3(a) Calibration response of the sensing voltage at different temperatures for device 3, (b) TSEP calibration for the evaluated GaN HEMTs

It can be seen that the relationship between V_{SENSE} and temperature follows a quadratic formula. Hence, equations (3) and (4) can be used to extract the junction temperature from V_{SENSE} once the parameters A, B and C have been determined using curve fitting and normalization techniques.

$$V_{SENSE} = A \cdot T_j^2 + B \cdot T_j + C \tag{3}$$

$$T_J = \frac{-B + \sqrt{B^2 - 4 \cdot A \cdot (C - V_{SENSE})}}{2A} \tag{4}$$

3. Analysis of Experimental Measurements

To evaluate the use of the leakage current under power cycling conditions, the experimental set up shown in Fig. 4(a) was set up. This comprises of an IGBT switching in a constant current through the GaN HEMT which is the DUT. The heating and cooling of the DUT are controlled by the IGBT which is switched ON (for heating the DUT) and switched OFF (for cooling the DUT). The DUT is left ON during the test. Fig. 4(b) shows a typical heating/cooling sequence. A thermocouple is used for measuring the case temperature. The duration of the heating pulse as well as the magnitude of the current are used as parameters to control the junction temperature. Fig. 5(a) shows the measured V_{SENSE} for a DUT with 2 heating pulses (12 A and 15 A) at different pulse durations while Fig. 5(b) shows the measured ON-state resistance ($R_{DS\text{-}ON}$) for different heating pulses. The ON-state resistance has a known temperature dependency that can be read off from the datasheet. Fig. 6(a) compares the temperatures extracted using V_{SENSE} with those extracted using $R_{DS\text{-}ON}$, for a 15 A heating pulse. It can be seen from

Fig. 6(a) that for a 16 second pulse, the rise in case temperature (T_C) is under 5°C while the rise in junction temperature is over 55°C. It is also important to mention that V_{SENSE} (gate leakage current) allows to capture both the heating and cooling transient, as shown in Fig. 6(a). Fig. 6(b) shows good agreement between the peak junction temperatures predicted by the 2 TSEPs (V_{SENSE} and $R_{DS\text{-}ON}$)

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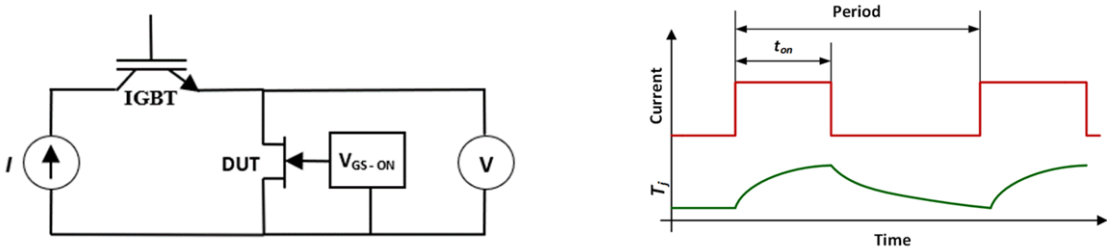
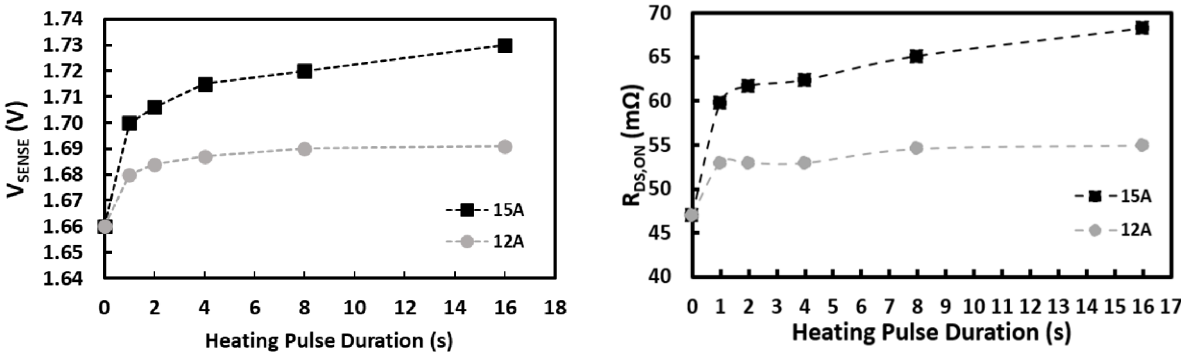


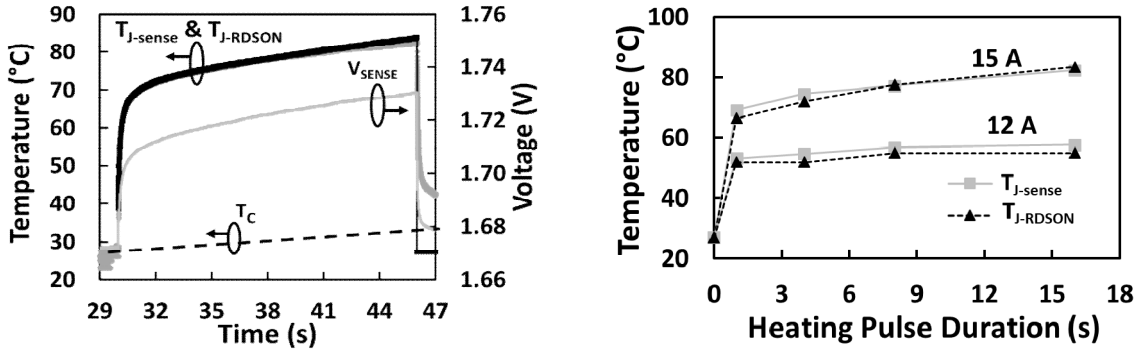
(a) (b)

Fig. 4 (a). Experimental set-up for heating and cooling the DUT, (b) Heating/cooling transient



(a) (b)

Fig. 5 (a) V_{SENSE} for different heating pulses, (b) Measured $R_{DS\text{-}ON}$ for different heating pulses

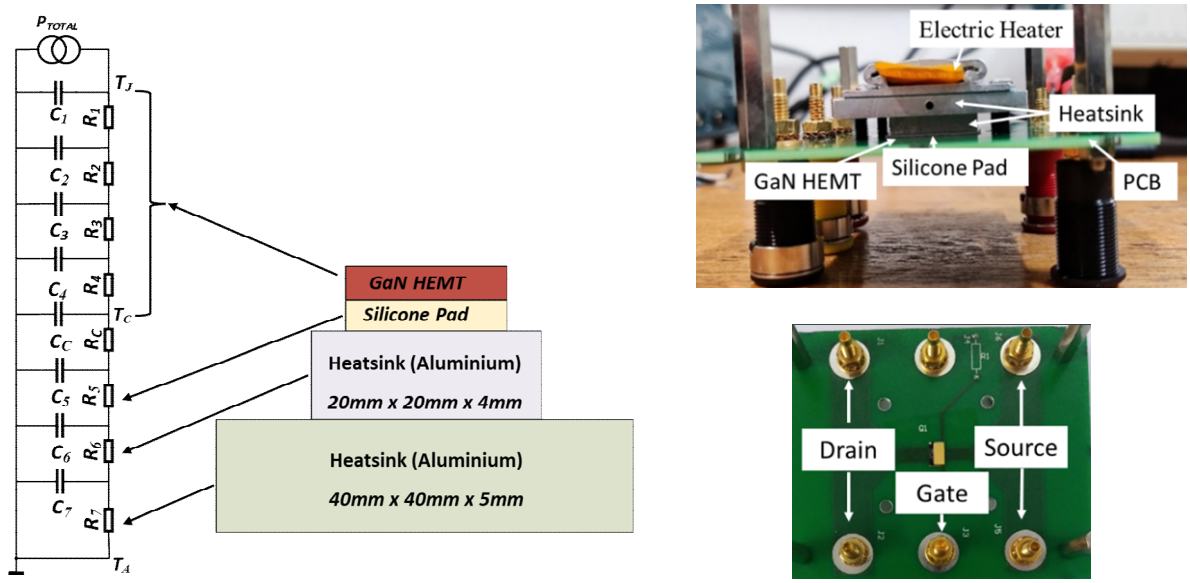


(a) (b)

Fig. 6 (a) Extracted temperature from V_{SENSE} and $R_{DS\text{-}ON}$ for the GaN DUT during a heating transient (b) Comparison of the peak junction temperatures predicted using $R_{DS\text{-}ON}$ and V_{SENSE}.

To check the validity of the junction temperature measured using the TSEPs, the junction temperature is simulated in Simulink, using the measured heating power (current and voltage) and the thermal network provided by the manufacturer. As the device is mounted on a heatsink, the thermal resistance and capacitance of the heatsink is also an input to the simulation. Fig. 7(a) shows the Cauer thermal network of the device while Fig. 7(b) shows the picture of the device on the heatsink, as well as the custom PCB for testing the GaN e-HEMT. The parameters of the thermal network used in the simulation are shown in Table II. The thermal capacitances and resistances are taken from the GaN e-HEMT datasheet while the parameters from the heatsink are calculated using the physical dimensions and material properties of the heatsink. Fig. 8(a) shows a comparison of the electrothermal simulations with

the measured junction temperatures using the gate leakage current TSEP for a 1 second heating pulse while Fig 8(b) shows the same comparison for an 8 second pulse. Good matching of the measured and simulated junction temperatures demonstrates the accuracy of the electrothermal model.

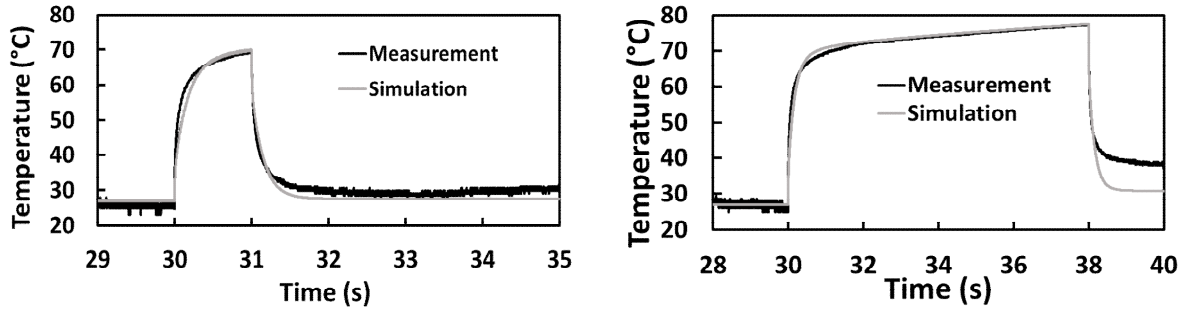


(a) (b)

Fig. 7 (a). Schematic diagram showing thermal network of the GaN HEMTs and heatsink, (b) Pictures of the DUT on heatsink

Table II: Parameters of thermal network used in GaN Thermal simulations

Material	R (°C/W)		C (Ws/°C)	
GaN HEMT (GS66508T)	R_{TH1}	0.150	C_{TH1}	8×10^{-6}
	R_{TH2}	0.230	C_{TH2}	7.4×10^{-4}
	R_{TH3}	0.240	C_{TH3}	0.065
	R_{TH4}	0.015	C_{TH4}	0.002
Silicone Pad	R_{TH5}	2.100	C_{TH5}	0.060
Heat Sink (20 mm x 20 mm x 4 mm)	R_{TH6}	0.049	C_{TH6}	3.880
Heat Sink (40 mm x 40 mm x 5 mm)	R_{TH7}	0.015	C_{TH7}	19.440

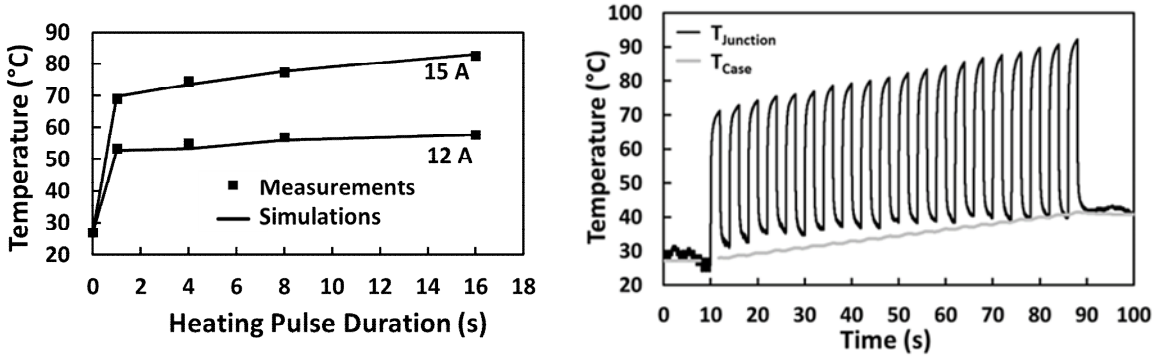


(a) (b)

Fig. 8 (a) Junction temperature measurements and simulations for a 1 second pulse, (b) Simulated and measured junction temperature for an 8 second pulse

The measured and simulated peak junction temperatures are shown in Fig. 9(a), indicating good agreement between the model and the measurement. Additionally, one of the main benefits of this TSEP (V_{SENSE}) is that it allows to capture both the heating and cooling transient during power cycling. This is

shown in Fig. 9(b) for a heating/cooling sequence of 40 pulses (2 s ON/ 2 s OFF) and a heating current of 15 A. The case temperature, measured with at thermocouple is also shown, indicating the effectiveness of the TSEP for monitoring the junction temperature during power cycling. The next section of the paper will perform some gate stress tests on the DUT and evaluate the impact of threshold voltage shift on the TSEPs. This is particularly relevant for power cycling, as it is the case of SiC MOSFETs [18].

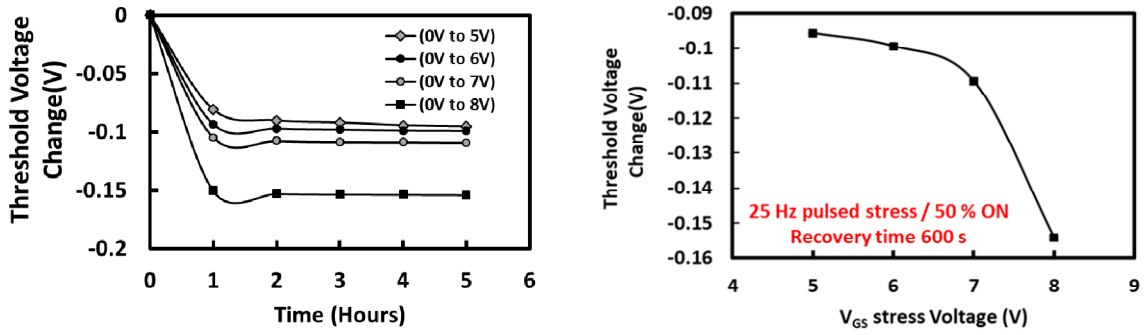


(a) (b)

Fig. 9 (a). Simulated and measured peak junction temperature (using V_{SENSE} as TSEP)
(b) Repetitive heating/cooling pulses. 15 A heating current – 2 s ON – 2 s OFF

4. Impact of Gate Stress on Junction Temperature Measurement

At high gate stress voltages, V_{TH} in GaN HEMTs have been known to exhibit both upward and downward shifts [2, 19, 20] depending on which stress mechanism dominates i.e. if negative charge trapping in the p-GaN gate dominates, then V_{TH} shift upwards and if positive charge trapping in the AlGaN layer dominates, V_{TH} shifts downwards. The polarity of the V_{TH} shift is also recovery time dependent being initially positive (due to more electron trapping) and then becoming negative (due to faster electron release) [9]. Fig. 10(a) shows the results of positive gate voltage stress applied for 5 hours (25 Hz pulsed stress and 50% duty cycle) on the 650 V GaN e-HEMT with different stress voltages. It is clear that there is saturation of V_{TH} shift within the first hour. The recovery time (time between V_{GS} stress removal and V_{TH} measurement) in these measurements was over 600 seconds. The results show a negative shift in V_{TH} which increases with the magnitude of the V_{GS} stress. Fig. 10(b) shows the measured V_{TH} shift as a function of V_{GS} stress. This change in V_{TH} is likely to impact both the $R_{DS\text{-}ON}$ (through the gate overdrive voltage: V_{GS} - V_{TH}) and V_{SENSE} (through the change in leakage current).

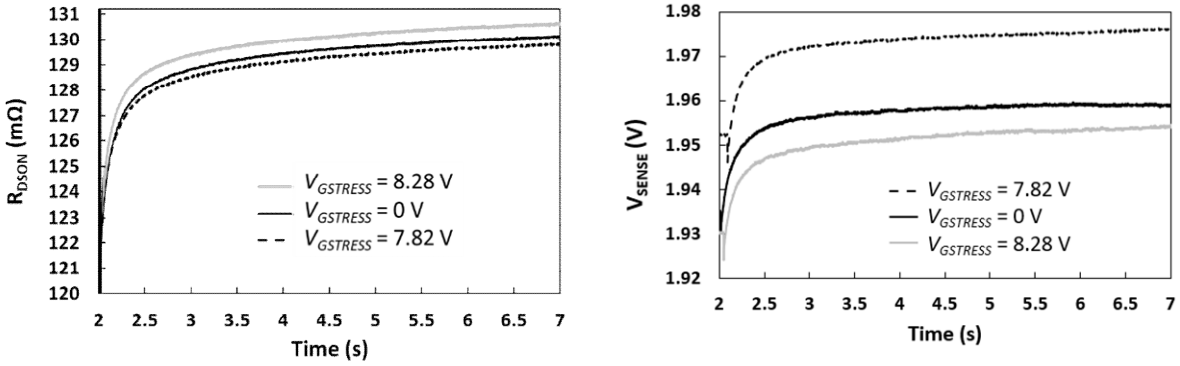


(a) (b)

Fig. 10 (a) Impact of gate stress voltage level on V_{TH} shift (25 Hz pulsed stress and 50% duty cycle)
(b) Change in V_{TH} as a function of stress voltage

To investigate the impact of V_{TH} shift on the consistency of V_{SENSE} and $R_{DS\text{-}ON}$ as TSEPs, accelerated V_{GS} stress tests were performed, by applying gate-source voltages higher than the rated value of the selected GaN HEMT. Fig. 11(a) shows the measured $R_{DS\text{-}ON}$ for a GaN HEMT that has been subjected to cumulative gate stresses of 8 V and 8.5 V for 300 s at 150 °C. The effective $V_{GS\text{-}STRESS}$ values were 7.82 V and 8.28 V after accounting for the voltage drop across a 15 Ohm series resistance used for

limiting the peak current during the gate stress sequence. These stress voltages were selected to cause a more permanent V_{TH} shift, enabling the study of the impact of the V_{TH} shift on the TSEPs. Fig. 11(b) shows the measurements of V_{SENSE} for the same device.



(a) (b)

Fig. 11 (a) Impact of $V_{GSTRESS}$ on R_{DSON}, (b) Impact of $V_{GSTRESS}$ on V_{SENSE}

The characterization was performed using a 5 A and 5 second single pulse. In the absence of stress-induced V_{TH} shift, the characteristics in Fig. 11(a) and Fig. 11(b) should all be super-imposed with no apparent variation. However, it is clear from Fig. 11(a) that $R_{DS\text{-}ON}$ shifts first downwards for $V_{GS\text{-}STRESS}$ = 7.82 V and upwards for $V_{GS\text{-}STRESS}$ = 8.28V. V_{SENSE} shifts in the opposite directions by first going up at $V_{GS\text{-}STRESS}$ = 7.82V and then going down after the 8.28V gate stress. This means both parameters will record different junction temperatures in contradiction to the plots shown in Fig. 6(b) where both TSEPs show a good agreement on junction temperature estimation. Evaluating both TSEPs after the stress sequences, it can be observed that the $R_{DS\text{-}ON}$ is less affected than V_{SENSE}. The difference in $R_{DS\text{-}ON}$ after the stresses is around ±0.5 mΩ and the impact on temperature estimation would be less than -1°C for the 7.82 V stress and around +1°C for the 8.28 V stress. The impact of the gate stress is more apparent in V_{SENSE}. For example, considering the 7.82 V stress, a difference of +17 mV is observed, which corresponds to a difference in temperature estimation around +4°C. For the 8.28 V stress, the difference is around -1°C.

5. Conclusion

The use of TSEPs in junction temperature estimation of GaN e-HEMT power devices is important not just for power cycling but potentially in condition monitoring systems where instantaneous junction temperature estimation is important. The ON-state resistance, measured from the forward voltage during ON-state and the gate leakage current have been cited as TSEPs in GaN. In this paper, a previously presented circuit used to measure the gate leakage current of the GaN device is used to estimate the junction temperature. The measured junction temperature is compared to the temperature measured using the ON-state resistance as TSEP and both are shown to have numerical agreement. Using electrothermal simulations, the accuracy of the peak junction temperature measured by the TSEPs (gate leakage current and ON-state resistance) was confirmed using the measured heating power and thermal network parameters taken from the device datasheet as well as heatsink parameters. Threshold voltage shifting from gate voltage stress impacts that ON-state resistance and gate leakage current. If the threshold voltage increases due to electron trapping in the p-gate of the GaN e-HEMT, the ON-state resistance increases due to lower carrier density while the sensing voltage (measured from the gate leakage current) decreases. Similarly, a decrease in the threshold voltage will cause a decrease in the ON-state resistance and an increase in the gate leakage current. Measurements show ON-state resistance is less sensitive to V_{TH} shifting compared to gate leakage current. However, the gate leakage current can provide junction temperature estimation during both the heating and cooling part of the thermal transients while the ON-state resistance gives junction temperature measurement only during the heating part of the transient.

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