

# A new metallization technology for solar cells application

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To my daughter Dolina In memory of my grandfather Yuliy

# Abstract

This Ph.D. thesis is focused on the development and optimization of front and rear side metallization of industrial silicon solar cells. The commonly adopted screenprinted silver metallization has several well-known issues, such as low contact resistance, moderate bulk conductivity and high cost. The approach of this work allows complete silver replacement, both on the front and the rear sides. The development of such a new technology is divided into several parts, each resulting in appropriate feedback in terms of solar cell operation parameters.

A detailed investigation of the aluminum-silicon interdiffusion that occurs during the firing process of screen-printed aluminum layer usually deposited onto the rear of solar cells is reported. This process is very important because it affects solar cell operation and performance through back-surface field passivation. In this study different screen-printing aluminum pastes, differing one from each other in aluminum particle dimensions and glass frit composition, are evaluated in terms of their bulk resistivity, contact resistance to silicon, back surface field depth and solar cell performance. Finally, this study allowed to reveal certain dependences between pastes parameters and their effect on solar cells and to develop useful recommendations for better solar cell performance.

In this work, a new metallization technology is based on an electroplating technique, which for a real industrial application, however, has some critical issues as throughput, floor space, quantity of liquid to manage and the necessity to use some masking technique, such as photolithography. These issues are strongly influencing the metallization technology cost, making it not economically convenient respect silver screen-printing technology. For this purpose, the proposed metallization technique is based on a novel [1] dynamic liquid drop/meniscus (DLD/DLM) technique able to solve both issues.

In this work DLD/DLM technique is studied for possible application in a new rear side metallization technology for solar cells, allowing localized formation of solder pads without any use of photolithography, limiting the cost of the process mainly to the cost of materials, such as nickel and tin, which are significantly cheaper than a silver counterpart that is currently adopted by the industry. The cost reduction is not a single advantage of the proposed technology. An efficiency improvement of up to 0.5  $\%_{abs}$  is obtained due to a better back-surface field conditions.

The development of a new front side metallization is based on a new approach [1] which introduces a layer of mesoporous silicon helpful for further creation of nickelcopper electrical contacts to the emitter region of a solar cell. Process conditions of mesoporous silicon formation and further electroplating steps are studied and optimized in terms of contact resistance and adhesion of such a contacts, in order to guarantee a beneficial influence for solar cells fabricated with the new metallization approach.

As for combination of both front and rear side metallization technologies, together, they result in complete silver removal from a metallization technology of a solar cell with a feasible efficiency enhancement of up to  $1 \%_{abs}$ .

# Motivation

Worldwide energy consumption has grown exponentially during the entire period in which energy consumption has been observed. Over the period 1925 to 1968 worldwide energy consumption had an average growth rate of about 3.5 % per year [2]. According to the U.S. Energy Information Administration, worldwide energy demand had 2 % growth rate over the period 1980 to 2011 and will still experience stable 0.9 % average growth rate at least up to 2040 [3]. Today the major part of energy is produced from fossil fuels, and discussions and speculations on their either physical or economical limits remain relevant. Development of renewable energy technologies could possibly smooth the transition period in future, as conventional fossil fuels become depleted.

In 2011, the International Energy Agency reported that "the development of affordable, inexhaustible and clean solar energy technologies will have huge longerterm benefits. It will increase countries' energy security through reliance on an indigenous, inexhaustible and mostly import-independent resource, enhance sustainability, reduce pollution, lower the costs of mitigating climate change, and keep fossil fuel prices lower than otherwise. These advantages are global. Hence the additional costs of the incentives for early deployment should be considered learning investments; they must be wisely spent and need to be widely shared" [4].

The photovoltaic (PV) market has experienced double digit growth in the past decade and has now reached a global capacity of approximately 67 GW [5]. Average European electricity generation costs from PV modules today are 0.20 €/kWh [5], which is not really competitive with retail electricity prices in majority European countries. Thus, to fully penetrate the market, the cost of PV electricity has to be driven down further. Cost of PV electricity is mainly composed from module installation costs. These costs are composed from costs of production of silicon wafers (i.e. silicon feedstock, saw wires, saw slurry, equipment, labor, cost of capital, manufacturing margin, etc.), solar cells manufacturing (i.e. metallization, SiN<sub>x</sub>, dopant, chemicals, equipment, labor, cost of capital, manufacturing margin, etc.) and module assembling (i.e. glass, EVA, metal frame, j-box, equipment, labor, cost of capital, manufacturing margin, etc.). Today, shares are 32, 23, and 44 % respectively [6]. It is clear that PV electricity cost reductions depend on the cost reduction in each of these directions.

In order to decrease the solar cell production cost, new technologies or improvements to existing have to be implemented. In particular, in the field of solar cells production efforts are concentrated on three main directions: thinner silicon wafers, higher cell efficiency and low-cost processes development. At the same time, innovations are challenged by industrial requirements, such as throughput of not less than 3000 cells per hour, small foot-print and production lines automation.

This Ph.D. project is focused in the field of solar cells technology, in particular in the development of a new metallization technology for solar cells aimed to replace expensive silver, improve conversion efficiency and, thus, drive cost reduction.

Silver that is commonly used for front- and rear-side metallization represents the most expensive material used in current solar cell technologies aside of the silicon wafer itself. According to the most recent International Technology Roadmap for Photovoltaic (ITRPV) silver is consumed around 100 mg per cell [6]. The average price of silver in 2014 of 550  $\in$  resulted in costs of 5.5  $\notin \in$  per cell, or about 10-15 % of the cell cost. Considering the price of silver is expected to remain high, research and development of alternative metallization technologies is of extreme relevance.

# **Thesis outline**

In **Chapter 1** the solar cell operation on the level of semiconductor physics is discussed, and physical and technological limitations are analyzed to define possible directions for solar cell improvement. Since this work concerns the development of a new metallization technology consisting of both front and rear metallization procedures, commonly used and alternative metallization techniques are discussed.

In this work, a new metallization technology is based on an electroplating technique, which for its industrial application, however, suffers of low throughput and necessity of using some masking technique, such as photolithography. These disadvantages could result in such an increase of cost for a metallization technology that finally could cancel the cost savings due to silver removal. For this purpose, the proposed metallization technology uses a novel DLD/DLM technique able to solve both issues. DLD/DLM technique allows very fast electroplating rates, and can be applied in a localized manner without any use of photolithography. The state-of-the-art of the high speed electroplating is reviewed in the **Chapter 2** as well as its compatibility with the DLD/DLM technique used.

In **Chapter 3** experimental and measurement setups used for sample preparation and characterization in this work are described.

A detailed investigation of the aluminum-silicon interdiffusion that occurs during the firing process of screen-printed aluminum layer usually deposited onto the rear of solar cells is reported in **Chapter 4**. This process is very important because it affects solar cell operation and performance through back-surface field passivation. In this study different screen-printing aluminum pastes, differ one from each other by aluminum particle dimensions and glass frit composition, are evaluated in terms of their bulk resistivity, contact resistance to silicon, back surface field depth and solar cell performance. Finally, this study allowed to reveal certain dependences between pastes parameters and their effect on solar cells and to develop useful recommendations for better solar cell performance.

Development of a new rear side metallization technology for solar cells is described in **Chapter 5**. The technology is based on DLD/DLM technique allowing localized formation of solder pads without any use of photolithography, limiting the cost of the process mainly to the cost of materials, such as nickel and tin, which are significantly cheaper than a silver counterpart that is currently adopted by the industry. The cost reduction is not a single advantage of the proposed technology. An efficiency improvement of up to 0.5  $\%_{abs}$  is obtained due to a better back-surface field conditions.

In Chapter 6 development of a new front side metallization technique is discussed. In particular, it is discussed a new approach of introduction of a layer of

mesoporous silicon helpful for further creation of nickel-copper electrical contacts to the emitter region of solar cell. Process conditions of mesoporous silicon formation and further electroplating steps are studied and optimized in terms of contact resistance and adhesion of such contacts, guaranteeing a beneficial influence for solar cells fabricated with the metallization technique presented.

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# Chapter 1. Introduction to solar cell technology

Solar cell is an electrical device that converts energy of light directly into electricity through the photovoltaic effect. The operation of solar cell requires several conditions, such as the absorption of light and the generation of charge carriers, their separation and extraction to an external circuit. Semiconductor material in the form of a p-n junction having appropriate conductive areas is the most common realization of a solar cell.

### 1.1. Crystalline silicon solar cells and operation

The most common manufacturing technology for solar cells is a p-type based crystalline silicon solar cell having a front anti-reflection texturization, a front phosphorus diffused emitter, passivated by a silicon nitride layer and contacted by a screen printed silver grid, and the back contact is formed by screen printing of both aluminum and silver pastes (see figure 1.01). Emitter of a conventional solar cell is exposed to light. Electron-hole pairs that are generated under irradiation are separated by p-n junction and extracted at the front and rear side contacts via an external load. The front contact is usually made from a metal grid that has the lowest possible dimensions to reduce shading losses. Instead, the rear contact is usually a metal layer that covers the whole rear side of a cell.

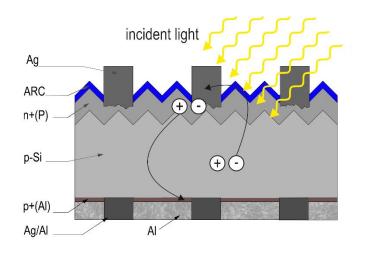


Figure 1.01. Schematic drawing of a typical p-type c-Si solar cell.

## **1.2. Solar cell parameters**

To describe electronic behavior of a solar cell the electrically equivalent model is shown in figure 1.02. A solar cell is usually represented as a diode having shunt and series resistances connected in parallel with a current source. It is clear that the currentvoltage curve (*IV*-curve) of a solar cell exposed to light is affected by both the *IV*-curve of a single diode ( $I_D$ ) and a value of the light-generated current ( $I_L$ ) that is resulted in shifting of the *IV*-curve as it is shown at figure 1.03.

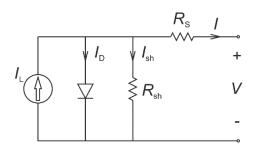


Figure 1.02. The equivalent circuit of a solar cell.

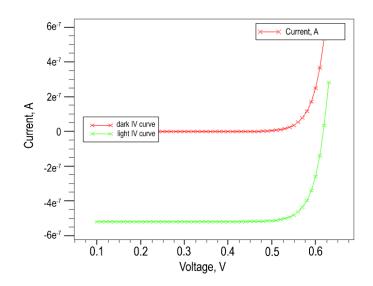


Figure 1.03. Illuminated and dark *IV*-curves of a solar cell.

Considering the Shockley diode equation and the equivalent circuit, the current produced by a solar cell is equal to that produced by the current source after deduction of the current that passes through the diode and the current that passes through the shunt resistor:

$$j(V) = j_0 \left[ e^{\frac{q(V-j(V)R_S)}{nkT}} - 1 \right] + \frac{V-j(V)R_S}{R_{sh}} - j_L,$$
(1.01)

where q is the elementary charge, V is the voltage across the solar cell, n is the diode ideality factor, k is the Boltzmann's constant, T is the absolute temperature,  $R_S$  and  $R_{Sh}$  are series and shunt resistances respectively,  $j_L$  is the photo-generated current and  $j_0$  is the dark saturation current density given by:

$$j_0 = \frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n},$$
(1.02)

where  $p_{n0}$  and  $n_{p0}$  are equilibrium hole and electron densities in n- and p-type regions,  $D_n$  and  $D_p$  are diffusion coefficients for electrons and holes, and  $L_n$  and  $L_p$  are the electron and hole diffusion lengths respectively.

For convenience, the *IV*-curve of a solar cell is usually represented in the first quadrant of the current-voltage plot, where several parameters defining the electronic behavior of a solar cell can be extracted, such as the open-circuit voltage ( $V_{OC}$ ), the short-circuit current ( $I_{SC}$ ) and the maximum power density ( $P_{MAX}$ ), as it is shown in figure 1.04. Using these parameters it becomes possible to calculate several additional parameters, such as the fill factor (*FF*), the efficiency ( $\eta$ ), series ( $R_S$ ) and shunt ( $R_{sh}$ ) resistances and the ideality factor (n).

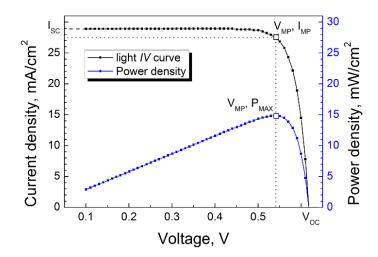


Figure 1.04. Illuminated *IV*-curve and the power density of a solar cell illustrating the *IV*-parameters.

The open-circuit voltage  $V_{OC}$  and the short-circuit current  $I_{SC}$  are the intersection points of the *IV*-curve with the voltage and current axes. The point at which a solar cell demonstrates the maximum power is called the maximum power point ( $P_{MAX}$ ) and is characterized by  $I_{MP}$  and  $V_{MP}$  coordinates.

The short-circuit current is the current that passes through the cell at zero voltage. The short-circuit current depends mainly on the generation and collection of light-generated carriers. For an ideal solar cell the short-circuit current has to be equal to the light-generated current, but in practice, it is limited by resistive loss mechanisms and depends on number of factors, such as the area of the solar cell, the power of the incident light source and its spectrum, optical properties of the surface of the solar cell, its passivation and minority carrier lifetime in the base. In an ideal solar cell each photon having energy higher than the band gap provides one charge carrier to the external circuit, thus, the highest short-circuit current is available for materials with the lowest band gap [7]. The empirical equation for the short-circuit current can be expressed as:

$$j_{SC} = qG(L_n + L_p), \qquad (1.03)$$

where G is the generation rate, and  $L_n$  and  $L_p$  are the electron and hole diffusion length respectively.

The open-circuit voltage is the maximum voltage that is possible to obtain from a solar cell, which occurs at zero current. Considering the Shockley diode equation, the simplified equation for the open-circuit voltage is given by:

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{j_L}{j_0} + 1\right).$$
 (1.04)

As it is seen form the equation, the open-circuit voltage depends on both the dark saturation current of the solar cell and light-generated current. The dark saturation current depends on recombination processes in a solar cell and may vary by orders of magnitude. Thus, the open-circuit voltage is usually considered as a measure of recombination rates in a solar cell. The open-circuit voltage can be also determined from the carrier concentration [8]:

$$V_{OC} = \frac{kT}{q} \ln \left[ \frac{(N_A + \Delta n)\Delta n}{n_i^2} \right], \tag{1.05}$$

where  $N_A$  is the doping concentration,  $\Delta n$  is the excess carrier concentration and  $n_i$  is the intrinsic carrier concentration.

While the short-circuit current decreases with increasing of the band gap, the open-circuit voltage increases as the band gap increases. The phenomena of increasing of the open-circuit voltage comes from determination of the dependence of the dark saturation current on the band gap, that using thermodynamic approach may be given by [9]:

$$j_0 = \frac{q}{k} \frac{15\sigma}{\pi^4} T^3 \int_{E_G/kT}^{\infty} \frac{x^2}{e^{x-qV/kT} - 1} dx, \qquad (1.06)$$

where  $\sigma$  is the Stefan-Boltzman constant, k is the Boltzmann constant,  $E_G$  is the band gap, and x is the wavelength of the incident irradiation.

The equation  $x^2/(e^x - 1)$  is the approximation of the AM1.5 spectrum, and two spectra together are shown in figure 1.05. Integration of such a spectrum results in the value of the power intensity of the irradiation that is absorbed by a solar cell, which in conditions of the equation 1.06 decreases with increasing of the band gap.

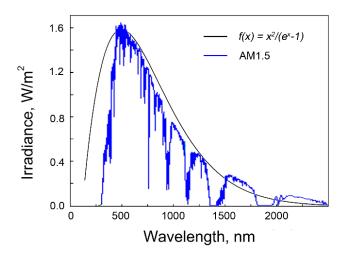


Figure 1.05. Spectrum of the AM1.5 illumination and its mathematical approximation.

Since the dark saturation current decreases by orders of magnitude with increasing of the band gap, it results in increasing of the open-circuit voltage considering the equation 1.04, confirmed in [7].

The "fill factor" (usually "*FF*") is a parameter that determines the maximum power of a solar cell and is defined as the ratio of this power to the product of the opencircuit voltage and the short-circuit current:

$$FF = \frac{P_{MAX}}{I_{SC}V_{OC}} = \frac{I_{MP}V_{MP}}{I_{SC}V_{OC}}.$$
(1.07)

The fill factor is considered as a measure of the "squareness" of the *IV*-curve of a solar cell. In principle, higher possible fill factor is achievable at higher voltages, however, this requires change of a semiconductor material since the open-circuit voltage is limited mainly by the material parameters, such as the band gap.

The ideality factor is a measure of the junction quality and the type of recombination in a solar cell. For simple recombination mechanisms, such as band to band and Shockley-Read-Hall recombinations, the ideality factor has a value of 1. However, some recombination mechanisms in space charge region, in particularly in the high level injection condition, may influence the ideality factor of up to a value 2. This causes degradation of the fill factor.

The efficiency is the basic parameter to compare performances of solar cells between each other. Efficiency is defined as the ratio of the energy that is harvested by a solar cell to the energy that is coming from the AM1.5 solar simulator. In order to provide fair comparison of solar cells between each other, measurement conditions must be carefully controlled, because the efficiency depends on such parameters as the temperature, the spectrum and the intensity of the incident light.

Thus, the efficiency of a solar cell is given by:

$$\eta = \frac{V_{OC}I_{SC}FF}{P_{in}},\tag{1.08}$$

where  $P_{in}$  is the input power. Considering the power density of the AM1.5 spectrum is 100 mW/cm<sup>2</sup>, for 100×100 mm or 156×156 mm solar cells the input powers are 10 and 24.3 W respectively.

Resistive effects in solar cells reduce the power produced by a solar cell due to dissipation of power that occurs on parasitic resistances, such as series and shunt resistances (see figure 1.02). Typically, the influence of resistive effects is evident from the *IV*-curve of a solar cell, which causes significant degradation of the fill factor. Taking into account equivalent circuit of a solar cell (see figure 1.02), the terminal voltage is given by:

$$V = V_D - IR_S, (1.09)$$

where  $V_D$  is the voltage across the junction of the solar cell. As it is seen from the equation, as series resistance increases, the voltage across the solar cell decreases. Behavior of a solar cell having different values of series resistance is illustrated in figure 1.06.

Sometimes, due to manufacturing defects, an alternative current path for lightgenerated current may appear in a solar cell resulting in significant power losses. These losses are caused by the presence of a shunt resistance, which reduces the amount of current flowing through the p-n junction and reduces voltage from the solar cell. The equation for a solar cell in presence of a shunt resistance is given by:

$$j = j_L - j_0 e^{\frac{qV}{kT}} - \frac{V}{R_{Sh}}.$$
 (1.10)

The effect of shunt resistance on the *IV*-curve of a solar cell is shown at figure 1.07. Typical values of shunt resistance for industrial solar cells are in the range of kiloohms. As shunt resistance decreases, the current from the solar cell decreases. Very low values of shunt resistance also cause significant reduction of the open-circuit voltage.

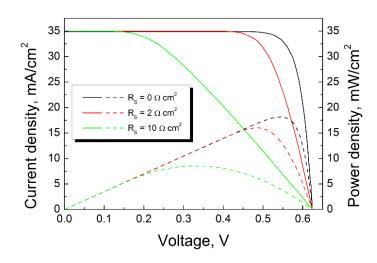


Figure 1.06. Effect of series resistance on the *IV*-curve of a solar cell.

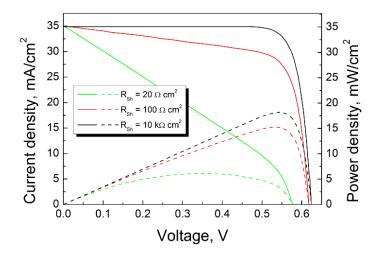


Figure 1.07. Effect of shunt resistance on the *IV*-curve of a solar cell.

# **1.3. Recombination losses in solar cells**

Recombination is the opposite effect of generation, and leads to reduction of free charge carriers. Recombination occurs at impurities and defects of the crystal structure, as well as at the surface. Recombination effect in semiconductors is explained through several mechanisms, occurring independently from each other, such as radiative, non-radiative, and Auger recombination. For each type of recombination process *i* a recombination rate  $U_i$  and a minority carrier lifetime  $\tau_i$  parameters can be assigned. The carrier lifetime parameter  $\tau_i$  though is defined as an average time that charge carrier is able to travel in the crystal before it will recombine.

$$\tau_i = \frac{\Delta n}{U_i} \text{ or } \tau_i = \frac{\Delta p}{U_i},$$
 (1.11)

where  $\Delta n$  and  $\Delta p$  are excess carrier concentrations.

Radiative recombination takes place when an electron goes from the conduction band to the valence band and excites a photon, causing so-called spontaneous emission. In the indirect semiconductor, such as silicon, the radiative recombination occurs with participation of a phonon.

Auger recombination occurs when recombined electrons and holes give their energy excess to a third charge carrier. Normally, this charge carrier receives an increase in kinetic energy, which will be lost during relaxation to a band edge. The Auger recombination is especially active in highly doped semiconductors, as concentrations of charge carriers is increased, as it is seen from formulas defining this process:

$$\tau_{An} = \frac{1}{C + D_n n^2} \text{ or } \tau_{Ap} = \frac{1}{C + D_p p^2},$$
 (1.12)

where *C* is Auger recombination rate constant and  $D_n$  and  $D_p$  are diffusion constants of electron and holes.

Non-radiative recombination or Shockley-Read-Hall (SRH) recombination takes place when charge carrier loses its energy through multiple relaxations over traps and recombination centers in the band gap.

$$\tau_{SRH} = \frac{\sigma_p^{-1}(n_0 + n_1 + \Delta n) + \sigma_n^{-1}(p_0 + p_1 + \Delta n)}{v_{th} N_T(n_0 + p_0 + \Delta n)},$$
(1.13)

where  $n_1$  and  $p_1$  are defined as:

$$n_1 = N_C \exp \frac{E_T - E_V}{kT}$$
 and  $p_1 = N_C \exp \frac{E_V - E_T}{kT}$  (1.14)

where  $E_T$  is the energy level of the trap,  $\sigma_n$  and  $\sigma_p$  are the capture cross sections for electrons and holes,  $v_{th}$  is the thermal velocity of the charge carrier and  $N_T$  is the trap density. It is seen, that the closer is the energy level of the trap to the middle of the band gap and the higher cross section, the lower is the carrier lifetime. For a typical multicrystalline or Cz-silicon material this is the main recombination process, while for a FZ-silicon SRH recombination can be neglected.

Surface recombination appears due to abrupt endings of the crystal lattice. The energy levels of these defects can be found throughout the band gap. This type of recombination is described by an extended SRH model. The recombination activity of all energy levels in the band gap is integrated, assuming a continuous distribution throughout the surface, thus surface recombination can be defined:

$$S = \frac{(n_{s}p_{s} - n_{i}^{2})v_{th}}{\Delta n} \int_{E_{V}}^{E_{C}} \frac{D_{it}(E_{T})}{\frac{n_{s} + n_{1}}{\sigma_{p}(E_{T})} + \frac{p_{s} + p_{1}}{\sigma_{n}(E_{T})}} d(E_{T}) , \qquad (1.15)$$

where  $n_s$  and  $p_s$  are electron and hole concentrations at the surface,  $D_{it}$  is the surface density of defects.

The reduction of the surface recombination can be achieved through reduction of the minority carrier density at the surface and reduction of defects. Minority carriers can be reduced by doping the surface forming back surface field or field effect passivation. Defects concentration can be decreased through the passivation of abrupt endings of the crystal lattice by an appropriate dielectric layer, such as silicon oxide or silicon nitride in case of silicon.

#### **1.4.** Physical limitations of solar cells

According to De Vos et al. [10], the maximum energy conversion efficiency of the sunlight is 86.8 %. However, the theoretical maximum efficiency of the energy conversion for a silicon solar cell at AM1.5 irradiation is about 29.8 % according to Tiedje et al. [11], and there are at least six main physical limitations:

- 1. only photons with energy higher than the band gap (1.12 eV for silicon) can generate an electron-hole pair;
- 2. only one electron-hole pair can be generated by a photon having sufficient energy, the excess of energy is transferred to heat;
- 3. the separation of quasi-Fermi levels defines the maximum achievable opencircuit voltage [8], and, according to Green, may achieve as high as 800 mV for

a 20  $\mu$ m thick solar cell [12], however, high-efficiency silicon solar cell achieve open circuit voltages in the range of 680-720 mV;

- 4. due to unpreventable recombination losses the fill factor is limited to a certain value, which is around 85 % for silicon solar cells;
- 5. optical losses due to reflection caused by mismatch of refractive indexes of the media and the material of a solar cell;
- 6. parasitic resistance losses on solar cell outputs.

In order to balance and reduce the impact of described limitations, researchers all over the world are working on improvement of the quality of materials used for solar cell fabrication, optimization of solar cell design, and invention of new processes and treatment procedures. Today the highest energy conversion efficiency reported for silicon solar cell measured under standard testing conditions is 25.6 % [13]. It was measured by the Japanese National Institute of Advanced Industrial Science and Technology (AIST) for a large area of 144 cm<sup>2</sup> n-type crystalline silicon solar cell fabricated by Panasonic. This cell uses both heterojunction and back-contact cell technologies to reach such performance.

### 1.5. Solar cell technology

Solar cells are usually divided into three main categories named generations. First generation solar cell are typically based on mono- or multicrystalline silicon wafers employing semiconducting p-n junctions or heterojunctions. This is the most widely spread solar cell technology today: more than 80 % of all solar panels sold around the world. Second generation solar cells, also called thin-film solar cells, are usually made of thin layers of semiconductor materials, such as amorphous silicon, cadmium telluride or copper indium gallium diselenide, of just few micrometers thick. Industry expects the possibility of production of solar cell with much lower cost with respect to first generation solar cells due to the combination of using less material and lower cost manufacturing processes. The main feature of third generation solar cells is their possibility to overcome Shockley-Queisser limit of the power efficiency for single band gap solar cells. Among such a type of solar cells there are tandem cells that use multiple p-n junctions based on different semiconductor materials to be able to harvest the energy of the light in several spectral ranges in a more efficient way, quantum dot solar cells, solar cells using photon upconversion or downconversion technologies etc.

Today the most common manufacturing technology for solar cells includes several steps:

1. Choice of the substrate material. Currently Cz monocrystalline and multicrystalline silicon wafers are used. The general trend is to move to larger

size substrates. Currently, typical substrates are 156×156 mm quasi-square wafers.

- 2. Homogenous phosphorus diffusion to form the emitter. Usually to keep lower contact resistance, a higher surface concentration is required, however, too high surface concentration may reduce the cell's response in the blue part of the spectra. To balance between these limitations, technologies of shallow and selective emitters have been developed. Shallow emitters provide surface concentrations high enough to form 55 Ohm/sq emitters and, at the same time, are very thin, usually less than 300 nm, thus improving the cell's blue response. Selective emitter technology [14] introduces additional doping of silicon surface under metal contacts, which in any case is not irradiated, thus lowering the contact resistance and not affecting the cell's blue response.
- 3. Surface texturing to reduce optical losses due to reflection. The reflectivity of flat silicon surface is around 36 %. Application of surface texturing increases the probability of the absorption due to multiple reflections. This operation can be implemented mechanically [15], using chemical [16] or plasma etching [17] also in combination with lithographic mask [18–20].
- 4. Antireflection coating and surface passivation. The most common technology today is chemical vapor deposition of silicon nitride (SiN<sub>x</sub>), which additionally reduces the reflectivity of the surface and effectively passivates surface defects.
- 5. Edge isolation removes shunts from perimeter of the cell, and typically laser cutting is used.
- 6. Front fire-through and rear contacts. Using the screen-printing technology today, both front silver grid and rear aluminum layer and silver solder pads are applied. Screen-printing pastes for the front contact contain chemical agents that help silver metal particles to fire through the antireflection coating and bond to the underlying silicon. Rear contacts are usually made by applying aluminum paste. Common screen printable aluminum pastes are able to form deep and effective aluminum back surface field (Al-BSF), providing also surface recombination velocity values in the range of a few hundred cm/s and performing a backside segregation gettering of undesired metal content within the silicon network. However, conventional solar cell suffers from moderate and incomplete rear passivation with Al-BSF due to silver contact pads that are formed directly on silicon. Silver contact pads are usually applied using second print and are required to create a solderable contact.

# 1.6. Technological limitations of solar cells

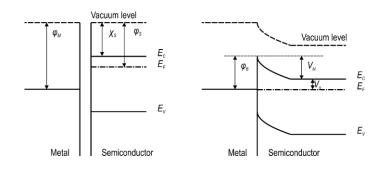
Technological limitations of solar cells are caused by optical and electrical losses due to front side metallization pattern, as well as electrical losses on the rear. As for the front side metallization, optical losses are caused by shadowing and reflection of the light on the metal grid, typical front metal grid of a solar cell results in approximately 8 % of optical losses. Electrical losses are caused mainly due to series resistance, which affects fill factor of a conventional 156 mm solar cell by approximately 5 % for each 1  $\Omega \cdot \text{cm}^2$  increase. The rear side of the cell is almost completely metallized with aluminum, however, in order to ensure the solderability of rear contacts for module assembly, the rear aluminum layer is not homogenous, it contains openings for silver solder pads, that cause inhomogeneous Al-BSF passivation and, as will be shown in this work, reducing the solar cell efficiency by up to 0.5 %<sub>abs</sub>.

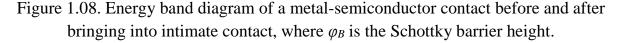
# 1.7. Metal-semiconductor contact

The metal-semiconductor contact was discovered by Braun in 1874 [21]. Before 1930 it was used without complete understanding, however Schottky developed the first acceptable theory of rectification of metal-semiconductor contacts and suggested a potential barrier between the two materials [22,23]. The Schottky model is shown in figure 1.08 and the barrier height  $\varphi_B$  is given by:

$$\varphi_B = \varphi_M - \chi \,, \tag{1.16}$$

where  $\varphi_M$  is the metal work function (the energy from the Fermi level to the vacuum level) and  $\chi$  is the semiconductor electron affinity (the energy from the bottom of the conduction band to the vacuum level). Since the barrier height is not dependent from the Fermi level in the bandgap, the barrier height is not dependent on the doping density.





The model predicts that when the intimate contact between a metal and a semiconductor is established, depending on the metal work function, it results in formation of accumulation, neutral, or depletion contacts as it is shown in figure 1.09. While for rectifying devices a high barrier height is required, an ohmic contact is required for such devices as solar cells, indicated as "accumulation" contact. This type of a contact allows charge carriers to pass freely from the semiconductor to the metal as well as in the opposite direction.

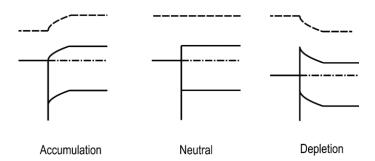


Figure 1.09. Metal-semiconductor contact types according to the Schottky model.

The simple Schottky theory predicts that the barrier height depends directly on the work function of a metal, however, for a real contact this cannot be measured. Plots of a barrier height that depends on a metal work function for silicon are shown in figures 1.10 and 1.11. For simple metals the dependence is weak, however, the silicides can approach values predicted by the Schottky model. This happens probably since the silicide/silicon interfaces located inside the silicon crystal, which eliminates surface effects.

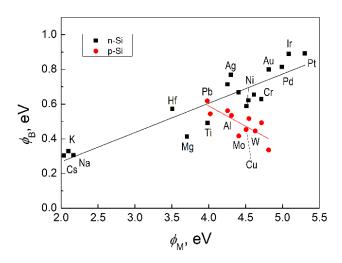


Figure 1.10. Measured barrier heights as a function of metal work function for metal-n-Si and metal-p-Si contacts.

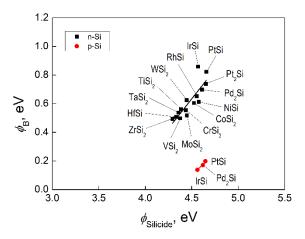


Figure 1.11. Measured barrier heights as a function of metal work function for silicide-n-Si and silicide-p-Si contacts.

Normally there is all the time a barrier for both n- and p-type materials [24], which means that "accumulation" contact (figure 1.09) is impossible to implement. Thus, other way to create ohmic contacts to semiconductors must be found.

Formation of Shottky-barrier is not yet completely understood. Bardeen [25] was the first to suggest that surface states at the semiconductor surface determine the barrier height. These states are abrupt endings in the crystal lattice and impurities [26], as well as other defects that introduce discrete energy levels into the bandgap [27,28]. Moreover, when metal is deposited, there are regions at the interface that contain mixtures of different phases, each having its own work function [29,30]. The Bardeen model claims that there is an energy level for surface states that at normal conditions tends to find equilibrium with energy band structure of the crystal and distort it, forming a barrier. These surface states are acceptor states because occupation of such a state by an electron is associated with removal of an electron from the crystal and formation of a fixed, negatively charged ion at the surface, which results in a space-charge region (SCR) and a barrier as it is shown in figure 1.12. If the surface states density is given by  $N_{SS}$  (cm<sup>2</sup>·eV)<sup>-1</sup>, then

$$E_F - E_0 = \frac{N_D W_{SCR}}{N_{SS}},$$
 (1.17)

where  $N_D$  is the doping density of the substrate and  $W_{SCR}$  is equilibrium width of SCR.

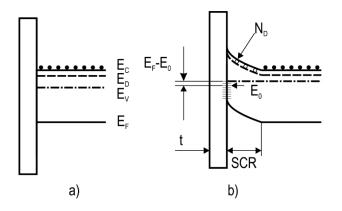


Figure 1.12. A semiconductor energy band diagram without surface states (a) and with surface states (b) according to the Bardeen model.

When metal is brought in contact with a semiconductor, their Fermi levels line up. Excess electrons that usually flow from metal into semiconductor to accumulate the surface, now, instead, are captured by empty acceptor surface states. This shifts the Fermi level slightly due to high density of surface states, and the more the density is, the less is the shift according to (1.17). Therefore, for real semiconductors the barrier height changes hardly (figure 1.13).

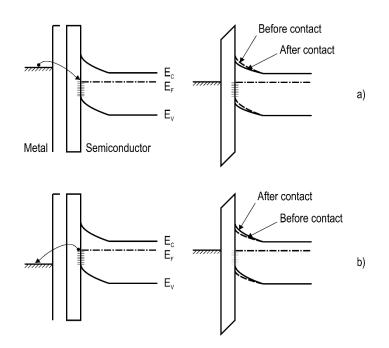


Figure 1.13. The effect of surface states on the barrier height for a low  $\varphi_M$  metal (a) and a high  $\varphi_M$  metal (b).

Northrop and Rhoderick give barrier height as [31,32]:

$$\varphi_B = \gamma(\varphi_M - \chi) + (1 - \gamma)(E_G - E_0), \qquad (1.18)$$

where  $\gamma$  is the surface state parameter,  $E_G$  is the band gap energy,

$$\gamma = \frac{1}{1 + \frac{qtN_{SS}}{\varepsilon\varepsilon_0}},\tag{1.19}$$

and t is the interfacial layer thickness given in figure 1.12, and  $\varepsilon$  is the dielectric constant of the interfacial layer.

It is clearly seen that  $N_{ss} = 0$  results in  $\gamma = 1$ , which leads to the Schottky limit (1.16). For  $N_{ss} \rightarrow \infty$ ,  $\gamma \rightarrow 0$ , resulting in the Bardeen limit and  $\varphi_B = E_G - E_0$ , which means that barrier height is constant and independent of the metal work function  $\varphi_M$ . For real semiconductors, for the Schottky limit the surface states density has to be less than  $10^{12} \text{ (cm}^2 \text{ eV)}^{-1}$ , while for the Bardeen limit more than  $10^{14} \text{ (cm}^2 \text{ eV)}^{-1}$ . In practice, the Schottky model is mainly observed in silicide contacts, because silicide formation incorporates the metal inside the semiconductors crystal and thus causes intimate contact. In other cases, the barrier height is independent on the metal work function, which makes impossible to fabricate accumulation contact, thus, ohmic contact have to be made by other methods.

Even though the barrier height can be significant, the narrow SCR caused by heavily doped semiconductor can allow tunneling of carriers between the metal and the conduction or the valence bands for contacts to n- and p-type semiconductors [33]. The conduction mechanism for a metal/n-type semiconductor contact with increasing doping concentration is shown in figure 1.14. For lowly doped semiconductors ( $N_D < 10^{17}$  cm<sup>-3</sup>), the current flow is the result of termoionic emission over the barrier. In the range of doping concentration from  $10^{17}$  cm<sup>-3</sup> to  $10^{19}$  cm<sup>-3</sup> thermoionic/field emission is dominant. At doping concentration higher than  $10^{19}$  cm<sup>-3</sup> the barrier becomes sufficiently thin to allow the tunneling process to take place.

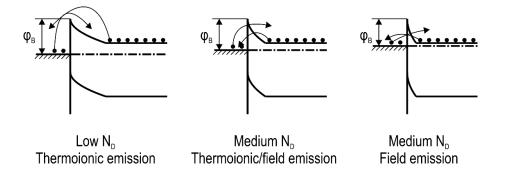


Figure 1.14. Conduction mechanisms for metal/n-type semiconductor as function of semiconductor doping concentration

Therefore, for each conduction mechanism, the current density J depends on both the applied voltage V and the barrier height:

$$J = f(V, \varphi_B). \tag{1.20}$$

The contact resistivity also called specific contact resistance used to characterize the contact independently of the contact are then is given by:

$$\rho_C = \left(\frac{\partial V}{\partial J}\right)_{V=0}.\tag{1.21}$$

The contact resistivity for thermoionic emission is defined:

$$\rho_{C\_TE} = \frac{k}{qA^*T} e^{\frac{q(\varphi_B - \Delta\varphi_B)}{kT}}.$$
(1.22)

where  $A^* \approx (m^*/m_0) \cdot 120 \text{ A} \cdot \text{m}^{-2} \cdot \text{K}^{-2}$  is the effective Richardson constant,  $m^*$  is the effective electron mass and  $m_0$  is the free electron mass.

For the thermoionic/field emission, the contact resistivity is defined [34]:

$$\rho_{C\_TFE} = C_1 \frac{k}{qAT} e^{\frac{q(\varphi_B - \Delta \varphi_B)}{E_0}}, \qquad (1.23)$$

where

$$C_1 = \frac{k_B T \cosh \frac{E_0}{k_B T} \sqrt{\coth \frac{E_{00}}{k_B T}}}{\sqrt{\pi(\varphi_B + E_F) E_{00}}} \exp\left(\frac{E_F}{E_{00} \coth \frac{E_{00}}{k_B T}} - \frac{E_F}{k_B T}\right).$$
(1.24)

And for the field emission [34]:

$$\rho_{C\_FE} = C_2 \frac{k}{qAT} e^{\frac{q\varphi_B}{E_{00}}}, \qquad (1.25)$$

where

$$C_{2} = \frac{\pi}{\sin\left(\frac{\pi kT}{2E_{00}}\ln\frac{4\varphi_{B}}{E_{F}}\right)} - \frac{2E_{00}}{kT\ln\frac{4\varphi_{B}}{E_{F}}} \exp\left(-\frac{E_{F}\ln\frac{4\varphi_{B}}{E_{F}}}{2E_{00}}\right).$$
 (1.26)

 $C_1$  and  $C_2$  are functions of doping, temperature and the barrier height. The energies  $E_0$  and  $E_{00}$  are characteristic energies that describe the tunneling process and relate one to another through [35]:

$$E_0 = E_{00} \coth \frac{E_{00}}{kT} \,. \tag{1.27}$$

The expression  $kT/E_{00}$  is the measure of the ratio of thermoionic emission current to tunneling current. For lightly doped semiconductors  $kT/E_{00} \gg 1$  and thermoionic emission is dominant, for heavily doped semiconductors  $kT/E_{00} \ll 1$  and tunneling is dominant. Thermoionic/field emission is characterized by $kT/E_{00} \approx 1$ .

Therefore, considering the barrier height is usually given as is, the only way to affect contact resistivity is the doping concentration. In figure 1.15 contact resistivity is shown as a function of doping concentration and barrier height. These plots clearly show that for low contact resistivity, such as 1  $\mu\Omega$ ·cm<sup>2</sup>, the doping level for n-type semiconductor must be more than 10<sup>20</sup> cm<sup>-3</sup>, while for p-type more than 10<sup>19</sup> cm<sup>-3</sup>.

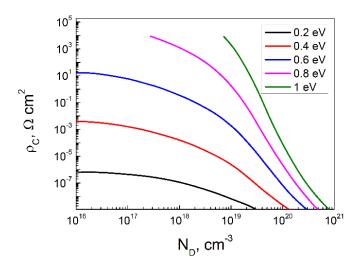


Figure 1.15. Contact resistivity  $\rho_C$  as a function on the doping concentration  $N_D$  and barrier height [21].

#### **1.8.** Metallization technologies

Solar cell is an electrical device having two semiconductor regions, therefore it must have two types of electrical contacts. Normally solar cell is a p-type silicon monocrystalline wafer having front-side phosphorous-diffused emitter. Thus, electrical contacts are located on the front and the rear sides of the wafer. Typical front side electrical contacts are fabricated as a silver grid, while for the rear side a uniform aluminum layer is used. Depending on optimization of parameters that cause losses in solar cell, final solar cell design, as well as metallization technology, may vary.

#### **1.8.1. Screen-printing**

Today, the most common metallization technology is the screen-printing of silver and aluminum pastes [6], which is applicable for almost any type of solar cells, such as crystalline and multicrystalline [36], heterojunction solar cells [37], passivated emitter and rear cell (PERC) [38], passivated emitter rear locally diffused (PERL) solar cells [39], interdigitated back contact (IBC) cells [40] and many others. Now with shallow and selective emitter technologies [14] is possible to achieve efficiencies as high as 21 % [41]. Further improvement of efficiency is limited with contact resistance between fired silver paste and silicon, that is usually higher than 1 m $\Omega \cdot cm^2$  [21,42], while electroplated contacts can reach contact resistance values down to 0.1 m $\Omega \cdot cm^2$  [43], which can cause additional increase in efficiency at least by 0.4 % [44]. Another drawback of the silver screen-printing metallization technology is very high silver cost. Therefore, researchers all over the world are focused on development of metallization technologies based on low cost materials, such as electroplated copper and nickel.

Screen-printed electrical contacts formation occurs in several steps. In the first step two or three bus bars are printed using silver/aluminum paste onto the rear of a cell. The rest area on the rear is then printed with aluminum paste, and the obtained structure is dried using conveyor belt furnace. Finally, the front grid is printed using silver paste, dried and fired.

The printing setup employs a steel-wired mesh having photolithographically defined pattern enclosed in a metal frame. This structure is the screen. The printing occurs due to the process that includes transfer of the wafer, its alignment with the screen and squeezing of the screen filled with metal paste. Typical lines definition is around  $60 \ \mu m$  [45]. The complete procedure requires 2-3 seconds allowing throughput of more than 1000 wafers per hour.

### 1.8.2. Stencil-printing

Stencil printing is known mainly as metallization technology for printed circuit boards. It utilizes the same equipment and pastes as for screen-printed technology. The only difference is the mask used, which represents usually a metal foil. The main advantage of stencil printing is the possibility to print lines with high aspect ratio (height to width), keeping the line resolution as low as  $30 \,\mu\text{m}$ .

#### 1.8.3. Ink- and aerosol-jet printing

Ink-jet and aerosol-jet printing are non-contact localized deposition technologies allowing high line resolution of less than 20  $\mu$ m [46]. Ink-jet printer continuously creates a stream of ink that is jetted under high pressure through the nozzle. Aerosol-jet printer does not apply metal-containing ink directly. Instead, an aerosol is created from the ink, which is transported through a nozzle to the deposition area and focused by a gas stream. These techniques, however, are still necessary to optimize in terms of contact resistance to lowly doped silicon wafers [46].

#### **1.8.4.** Metal evaporation and photolithographical patterning

Metal evaporation together with photolithographic patterning allows formation of contact grid with very fine dimensions, however, due to their costs are competitive only in application to the front side metallization of high-efficiency solar cells [47]. The process includes deposition, exposition and development of photoresist, followed by chemical etching of passivation layer of a solar cell. Then high vacuum evaporation process of a metal or a metal stack occurs. Usually titanium-palladium-silver metallization stack is used. Titanium is used to provide very low contact resistance and good adhesion through formation of the silicide. Palladium is used as diffusion barrier and adhesion promoter between titanium and the last layer, usually silver, is the conductor layer. Lift-off process is used to remove excess of metals, leaving welldefined metallization grid. Finally, thin conductor layer is thickened by a plating step and sintered.

#### 1.8.5. Plating

Plating is a metallization technique that uses the deposition of metal ions out of solution containing appropriate metal salt onto a desired surface. The plating can be of two types: electrochemical deposition and electroless deposition. Electrochemical deposition (electroplating) occurs between electrodes placed inside a chemical solution under a potential bias. At the cathode metal is reduced, at the anode metal is oxidized. For electroless deposition no external potential is required, however, the plated surface has to be autocatalytic to perform corresponding chemical reaction.

Plating for solar cells is not new, for the first time it was employed at Bell laboratories in the 1950s [48], however, due to drawbacks with adhesion of plated metals to silicon and low deposition rate, the screen-printed metallization commercialized the market. The interest to the electroplated metallization revived as soon as screen-printed metallization reached its physical limits.

According to the state-of-the-art, plating is a common technique for nickel- and copper based metallization of solar cells. Today many publications report the application of electroless, electrochemical, or light-induced plating (LIP) techniques, which have been thoroughly reviewed by Lennon et al. [48]. Industrial applicability of the plating processes foresees two main issues. One is the solar cell masking needed to protect the active area of the solar cell, in order to form the front grid metallization. Another issue concerns the cell throughput of plating technique at industrial level, which directly depends on the plating speed. Even though in the semiconductor industry deposition rate of several micrometers per minute is considered rather high, in turn, it does not satisfy industrial requirement of solar cell manufacturing that demands a throughput of more than 1000 cells per hour. The most attractive solution is represented by high speed electroplating procedure using localized plating and dynamic liquid drop/meniscus technique, recently proposed in ref. [49–52] and will be thoroughly discussed in the following chapter.

### **1.9.** Porous silicon in solar cells

The first samples of porous silicon were obtained during the study of electropolishing of silicon wafers in aqueous hydrofluoric acid solutions in 1956 [53]. First time porous silicon was considered as an issue, since it was significantly lowering the quality of the silicon surface after electropolishing. In 1972 Watanabe et al. [54] revived the interest to porous silicon after publication of its application as isolation material for integrated circuits. Ten years later Prasad [55] proposed to use porous silicon as an antireflection coating (ARC) material for solar cells. In 1991 Canham [56] reported visible photoluminescence from porous silicon layers and suggested that porous silicon is the material, where silicon skeleton can be considered as an array of silicon nanowires, where quantum confinement occurs. Canham's work caused in application to integrated circuits, as buffer layer for epitaxy and formation of semiconductor heterostructures, microelectromechanical systems, biological sensors, photoelectric devices and optical filters.

#### **1.9.1.** Fabrication of porous silicon

Porous silicon layers can be obtained with different pore sizes and porosity. Porous silicon is usually classified in three categories: nanoporous silicon has pore diameters less than 2 nm, mesoporous silicon has pores with diameters in the range between 2 nm and 50 nm, and diameters of pores for macroporous silicon are greater than 50 nm.

Porous silicon is usually obtained by electrochemical etching (anodization) of silicon crystals in a hydrofluoric acid containing electrolytes. The substrate doping, its crystallographic orientation, the electrolyte composition and the current density are among process variables that affect porous silicon morphology and, thus, its electrical and mechanical properties. The influence of anodization parameters on properties of porous silicon layers is thoroughly studied in literature [57–60]. For instance, figure 1.16 shows porosity of porous silicon layers as a function of the anodization current density. Porosity is a macroscopic parameter which is defined as the fraction of void spaces within the porous silicon layer. It is determined easily by the weight measurement of silicon before and after the anodization procedure. As can be seen from figure 1.16, for series porous silicon samples obtained on highly doped n-type silicon wafer at 3-100 mA/cm<sup>2</sup> anodization current density, the porosity varies from 30 % up to 85 %. The porosity as a function of the current density exhibits a distinct minimum around  $20 \text{ mA/cm}^2$ . It is interesting to note that the same magnitude of porosity can be observed for two samples obtained at different current densities. Thus, the plot depicted can be divided up on two branches. When going from 20 mA/cm<sup>2</sup> value (that is characteristic of a minimal porosity) to lower current densities, the porosity increases dramatically. The analysis of the cross-sectional SEM image of such porous silicon samples (figure 1.17a) shows that the porous material fabricated at these conditions has a sponge-like structure. At higher current densities (25-100 mA/cm<sup>2</sup>) the porosity increases progressively with increasing the current density. Material obtained at the high current density anodization regime has a columnar pore structure. The cross-sectional SEM image of such kind of porous silicon sample is shown in figure 1.17b.

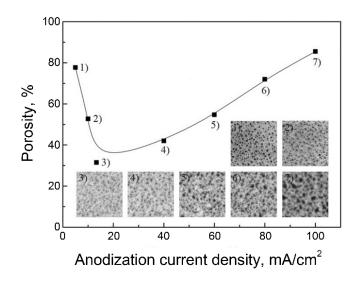


Figure 1.16. Dependence of porosity and morphology of porous silicon layers on anodization current density.

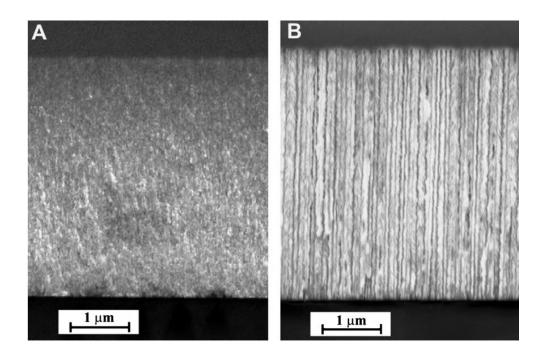


Figure 1.17. Cross-sectional SEM images of porous silicon samples, fabricated at (a)  $10 \text{ mA/cm}^2$  and (b)  $60 \text{ mA/cm}^2$  anodization current densities.

Thus, for the given type of silicon crystal and the used electrolyte 13-25 mA/cm<sup>2</sup> current density interval, relating to the samples with minimal porosity, corresponds to the region where the transition from the sponge-like to columnar porous structure occurs. The distinction in the structure of the porous silicon samples fabricated at different anodization currents is, probably, associated with the competition of two processes: the electrochemical anodization and the chemical silicon dissolution. At the low current density (left branch of the plot in figure 1.16), both processes take place in the same measure. At the higher current density regime, process of the electrochemical anodization of the pore bottom than the chemical dissolution of the pore walls resulting in the formation of the porous columnar structure.

Morphologic parameters of the surface for porous silicon samples obtained in  $5-100 \text{ mA/cm}^2$  anodization current density range (at the lower current density such analysis is not reasonable). SEM images of the porous silicon samples are shown in figure 1.16. The pore concentration was estimated at  $3\cdot10^{10} \text{ cm}^{-2}$ . It is appeared that this value does not depend on the current density. Likewise, in this range of current densities, the interpores distance also remains constant being about 54 nm. At the same time, when the current density increases from 13 to 100 mA/cm<sup>2</sup>, the mean diameter of pores increases from 14 nm up to 25 nm (see figure 1.18). The inset in figure 1.18 shows distribution diagrams of mean pore diameters for the samples with minimal and maximal porosities. Attention is drawn to the fact that the dispersion of the mean pore size increases with increasing the porosity.

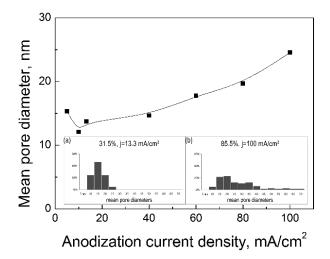


Figure 1.18. Dependence of average pore diameter on anodization current density. The inset displays distribution diagrams of average pore diameters for porous silicon samples: (a) minimal porosity, (b) maximal porosity.

#### **1.9.2.** Porous silicon formation mechanism

There are many research articles published on studies of porous silicon formation mechanism, however, up to now a universal theory that could explain large variety of morphological forms of porous silicon layers is not reported yet. Mainly it is complicated to define all the process parameters of the anodization treatment because of its huge number. Besides, quite often different physical parameters of porous silicon layers are reported even if the same process conditions are used. Among the anodization conditions are: doping type and level, crystallographic orientation of the substrate, electrolyte composition, anodization current density, configuration of the electrochemical cell, surface condition of the substrate caused by the cleaning method used etc.

Models of porous silicon formation can be divided in three groups. Models of the first group resolve small perturbations of surface states that cause initiation of pores. Among the perturbations there are such parameters as acceptors localized at the surface, vacancies on the abrupt endings of crystal lattice, fluorine ions diffusion through the double layer. The second group models are focused on the pore growing. Usually these models evaluate carriers transport through the semiconductor/electrolyte system, while neglect such electrochemical parameters as diffusion limits and adsorption of ions. Model of the third group define both processes, pores initiation and growth.

For complete understanding of the porous silicon formation mechanisms it is necessary to consider the electrochemical processes as well. During the anodic electrochemical etching (anodization) of silicon several side reaction occurs, such as synthesis of bivalent (SiF<sub>2</sub>, SiO) and tetravalent silicon compounds ( $H_2SiF_6$ , SiF<sub>4</sub>, SiO<sub>2</sub>). Porous silicon formation takes place when formation of bivalent compounds dominates, otherwise the electropolishing occurs.

Dissolution of silicon during the anodization can be described using the following equation:

$$Si - SiH_X^S + 6HF = SiH_X^S + SiF_6^{2-} + H_2 + 4H^+ + 2e^-.$$
(1.28)

Hydrogen passivation of silicon in hydrofluoric acid solutions is thermodynamically most favorable state [61]. During the anodization of silicon fluorine atoms replace the hydrogen. Charge carriers redistribution at the surface occurs due to very high electronegativity of fluorine ions. As a result, silicon atom acquires excess of negative charge that helps the surface atom to brake bonds with the crystal lattice. Hydrogen passivates abrupt bonds again and the process repeats.

Synthesis of silicon dioxide may take place during the anodization. However, due to solubility of silicon dioxide in hydrofluoric acid this process also contributes to etching of silicon during the anodization:

$$SiF_6^{2-} + H_2O = SiO_2 + 6HF + 2e^-.$$
(1.29)

Calculation of the equilibrium thermodynamic potentials shows that in case of gradually growing potential of the anodic system the reaction (1.28) will precede the reaction (1.29). Using of model of diffusion limitations on the transfer of reactants through the porous structure, this approach allows to explain many phenomena observed during the formation of porous silicon. Thus, in the galvanostatic anodization regime, as far as process is running the growth rate of porous silicon is proportional to the square root of anodization time [62]. Furthermore, when thickness of the porous silicon layer reaches a certain limit, spontaneous change of anodization mechanism occurs, resulting in an increase of the porosity of the bottom of the porous silicon layer [63]. This is related to the critical ionic diffusion flux density of fluorine ions that corresponds to a certain pore length. The critical ionic diffusion flux density decreases as the pore depth increases. According to the laws of electrochemical kinetics, conditions for the formation of tetravalent silicon compounds, in particular silicon dioxide (1.29), appear in the moment when the predetermined current density in the galvanostatic regime exceeds the critical ionic diffusion flux density. The dielectric layer in the pores bottom causes redistribution of charge carriers and initiates dissolution of the pore walls, which leads to an increase in pore radii and, therefore, porosity. Additionally, porous silicon layer growth rate decreases due to decrease of the effective anodization current density (caused by increase of the effective area where electrochemical reactions occur) and due to increase of the dissolution valence (Faraday's law). At the same time, in the potentiostatic regime, if the applied potential is not sufficient for the reaction (1.29) to form silicon dioxide, silicon dissolution occurs according to the reaction (1.28). In this case, reduction of the etching rate can be caused only by decrease of concentration of hydrofluoric acid at the silicon/electrolyte interface. Thus, no etching of the pore walls should take place and the porosity should be stable through the entire depth of the porous silicon layer.

As it can be seen, in terms of calculation of the amount of dissolved silicon, galvanostatic anodization regime is easier rather than potentiostatic anodization regime. However, potentiostatic anodization regime is preferable to obtain more uniform and homogeneous porous silicon layers.

#### **1.9.3.** Applications of porous silicon to solar cells

Research and application of PS to solar cells lies mainly in the field of antireflection coating (ARC) material and the first development started more than 30 years ago by Prasad et al. [55]. To characterize solar cells having PS as ARC, Vinod [42] studied the application of standard screen printed silver metallization on it. According to his methodology, it was necessary to remove completely the PS layer by molten glass frit contained in the silver paste, to achieve good electrical contact parameters between metal and silicon.

#### **1.10. Summary to the Chapter 1**

The first chapter of the present work discusses solar cells operation. On the level of semiconductor physics that governs a solar cell, physical and technological limitations are analyzed to define possible directions for solar cells improvement. It was shown that the efficiency of a solar cell is a parameter that defines ratio between output power of a solar cell and input power of the incident irradiation. The maximum power of a solar cell depends on current and voltage parameters. Current in a solar cell depends mainly on the generation and collection of light-generated carriers. For an ideal solar cell, for example, the short-circuit current has to be equal to the light-generated current, but in practice, it is limited by resistive loss mechanisms caused, in general, by defects on the surface and in the bulk that affect charge carrier lifetimes. The open-circuit voltage depends on both the dark saturation current of the solar cell and light-generated current. The dark saturation current depends on recombination processes in a solar cell and may vary by orders of magnitude. Thus, the open-circuit voltage is usually considered as a measure of recombination rates in a solar cell.

The reduction of the surface recombination can be achieved through reduction of the minority carrier density at the surface and reduction of defects. Minority carriers can be reduced by doping the surface forming back surface field or field effect passivation. Defects concentration can be decreased through the passivation of abrupt endings of the crystal lattice by an appropriate dielectric layer, such as silicon oxide or silicon nitride in case of silicon.

Metallization technologies cause optical and electrical losses. As for the front side metallization, optical losses are caused by shadowing and reflection of the light on the metal grid, typical front metal grid of a solar cell results in approximately 8 % of optical losses. Contact resistance between fired silver paste and silicon is usually higher than 1 m $\Omega \cdot \text{cm}^2$ , and silver paste bulk resistivity is  $3.2 \cdot 10^{-8} \Omega \cdot \text{m}$ , while electroplated nickel reaches contact resistance values down to 0.1 m $\Omega \cdot \text{cm}^2$  [43], and bulk resistivity of electroplated copper is less than  $2.4 \cdot 10^{-8} \Omega \cdot \text{m}$  [64]. Shift to nickel-copper metallization can cause additional increase in efficiency at least by 0.4 ‰abs obtained due to the front metallization [44].

The rear side of a solar cell is almost completely metallized with aluminum, however, in order to ensure the solderability of rear contacts for module assembly, the rear aluminum layer is not uniform, it contains openings for silver solder pads, that cause inhomogeneous Al-BSF passivation and, as will be shown in this work, reduce the solar cell efficiency by up to 0.5  $%_{abs}$ .

In order to balance and reduce the impact of described limitations, researchers all over the world are working on improvement of the quality of materials used for solar cell fabrication, optimization of solar cell design, and invention of new processes and treatment procedures. In this Ph.D. project, novel techniques for the front and rear electroplated metallization are proposed that can provide efficiency enhancement of up to  $1 \%_{abs}$ .

# Chapter 2. High-speed electroplating and meniscus process

In solar cell technology, plating is considered as possible replacement of expensive screen-printed silver. However, throughput in such a PV production line still must be higher than 3000 cells/hour and use of any kind of photoresist and/or resist process is not considered as a feasible industrial solution. An ideal solution would be to perform selective localized plating, touching the solar cell only where metal is necessary to plate by a mask-free technique. Moreover, to guarantee high throughput, the plating speed must be increased respect to LIP process, in which the maximum current density is in the range of 6 to 30 mA/cm<sup>2</sup>.

Currently, the highest deposition rate of copper is 5  $\mu$ m/min [65,66]. Considering that current solar cell design requires approximately 35  $\mu$ m thick copper fingers and bus bars, it means very long line equipment. Single plating cell equipment must be about 56m long for warranting a throughput of 3000 cell/hour managing more than one thousand liter of copper solution. Industrial scree-printing with even an higher throughput (i.e. 4800 cell/hour) is long 13m. With such huge waste of floor-space the plating technology is facing an hard acceptance from industrial solar cell manufactures. In order to increase throughput and at the same time reduce floor-space, the only solution is to improve the speed of plating. Several attempts in optimization of plating baths were already made [65,66], such as use of higher solubility copper salt (i.e. methane sulfonic) and better performance-enhancing organic additives. In any case, plating bath optimization didn't revolutionize the industry of electrochemical plating.

In electroplating, deposition rate of a metal is governed by the mass transport. It was shown that copper deposition rate can be intensified up to  $3000 \mu$ m/min using jetplating technique [67]. Unfortunately, fine dimensions of nozzles and deposits obtained thereby as well as certain liquid management issues didn't allow this technique to be commercialized. In this work, the jet-plating is used in the new high speed plating technique based on dynamic liquid drop (DLD) and dynamic liquid meniscus (DLM) [49–52,68,69] that allows to both perform localized electroplating and significantly increase the mass transfer, through the speed of flow of an electrolyte, and, thus, electroplating rates.

# 2.1. High-speed plating

In electroplating, the deposition rate is defined by current density through the Faraday's law of electrolysis:

$$\frac{d_i}{t} = \frac{M_i}{e z_i N_A \rho_i} j, \tag{2.01}$$

where  $d_i$  is the thickness of a metal, t is the plating time,  $M_i$  is the molecular weight of a metal,  $z_i$  is the valence of a metal, e is the elementary charge,  $N_A$  is the Avogadro constant,  $\rho_i$  is the density of a metal, and j is the applied current density.

As it seen from the formula 2.01, higher deposition rates are achievable only through increase of the current density. However, the current density is limited by the mass transport in the diffusion layer near the interface between the cathode and the bulk solution and, thus, cannot be increased indefinitely, due to depletion of concentration of metallic ions near the cathode area. Diffusion issues result in increased hydrogen reduction that usually leads to burnt and irregular deposits.

The maximum deposition rate is obtained when the whole cathode current is utilized for reduction of metallic ions ( $Cu^{2+}$  ion, for instance). In practice, deposition rate is limited by side reactions (the reduction of hydrogen, for instance) which participating in the cathode current negatively influences the plating efficiency. It was determined experimentally that the plating efficiency is a function of the current density and the mass transport in the electrolyte (i.e. diffusive ionic species flux density) in the current range where hydrogen evolution occurs at a high rate. The study [70] showed that the plating efficiency increases with increasing of the mass transfer in the electrolyte. The mass transfer may be increased by introduction of the agitation, for instance. It may be deduced that hydrogen evolution tends to participate less in the cathode current with increase of the agitation intensity making the transport issues through the diffusion layer negligible. This work proves that significantly intensified mass transport during the plating process increases the limiting current density, thus, allowing to achieve higher plating rates.

The mass transport is theoretically described by the Nernst-Planck equation. The equation describes the flux of ionic species under the influence of an ionic concentration gradient, a velocity of the fluid and an electric field [71,72]:

$$\vec{j}_i = -D_i \nabla c_i + \vec{u}_i c_i - \frac{D_i z_i e}{k_B T} c_i \nabla \varphi, \qquad (2.02)$$

where  $\vec{j}_i$  is the diffusive species flux density,  $D_i$  is the diffusivity of species in the solvent,  $c_i$  is the concentration of species,  $\vec{u}_i$  is the molar average velocity,  $z_i$  is the valence of ionic species,  $\nabla \varphi$  is an electric field. The molar average velocity is given by the vector sum of the velocity of the fluid  $\vec{u}$  and the electrophoretic velocity of species with respect to the fluid:

$$\vec{u}_i = \vec{u} - \mu_{EP,i} \nabla \varphi, \qquad (2.03)$$

where  $\vec{u}$  is the velocity of the fluid,  $\mu_{EP,i}$  is the electrophoretic mobility of species.

Figure 2.01 shows the calculated diffusive flux density for the jet-plating configuration as a function of the electric field between cathode and anode, the velocity of the movement of the electrolyte through nozzles and the concentration of copper ions [68]. It is seen that at low fluid speeds (0 and 0.01 m/s) the dependence has clear relation to the electric field and the concentration of copper ions. With increase of the electrolyte flow speed, the influence of the electric field on the mass transport (on the electrophoretic mobility of ions) reduces. Then, at high flow speeds of the electrolyte, mainly the velocity of the fluid defines the diffusive flux density. It is clearly seen that the mass transport of copper ions increases proportionally to the electrolyte flow speed. Thus, it also has to affect the limiting current density.

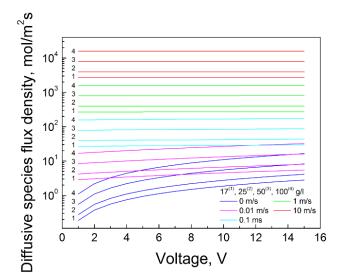


Figure 2.01. Calculated diffusive flux density as a function of the electric field, the solution flow speed, and the concentration of copper ions during the plating in DLD/DLM configuration.

The effect of the fluid speed on the quality of the deposit goes in agreement with experimental data obtained in this work. Figure 2.02 shows images of copper deposits obtained for different flow speeds and electrolytes with different concentration of copper ions. As it seen from figure 2.02, for a 30 g/l copper concentration and 0.13 m/s flow speed the deposit comes burned already at 2.5 A/cm<sup>2</sup> current density. An increase of the flow speed up to 0.77 m/s shifts the limiting current density to 2.9 A/cm<sup>2</sup>, which corresponds to 1.07  $\mu$ m (64.2  $\mu$ m/min) deposition rate. Further increase of copper concentration to 38 g/l keeping the flow speed the same shifts the limiting current

density to 3.5 A/cm<sup>2</sup>, which corresponds to 1.3  $\mu$ m/s (78  $\mu$ m/min) deposition rate. Finally, 45 g/l copper concentration results in 4.4 A/cm<sup>2</sup> limiting current density and 1.61  $\mu$ m/s (96.6  $\mu$ m/min) deposition rate.

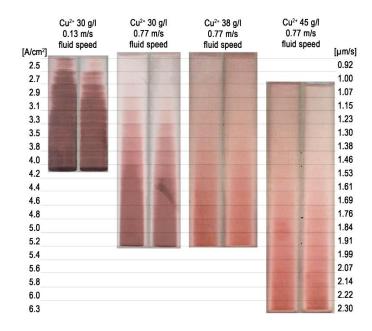


Figure 2.02. Images of copper deposits showing the limiting current density as a function of electrolyte flow speed and copper concentration.

The obtained values are much higher than normally obtained for industrial use. The record of copper deposition rate is 50  $\mu$ m/s that was obtained using jet-plating technique at 150 A/cm<sup>2</sup> current density [67]. Due to a high velocity of liquid electrolyte (i.e. 10 m/s) the main issues for such equipment were mask resist erosion and how to limit and contain the splashes of the liquid. Sub 0.10  $\mu$ m copper interconnects already use a jet-plating technique but both wafer and anode jet assemblies are immersed in electrolyte bath to remove splashes [73]. Nowadays, jet plating in air is mainly used in reel-to-reel plating equipment for printed circuit board (PCB) industry with a maximum deposition rate of 16  $\mu$ m/min.

# 2.2. Localized wet treatment technique: dynamic liquid drop/meniscus

Localized electrochemical deposition (LECD) was already introduced [74] where a conducting micro-electrode is used to fabricate high aspect ratio metal structures. LECD is performed by placing an electrode tip, which has micrometer dimensions, near a substrate in an electrolyte and bias a potential difference between them. Due to the highly localized electric field in the region between the electrode tip and the substrate, confined deposition is produced. In any case, there is a severe spread at columns bases, which limits the resolution of the LECD technique [75]. A liquid static meniscus obtained by a micropipette in close proximity to the substrate solves the problem of spread of the LECD technique, and wire dimensions down to 100 nm were obtained [76]. A static liquid drop is formed at the end of the micropipette, and, as the liquid drop gets in contact with the substrate surface, a static liquid meniscus is formed spreading on the surface depending on the wetting angle. As dimensions get bigger, gravity influences and, the micropipette, with all the liquid inside, must be fully closed; or as the liquid touches the substrate surface, the liquid spreads out until a new equilibrium is reached between surface tension and gravity. Static meniscus imposes tight control on the distance between micropipette and substrate due to finite quantity of liquid in the meniscus. Increasing such distance breaks the formed meniscus. Furthermore, with a static meniscus is impossible to have agitation of the solution and this will limit seriously the deposition speed and decrease the morphology characteristics of the deposit.

In this work, dynamic liquid drop/meniscus (DLD/DLM) technique is used. Figure 2.03 presents 2D view of DLD. The system, to implement such a technique, is composed of an internal jetting channel (input channel) where movement of the liquid is forced by a liquid pump, and an external recalling channel (output channel) where liquid under a depression (e.g. obtained by a vacuum pump) is recalled back into the tank. The input channel, that can be of any shape (e.g. circular, rectangular, etc.), confined by rigid wall (i.e. solid material), pumps a constant liquid flow with a velocity that depends on the pressure and dimensions of the input nozzle. Due to a lower pressure in the surrounding of the output channel, an airflow (gas) sustains liquid (figure 2.03: white arrows in the blue gas) forming a drop (i.e. DLD). Confined drop is dynamic because of continuous refreshment of the liquid inside it. A schematic view of 3D DLD for a rectangular input channel is also sowed at figure 2.03.

As a substrate gets in contact with DLD, DLM is formed as shown in figure 2.04. The contact angle depends on the wettability of the surface. Once DLM is formed and its parameters (i.e. fluid velocity and pressure) are kept constant, lateral movement of the nozzle or the substrate is not causing changes in the shape of DLM. In figure 2.04 a situation when rectangular DLD touches a substrate is shown. In the same figure, output channels and gas inlet are shown.

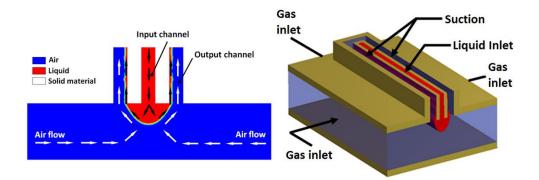


Figure 2.03. 2D and 3D schemes of the dynamic liquid drop (DLD).

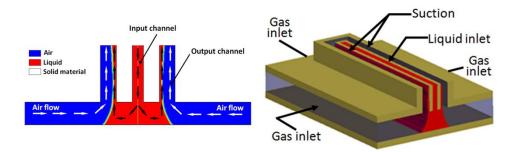


Figure 2.04. 2D and 3D schemes of the dynamic liquid meniscus (DLM).

In order to avoid liquid losses, DLD formation is obtained by, first, applying a pressure drop to the output channel and, second, switching on the pumping of the liquid in the input channel. As DLD is formed, the substrate can be brought in contact by movement of the nozzle or the substrate or by combination of them. In this way, it is possible to perform two ways of processing:

1) Continuous process in which the nozzle is fixed and the substrate moves continuously.

2) Stop and go process, in which the substrate or the nozzle move up/down in the z-direction, which is orthogonal to the plane of the substrate, to get in contact and form DLM, stop and, as an example, start the plating process. As finished, the substrate moves away in the lateral plane with speed up to tens of m/s to get positioned at a new processing site.

Figure 2.05 illustrates geometrical parameters of input and output channels and obtained DLD. Among main parameters are width of output channel O, width of separating walls W, width of input channel I, distance between channels and substrate H, and height of DLD  $H_d$ . Using this geometrical parameters, properties of the liquid flow can be calculated. Table 2.1 contains configuration geometries of nozzles and parameters of liquids flowing through them (where  $\Delta P$  is depression, Q is the flow of a

liquid, and *V* is the velocity of the fluid). It is seen that theoretically is possible to obtain very intensive flow rates with up to 10 m/s speed of liquid. Practically, several obstacles appear. A simplified calculation model is not taking into account the volume of the entire pipelines of the system that actually provides the movement of a liquid. Thus, the calculated depression is a real value only for a certain type of nozzles. Secondly, the momentum conservation between liquid and gas flows has to be respected always in order to form stable DLD. Considering the mass ratio between a liquid (e.g. the water) and a gas (usually the air) is approximately 3 orders of magnitude, it has to be respectively compensated by velocities of flows, which may not be possible to achieve practically due to very high resulting velocity of the gas flow.

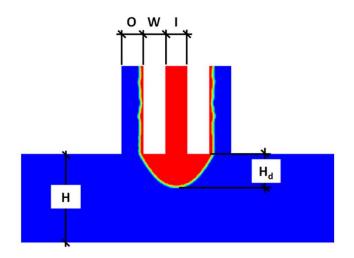


Figure 2.05. 2D scheme of the DLD, where O is the width of the output channel, W is the width of walls, I is the width of the input channel, H is the distance of a substrate,  $H_d$  is the height of the DLD.

Table 2.1. Geometry of the nozzle of the plating head and calculated parameters of the liquid flowing through it.

Nozzle Dimensions										
O, μm	W, μm	I, µm	Η <sub>d</sub> , μm							
400	300	400	500							
Calcula	Calculated parameters of a liquid flow									
ΔP, kPa	Q, l/mir	1	V, m/s							
1.150	0.072		0.25							
5.250	0.72		2.50							
10.0	1.44		5.0							
20.0	2.88		10.0							

Figure 2.06 shows a possible design of a device that may be used for implementation of DLD/DLM technique. This device contains input and output channels confined by rigid walls and separated from each other. Such kind of a device can be easily manufactured using stereolithography (3D printing technology).

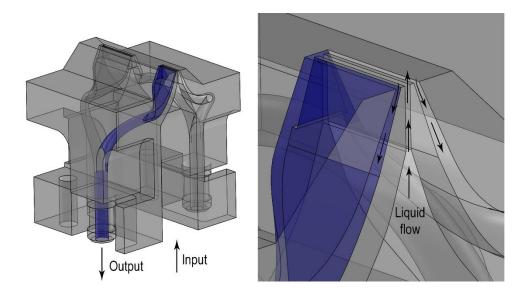


Figure 2.06. Design of the plating head used in this work.

In order to perform plating, the device has to be connected to the system that provides movement of liquid and gas flows. Inlet channel is connected directly to a tank that contains an electrolyte. In order to start a flow the additional pressure  $\Delta P_I$  has to be applied. In order to confine a DLD a gas has to start flow immediately. That is reached applying a depression in the outlet channel, allowing continuous gas flow that confines a DLD and recalls the electrolyte. Table 2.2 summarizes working parameters obtained experimentally. It is seen that 1.56 m/s liquid flow is possible to reach using the DLD/DLM configuration.

Table 2.2. Parameters of the liquid flow obtained experimentally.

Inlet ΔP <sub>I</sub> , kPa	Suction ΔP <sub>S</sub> , kPa	Q, l/min	V, m/s
30	-50	0.20	0.69
40	-50	0.30	1.06
60	-50	0.35	1.22
80	-50	0.40	1.39
100	-50	0.45	1.56

# 2.3. Summary to the Chapter 2

The mechanism of high speed plating is discussed in terms of hydrodynamics of the electrolyte. It is shown that significantly intensified mass transport during the plating process increases the limiting current density, thus, allows to achieve higher plating rates. Calculations of diffusive flux density as a function of the electric field, the solution flow speed, and the concentration of copper ions during the plating in DLD/DLM configuration according to Nernst-Plank equation are provided. It is shown that the mass transfer of copper ions can be increased three orders of magnitude intensifying the solution flow speed. In this work, the limiting current density of 4.4 A/cm<sup>2</sup> resulting in 1.61  $\mu$ m/s (96.6  $\mu$ /min) deposition rate is achieved. Thus, a plating procedure using the DLD/DLM technique that allows to implement high speed plating of metals is developed.

# Chapter 3. Methods and measurements

### **3.1.** Materials

Reagent grade quality is adopted throughout the experiments in this work. Solar cells coming from industrial production lines are used. Plating electrolytes, such as nickel sulfamate-, copper sulfate- and tin metanesulfomate-based, are supplied from Enthone.

## **3.2. Electrochemical methods**

#### 3.2.1. Two-electrode electrochemical cell

An electrochemical cell is a device capable to facilitate chemical reactions through the introduction of electrical energy, as well as to generate electrical energy from chemical reactions. In this work, the two-electrode configuration is used to perform such electrochemical processes as anodic etching (anodization) and deposition. In order to control these processes AMEL 2055-2056 potentiostat-galvanostat controlled by AMEL 568 function generator and a PC equipped with Advantech PCI-1731 DAC card.

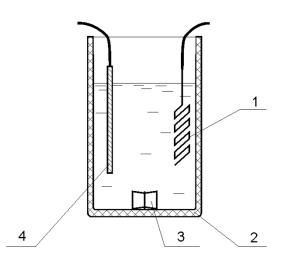


Figure 3.01. The construction of the two-electrode electrochemical cell suitable for electrochemical etching or deposition processes:1) counter electrode, 2) glass beaker, 3) magnetic mixer,4) working electrode.

#### 3.2.2. Meniscus process for localized electroplating

Commonly localized plating is obtained by photolithography process. This is not a simple process and is considered expensive in solar cell application. In this work, the approach to plating process is completely different, indeed it may not involve any photolithographic step since based on innovative DLD/DLM technique, described in the Chapter 2 of this work, which is able to produce any kind of wet process in specific defined positions. Rapidity and easy to automate are the main advantages of this technique. A dynamic liquid drop (DLD) is formed from a liquid jetted from a nozzle and confined by a pumping system able to recall the liquid avoiding any leakage. When a substrate comes in contact with DLD, the liquid is confined by both the pumping system and the substrate thus forming a dynamic liquid meniscus (DLM). Schematic designs of DLD and DLM in contact with a substrate are reported in figures 3.02a and 3.02b.

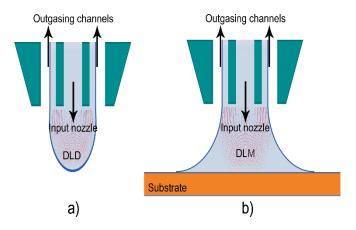


Figure 3.02. The dynamic liquid drop (DLD) (a) and the dynamic liquid meniscus (DLM) (b).

In order to perform a localized plating process with desired configuration, specific device, so-called "plating head", is carefully designed and is shown in figure 3.03. This plating head implements a monolithic structure that embodies input and output nozzles and vacuum channels together with the chamber for the anode. This structure requires external liquid and vacuum pumps, in order to provide at the same time movement of liquid (e.g. an electrolyte), a sample substrate for DLM confinement, and external power supply, in order to perform electroplating. The plating occurs in two-electrode configuration: the anode is placed inside the anode chamber of the plating head, and the cathode is the substrate. Electrodeposition occurs as soon as DLM is confined and the potential bias is applied between anode and cathode.

dimensions of DLM depend on nozzle configuration, substrate position, surface wettability, pressure drop between input and output nozzles as detailed in ref. [51,69].

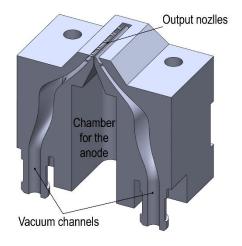


Figure 3.03. Design of the plating head to perform DLD/DLM treatment.

In this work, Rapid Prototyping Stereo-lithography is used to fabricate plating heads. In particular, three plating heads are used to simultaneously perform three dashed bus bars, each one having 6 equal contact pads of  $4 \times 13$  mm dimension as shown in figure 3.04. In this work, for a partial automation, a belt conveyor system is used to position each wafer under the plating head [77].

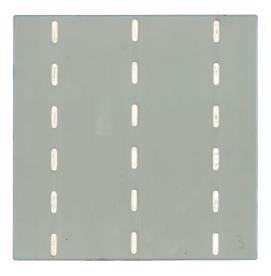


Figure 3.04. The layout of the rear side metallization of the solar cell achieved in this work.

# **3.3.** Measurements and characterization

#### **3.3.1. Scanning electron microscopy**

Carl Zeiss Auriga Cross Beam (FIB-SEM) Workstation is used to investigate surface morphology and composition of samples after anodization and metal plating processes by means of scanning electron microscopy (SEM) and energy dispersive Xray microanalysis (EDX). Samples with PS layers are cleaved along their crystallographic structural planes. Plated samples are cut by focused ion beam (FIB) technique.

#### **3.3.2.** Doping profiling

Doping profile measurements are carried out using striping Hall profile measurement by means of BioRad system. This technique measures the sheet conductivity and the Hall coefficient by van der Pauw method. A depth profile is obtained by gradually removing layers of the material by anodization and etching procedures. The carrier concentration and the Hall mobility as a function of depth can be obtained [78].

#### **3.3.3.** Adhesion measurements

A 180° peel test configuration was used by Lloyd Instruments LRX Plus to evaluate adhesion properties of 2-mm wide ribbons bonded onto solder pads and bus bars. The peeling rate was kept constant at 100 mm/min. In order to determine the mean peel force, peeling profiles were integrated and divided by the length of the solder pad or bus bar.

#### 3.3.4. Dark *I-V* and light *I-V* measurements

Photovoltaic parameters of solar cells were carried out under standard testing conditions 25 °C, 100 mW/cm<sup>2</sup>, AM1.5 G (IEC 60904-3 ED.2) class A sun simulator.

#### 3.3.5. Transmission line method

Electrical characterization of emitter/metal contacts is performed using transmission lime method (TLM) measurements. This method is one of the most valid electrical measurement of contact resistance between metal and semiconductors [79] and is based on the concept of transfer length can be applied mainly for planar devices when the current flows laterally into the contact, such as it happens in thin diffused layers of solar cells. The transfer length  $L_T$  is defined as the distance under the conductor

area where the potential is reducing by 1/e. This results in the current crowding that is described in figure 3.05: when current passes through a conductive layer (e.g. emitter or a TCO) and reaches a metallic contact, it does not flow through the entire area of the contact. Instead the current is collected in the effective area under the contact and this area depends on the contact resistivity ( $\rho_c$ ). If the contact resistivity is very small, the current travels mostly along the edges of the contact. On the other hand if it is high, the current path below the contact expands. A typical measurement scheme supposes fabrication of array of rectangular metal contacts shown in figure 3.06.

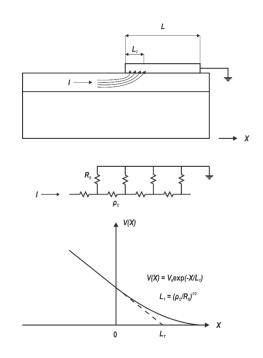


Figure 3.05. Contact current crowding at the edge of the contact. The contact resistivity and sheet resistance are of a distributed nature, resulting in the nearly exponential voltage decay under the contact.

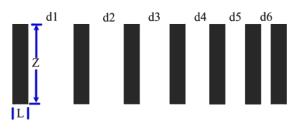


Figure 3.06. A typical contact layout for TLM measurement.

Thus, from the transfer length, the contact resistance can be deduced for a metal/semiconductor contact of a width L, and length Z as:

$$R_C = \frac{\rho_C}{ZL_T} \coth\left(\frac{L}{L_T}\right). \tag{3.01}$$

As it is seen from the figure 3.06, usually there are 7 contacts, each placed away from another with a certain distance  $d_i$ . The complete resistance of such a two adjacent contacts can be defined:

$$R_{Ti} = \frac{R_S d_i}{Z} + 2R_c = \frac{R_S d_i}{Z} + 2\frac{\rho_C}{ZL_T} \operatorname{coth}\left(\frac{L}{L_T}\right).$$
(3.02)

The complete resistance for each two adjacent contacts can be reported as a function of the distance between them, and liner approximation of all the measurements allows to determine several parameters:

1. the sheet resistance of the semiconductor layer is the slope of the linear fit of the measurements multiplied by the length of the contact:

$$R_S = \text{Slope} \cdot \text{Z}; \tag{3.03}$$

- 2. the transfer length is related as  $-2L_T$  to the intercept of the linear fit of the measurements with *d* axis;
- 3. the contact resistivity is given by:

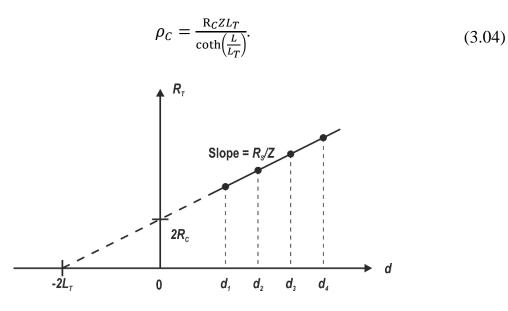


Figure 3.07. Graph of the TLM measurements as a function of a distance between adjacent contacts.

# 3.4. Summary to the Chapter 3

In this chapter, experimental setups used for sample preparation in this work, such electrochemical etching and deposition using standard two-electrode configuration and DLD/DLM technique, are described, more detailed information regarding conditions of samples treatment are discussed in corresponding chapters.

Measurement setups that are used throughout the present work for characterization of samples, such as SEM microscopy and EDX microanalysis, electrical measurements using Hall stripping and TLM methods, *I-V* and mechanical measurements are also discussed.

# Chapter 4. Study and characterization of the aluminum-silicon interdiffusion, application to solar cells

The most common technology for p-type based crystalline silicon solar cell manufacturing involves a front phosphorus diffused emitter, passivated by a silicon nitride layer and contacted by a screen-printed silver grid, while the rear contact is a screen-printed aluminum layer. Common screen printable aluminum pastes are able to form deep and effective industrial Al-BSF, providing also surface recombination velocity values in the range of a few hundred cm/s and performing a backside segregation gettering of undesired metal content within the silicon network.

It is widely known that during co-firing process needed to form both front and rear contacts of solar cells, aluminum and silicon interdiffuse into each other. Details of this process are still under investigations to improve Al-BSF, contact resistance, as well as screen printed aluminum paste bulk conductivity to enhance solar cell performance. On the other hand, there is a growing industrial interest on passivated emitter and rear cell (PERC) solar cells [80], because of their higher efficiency potential. In this technology the rear of the cell is passivated by an insulating layer, such as  $Al_2O_3$ ,  $SiN_x$ , SiO<sub>2</sub> or stacks of them [81–83]. The passivation layer is treated by laser to create microopenings with different configuration, in order to provide electrical contact [84,85]. Then, the same metallization layout as for conventional cells is commonly adopted, with an extended screen-printing of aluminum layer having some silver zones to allow cell interconnections into a module. Even if in this way the screen-printing is kept as simple as possible, there are some new requirements for the aluminum paste, such as ability form a good ohmic contact, to have higher conductivity for better transport carriers from contact points to silver solder pads, to have good adhesion on insulating material and to ensure no bowing for the finished cells. Several studies have been carried out on such kind of cells and pastes, especially concerning the filling of insulating layer openings and silicon diffusion into aluminum suitable to avoid formation of undesired voids [86,87]. This last point still requires a deep investigation about the mechanism of aluminum-silicon interdiffusion, and in particular its dependence on the primary paste composition elements: aluminum particle size and frit presence and composition. Basically the thermodynamic behavior that occurs at the aluminum/silicon interface at equilibrium is described by the aluminum-silicon phase diagram as reviewed in [88]. Due to fast temperature ramp-up and cooling in industrial solar cell firing process, explanation of microstructural behavior between screen-printed aluminum paste and silicon based only on the phase diagram, which is only applicable to conditions close to thermodynamic equilibrium, is not easy. Indeed, after the firing process, the aluminumsilicon lamellar microstructures, having a volume fraction of the minor phase always higher than 0.25, are commonly found at aluminum/silicon interface [89].

In this work, a detailed investigation of the aluminum-silicon interdiffusion that occurs during the firing process, based on high resolution Scanning Electron Microscopy (SEM) and compositional microanalysis with Energy Dispersive X-Ray microanalysis (EDX), is conducted. Relations for aluminum-silicon content, in particular the dependence of Al-BSF configuration on the aluminum paste, are investigated and explained.

# 4.1. Preparation of samples

Six different aluminum screen-printable pastes are tested, differing one from each other in the particle size distribution and composition. The six pastes were produced as experimental lots by R&D labs of Chimet S.p.A. thick film division, according to the following labels reported in Table 4.1:

Description	Min. diameter, µm	d(0.1) µm	d(0.5), μm	d(0.9) μm	Glass frit	Sample reference
Al-3027 small particle size	0.955	1.537	2.733	4.746	No	S27
Al-3028 large particle size	2.512	3.928	5.849	8.703	No	S28
Al-3029 small particle size	0.955	1.537	2.733	4.746	2 % Pb free	S29
Al-3030 large particle size	2.512	3.928	5.849	8.703	2 % Pb free	S30
Al-3041 80% of S29 and 20% of S30						S41
Al-3042 20% of S29 and 80% of S30						S42

Table 4.1. Aluminum paste distribution: d(0.X)=Y represents the X·100 % probability that aluminum particles diameter is smaller than Y.

Small and large particle size powders were supplied from one dealer; therefore they were produced with the same process and same surface characteristics.

Each aluminum paste is tested by measuring: a) contact resistance with a silicon wafer, evaluated TLM method; b) conductivity, evaluated with 4 points probe sheet resistance measurement. Then, solar cells are fabricated using each type of aluminum paste as rear metallization contact. For contact resistivity measurements samples are produced by screen-printing patterns for TLM measurements of each paste on 5  $\Omega$ ·cm p-type doped Cz silicon wafers. All pastes are printed, dried and fired according the following process parameters: (i) screen printing: squeegee hardness 70-75 shore, force 7 Kg, speed 100 mm/s, snap off: 0.5 mm. (ii) Screen: 250 mesh stencil screen, wires

 $36 \mu m.$  (iii) Dry: 4 zones IR belt Aurel furnace 250-250-250°C, total duration time 2 min. (iv) Firing: 3 zones IR belt RTC furnace, settled temperatures 580-640-910 °C speed 50 ipm. To estimate the fired paste conductivity a 4 cm × 2 cm area is fully printed on a similar substrate using the same parameters as just described. These fired paste layers are measured by 4 points probe, mapping the whole 4 cm × 2 cm area on 6 different points and extracting an average value. The bulk conductivities are calculated by considering the paste layer thicknesses.

Solar cells are fabricated on a 1  $\Omega$ ·cm silicon p-type doped 200 µm thick Cz alkaline textured wafers. The front side emitter is diffused up to 70  $\Omega$ /sq sheet resistance. The rear side contact is obtained by screen-printing a full aluminum layer, while the front side is ensured by screen-printing of silver grid. A co-firing process is performed in a 3-zone IR belt RTC furnace with settled temperatures of 580-640-950 °C and belt speed of 80 ipm. Solar cell samples are cut from a larger wafer to obtain edge isolation. The solar cells are measured by means of *V*<sub>oC</sub> and *FF* under AM1.5G class A sunlight simulator conditions. Internal Quantum Efficiency (IQE) measurements is performed in the spectral range between 900 nm and 1200 nm to evaluate Al-BSF depth. To evaluate active doping concentration of Al-BSF region, aluminum is removed and Hall profile measurements are carried out.

Aluminum/silicon interfaces are investigated in detail by means of FIB-SEM imaging and EDX microanalysis mapping.

# 4.2. Experimental data

Aluminum-silicon content is measured by EDX at different magnifications and using two different acceleration voltage settings to modify electron penetration range (i.e. about 1.0  $\mu$ m @ 10 kV and 0.3  $\mu$ m @ 5 kV) and, therefore, the pear-shape of the volume (1  $\sigma$ ) is analyzed. SEM images of screen-printed aluminum pastes after the firing process at three different magnifications are shown in figure 4.01a, 4.01b, 4.01c for samples S27, S28, S29 respectively. The yellow square indicates the area of the average chemical composition measurement. Table 4.2 contains the list of amounts of aluminum, silicon and oxygen for each of the six samples as deduced from quantitative microanalysis performed at different magnifications and energies.

SEM micrographs and EDX maps showing silicon content of samples S42 and S41 are shown in figure 4.02a and 4.02b respectively. FIB-SEM cross-section of compositional mapping and quantitative analysis of sample S28 are shown in figure 3.

Magnification	Contont	S2	7	S2	8	S29		S29 S30		<b>S41</b>		S42	
and energy	Content	at.%	1σ	at.%	1σ	at.%	1σ	at.%	1σ	at.%	1σ	at.%	1σ
	Al	76.2	3.1	68.6	3.0	68.7	3.3	53.9	2.5	68.7	2.5	71.0	3.1
10000, 10kV	Si	10.9	0.4	17.7	0.8	15.7	0.7	29.3	1.3	12.7	0.5	11.8	0.5
	0	8.0	0.6	8.5	0.7	10.0	0.8	10.8	0.9	13.9	0.8	11.8	0.9
	Al	74.9	3.1	62.8	2.7	68.2	3.3	60.9	2.8	68.9	2.6	69.2	3.2
2500, 10kV	Si	11.7	0.5	23.5	1.0	15.3	0.7	22.2	1.0	10.7	0.4	13.2	0.6
	0	8.0	0.6	8.6	0.7	10.3	0.8	10.9	0.9	14.9	0.9	11.6	0.9
	Al	62.6	2.6	49.1	2.1	59.0	2.6	51.3	2.2	63.6	2.6	60.6	2.5
1000, 5kV	Si	21.5	1.0	31.7	1.4	19.9	0.9	24.6	1.1	11.4	0.5	16.8	0.7
	0	14.1	1.0	17.1	1.2	17.4	1.2	19.4	1.3	22.4	1.4	20.0	1.3

Table 4.2. Microanalysis composition of the different samples.

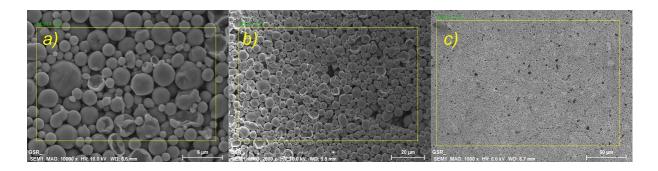


Figure 4.01. SEM micrographs of screen-printed aluminum pastes: (a) sample S27, (b) sample S28, (c) sample S29.

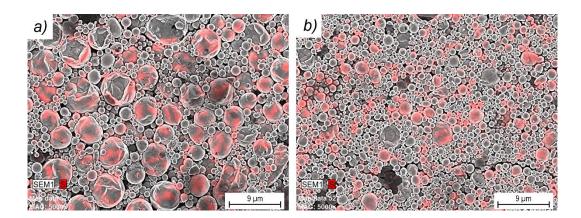


Figure 4.02. SEM micrographs and EDX maps showing silicon content for (a) sample S42 and (b) sample S41.

Electrical parameters of the different samples are given in Table 4.3, such as contact resistance ( $\rho_C$ ) of the aluminum/silicon contact, aluminum paste bulk resistivity

( $\rho$ ) after firing, open circuit voltage ( $V_{OC}$ ), normalized fill factor (*FF*) with respect to sample S28 and Al-BSF thickness.

Sample	$ ho_c, \mathbf{m} \mathbf{\Omega} \cdot \mathbf{cm}^2$	<i>ρ</i> , Ω∙cm	Voc, mV	FF, % normalized to S28	Al-BSF, µm
S27	47.3	32.3	614	0.938	6.1
S28	57.8	26.2	620	1.000	5.1
S29	53.8	28.4	625	0.949	5.9
<b>S</b> 30	58.7	23.8	628	0.912	4.9
S41	n.m.	49.3	622	0.946	5.0
S42	n.m.	27.7	613	0.914	5.3

Table 4.3. Electrical properties of samples (n.m. – not measured).

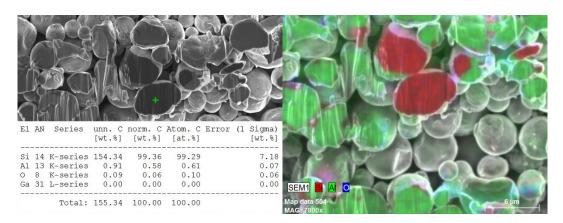


Figure 4.03. FIB-SEM micrographs and EDX microanalysis maps of sample S28 for silicon, aluminum and oxygen content. Quantitative analysis is performed for the location marked with the green cross.

# 4.3. Discussion

It was found that the relevant mechanism of silicon dispersion within aluminum is strongly correlated to aluminum particle dimensions. This behavior, opposite to what asserted in ref. [90], occurs because interfaces become extremely important in the early stages of phase transformation where the two phases (i.e. aluminum and silicon) are influenced by the pressure difference modifying the solubility (interdiffusion coefficient) that depends on the curvature radius of the interface between the two phases. This effect can be explained as a soap bubble exerts an extra pressure on its contents [91] and as given by the well-known Laplace-Young equation that is proven to be valid in the phenomenological description of internal pressure and surface tension of nanoparticles with dimension down to 2 nm [92]:

$$\Delta \mathbf{P} = \frac{2\gamma}{r},\tag{4.01}$$

where  $\gamma$  and *r* are the surface tension and radius of aluminum spherical particle.

Also it was found that aluminum-silicon interaction strongly depends on the presence of the glass frit inside aluminum screen-printing paste. The glass frit influences aluminum-silicon interaction modifying the surface tension of the molten aluminum. Materials, such as bismuth, calcium and magnesium, at low concentration (i.e. Bi ~ 0.3 at.%, Ca ~ 1.5 at.%, Mg ~ 3.5 at.%) are able to almost half the surface tension of molten aluminum [93–95]. Furthermore, these elements, even at a low concentration, weaken or thin the surface oxide film surrounding aluminum particles. In particular bismuth is able to disrupt the aluminum oxide [96], while silicon does not reduce surface tension but improves the fluidity [97].

In this experiment, investigation of the aluminum-silicon interdiffusion begins considering the case of glass frit absence in the aluminum paste, as for the samples S27-S28. During the thermal heating process, the interdiffusion of silicon into aluminum starts at approximately 300 °C and increases reaching its maximum (i.e. 1.5 at.%) at the eutectic temperature (577 °C). Considering that particle dimensions of the aluminum paste have a radius (*r*) greater than 100 nm (i.e.: S27 r  $\geq$  477 nm, S28 r  $\geq$  1250 nm), the melting temperature of such microspheres can be considered equivalent to that of bulk aluminum and not reduced as happens for smaller metallic particles [98]. It must be also recalled that silicon diffusion in aluminum is faster than aluminum diffusion in silicon, therefore aluminum-silicon solid particles appear before the eutectic temperature is reached.

Storaska and Howe [99] observed that aluminum-silicon particles contain a single crystal  $\alpha$ -Al matrix with multiple silicon precipitates embedded within. Since the aluminum-silicon particle is rich of aluminum and aluminum has a greater affinity to oxygen rather than to silicon, the amorphous oxide, covering the aluminum-silicon particle, contains mainly aluminum and oxygen elements. Analyzing diffraction patterns, Storaska and Howe, found prominent  $\alpha$ -Al matrix reflections in solid aluminum-silicon particles, as well as weaker silicon precipitate reflections and some aluminum silicate (Al-Si-O) reflections. Weak aluminum silicate diffraction spots indicate the presence of small nanocrystallites of aluminum silicate in, or adjacent to, the oxide shell. Silicon precipitates are observed to migrate at the oxide-matrix interface.

Solid aluminum-silicon particles start to melt as soon as the eutectic temperature is exceeded. Observation using transmission electron microscopy (TEM) showed that melting process starts near the interface with silicon precipitate, creating a liquid sheath which thickens as temperature increases [100]. The sheath continues to thicken as the

temperature rises and the remaining small, solid core rapidly melts. Similar behavior was observed also for pure aluminum particles [101].

At liquid state the aluminum-silicon particles develop two internal pressure contributions. The first is due to volume expansion of aluminum-silicon spherical particle, where the volume of a spherical particle with the radius r changes at a rate of:

$$\frac{dv}{dr} = 4\pi r^2 = 3\frac{v}{r}.$$
(4.02)

Rearranging (4.02), it shows that the radial strain is one-third of the fractional volume change:

$$\frac{dr}{r} = \frac{1}{3} \frac{\mathrm{dV}}{\mathrm{V}}.\tag{4.03}$$

Since silicon is present as a second phase in the particles, the fractional volumechange associated with melting of an aluminm-silicon alloy can be estimated by:

$$\frac{\Delta V_{melt}}{V_0} = \frac{\left(X_{Si}V_{Si}^l + X_{Al}V_{Al}^l\right) - \left(X_{Si}V_{Si}^S + X_{Al}V_{Al}^S\right)}{\left(X_{Si}V_{Si}^S + X_{Al}V_{Al}^S\right)},\tag{4.04}$$

where  $X_{Si}$ ,  $V_{Si}^{l}$ ,  $V_{Si}^{S}$ ,  $X_{Al}$ ,  $V_{Al}^{l}$ , and  $V_{Al}^{S}$  are the mole fractions and liquid and solid volumes of silicon and aluminum respectively, and  $V_0$  is the initial volume. Considering, as a first approximation, the density values of silicon and aluminum as  $\rho_{SiSolid} = 2.33$  g/cm<sup>3</sup>,  $\rho_{SiLiquid} = 2.54 \text{ g/cm}^3$ ,  $\rho_{AlSolid} = 2.70 \text{ g/cm}^3$  and  $\rho_{AlLiquid} = 2.375 \text{ g/cm}^3$ , at the eutectic concentration of 12.2 at.% aluminum-silicon alloy, the volume change (4.04) is 10.21 %. This produces a corresponding radial strain (4.03) of 3.4 %, which is also equivalent to the tangential strain in the oxide shell, since the radius and circumference are linearly related. Storaska and Howe [99] measured a linear change in diameter on melting that was approximately 3%. This is in reasonable agreement with the value calculated above and is a large strain compared to the measured 0.2 % critical tensile-strain of the aluminum oxide [102,103]. Following these data, the volume expansion induces a very strong stress on the thin oxide leading to aluminum-silicon particle explosion. In practice more than 90 % of the oxide survives during melting [99] suggesting that a kind of stress-relief mechanism should be present that allows the oxide to relieve the tangential stress. Observations by TEM and also molecular dynamic simulations, revealed that if there exists a non-uniform oxide layer, during melting it experiences a further thinning. This allows a molten particle to spur the liquid through the crack decreasing the internal pressure [99,104,105]. The influence of curvature radius on the internal pressure due to the volume expansions can be determined by using thin-walled pressure vessel

mechanism. The maximum internal pressure of the aluminum-silicon liquid phase due to the stressed oxide-shell can be determined from the following force-balance equation [106]:

$$P_I = P_S\left(\frac{2t}{r}\right),\tag{4.05}$$

where  $P_I$  is the internal pressure on the aluminum-silicon liquid,  $P_S$  is the pressure in the oxide shell, *t* is the oxide thickness and *r* the radius of the aluminum-silicon particle. Thus, for a given internal pressure, as the radius decreases, the pressure of the oxide shell must increase in order to allow the force-balance. This clearly shows that a smaller aluminum-silicon particle experiences higher pressure and tends to start the stress-relief mechanism before that in the bigger particles. This stress-relief mechanism is not observed for aluminum-silicon particles with dimensions lower than about 40 nm [105]. Considering that the stress-relief mechanism due to oxide thinning seems to be a creep mechanism, at nanoscale the creep mechanism is quite reduced [107], therefore it makes no sense to use aluminum pastes formed of aluminum powder having nanoscale dimensions.

The described mechanism reasonably explains why aluminum paste, with smaller particles, shows higher aluminum concentration at the aluminum/silicon interface with respect to that with bigger particles. The aluminum concentration increment improves the Al-BSF depth and enhances the peek of doping profile of the Al-BSF region. Smaller aluminum particles are available and more aluminum spheres will undergo the stress-relief mechanism increasing the aluminum concentration at the silicon surface inducing also a decrease of contact resistance as can be seen in Table 4.3. As predicted, the Al-BSF depth values reported in Table 4.3 show that smaller aluminum particles produce a deeper Al-BSF region.

The increment in peak is confirmed by the comparison of active doping profiles of Al-BSF regions measured on samples S29 and S30 reported in figure 4.04 and listed in Table 4.3. Consequently a benefit occurs on the  $V_{OC}$  values of a solar cell, due to a built-in voltage increment on the overall cell structure.

The second internal pressure contribution that the aluminum-silicon particle develops, and that does not influences the oxide shell stress, is the pressure given from (4.01). The total pressure (4.01) + (4.05) inside the liquid aluminum-silicon particles affects the interfusion of silicon into aluminum. As shown in ref. [108], the diffusion coefficient is reverse proportional to the total pressure inside the aluminum-silicon particle. At nanometer scale, (4.01) can reach pressures of a GPa magnitude [109]. Thus, the pressure can affect the silicon interdiffusion coefficient if is in the range between 15 to 20 atm. or higher.

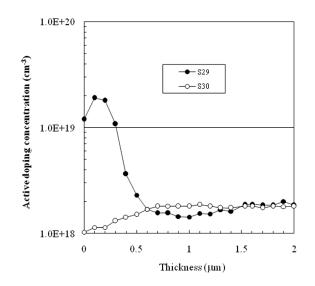


Figure 4.04. Active doping profiles of Al-BSF regions of samples S29 and S30.

The calculated internal pressures for different particle dimensions, taking into account that the surface tension of molten aluminum is 0.865 N/m [93], is reported in Table 4.4 for samples S27 and S28. It is seen that a radius dimension reduction of a factor of two, halves the diffusion coefficient of silicon inside aluminum. Analyzing in detail all the samples, it was found that the microstructure is always lamellar, independently of where the observation is taken (i.e.: aluminum/silicon interface) as shown in figure 4.5, or figure 4.6 within the aluminum matrix.

Lamellar structures are always formed from rich phases, such as aluminum with concentration higher than 98 at.% and silicon with concentration higher than 99 at.%. In this configuration silicon mainly tends to segregate at the interface. As already found in ref. [110], in this experiment, strong presence of silicon at the interface is confirmed. And it can be suggested that aluminum oxidation at the interface may be strongly influenced by silicon segregation. Both silicon and aluminum can be easily oxidized because of their low equilibrium oxygen partial pressure. A competition between aluminum oxidation and silicon segregation at the interface can then be supposed as possible inhibition mechanism, resulted in the Al<sub>2</sub>O<sub>3</sub> step formation or a pure Al-Al<sub>2</sub>O<sub>3</sub> interface [110], as shown in figure 4.07 where no silicon segregation is found.

Table 4.4. Calculated internal pressures (4.01) inside aluminum-silicon particles.

Sample	Min. diameter,	Р,	d(0.1),	P,	d(0.5),	Р,	d(0.9),	Р,	Glass frit
	μm	atm.	μm	atm.	μm	atm.	μm	atm.	
S27	0.955	36.2	1.537	22.5	2.733	12.66	4.746	7.3	No
S28	2.512	13.8	3.928	8.8	5.849	5.9	8.703	4.0	No

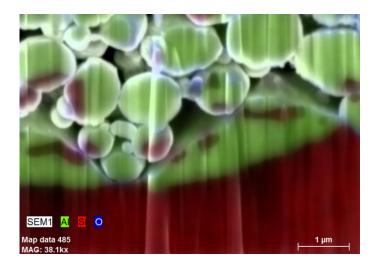


Figure 4.05. FIB-SEM micrograph and EDX microanalysis map of silicon, aluminum and oxygen content of sample S41 close the aluminum/silicon interface.

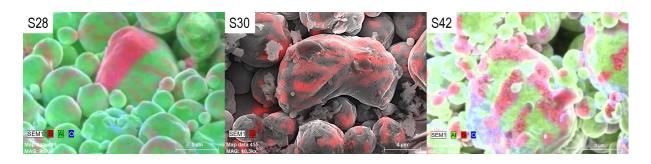


Figure 4.06. SEM micrographs and EDX microanalysis maps of silicon, aluminum and oxygen content of samples S28, S30 on top of the screen-printed aluminum layer.

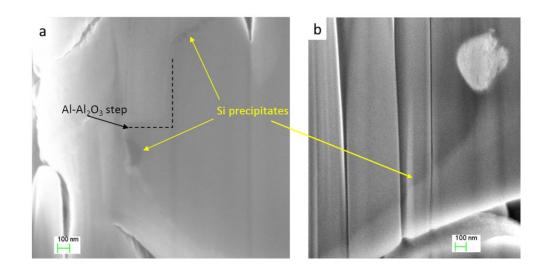


Figure 4.07. FIB-SEM micrographs of (a) Al-Al<sub>2</sub>O<sub>3</sub> abrupt step where no silicon precipitate is present, (b) silicon precipitate (darker area) along the Al-Al<sub>2</sub>O<sub>3</sub> interface.

Considering data from Table 4.2, it is evident that during the EDX measurement as the electron penetration range decreases, decreasing the energy (i.e. down to 5 kV), the concentration of silicon and oxides increases. This is because the pear-shaped electron beam penetrates less, thus more information from the surface is gained, indicating a greater oxide amount due to the  $Al_2O_3$  interface and greater amount of silicon due to the presence of silicon precipitate at the  $Al_2O_3$  interface.

It was found, that aluminum particle dimensions influence the silicon interdiffusion. As can be seen from Table 4.2, samples with smaller aluminum particles (i.e. S27 and S29) show lower content of silicon with respect to samples with bigger particles (i.e. S28 and S30). Moreover, from figure 4.02 it can be observed that bigger particles getters a greater amount of silicon due to the lower internal pressure meanwhile is in the liquid state, thus reducing the silicon diffusion elsewhere. Also from figure 4.02b it is possible to see that many small particles have silicon inclusions even not as pronounced as in case of bigger spheres. It is possible to conclude that only big aluminum particles can be totally filled with silicon and this is easily explained by the low internal pressure of the big particles with respect to the small ones. This is a sort of gettering mechanism, which effect also modifies the thermal expansion coefficient (TEC). Indeed, as an example, TEC of pure aluminum is 24 ppm/°C, TEC of eutectic aluminum-silicon alloy is 20 ppm/°C and TEC of Al-27at%Si is 16 ppm/°C [111].

Now, taking into account that: (i) silicon precipitates at the Al<sub>2</sub>O<sub>3</sub> interface; (ii) bigger particles getter silicon leaving the smaller particles with less silicon inside; (iii) aluminum pastes bulk resistivity values after firing as listed in Table 4.3; (iv) current mainly flows through a small curvature radius, so it preferentially passes through smaller aluminum-silicon particles and if these particles have an amount of Si precipitates these last increase the percolation resistance influencing the bulk resistivity. On the other hand we can deduce that the aluminum paste bulk resistivity is lower when a silicon gettering mechanism is effective as in case of big aluminum particles. This can be seen from Table 4.3 comparing sample S28 with sample S27, sample S30 with sample S29 and sample S42 with sample S41.

Finally, the presence of a glass frit reduces the surface tension and homogenizes the diffusion process. Reduction of surface tension decreases the internal pressure and increases silicon interdiffusion in aluminum. As an example bismuth, at a concentration of only 0.3 at.% reduces the surface tension by a factor of two (i.e. 0.5 N/m [93]). This effect is similar to doubling the curvature radius of aluminum-silicon particles and in presence of the glass frit it is possible to see also small particles fully filled with silicon, as shown in figure 4.08 for sample S41. In turn, aluminum paste from sample S27 does not show small particles fully filled with silicon.

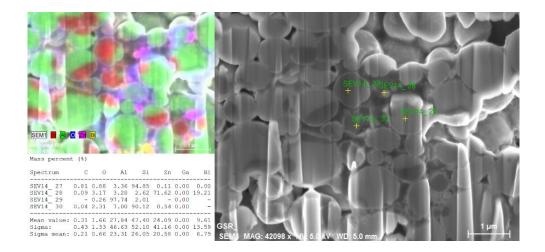


Figure 4.08. FIB-SEM micrograph and EDX microanalysis map of silicon, aluminum, oxide, zinc and bismuth content of sample S4. Quantitative analysis is performed and averaged for the locations marked with the yellow crosses.

# 4.4. Summary to the Chapter 4

Study of aluminum-silicon interdiffusion mechanism that occurs during the firing process of screen-printed aluminum layer required for the formation of the conventional rear metallization is very important because it affects solar cell operation and performance through Al-BSF passivation. In this study different screen-printing aluminum pastes, differs one from each other by aluminum particle dimensions and glass frit composition, are evaluated in terms of their bulk resistivity, contact resistance to silicon, Al-BSF profile depth and solar cell performance. Finally, this study allowed to reveal certain dependences between pastes parameters and their effect on solar cells and to develop useful recommendations for better solar cell performance. It was found that the mechanism of the silicon dispersion within aluminum screen-printed layers strongly related to initial dimensions of aluminum particle.

Initially aluminum spherical particles are free of silicon content. As temperature arises, phase transformation begins, as well as interdiffusion. At the liquid state, melted aluminum experiences volume expansion that is kept by the aluminum oxide, thus, creating the internal pressure inside the aluminum particle. This internal pressure should cause radial strain, which is however balanced by the oxide shell and can be expressed in terms of surface tension. It was calculated that the majority of aluminum particles experience very huge radial strain that should lead to particle explosion, which in real situation is not observed. SEM and EDX investigations, as well as the literature data, allowed to establish a stress-relief mechanism, helpful in the explanation of the effect of aluminum paste composition on solar cell parameters gained after the process of

aluminum paste firing. It was calculated that smaller particles experience higher pressure and tend to start the stress-relief mechanism before bigger ones. It was confirmed by the experiment, and one an interesting effect was observed for aluminum pastes having smaller particles. These smaller particles induced higher concentration of the liquid aluminum near the interface with silicon, promoting aluminum diffusion process and, therefore, the Al-BSF depth and solar cell  $V_{OC}$ .

As well as aluminum diffuses in silicon, silicon diffuses in aluminum. Microstructural investigation showed that silicon diffusion process is also affected by particle dimensions. Due to lower pressure in bigger particles, and the fact that diffusion coefficient is inversely proportional to the pressure, it was observed that bigger particles gettered bigger amount of silicon. This gettering effect allowed to describe a selective collection of silicon content inside bigger aluminum spheres during aluminum paste firing, helpful to reduce overall bulk resistivity of the aluminum paste, that positively influences the efficiency of a solar cell. One possible feedback of this research is that considering these relations between aluminum paste compositions, one is able to design optimized composition of aluminum paste having lowered laydown, keeping solar cell performance improved at the same time.

Finally, the conducted microstructural investigation allowed to understand the composition of a fired screen-printed aluminum layer, that consists of aluminum spherical particles having silicon precipitate and passivated with aluminum oxide shell. Both silicon and aluminum oxide phases represent an issue for direct electrical contact to such an aluminum layer, which is going to be solved in the next chapter.

# Chapter 5. Development of a new rear side metallization technology for solar cells based on solder pads electroplated using DLD/DLM technique

Applied research is usually focused on improvement of performance and cost reduction of a current technology. In the solar cells industry efforts are concentrated on three main directions: higher cell efficiency, thinner silicon wafers and low-cost process development. Nevertheless all the innovations introduced in cell manufacturing processes at the industrial level become acceptable only if they fit a minimum throughput higher than 1000 cells per hour requirement.

Today, screen-printed aluminum layer and silver pads for soldering are standard procedures to provide rear electrical contacts of silicon solar cells. Even though this process is consolidate it has several drawbacks: i) expensive silver that guarantees solderability for module manufacturing; ii) moderate and incomplete rear passivation with aluminum back surface field (Al-BSF), indeed silver solder pads are directly deposited on silicon; iii) wafer warpage due to thermal expansion of thick aluminum screen printed layer that limits wafer thickness [112]. Alternative technologies for rear electrical contacts of solar cells exist but they also utilize screen printing of aluminum and silver pastes. For instance, back contacted solar cells gain efficiency by putting all electrical contacts to the rear of the cell, however, this technology is not industrially ready for massive production because it uses complicated and time consuming processes, e.g. several photolithography steps [40]. Passivated emitter and rear cells (PERC) technology, instead, significantly improves solar cell performance through reduction of recombination losses using better passivation. This could be improved even more lowering the series resistance of metallization [38,113]. Industrially ready PERC cells also need silver pads to provide contact solderability.

Fired aluminum screen printed contact is a thick film consisting of aluminum/silicon microspheres passivated by alumina [114] that can reach a thickness up to 150 nm. This film represents an issue for the electrical performance of any heterogeneous contact and does not provide solderability. For this reason additional screen-printing of silver directly in contact with silicon is utilized for rear solder pads or bus bars. Today, these solder pads utilize at least 30 mg of silver per  $156 \times 156$  mm cell. Even though silver guaranties low resistivity and ribbon adhesion by soldering, its cost still affects the overall solar cell price. Therefore silver replacement is mandatory with

other metals, however, it is acceptable only if similar performance is ensured in terms of resistivity, solderability and adhesion.

In the past adhesion to aluminum was a well-known issue in packaging technology. In general, adhesion enhancement to aluminum was achieved using eutectic bonding through several treatment procedures, such as surface preparation and cleaning, aluminum oxide removal and activation of exposed aluminum surface using zincation for further nickel and gold plating [115].

The screen-printed aluminum layer can be considered as a porous layer. Therefore, this porous layer, in principle, allows mechanical adhesion anchoring metal inside inter-microspheres voids. On the other hand, electroplating techniques are not able to provide a fine control of metal deposition to fill such tiny voids with several metal layers and achieve eutectic bonding.

According to the International Technology Roadmap for Photovoltaic silver is consumed around 100 mg per cell [6], while around one third is utilized for rear side bus bars. Today, there are at least three approaches for silver reduction in rear side metallization that are described in literature: i) optimization of silver paste composition [116]; ii) tin ultra-sonic soldering [117,118]; iii) adaptation of standard microelectronic Al/Ni:V/Ag metallization [119]. According to the first approach, silver content on the rear side is lowered only by 30 % and Al-BSF issue still remains [116]. Tin ultra-sonic soldering shows adhesion in the range from 1 N/mm to 2 N/mm [117], which is sufficient to satisfy the DIN EN 50461 specimen, however, solder pads obtained thereby suffer from aging, showing significant degradation of the peeling force within 90 days [118]. Al/Ni:V/Ag metallization via sputtering technology shows great mechanical and electrical performance, as well as stability and low silver consumption down to 6 mg per cell [119]. However, sputtering processes have low throughput and high cost with respect to screen-printing. Plating technique that is widely proposed for the front side metallization [48], in principle, could be applied to the rear side metallization of solar cells. However, it suffers of low deposition rates thus resulting in very high cost of the ownership of an industrial production lines. Electroless plating was also proposed as a metallization technology for wrap through back contact solar cells [120], which is, however, far from low cost industrial applicability. Therefore, there is still a room for improvement in the technology for rear side metallization of solar cells.

The approach proposed in this work is based on innovative selective wet processing technique based on dynamic liquid drop/meniscus (DLD/DLM) concept [49–51,69]. This technique allows localized formation of metal pads that are directly electrodeposited on fired aluminum screen printed rear metallization layer. This approach permits to completely replace silver and provide mechanically and electrically stable solder pads that don't require flux during soldering procedure. Metal contacts obtained thereby show lower contact resistances as well as good adhesion. Solderability

is ensured by addition of a layer of tin that is plated using the same technique. Therefore openings in the aluminum layer in the rear side metallization are no longer required, thus increasing the solar cell efficiency due better back surface filed performance.

# **5.1. Preparation of samples**

In this work, 156×156 mm solar cells coming from industrial production line having full aluminum rear side contact without aperture area for silver pads are used. All electrochemical treatments in this work are performed using a novel DLD/DLM technique described in the Chapter 2 and Chapter 3.2.2.

#### 5.2. Solving the adhesion issue to screen-printed aluminum

Several pre-treatment procedures of the screen printed aluminum layer are investigated to provide direct metal/aluminum interface eliminating silicon and alumina phases and achieve better electrical and mechanical performances of the metal/aluminum contact. Main results are disclosed in figure 5.01 where SEM images with corresponding EDX microanalysis maps of aluminum/silicon microspheres are shown. Each row of figure 5.01 contains top-view and cross-section images and EDX map of aluminum microspheres corresponding to a single sample. The fourth row of figure 5.01 (i.e. figures 5.01 j and 5.01 k) shows only cross-section images. Figures 5.01 a-5.01c, referring to the screen printed aluminum layer, show the microspheres with dimensions from hundreds of nanometres to ten micrometres. Cross-section view and corresponding EDX map reported in figures 5.01b and 5.01c, clarify the presence of silicon phase and aluminum oxide layer that forms a shell around the aluminum/silicon sphere. Figures 5.01d-5.01f refer to the aluminum layer after electrochemical pretreatment by anodization in fluoride-based electrolyte. Figures 5.01g-5.01i refer to the aluminum layer after anodization pre-treatment in fluoride-based electrolyte with subsequent etching in hydrochloric acid solution. Figures 5.01j and 5.01k refer to the aluminum layer after a two subsequent anodization pre-treatment steps in fluoride and alkaline electrolytes. Electrolyte compositions and treatment regimes are listed in Table 5.1.

As evident from figures 5.01d-5.01f, rapid anodization process in fluoride electrolyte intensifies the alumina thinning and enhances the shell local breakage. Subsequent chemical treatment in hydrochloric acid solution continues the alumina etching and intensifies the aluminum/silicon core etching (figures 5.01g-5.01i). Instead, subsequent anodization in the alkaline electrolyte results in almost complete removal of alumina and silicon phases.

Thus, anodization pre-treatment technique able to guarantee direct metal/aluminum interface suitable for screen-printed aluminum layer is developed. In principle, using such technique is possible to achieve better adhesion of plated metals to such aluminum layer, as well as reduce the contact resistance.

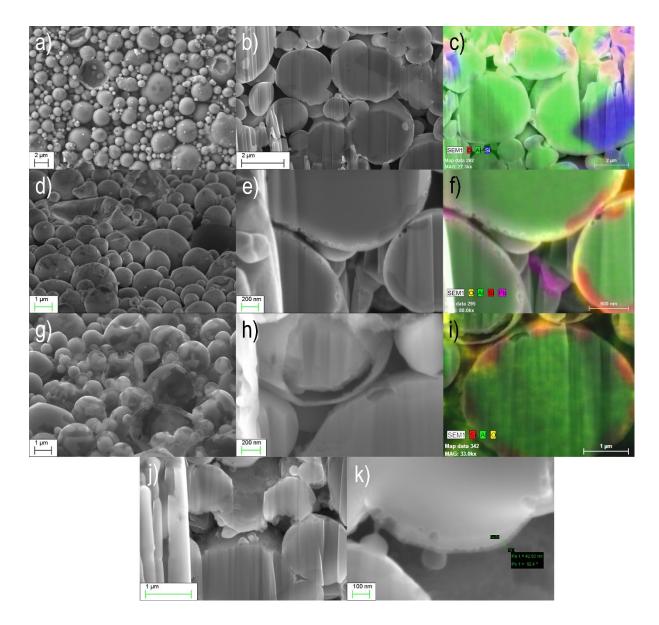


Figure 5.01. SEM images with corresponding EDX microanalysis maps of aluminum/silicon microspheres showing aluminum, silicon and oxide phases before (a, b, c) and after treatments in fluoride-based (d, e, f), hydrochloric acid (g, h, i), and alkaline (j, k) electrolytes.

Table 5.1. Chemical compositions of electrolytes and regimes of pre-treatment procedures for the aluminum rear side metallization layer in solar cells.

Name	Composition	Best regime
Fluoride-based electrolyte	0.5 wt. % HF and 0.4 wt. % NH4F	Anodization at 200 mA/cm <sup>2</sup> in 3 s
Hydrochloric acid solution	6 wt. % HCl	Stain etching in 10 s
Alkaline electrolyte	7 wt. % NH4F and 23 wt. % NH4OH	Anodization at 200 mA/cm <sup>2</sup> in 3 s

# **5.3. Electroplated tin solder pads**

Now, using anodization pre-treatment procedure described in previous paragraph, it is possible to obtain direct metal/aluminum interface for the rear screen-printed metallization layer. And, as the first experiment, tin electroplated solder pads are studied. DLD/DLM technique described in Chapter 3.2.2. is used in this experiment to perform both anodization pre-treatment and electroplating of tin. Tin solder pads are deposited directly into the screen-printed aluminum layer and a cross-section FIB-SEM micrograph with corresponding EDX microanalysis maps of such structure is shown in figure 5.02. It was found that electroplated tin is deposited inside inter-microsphere voids in the screen-printed aluminum layer. Using anodization pre-treatment it became possible to obtain direct tin/aluminum interface shown in figure 5.03.

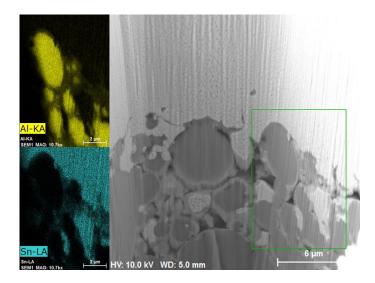


Figure 5.02. SEM and EDX color map of tin deposited inside screen-printed aluminum layer.

Such a tin electroplated solder pads allow direct bonding of a solar cell to a solder ribbon without using any flux. A typical load-deformation curve is shown in figure 5.04 obtained by the peel test for a bonded 2 mm wide solder ribbon. According to the DIN

EN 50461 specimen, industry looks for peeling strengths higher 1 N/mm. Considering the values reported in figure 5.04, the technique of electroplated tin solder pads passes the requirements. But still the obtained value is close to the limit and is much lower to the values of the tensile strength of a typical tin joint. Therefore, the detailed investigation of the failure reasons is performed revealing that the main issue with the tin solder pad on screen-printed aluminum layer is due to the reflow process that occurs during bonding. It was found that during bonding process tin deposited into the intermicrosphere voids melts and tends to move and adhere to more wettable surface, such as the solder ribbon rather than aluminum microspheres.

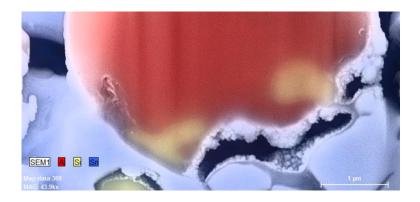


Figure 5.03. SEM and EDX color map of the tin/aluminum interface obtained after deposition of tin inside scree-printed aluminum layer.

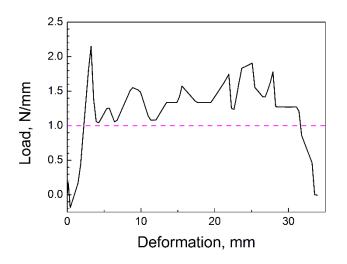


Figure 5.04. The peel force and displacement characteristic curve of a single tin electroplated solder pads. The dashed line remarks the required minimum adhesion according to DIN EN 50461 specimen.

Several samples of solar cells are manufactured using the above proposed approach for the tin solder pads fabrication. Samples are  $4 \times 4$  cm standard p-type silicon solar cells having equal front side texturization, passivation and silver screen-printed grid. 4 samples are fabricated with full aluminum print and kept for further processing with electroplating of tin, while other 4 samples are fabricated having 3 cm long and 2 mm wide screen-printed aluminum bus bars and are kept for reference. Table 5.2 contains the list of the samples and procedure steps.

Table 5.2. Samples and treatment conditions to fabricate solar cells with tin electroplated solder pads.

Sample	Process conditions
S27-1	
S28-1	Reference samples of solar cells having silver/aluminum bas bars on
S29-1	the rear.
S30-1	
S27-2 S28-2 S29-2 S30-2	1) anodization in fluoride-base electrolyte at $j = 200 \text{ mA/cm}^2$ , $t = 3 \text{ s}$ ; 2) anodization in alkaline-based electrolyte at $j = 200 \text{ mA/cm}^2$ , $t = 5 \text{ s}$ ; 3) Electroplating of tin at $j = 50 \text{ mA/cm}^2$ , $t = 790 \text{ s}$ at 50 °C.

The sun-light I-V parameters, listed in Table 5.3, allow comparing the effectiveness of tin rear metallization with the counterpart made by standard silver.

Two types of measurements are performed: i) contacting the full area (both solder pads and aluminum layer) of the cell rear side; ii) contacting only the solder pads. The first method allows neglecting major part of series resistance due to the rear contact, thus, showing the performance of a hypothetic cell with perfect metallization. Instead, the second method shows the cell performance in real operation conditions. The difference between these two methods numerically indicates the efficiency losses due to parasitic series resistances of the rear contact. The difference between losses numerically characterizes different metallization processes of the solar cells initially having different electrical parameters between each other. As reported in Table 5.3, standard silver based rear solder pads produce relative 30 % efficiency loss. Modified solar cells with tin electroplated solder pads show just relative 2-3 % efficiency loss. Thus, the solar cell efficiency gain is evident and it is mainly due to two reasons. One is the absence of openings in Al-BSF, no longer necessary since tin can be electroplated directly onto the screen-printed aluminum layer. The second is the lower contact resistance of tin/aluminum interface with respect to silver/aluminum since the area of tin/aluminum contact is the total area of the solder pad while the area of silver/aluminum contact is just the perimeter of each pad.

Therefore, the novel approach of electroplated rear side solder pads is definitely promising, since it provides a significant improvement of the electrical performance of solar cells. However, the use of tin as a metal for a solder pad seems unreasonable due to its reflow during bonding, leading to poor mechanical properties of such a solder pad. This is unacceptable due to requirements for the reliability of solar modules. However, tin replacement with a metal having higher melting point could be a better solution.

Table 5.3. Comparison of light *I-V* parameters of solar cells with standard industrial silver-aluminum rear side metallization and solar cells with tin electroplated solder pads.

Sample	V <sub>OC</sub> , mV	J <sub>SC</sub> , mA/cm <sup>2</sup>	Normalized FF	Normalized η	Rs
S27-1 – full rear contact	614	35,1	1,000	1,000	1,86
S27-1 – Ag pad contact	617	34,6	0,814	0,749	2,18
S27-2 – Sn pad contact	608	34,5	0,987	0,974	1,85
S28-1 – full rear contact	620	35,3	1,000	1,000	2,3
S28-1 – Ag pad contact	589	35,5	0,810	0,774	2,5
S28-2 – Sn pad contact	620	35,2	0,995	0,990	2
S29-1 – full rear contact	625	36,3	1,000	1,000	2,3
S29-1 – Ag pad contact	586	34,6	0,783	0,700	3,04
S29-2 – Sn pad contact	624	36,1	0,998	0,992	2,3
S30-1 – full rear contact	628	35,4	1,000	1,000	2,87
S30-1 – Ag pad contact	590	34,5	0,825	0,756	2,98
S30-2 – Sn pad contact	628	34,7	0,998	0,980	2,76

# 5.4. Electroplated nickel-tin solder pads

Since nickel has higher conductivity and melting point than tin, it is used as the main material for solder pads fabrication.

In this experiment, nickel deposition is performed after each kind of pretreatment procedure. The best mechanical performance is achieved after subsequent anodization in fluoride-based and alkaline electrolytes. Figure 5.05 shows cross-section SEM image of the aluminum layer in which voids between adjacent spheres are completely filled with electroplated nickel. This condition provides good mechanical adhesion. The aluminum/nickel interface can now be clearly observed in figure 5.05. Then, 3 µm thick electroplated tin layer is added to provide better soldering condition. SEM/EDX image of this structure is showed in figure 5.06.

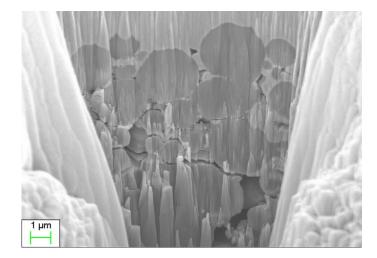


Figure 5.05. Cross-section SEM image of the aluminum layer, where the voids between adjacent spheres are filled with electroplated nickel.

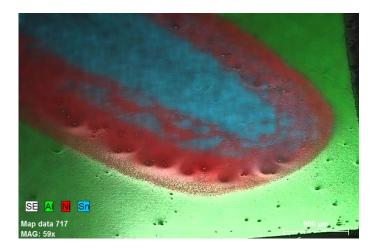


Figure 5.06. SEM/EDX image of the nickel-tin solder pads fabricated in this work.

The load-displacement characteristic curve obtained by the peel test is shown in figure 5.07. The 6 peaks reported in the figure refer to each solder pad within the dashed bus bar. Delamination of nickel and tin layers occurs smooth and the peel force varies in the range between 2.5 N/mm and 5.0 N/mm range. Figure 5.08 shows SEM image of a single solder pad after mechanical removal of the nickel layer form the aluminum layer. The damage profile illustrates mechanical nature of the adhesion obtained between the two metals. It was found that pre-treatment conditions and internal stress of electrodeposited nickel layer are among parameters affecting the adhesion. The best

mechanical adhesion performance is observed when anodization pre-treatment in fluoride-based and alkaline electrolytes are performed, which, in turn, result in variable adhesion depending on the anodization regime. Too high anodization current density and time can damage the aluminum layer producing powder and does not allow further additional treatment.

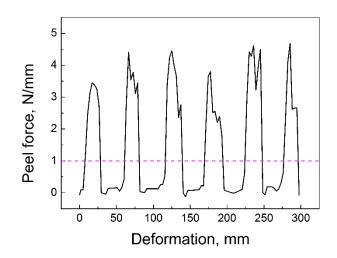


Figure 5.07. The peel force and displacement characteristic curve of nickel-tin electroplated solder pads of the solar cell bus bar. The dashed line remarks the required minimum adhesion according to DIN EN 50461 specimen.

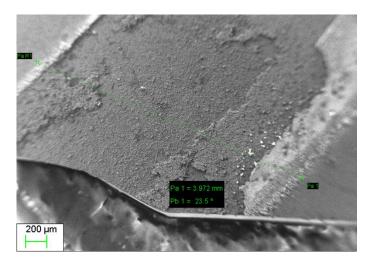


Figure 5.08. SEM image of the aluminum layer after nickel solder pad removal.

As reported in figure 5.09, different anodization regimes, listed in Table 5.4, are used to study the effect of anodization pre-treatment on the adhesion of bonded nickeltin solder pads. At the initial stage of this study, the nickel electrolyte was not optimized and the plating regime was kept constant: 200 mA/cm<sup>2</sup> current density for 200 s of deposition time. After investigation of different anodization pre-treatments, listed in Table 5.4, anodization regime #5 was selected for further experiments because of its better influence on the adhesion. Indeed, the adhesion measurements, related to the #5 pre-treatment regime, result always over the required minimum adhesion according to DIN EN 50461 specimen (dashed line in figure 5.09) and show also the lowest spread of measured values.

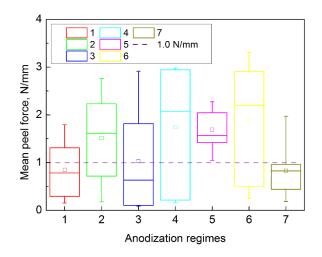


Figure 5.09. Box plot of peel force distributions for nickel-tin solder pads formed using non-optimized nickel electrodeposition process at 200 mA/cm<sup>2</sup> for 200 s deposition time. Box charts correspond to anodization pre-treatments performed in different regimes using fluoride-based and alkaline electrolytes according to Table 5.4. The dashed line remarks the required minimum adhesion according to DIN EN 50461 specimen.

Table 5.4. Electrochemical regimes used for the anodization pre-treatment optimization using fluoride-based (A1) and alkaline (A2) electrolytes.

Anodization	Anodization in fl based electroly		Anodization in alkaline electrolyte (A2)		
Regime #	Current density, mA/cm <sup>2</sup>	Time, s	Current density, mA/cm <sup>2</sup> Ti		
1	0	0	0	0	
2	50	2	100	2	
3	50	2	100	3	
4	50	2	200	2	
5	100	3	100	3	
6	100	3	200	3	
7	200	3	200	3	

The quality of electrodeposited nickel layer also affects the mechanical stability of the solder pad. Varying the pH of the plating electrolyte and the additives concentration, it becomes possible to regulate the internal stress of the deposit. Once the optimization of electrolyte parameters is obtained, the influence of the electrodeposition current density on the solder pads adhesion is investigated. As evident from figure 5.10, higher and more stable adhesion is obtained in regimes with lower current densities (see Table 5.5 for description of plating regimes). The adhesion measurements related to the #1 and #2 nickel deposition regimes result in the mean peeling strength ranging from 1.5 N/mm to 2.5 N/mm and from 2.5 N/mm to 3.8 N/mm and show low spread of values. The current density is the main responsible of the deposit quality in terms of stress and porosity. After numerous experiments, it is possible to suggest that deposit with the lowest stress and minimal porosity show the highest and stable adhesion.

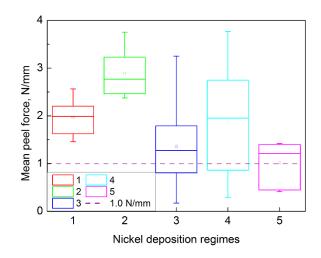


Figure 5.10. Box plot of peel force distributions for nickel-tin solder pads formed using optimized anodization pre-treatment regime listed in Table 5.5. Box charts correspond to nickel electrodeposition performed at different current densities. The dashed line shows the required minimum adhesion according to DIN EN 50461 specimen.

Table 5.5. List of electrochemical regimes investigated to optimize nickel deposition conditions.

Regime #	Current density, mA/cm <sup>2</sup>	Time, s
1	325	120
2	550	90
3	575	120
4	650	75
5	800	60

Several samples of solar cells are manufactured using the above proposed approach for the solder pads fabrication. The samples are standard  $156 \times 156$  mm solar cells coming from industrial production line having full aluminum rear side contact without aperture area for silver pads. The sun-light *I-V* parameters, listed in Table 5.6, allow comparing the effectiveness of nickel-tin rear metallization with the counterpart made by standard silver. As reported in Table 5.6, standard silver based rear solder pads produce 0.69 %<sub>abs</sub> efficiency loss. Modified solar cells with nickel-tin electroplated solder pads show just 0.21-0.38 %<sub>abs</sub> efficiency loss. Thus, the solar cell efficiency gain is approximately 0.5 %<sub>abs</sub> and it is mainly due to two reasons. The former is the absence of openings in Al-BSF, no longer necessary since nickel-tin can be electroplated directly onto the screen-printed aluminum layer. The latter is the lower contact resistance of nickel/aluminum interface with respect to silver/aluminum, since the area of silver/aluminum contact is just the perimeter of each pad.

Solar cell	V <sub>OC</sub> , mV	J <sub>SC</sub> , mA/cm <sup>2</sup>	FF, %	η, %
0 full rear contact	628.0	35.32	82.18	18.24
0 Ag pad contact	628.0	35.18	79.44	17.55
$ \Delta $				0.69
1 full rear contact	626.0	34.98	79.65	17.45
1 Ni-Sn pad contact	626.0	35.01	78.64	17.24
$ \Delta $				0.21
2 full rear contact	634.7	35.32	81.55	17.94
2 Ni-Sn pad contact	633.0	35.30	79.15	17.69
$ \Delta $				0.25
3 full rear contact	633.7	35.39	81.22	18.23
3 Ni-Sn pad contact	634.0	35.44	79.43	17.85
$ \Delta $				0.38

Table 5.6. Comparison of light *I-V* parameters of industrial solar cells with silver and nickel-tin solder pads.

Taking into account this result a further optimization of the rear pads design may be performed to achieve lower series resistance losses. Indeed the current industrial configuration of separate solder pads for the rear side metallization has now the only goal to decrease silver amount and then the cell cost. Using the proposed plating approach this configuration of solder pads is no longer necessary since nickel and tin are low cost materials, therefore, it can be modified to reduce the cell series resistance even more. Possible improvement of the proposed approach may be achieved using copper plating, since copper has higher conductivity than nickel. It is to remark that the pad deposition process can be speeded up through the deposition velocity or switching to the material more suitable for speed plating, such as copper. However, detailed study of copper diffusion and solar cells degradation has to be carried out.

# 5.5. Electroplated copper-tin solder pads

Copper has lower conductivity than nickel, however, copper is a lifetime killer in silicon crystal, and in order to use it with silicon, usually a barrier layer is applied, such as a thin nickel film. On the other hand, in this work, rear side solder pads are applied directly onto the screen-printed aluminum layer. The screen-printed aluminum layer experience thermal treatment, in order to form Al-BSF for both passivation and charge carriers segregation. SEM micrographs and corresponding EDX microanalysis maps of such an aluminum/silicon interface report formation of 2-3  $\mu$ m thick aluminum-silicon eutectic layer, as shown in figure 5.11.

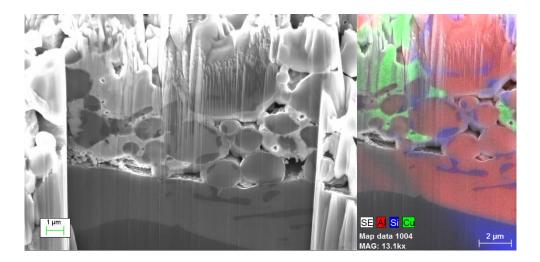


Figure 5.11. FIB-SEM micrograph and EDX microanalysis map of the aluminum/silicon interface obtained after firing of the screen-printed aluminum layer and copper electrodeposition.

It is seen that such a thick aluminum-silicon alloy could serve as a barrier layer for copper diffusion inside silicon crystal. Therefore, in this work, the same configuration of solder pads is adopted as it is described earlier. Using the same anodization pre-treatment conditions reported for nickel-tin solder pads formation, here, solar cells with copper-tin rear electroplated solder pads are fabricated. The loaddisplacement characteristic curve obtained by the peel test is shown in figure 5.12. The 6 peaks reported in the figure refer to each solder pad within the dashed bus bar. Delamination of copper and tin layers occurs smooth and the peel force varies in the range between 2.5 N/mm and 5.2 N/mm range. It is seen that mechanical performance of electroplated copper-tin solder pads demonstrate very good behavior, comparable to the behavior obtained for electroplated nickel-tin solder pads.

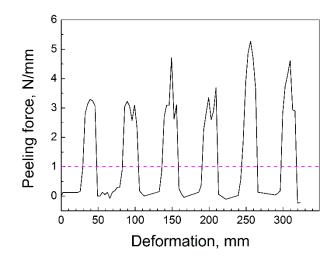


Figure 5.12. The peel force and displacement characteristic curve of copper-tin electroplated solder pads of the solar cell bus bar. The dashed line remarks the required minimum adhesion according to DIN EN 50461 specimen.

Degradation of solar cells having copper-based solder pads is studied by means of *I-V* measurements performed in dark and room temperature conditions before and after thermal annealing at 150 °C for 62 hours. The *I-V* measurement is shown in figure 5.13, it is seen that no any effect on electrical performance is observed.

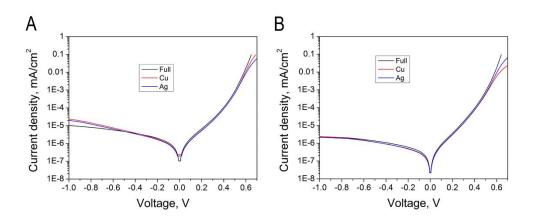


Figure 5.13. Dark I-V measurements before (A) and after (B) annealing at 150 °C for 62 hours.

As reported in Table 5.7, standard silver-based rear solder pads cause 0.69  $\%_{abs}$  efficiency loss. Modified solar cells with copper-tin electroplated solder pads show 0.43  $\%_{abs}$  and 0.54  $\%_{abs}$  efficiency loss. Thus, the best solar cell efficiency gain is equal to 0.26  $\%_{abs}$ , which is, however, almost two times lower than the efficiency gain obtained for electroplated nickel-tin solder pads. This fact requires further studies, but it may be related to another disadvantage of using copper for solder pads. It was found that copper electroplating is inconvenient, at least using acidic electrolytes. In this work, copper sulfate based electrolyte is used, which contains sulfuric acid that reacts with aluminum and aluminum oxide, creating an aluminum sulfate salt that cause significant degradation of the performance of the electrolyte. It can be true, that this salt is precipitated also in the area of electroplated solder pads, thus, affecting their homogeneity, porosity and, finally, the conductivity.

Table 5.7. Comparison of light *I-V* parameters of industrial solar cells with silver and copper-tin solder pads.

Sample	V <sub>OC</sub> , mV	J <sub>SC</sub> , mA/cm <sup>2</sup>	FF, %	η, %
0 full rear contact	628.0	35.32	82.18	18.24
0 Ag pad contact	628.0	35.18	79.44	17.55
$ \Delta $				0.69
4 full rear contact	628.6	36.54	80.63	18.52
4 Cu-Sn pad contact	627.9	36.46	79.04	18.09
$ \Delta $				0.43
5 full rear contact	629.0	36.56	81.36	18.71
5 Cu-Sn pad contact	629.2	36.37	79.42	18.17
$ \Delta $				0.54

### **5.6. Summary to the Chapter 5**

In this work, a new rear side metallization technology is developed for solar cells. The technology supposes localized formation of solder pads using electrodeposition of metals directly inside fired screen-printed aluminum rear layer of a solar cell. Localized electrodeposition is achieved using DLD/DLM technique that allows any kind of wet surface treatment in specific defined positions. This approach allows to avoid the use of photolithography, limiting the cost of the process mainly to the cost of materials. In this work, electroplated nickel-tin solder pads are proposed to use, which cost significantly lower to a silver counterpart that is currently adopted by the industry. The cost reduction is not a single advantage of the proposed technology. Since electroplated solder pads can be deposited directly inside screen-printed aluminum layer, uniform Al-BSF

performance can be provided for solar cells and, as it is shown in this Chapter, this results in up to  $0.5 \ \%_{abs}$  efficiency gain respect to current screen-printed silver technology.

Among the metals studied in this work are tin, nickel and copper. Deposition of these metals is investigated in present study. It was found that the highest adhesion of metals is achieved only using several pre-treatment procedures of the aluminum layer before the electrodeposition step. Such pre-treatments are studied and optimized in this work. As a result, two types of rapid anodization pre-treatments in fluoride- and alkaline-based electrolytes are able to guarantee superior stability of extreme adhesion of the proposed metallization technology.

It was found that the solder pads made of tin only experience reflow during bonding of solder ribbons, and this is a standard procedure for solar cells required for module assembly. The reflow issue limits adhesion of bonded ribbons to 1 N/mm at best, which is sufficient to satisfy DIN EN 50461 specimen. However, investigation of failure mechanism through the multiple tests revealed very high failure rates even for stable fabrication conditions.

Therefore, for further experiments it was reasonable to select any other metal having melting point higher than tin. Nickel-tin solder pads, as it was expected, showed much greater mechanical performance. Adhesion tests report of peeling strength in the range from 2.5 N/mm to 5.0 N/mm.

Copper-based solder pads despite a great mechanical performance demonstrated moderate electrical parameters. Moreover, it was found process incompatibility of copper electroplating, at least from acidic solutions, to an aluminum layer due to very fast degradation of copper-containing electrolyte.

# Chapter 6. Development of a new front side metallization technology based on porous silicon and electroplated nickel and copper

Silver represents one of the main issues to reduce the silicon solar cell cost per watt. In 2014 the International Technology Roadmap for Photovoltaics (ITRPV) predicts silver reduction down to 50 mg per cell in 2018 [6]. To achieve this goal many researchers are focusing on silver replacement using nickel- and copper-based metallization [48]. This approach introduces several issues to be solved to promote this process at industrial level. It is known that nickel contacts for both n- and p-type silicon exhibit good electrical properties through silicides formation [79]. Nevertheless, nickel alone cannot be used to replace silver due to its conductivity significantly lower than silver. On the other hand copper shows conductivity comparable to silver but copper is a lifetime killer for silicon-based solar cells due to its high mobility inside the silicon crystal even at low temperature [121]. Consequently, a barrier layer is required to prevent copper diffusion and to guarantee low contact resistance on silicon. Two-layer metallization consisting of thin nickel barrier layer and thick copper conductive layer is a solution to address both metal conductivity and copper diffusion issues.

According to the state-of-the-art, plating is a common technique for nickel- and copper based metallization of solar cells. Today many publications report the application of electroless, electrochemical, or light-induced plating (LIP) techniques, which have been thoroughly reviewed by Lennon et al. [48]. Industrial applicability of the plating processes foresees two main issues. One is the solar cell masking needed to protect the active area of the solar cell, in order to form the front grid metallization. Another issue concerns the cell throughput of plating technique at industrial level, which directly depends on the plating speed. Even though in the semiconductor industry deposition rate of several micrometers per minute is considered rather high, in turn, it does not satisfy industrial requirement of solar cell manufacturing that demands a throughput of more than 1000 cells per hour. The most attractive solution is represented by high speed electroplating procedure using localized plating and dynamic liquid drop/meniscus technique, recently proposed in ref. [51,69].

According to the most recent ITRPV overview, before the introduction of alternative metallization technique adhesion issue has to be solved [6]. Adhesion of plated metals to silicon is a well-known issue, indeed special surface treatment is necessary before the metal deposition step [122]. Such surface treatment, as chemical etching, results in rougher surface but considering that silicon solar cells are moving to shallower junctions (i.e.  $0.3 \mu m$ ) that roughness can cause damage up to the depletion region. Another approach to the adhesion issue is featuring the silicon substrate with

25  $\mu$ m deep grooves that allow to anchor metal layers inside the silicon substrate [123]. But now silicon wafers for solar cells are thinner than 200  $\mu$ m, therefore groves are not welcomed since they reduce the mechanical strength of the silicon substrate, thus reducing the yield of solar cell production line. On the other hand the use of silicide can promote the adhesion of nickel film plated on silicon [124]. However, recently, it has been shown that poor adhesion of nickel to silicon is still observed even after silicide formation [124]. Accumulation of Kirkendall voids at the silicide-nickel interface, attributed to unbalanced diffusion rates of nickel and silicon into each other and defects inside the plated nickel film can result in poor adhesion on silicon substrate, therefore the uniformity of the silicide-nickel interface becomes relevant, taking also into account that nickel silicide sintering contributes to the contact resistance between metal and silicon emitter layer.

In this work, the electrical contact formation performed by nickel and copper electrodeposition on n-type doped emitter regions of silicon-based solar cells is investigated. The main innovation of this work concerns the introduction of approximately 30 nm thick layer of mesoporous silicon layer that allows to simultaneously obtain two characteristics: metal anchoring inside pores to promote the adhesion avoiding emitter damaging and improved distribution of phases due to the large area contact between nickel and silicon for subsequent homogenous silicide formation. Research and application of porous silicon to solar cells lies mainly in the field of antireflection coating (ARC) material and the first development started more than 30 years ago by Prasad et al. [55]. To characterize solar cells having porous silicon as ARC, Vinod [42] studied the application of standard screen printed silver metallization on it. According to his methodology, it was necessary to remove completely the porous silicon layer by molten glass frit contained in the silver paste, to achieve good electrical contact parameters between metal and silicon. Instead, in this work, a porous silicon layer is introduced in solar cell manufacturing process to enhance metal/semiconductor contact performance in terms of contact resistance and adhesion, thus, expecting higher efficiencies for solar cells and better reliability for solar modules. Indeed mesoporous silicon layer having porosity gradient and completely filled with nickel, warranties both electrical and mechanical properties of the metal/silicon contact resulting in adhesion strength higher than 4.5 N/mm and contact resistance of 350  $\mu\Omega$ ·cm<sup>2</sup> on 80  $\Omega$ /sq emitter.

Moreover, cost reduction in solar cell manufacturing can be obtained replacing silver with inexpensive metals (i.e. nickel and copper). To this aim in this work is proposed a very simple technique due to easy and cheap processes, as anodization and electroplating. This technique is not particularly sensitive to sheet resistances and thicknesses of emitters of solar cells, leading to a process easily transferable to the industrial cell manufacturing.

# **6.1.** Preparation of samples.

The formation of porous silicom layer on the emitter regions is obtained by anodization in hydrofluoric acid (HF) based electrolytes. Chemical composition of the electrolyte is used starting from 48 % HF acid, deionised water and isopropanol mixed in variable ratios. Thicknesses of porous silicon layers around 30 nm are chosen for all the samples. Porous silicon layers are formed in both galvanostatic and galvanodynamic regimes using standard two-electrode electrochemical cell. During the anodization, a voltage is applied to the samples to forward bias the p-n junction.

Metal plating of solar cell emitters is performed inside a glass beaker filled with electrolyte. The electrodeposition is obtained using two-electrode configuration described in the Chapter 3.2.1. After coating the aluminium backside contact with chemically resistive film, the samples are vertically placed inside the liquid solution. Illumination to promote the plating of samples is then added by Olympus ILK-7B 150 W tungsten-halogen light source. To form nickel and copper layers, Enthone® industrial electrolytes, LECTRO-NIC 10-03 nickel sulfamate based and MICROFAB SC 40 MD copper sulfate based are adopted. In order to form high quality dense nickel layers, both plating in galvanostatic regime and the pulse-reverse plating (PRP) technique are studied. The latter process is completely described by Chandrasekar et al. [125]. Nickel plating is carried out onto porous silicon layers and consisted of the two stages. At the first stage, nickel is supposed to fill the pores (i.e. inner volume) of the porous silicon layer. To avoid oxide formation in porous silicon layer that is known to inhibit silicidation process [126], 0.5 % fluoride content is introduced into the nickel plating electrolyte. At the second stage, thick barrier layer is formed. Temperature of the liquid solution during plating is kept at 60 °C. Current densities are chosen in the range between 10-1000 mA/cm<sup>2</sup>. Thus, around 300 nm thick nickel films are obtained. In order to form the silicide, annealing on a hot-plate for 3 minutes at 350 °C in air is carried out. Then, 9 µm thick copper layer is deposited on top of the nickel barrier layer, to reduce the overall resistance of the metal contact. Copper layer is formed by electroplating in galvanostatic regime. During the plating procedure, the temperature of the liquid solution and the current density are chosen at 50 °C and 200 mA/cm<sup>2</sup>.

PRP regime consisting of three repeatable steps is used and the current density profile is shown in figure 6.01. At the first step, electrochemical deposition with a short ( $t_{dir} = 100 \text{ ms}$ ) pulse of current ( $j_{dir}$ ) is performed. In order to slightly dissolve the deposit obtained during the first step, the voltage polarity of the electrochemical cell is switched and a short ( $t_{rev} = 100 \text{ ms}$ ) pulse of reverse current ( $j_{rev}$ ) is applied. Then, as third step, a relaxation time of 50 ms ( $t_{off}$ ) is used to "refresh" the reaction area. Values of these parameters,  $j_{dir}$  and  $j_{rev}$ , are relevant variables in the investigation. Approximate number

of periods of PRP and time of galvanostatic deposition are estimated from the total electric charge value, which is kept in range of 100-300 mC/cm<sup>2</sup> in this study.

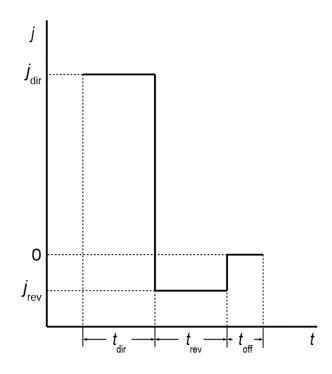


Figure 6.01. Current density profile used for the PRP plating procedure.

# 6.2. Study of mesoporous silicon formation

The influence of anodization parameters on properties of porous silicon layers is thoroughly studied in literature [57–60] and described in Chapter 1.9 of the present work. Porous silicon is usually obtained by electrochemical etching (anodization) of silicon crystals in a hydrofluoric acid (HF) containing electrolytes. The substrate doping, its crystallographic orientation, the electrolyte composition and the current density are among process variables that affect porous silicon morphology and, thus, its electrical and mechanical properties. In this work, it was found that the emitter's sheet resistance did not affect the porous silicon layer morphology. Electrolytes with HF concentration in the range between 9 and 25 wt. % are tested. As the result, as shown in figure 6.02 the porous silicon morphology with randomly distributed straight pores having average diameter in the range between 5 and 20 nm is observed.

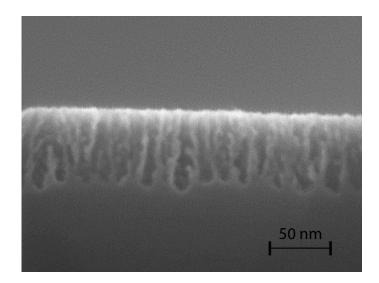


Figure 6.02. Cross-section SEM micrograph of the porous silicon layer formed on 70  $\Omega$ /sq emitter at 40 mA/cm<sup>2</sup> in electrolyte composed of 48 % HF, deionised water and isopropyl alcohol in 1:1:1 ratio.

It was found that the morphology of porous silicon layer did not depend on the emitter's sheet resistance due to almost equal doping profile in the region that extends up to 50-100 nm from the top surface. Figure 6.03 shows the phosphorus doping profile of the 70  $\Omega$ /sq emitter region. The region extending up to 100 nm from the top surface shows phosphorus doping concentration in the range between 10<sup>19</sup> and 3·10<sup>19</sup> cm<sup>-3</sup>. It precisely correlates with the doping profile measurement for 100  $\Omega$ /sq solar cells reported by Rauer et al. [127]. According to Sze [128], such phosphorus doping concentration in silicon corresponds to 10<sup>-3</sup>  $\Omega$ ·cm resistivity, and properties of pores for such type of silicon wafers are already studied by Herino [59]. In this work strong correlation with Herino's data for the pore morphology, pore sizes distribution, electrolytes and anodization regimes is observed.

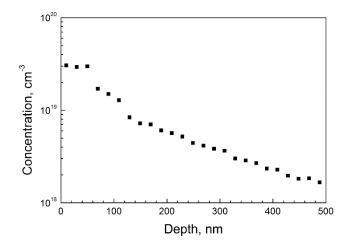


Figure 6.03. Phosphorus doping profile on the front of the 70  $\Omega$ /sq solar cell measured by means of Stripping Hall profile technique (Chapter 3.4).

It is known that for highly doped n-type silicon crystals the pore morphology of the top part of porous silicon layer is different from the bottom one [129]. There is a thin layer (less than 15 nm) close to the surface consisting of a significantly larger number of narrower pores that merge together forming larger pores at the bottom part of porous silicon layer. Such structure is shown in figure 6.04. The sample is formed at 100 mA/cm<sup>2</sup> current density. It is clear that such a porous silicon layer represents an issue for the further electroplating step blocking penetration of the electrolyte and thus affecting the deposition of a metal inside pores of porous silicon. However, porous silicon is a versatile material with large tunability of its physical and morphological properties. Therefore current controlled anodization or anodization in galvanodynamic regimes are used to design some specific structures of porous silicon layer controlling pore diameters through the current density during anodization process. Porous silicon layer that seems like an array of sharp pyramids is presented in figure 6.05. Pore walls tapering is obtained linearly varying in 0.75 s the anodization current density between 120 and 25 mA/cm<sup>2</sup>. At 120 mA/cm<sup>2</sup> current density is too high and performs electropolishing of silicon. Short period of the electropolishing process during the anodization in the galvanodynamic regime is helpful to eliminate the thin layer of low porosity (i.e. the top blocking part), while during the remaining time, formation of regular pores occurs. Similar structure can be obtained using different anodization parameters, and through the optimization of these parameters (e.g. current density values) a suitable profile of pores is obtained to allow a full filling of pores with metal, thus warranting good anchoring of metal into silicon. The best contact performances are observed on samples with gradient porosity of the PS layer as shown in figure 6.05.

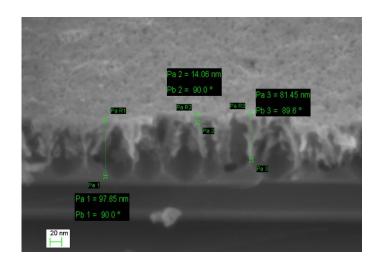


Figure 6.04. Cross-section SEM micrograph of the porous silicon layer formed on 70  $\Omega$ /sq emitter at 100 mA/cm<sup>2</sup> in electrolyte composed of 48 % HF, deionised water and isopropyl alcohol in 1:1:1 ratio.

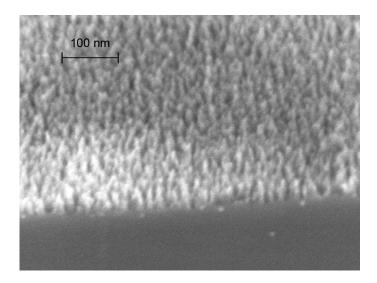


Figure 6.05. Cross-section SEM micrograph of the porous silicon layer formed on 70 Ω/sq emitter in galvanodynamic regime with current density profile linearly descending in 0.75 s from 120 to 25 mA/cm<sup>2</sup> in electrolyte composed of 48 % HF, deionised water and isopropyl alcohol mixed in 1:1:1 ratio.

# **6.3. Electroplated nickel contacts**

Nickel layer is introduced to form a barrier against copper atom diffusion into silicon. To this aim nickel layer should be dense and uniform promoting low contact

resistance and high adhesion to silicon. Moreover it is absolutely mandatory to achieve high homogeneity of the silicon-nickel interface. Mesoporous silicon layer proposed in this work does help nickel to achieve these goals. Indeed the mesoporous silicon layer significantly increases the effective area of the silicon-nickel interface and improves both mechanical and electrical properties of the metal/silicon structure. This opens possibility to tune the adhesion and contact resistance of thin nickel films on silicon through easy procedures, such as anodization of silicon and electrodeposition of nickel.

The mechanisms of nickel deposition onto porous silicon are deeply investigated in the past [130–133]. The most relevant concern for this work is that filling of mesoporous silicon by nickel reaches only 67 % using galvanostatic electrodeposition regime [133], while in this work a complete filling of porous silicon layer to ensure adhesion is necessary. On the other hand nickel contacts on porous silicon layers are poorly reported in literature, not always useful for solar cell applications. For instance, Kanungo et al. [132] studied electroless nickel deposition on relatively thick 30  $\mu$ m nanoporous silicon layers, showing contact resistance of 17.6 m $\Omega \cdot cm^2$  without any silicide formation, but in that case the thickness of nanoporous silicon layer exceeds the actual constrain of very thin emitter layer that is of common use.

The contact resistance of the nickel-silicon interface depends on the silicon resistivity, the doping type and the surface condition. To obtain the lowest contact resistance, silicon dopant concentration should be higher than  $10^{19}$  cm<sup>-3</sup> [21]. Considering the doping profile of the typical solar cell emitter, as used in this work, reported in figure 6.03, it is evident that the doping profile region higher than  $10^{19}$  cm<sup>-3</sup> extends not less than 100 nm from the top surface, a contact resistances in the range between 1 and 100  $\mu\Omega$ ·cm<sup>2</sup> can be obtained according to Thibert et al. [134]. Moreover as-deposited nickel does not provide ohmic contact to silicon. A thermal annealing process is necessary to form a nickel-silicide layer able to provide low contact resistance with silicon. The thermal annealing temperature is critical for the stoichiometry of silicide compounds [135,136]. Among the three kinds of silicides that can be formed, SiNi is the one providing the lowest contact resistance on silicon and in order to form SiNi, annealing temperature should be chosen in the range between 400 and 700 °C. Even many publications speculate on the necessity of the precise temperature control, however, no specific study to which extents this is useful in application to solar cells is presented in the literature to our knowledge. Table 6.1 summarizes the most recent values of contact resistances of nickel-silicon contacts depending on emitter sheet resistances and thermal annealing regimes [127,135,137–139]. As it seen from Table 6.1, contact resistance values lower than 1 m $\Omega \cdot cm^2$  can be obtained on 5-100  $\Omega/sq$ emitters using annealing temperature range between 200 and 500 °C. This represents a relevant information since common industrial screen printed silver on silicon achieve at the best 1 m $\Omega$ ·cm<sup>2</sup> of contact resistance [21,42]. This means that electrical contacts suitable for the solar cell application can be obtained despite the nickel silicide stoichiometry. Nevertheless, often quite dissimilar electrical parameters of nickel-silicon contacts are reported in literature even if equal nickel silicide sintering regimes are used. That may be explained by interface defects between nickel and silicon, as already suggested by Mondon [124], which confirms the relevance of the nickel-silicon interface quality.

Emitter sheet resistance, $\Omega/sq$	Annealing regime	Contact resistance, $m\Omega \cdot cm^2$	Reference		
5	500 °C, 20-40 min	0.1	Klochko et al. [137]		
40	450 °C, 30 s	3.5	Boulord et al. [138]		
40	200 °C, 30 s 400 °C, 30 s 500 °C, 30 s	0.6 0.3 0.09	Boulord et al. [135]		
40-60	390 °C, 60 s 400 °C, 60 s 410 °C, 60 s 420 °C, 60 s 430 °C, 60 s	10.949 9.876 8.969 9.546 9.381	Chaudhari et al. [139]		
65	300 °C, 600 s 350 °C, 600 s 400 °C, 600 s 450 °C, 600 s	0.345 0.292 0.517 0.305			
100	300 °C, 600 s 350 °C, 600 s 400 °C, 600 s 450 °C, 600 s	0.941 1.564 2.042 1.723	Rauer et al. [127]		

Table 6.1. State-of-the-art of contact resistances of nickel-silicon contacts for solar cells and their dependence on emitters sheet resistances and silicide sintering regimes.

The key point to obtain both low contact resistance and high adhesion of nickel films on porous silicon is to achieve a complete filling of the pores with nickel. Such conditions can be obtained only using PRP technique, which provides more homogeneous filling of small pores. Moreover, only nickel films obtained by PRP on top of the proposed mesoporous silicon layer succeed to a qualitatively adhesive tape tests proving their higher adhesion properties. Comparative characterization of nickel films obtained by plating in galvanostatic (a), galvanodynamic (b) and PRP regimes (cd) is presented in figure 6.06. As it is evident from micrographs, only PRP technique at low current densities (figure 6.06c) results in a complete filling of the mesoporous silicon layer, while other regimes suffer of voids (figure 6.06a, 6.06b, 6.06d) between nickel and silicon.

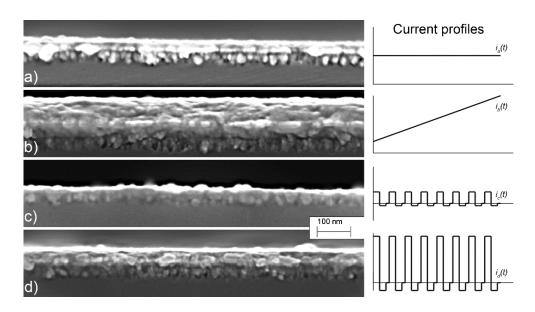


Figure 6.06. Cross-section SEM micrographs of nickel films deposited onto porous silicon layers at different plating regimes and their current profiles during the electrodeposition: a) current profile  $i_a(t)$  is constant (j=50 mA/cm<sup>2</sup>), b) current profile  $i_b(t)$  is linearly increased during the plating (from 50 to 500 mA/cm<sup>2</sup>), c) current profile  $i_c(t)$  corresponding to the PRP regime at low current densities ( $j_{dir}$ =20 mA/cm<sup>2</sup>,  $j_{rev}$ =4 mA/cm<sup>2</sup>), d) current profile  $i_d(t)$  corresponding to the PRP regime at high current densities ( $j_{dir}$ =100 mA/cm<sup>2</sup>,  $j_{rev}$ =20 mA/cm<sup>2</sup>).

## 6.4. Performance of proposed contacts

Formation process mesoporous silicon layers is investigated with different anodization regimes and electrolyte compositions. Mesoporous silicon layers formed by galvanodynamic regime, using electrolyte composition of 48 % HF, deionised water and isopropanol mixed in 1:1:1 ratio, show the greatest impact on the adhesion of the proposed metallization structure. Both galvanostatic and galvanodynamic anodization regimes are tested. Galvanostatic regimes (straight blocked pores) results in fragile contacts that never passed the qualitative adhesion tape test due to uncompleted filling of pores with nickel even using the PRP technique. Instead, galvanodynamic regime (tapering pores) shows greater stability due to better filling of pores with nickel. A 50×2 mm bus bars are formed using regimes for the mesoporous silicon layer formation, nickel and copper deposition described in this work. The characteristic loaddisplacement curve obtained by the peel test and the box plot showing the average result on 11 measurements are shown in figure 6.07. For a single test the peel force scatters during the delamination, however the peel force value can be considered as the average of the function of deformation in the range between 1.0 and 9.0 cm. The peel force for such bus bars is approximately 4.5 N/mm averaged over 11 measurements. The obtained result shows low spread (around 1 N/mm) and is higher than those already published in literature for nickel and copper plating based metallization techniques [124,140,141] and also higher than that commonly achieved using screen printed silver paste on n-type emitter layer of industrially manufactured solar cell (2 N/mm).

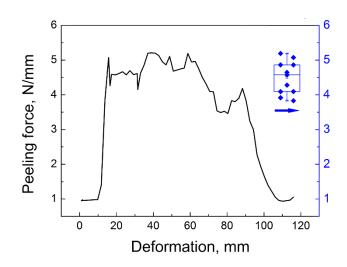


Figure 6.07. The peel force and the box plot showing the average result for each of 11 measurements of the bus bars formed on solar cells.

Figure 6.08 shows a micrograph of the nickel-copper stack obtained after mesoporous silicon layer formation by gradient current profile, nickel PRP, silicide sintering and subsequent copper plating processes. The cross-section cut reported in figure 6.08 is obtained using FIB technique. The obtained metal films are defects-free, in particular the nickel layer does not contain any microscopic defects or voids near nickel-silicon interface responsible for the silicide homogeneity [124].

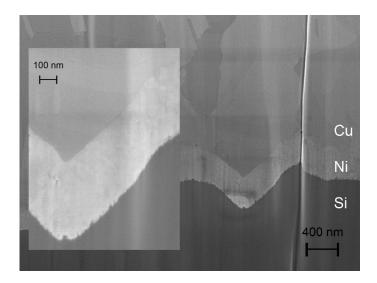


Figure 6.08. FIB cross-section micrograph of copper-nickel metallization stack obtained on the silicon solar cell with 70  $\Omega$ /sq emitter.

Figure 6.09 shows interfaces after delamination of plated metal films. In figure 6.09a delamination occurs at the interface between nickel and silicon due to wafer cleavage. Figure 6.09b shows silicon part in higher magnification. A uniform layer is observed, which is obtained after silicidation of the mesoporous silicon layer filled with nickel. The thickness of the silicide is higher than that of the initial mesoporous silicon layer, ensuring that the whole layer is converted into silicide. Figure 6.10 shows delamination after the peel test. The delamination occurs at the interface between nickel and copper films. It can be concluded that no damage of silicon surface happens due to mechanical stress in both cases, thus, the proposed metallization is suitable for the application to shallow emitter solar cells.

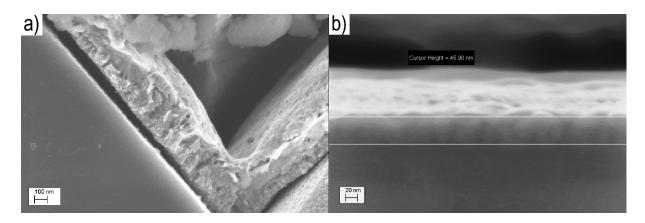


Figure 6.09. Cross section micrograph of copper-nickel metallization stack showing delamination of metal films obtained by wafer cleavage.

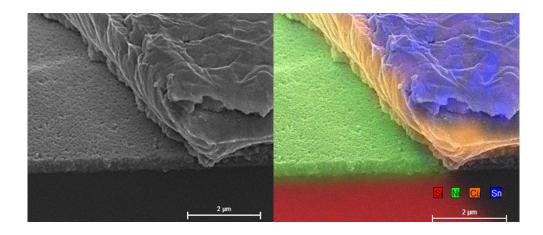


Figure 6.10. Cross-section micrograph of copper-nickel metallization stack showing delamination of metal films obtained by peel test.

In order to investigate the impact of the PS layer morphology on the contact resistance of the proposed metallization, three different PS formation regimes are tested together with plating regimes and resumed in Table 6.2. Only the right combination of the anodization in galvanodynamic regime, PRP (figure 6.06c), galvanostatic deposition and annealing at 350 °C results in low values of contact resistances as reported in Table 6.3 and figure 6.11. In this figure, considering that plating procedures are the same for the samples, it is evident a strong effect of the anodization regime on the contact resistance. For instance, the anodization regime 3 (see Table 6.2) results in the lowest contact resistance values ranging between 0.35 and 0.72 m $\Omega$ ·cm<sup>2</sup> (samples s5, s6, s10s12). The anodization regime 2 results in contact resistance values in the range between 0.61 and 1.65 m $\Omega$  cm<sup>2</sup> (samples s1, s2, s7) and the anodization regime 1 shows the worst performance of 4-7 m $\Omega$ ·cm<sup>2</sup> (samples s8 and s9) that is similar to the contact resistance values obtained without silicide formation (samples s3 and s4). It is clearly seen that the contact resistance error bars are higher for samples having higher values of the contact resistance. This is quite common for TLM methodology, considering the number of process parameters required for preparation of samples. Calculation of contact resistance using TLM requires linear approximation of number of measurements of resistances between number of contacts within a single sample [79]. If the sample is formed using non-optimized conditions, it results in a deviation of these multiple measurements that accumulate bigger errors. This means that error bars also indicate the reliability of selected process conditions. Considering the deviation of measurements in figure 6.11 for different anodization regimes, it can be noted that morphology of a mesoporous silicon layer is critical for the electrical performance of such metal contacts on silicon. And in this work, anodization regime 3 shows the most promising result. Thus, for all emitter diffusions between 70-90  $\Omega$ /sq contact resistance values in the range between  $0.35 \text{ m}\Omega \cdot \text{cm}^2$  and  $0.91 \text{ m}\Omega \cdot \text{cm}^2$  are obtained that are lower than that commonly used in the industrial manufacture of silver screen printed contacts [21,42] while comparable to values reported in literature for nickel and copper plating based metallization techniques [127,135,137,138]. Such contact resistance values are measured on porous silicon and metal junctions fabricated according the conditions reported in Table 6.2 and Table 6.3.

Table 6.2. Description of regimes for processes for samples preparation.

Treatments	Description
Anodization regime 1	electrolyte: $HF(48\%)$ :IP:H2O = 1:1:1 linear scan of the current density from 80 to 40 mA/cm <sup>2</sup> in 0.75 s
Anodization regime 2	electrolyte: $HF(48\%)$ :IP:H2O = 1:1:1 linear scan of the current density from 100 to 20 mA/cm <sup>2</sup> in 0.75 s
Anodization regime 3	electrolyte: HF(48%):IP:H2O = 1:1:1 linear scan of the current density from 120 to 25 mA/cm <sup>2</sup> in 0.75 s
Nickel PRP	Nickel sulfamate based electrolyte containing 0.5 wt. % of HF at 60 °C linear scan of $j_{dir}$ from 10 to 50 mA/cm <sup>2</sup> in $t_{dir} = 0.1$ s $j_{rev} = 10$ mA/cm <sup>2</sup> $t_{rev} = 0.1$ s $t_{off} = 0.05$ s total time 4 s, total number of periods 16
Nickel galvanostatic plating	Nickel sulfamate based electrolyte at 60 °C linear scan of the current density from 50 to 720 mA/cm <sup>2</sup> in 2 s
Copper galvanostatic plating	Copper sulfate based electrolyte at 50 °C constant current density 250 mA/cm <sup>2</sup> in 108 s

Table 6.3. Overview of process treatments of samples that are prepared during this work ( $\sqrt{\text{ process performed}}$ , × process not performed).

Samples	s1, s2	s3, s4	s5, s6	s7	s8, s9	s10, s11, s12
Sheet resistance, $\Omega/sq$	70	70	80	90	90	90
Anodization regime	2	3	3	2	1	3
Nickel PRP	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
Nickel galvanostatic plating	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$	$\checkmark$
Silicide sintering	$\checkmark$	×		$\checkmark$	$\checkmark$	$\checkmark$
Copper galvanostatic plating	$\checkmark$				$\checkmark$	$\checkmark$
Contact resistance, $m\Omega \cdot cm^2$	0.91 1.65	4.90 4.79	0.35 0.72	0.61	4.56 7.60	0.47 0.55 0.42

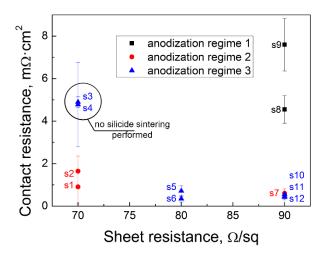
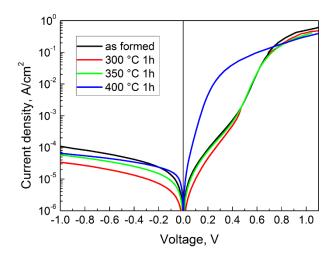


Figure 6.11. Specific contact resistances obtained for 70-90  $\Omega$ /sq emitters.

To verify the contact stability, thermal stress tests of samples with copper-nickelsilicon contacts are performed. According to the Arrhenius model [142] for a silicon solar cell, it is possible to estimate that 100 hours at 200 °C are equivalent to 1 hour at 350 °C. Bartsch et al. [143] evaluates that 100 hours at 200 °C are equivalent to more than 100 years of solar cell operation at standard conditions. Figure 6.12 shows the I-Vcurve of the sample s12 (see figure 6.11 and Table 6.3) measured after multiple thermal annealing steps. I-V measurements are performed in dark and room temperature conditions. After two steps of 1 hour thermal stress at 300 and 350 °C, a current density reduction is observed in both reverse and low forward bias conditions. Reduction of current is mainly attributed to continuous silicide sintering that occurs during annealing steps and improves the contact homogeneity. However, further 1 hour step of thermal stress at 400 °C strongly affects the p-n junction. Indeed the current density reduces in high injection regime and enhances in low forward and reverse bias conditions that indicate the formation of a recombination region at interfaces. This effect can be explained by copper atoms diffusion towards the junction where they form a strong recombination region that usually behaves as the double anti-series diode. Nonetheless, the stability of I-V characteristics after the two thermal annealing processes at 300 and 350 °C can be considered as a proof of the long-term stability performance of the coppernickel contact on silicon thin emitter layer for solar cell applications.



# Figure 6.12. *I-V* characteristics of n-p silicon junction measured after each subsequent thermal annealing stress of a sample processed with optimized metallization procedures. Thermal annealing tests are performed at 300 °C (red), 350 °C (green), 400 °C (blue) consequently for 1 h each. The black curve refers to as formed cell sample.

It is to remark that the proposed metallization technology does not affect the junction and the absorber material quality, as from data reported in figure 6.12, in turn it influences the series resistance of the solar cell in terms of contact resistance and the metal conductivity. Considering that the proposed metal contact formation process demonstrate lower contact resistance and higher adhesion with respect to the industrial state of the art and also stability, the conversion efficiencies of silicon based solar cell will definitively benefit of this kind metal contacts. To manufacture a complete solar cell, several technical issues of uniformity of anodization and light-induced plating processes has to be solved. Considering number of process variables in this work, multivariate experimental approach able to statistically and quantitatively study the effect of different process variables and their interactions on the solar cell parameters [144,145] is scheduled for future works, in order to find the best experimental conditions for solar cells with the proposed metallization configuration.

### 6.5. Summary to the Chapter 6

In this work, two layers of nickel and copper as front metallization for silicon solar cells is presented. It is well known that silicide sintering promotes both conductivity and adhesion. Considering the actual state of the art, the uniformity of silicon-nickel interface is the main reason of mechanical and electrical properties of plated contacts, which depends both on defects in the plated nickel films and on the accumulation of Kirkendall voids at the silicide-nickel interface attributed to unbalanced diffusion velocities of nickel and silicon into each other. Suitable conditions to form uniform silicon-nickel interfaces are found. In particular, it is demonstrated that a thickness of about 30 nm of mesoporous silicon layer allows metal anchoring to silicon, promoting metal adhesion and improving distribution of phases throughout the large area contact between nickel and silicon ensuring homogenous silicide formation. Low contact resistance and good adhesion of nickel films on porous silicon are achieved through optimization of mesoporous silicon layer structure and complete filling of pores with nickel and silicide sintering. To this aim, the mesoporous silicon layer formation and the nickel electrodeposition regimes are optimized.

Since porous silicon properties depend on the anodization parameters, different anodization regimes and electrolyte compositions are investigated. It is shown that the morphology of mesoporous silicon layers is similar among solar cells featured with 70-90  $\Omega$ /sq emitter layers, since the doping profile of these samples is approximately equal for a depths not exceeding 100 nm.

Using adhesive tape tests it is found that partial filling of pores in mesoporous silicon layer leads to poor mechanical stability of the entire metallization stack. Only the right combination of the anodization in galvanodynamic regime, PRP, galvanostatic deposition, and thermal annealing at 350 °C results in low contact resistance and good adhesion. For all the emitters in the range between 70 and 90  $\Omega$ /sq contact resistance values ranging from 350  $\mu\Omega \cdot cm^2$  to 910  $\mu\Omega \cdot cm^2$  are obtained that are lower than that commonly used in the industrial screen printed silver contacts on silicon, while comparable to those already reported in literature for nickel and copper plating based metallization techniques. Adhesion test of a bus bar formed on the emitter of solar cell using proposed approach shows an average peel force value of 4.5 N/mm that is definitively higher than the value required in solar cell application. Finally, thermal annealing stress tests demonstrate long-term stability of proposed configuration of the electrodeposited electrical contacts for solar cells consisting of copper conductive layer, nickel barrier layer, and mesoporous silicon layer as adhesion promoter. Therefore it may be concluded that a metallization technique suitable to replace silver in solar cell is now optimized and ready for solar cell application.

# Conclusion

This Ph.D. work is focused on the development and optimization of front and rear side metallization of industrial silicon solar cells. The commonly adopted screenprinted silver metallization has several well-known issues, such as low contact resistance, moderate bulk conductivity and high cost. The approach of this work allows complete silver replacement, both on the front and the rear sides. The development of such a new technology is divided into three parts, each resulting in appropriate feedback in terms of solar cell operation parameters.

The first part is the study of aluminum-silicon interdiffusion mechanism that occurs during the firing process of screen-printed aluminum layer required for the formation of the conventional rear metallization. This process is very important because it affects solar cell operation and performance through Al-BSF passivation. In this study different screen-printing aluminum pastes, differing one from each other by aluminum particle dimensions and glass frit composition, are evaluated in terms of their bulk resistivity, contact resistance to silicon, Al-BSF profile depth and solar cell performance. Finally, this study allowed to reveal certain dependences between pastes parameters and their effect on solar cells and to develop useful recommendations for better solar cell performance. It was found that the mechanism of the silicon dispersion within aluminum screen-printed layers strongly related to initial dimensions of aluminum particle.

Initially aluminum spherical particles are free of silicon content. As temperature arises, phase transformation begins, as well as interdiffusion. At the liquid state, melted aluminum experiences volume expansion that is kept by the aluminum oxide, thus, creating the internal pressure inside the aluminum particle. This internal pressure should cause radial strain, which is however balanced by the oxide shell and can be expressed in terms of surface tension. It was calculated that the majority of aluminum particles experience very huge radial strain that should lead to particle explosion, which in real situation is not observed. SEM and EDX investigations, as well as the literature data, allowed to establish a stress-relief mechanism, helpful in the explanation of the effect of aluminum paste composition on solar cell parameters gained after the process of aluminum paste firing. It was calculated that smaller particles experience higher pressure and tend to start the stress-relief mechanism before bigger ones. It was confirmed by the experiment, and one an interesting effect was observed for aluminum pastes having smaller particles. These smaller particles induced higher concentration of the liquid aluminum near the interface with silicon, promoting aluminum diffusion process and, therefore, the Al-BSF depth and solar cell  $V_{OC}$ .

As well as aluminum diffuses in silicon, silicon diffuses in aluminum. Microstructural investigation showed that silicon diffusion process is also affected by particle dimensions. Due to lower pressure in bigger particles, and the fact that diffusion coefficient is inversely proportional to the pressure, it was observed that bigger particles getter bigger amount of silicon. This gettering effect allowed to describe a selective collection of silicon content inside bigger aluminum spheres during aluminum paste firing, helpful to reduce overall bulk resistivity of the aluminum paste, that positively influences the efficiency of a solar cell. One possible feedback of this research is that considering these relations between aluminum paste compositions, one is able to design optimized composition of aluminum paste having lowered laydown, keeping solar cell performance improved at the same time.

Finally, the conducted microstructural investigation allowed to understand the composition of a fired screen-printed aluminum layer, that consists of aluminum spherical particles having silicon precipitate and passivated with aluminum oxide shell. Both silicon and aluminum oxide phases represent an issue for direct electrical contact to such an aluminum layer.

This issue is solved through development of special electrochemical treatment technique, which is actually **the second part** of this Ph.D. work, which is dedicated to the development of **a new rear metallization technique for solar cells**. The technology supposes localized formation of solder pads using electrodeposition of metals directly inside fired screen-printed aluminum layer of a solar cell. Localized electrodeposition is achieved using DLD/DLM technique that allows any kind of wet surface treatment in specific defined positions. This approach allows to avoid any photolithography use, limiting the cost of the process mainly to the cost of materials. In this work, electroplated nickel-tin solder pads are proposed, which cost significantly lower to a silver counterpart that is currently adopted by the industry. The cost reduction is not a single advantage of the proposed technology. Since electroplated solder pads can be deposited directly inside screen-printed aluminum layer, uniform Al-BSF performance can be provided for solar cells, which results in up to 0.5 %<sub>abs</sub> efficiency gain respect to current screen-printed silver technology.

Among the metals studied in this work are tin, nickel and copper. Deposition of these metals is investigated in present study. It was found that the highest adhesion of metals is achieved only using several pre-treatment procedures of the aluminum layer before the electrodeposition step. Such pre-treatments are studied and optimized in this work. As a result, two types of rapid anodization pre-treatments in fluoride- and alkaline-based electrolytes are able to guarantee superior stability and extreme adhesion of the proposed metallization technology.

It was found that the solder pads made of tin only demonstrate poor adhesion. Nickel-tin solder pads, showed much greater mechanical performance: adhesion tests reported the peeling strength in the range from 2.5 N/mm to 5.0 N/mm. Copper-tin solder pads despite a great mechanical performance demonstrated moderate electrical parameters. Moreover, it was found process incompatibility of copper electroplating, at least from acidic solutions, to an aluminum layer due to very fast degradation of copper-containing electrolyte.

The third part of the work is the development of a new front side metallization technology based on nickel and copper electroplating. It is well known that silicide sintering promotes both conductivity and adhesion. Considering the actual state of the art, the uniformity of silicon-nickel interface is the main reason of mechanical and electrical properties of plated contacts, which depends both on defects in the plated nickel films. Suitable conditions to form uniform silicon-nickel interfaces are found. In particular, it is demonstrated that introduction of a 30 nm thick mesoporous silicon layer (which one of the main innovation of this work) allows metal anchoring to silicon, promoting metal adhesion and improving distribution of phases throughout the large area contact between nickel and silicon ensuring homogenous silicide formation. Low contact resistance and good adhesion of nickel films on porous silicon are achieved through optimization of mesoporous silicon layer structure and complete filling of pores with nickel and silicide sintering. To this aim, the mesoporous silicon layer formation and the nickel electrodeposition regimes are optimized.

Using adhesive tape tests it was found that partial filling of pores in mesoporous silicon layer leads to poor mechanical stability of the entire metallization stack. Only the right combination of the anodization in galvanodynamic regime, PRP, galvanostatic deposition, and thermal annealing at 350 °C results in low contact resistance and good adhesion. For all the emitters in the range between 70 and 90  $\Omega$ /sq contact resistance values ranging from 350  $\mu\Omega \cdot cm^2$  to 910  $\mu\Omega \cdot cm^2$  are obtained that are lower than that commonly used in the industrial screen printed silver contacts on silicon, while comparable to those already reported in literature for nickel and copper plating based metallization techniques. Adhesion test of a bus bar formed on the emitter of solar cell using proposed approach shows an average peel force value of 4.5 N/mm that is definitively higher than the value required in solar cell application. Finally, thermal annealing stress tests demonstrate long-term stability of proposed configuration of the electrodeposited electrical contacts for solar cells consisting of copper conductive layer, nickel barrier layer, and mesoporous silicon layer as adhesion promoter. Therefore it may be concluded that a metallization technique suitable to replace silver in solar cell is now optimized and ready for solar cell application.

As for combination of **all the parts** of the present research, together, they result in complete silver removal from a metallization technology of a solar cell with a feasible efficiency enhancement of up to  $1 \%_{abs}$ .

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- K. Kholostov, L. Serenelli, M. Izzi, M. Tucci, D. Bernardi, M. Balucani, Electroplated nickel-tin solder pads for rear metallization of solar cells, Mater. Sci. Eng. B. in press (2015).
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