Hybrid Three-Phase Transformer-Based Multilevel Inverter With Reduced Component Count

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ABSTRACT This paper proposes a novel three-phase transformer-based multilevel inverter (MLI) topology to maximize the output voltage levels for high-power high-voltage applications while reducing component counts as compared to its transformer-based counterparts. The proposed hybrid topology is formed by connecting a three-level T-type module with full H-bridge cells through single-phase transformers. The T-type module is fixed while the full H-bridge cell can be repeated for enlarging the output voltage levels without increasing the voltage stress on switches. Key features of the proposed topology include low part count, capacitor-free, diode-free, voltage boosting, simple control, and modularity. Within the framework, a simple low-frequency pulse width modulation (LFPWM) switching scheme is used to control the output voltage, and the working principle is detailed for seven-, nine-, and N-level operation. The operability and performance of the proposed topology are numerically verified and experimentally validated at different loads. Moreover, its conversion efficiency is experimentally examined. Finally, a comparative study with existing transformer-based MLI circuits is conducted to prove its key merits.

INDEX TERMS Cascaded-transformer multilevel inverter (CTMI), DC-AC converter, hybrid multilevel inverter (MLI), multilevel inverter topology.

I. INTRODUCTION

Multilevel inverters (MLIs) concept has become a mature technology, being deployed in medium- and high-power DC-AC conversions. The MLIs have gained popularity due to their unique merits of producing high voltages at high quality, namely low THD value, low dv/dt, low electromagnetic interference (EMI), high conversion efficiency, voltage scalability, and reliability while using low-voltage semiconductor devices and low switching frequency [1]–[5]. The conventional MLIs include three topologies, being known as cascaded H-bridge (CHB) [6], neutral point clamped (NPC) [7], [8], and flying capacitor (FC) [9], [10]. The CHB, NPC, and FC MLIs can produce output voltages with N levels, requiring huge counts of DC sources, clamping diodes, and capacitors, respectively. For example, producing nine-level

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three-phase voltages requires 48 switches, twelve DC sources in CHB inverters, 168 clamping diodes in NPC inverters, and 92 capacitors in FC inverters, increasing inverter size, cost, losses, failure rate, and complexity. As argued in [11], increasing the number of voltage levels is a desirable necessity to enhance the MLI performance. Therefore, many MLIs are intensively developed to increase the output voltage levels with reduced component counts [11]–[22]. Among them, transformer-based MLIs have received great attention with key features of reducing DC source count and maximizing the output voltage [18]–[22]. Their structure, merits and demerits are briefly discussed hereafter.

The cascaded-transformer multilevel inverter (CTMI) in [18] comprises two stages: voltage generator stage (VGS) and polarity changer stage (PCS). Half-bridge modules are the building block in the VGS, thus adding more half-bridge modules enlarges the voltage level count. The PCS employs full H-bridges to bipolarize the generated unipolar multilevel

voltages from the VGS stage. Producing three-phase voltages requires three single-phase transformers to couple the PCS outputs with the load. This CTMI requires three power transformers, $3N + 9$ switches, and $0.5N$-0.5 DC voltage sources for generating N voltage levels. It can eliminate flying capacitors, clamping diodes and reduce the DC source count as compared to FC, NPC, and CHB inverters, respectively. However, using three H-bridge cells to produce bipolar voltages is a conspicuous drawback because of linking the switch blocking voltage to the output voltage level count. For example, the total standing voltage of PCS switches is $6V_{DC}(N - 1)$, where V_{DC} is the voltage rating of each DC source in the DC-link, limiting the modularity of this CTMI and other associated features such as THD and dv/dt.

To tackle the drawbacks of the CTMI in [18], a hybrid nine-level inverter (H9LI) is proposed in [19], which can produce bipolar voltages without a polarity changer with a lower part count. It employs twenty-four switches, nine capacitors, six power diodes, one DC source, and three single-phase transformers. It saves twelve switches and three DC sources as compared to the CTMI when producing nine-level voltages. However, the reduction of DC sources and switches requires higher numbers of power diodes and capacitors, decreasing the inverter efficiency, reliability, and life span. Further, during startup, the H9LI requires pre-charging circuits for three capacitors, as suggested by the authors in [19].

To reduce or eliminate capacitors in the H9LI, two transformer-based topologies were presented in [21], [22]. The modified active-neutral point-clamped (MANPC) topology in [21] uses thirty switches, five capacitors, three single-phase transformers, and one DC source to produce nine voltage levels. The MANPC topology has a lower part count than H9LI in [19]. Both circuits use the same count of transformers and DC sources, but MANPC topology eliminates the six power diodes in H9LI. Further, it uses only five capacitors instead of nine in H9LI, simplifying control algorithms and improving inverter reliability. However, using additional six switches is a disadvantage of the MANPC as compared to the H9LI. A transformer-based cascaded H-bridge (TB-CHB) topology in [22] can reduce the switch count to only twenty-four, being the same switch count as H9LI, and lower than MANPC by six switches. Furthermore, it can remove all capacitors in MANPC and H9LI inverters. For constructing each inverter leg in the TB-CHB topology, several full H-bridge cells sharing a single DC-link are cascaded through single-phase transformers. For a nine-level operation, it requires one DC source, twenty-four switches, and six single-phase transformers. Modularity, capacitor-free, diode-free, and reduced switch count are its key merits. However, using six transformers is the main drawback, increasing the size and cost of the inverter.

To address the disadvantages of the aforementioned transformer-based inverters, namely high counts of DC sources in CTMI [18], power diodes and capacitors in H9LI [19], switches in MANPC [21], or transformers in TB-CHB [22], this study proposes a novel three-phase

transformer-based MLI topology, which can reduce the total part count while preserving the key features of being capacitors-, diode-free, and low counts of DC sources, switches, and transformers. Further, the proposed circuit allows for increasing the voltage level count without increasing the voltage stress across the switches, being a good option for high-power high-voltage applications. This MLI topology is proposed as part of work carried out for the research in [23]. Section II details the working principle, symmetrical and asymmetrical operation modes, generalized configuration of the proposed topology, and suggests its applications. A switching modulation scheme based on low-frequency pulse width modulation (LFPWM) is given in Section III. Section IV presents and discusses the simulation and experimental verification of the proposed inverter. A comparative assessment between the proposed topology and recently developed transformer-based inverters is drawn in Section V. Finally, Section VI concludes the finding of this paper.

II. PROPOSED TRANSFORMER-BASED MLI TOPOLOGY
A. CIRCUIT CONFIGURATION
The circuit configuration of the proposed transformer-based inverter is shown in Fig. 1. It is a hybrid three-phase topology, being formed by connecting three T-type legs to three H-bridge inverters through three single-phase transformers. The proposed topology consists of two DC sources (E_1 and E_2), three transformers (T_A, T_B, and T_C), and twenty-four switches (S_1-S_{24}). The twenty-four switches are used to implement eighteen unidirectional switches and three bidirectional switches. The proposed topology does not require any clamping diodes or flying capacitors in its operation. It can produce different voltage level counts N, according to the selected transformer turns ratio β. For example, it produces seven voltage levels and nine voltage levels when selecting β to be 1 and 1.5, respectively. The proposed topology configuration keeps the maximum blocking voltage of the switches either below or equal to E, where E is the input DC-link voltage. The switches S_3, S_4, S_{11}, S_{12}, S_{19}, and S_{20} have a voltage stress of $0.5E$. Alternatively, the switches S_1, S_2, S_5-S_{10}, S_{13}-S_{18}, and S_{21}-S_{24} withstand a voltage stress of E.

B. OPERATING CONCEPT
The operating concept can be explained based on the pole voltage generation. The pole voltages are the voltage differences between the three load points (A, B, and C) and the reference point 0, being labelled as V_{A0}, V_{B0}, and V_{C0}, respectively. Considering V_{A0} as an example, it is synthesized by adding two voltage components: V_0 and V_1, as shown in (1) and Fig. 2. The V_0 is the voltage between the midpoint of the T-type leg and the reference point 0, and V_1 is the secondary voltage of transformer T_A. Both two voltage components can have three different voltage levels, V_0 has $0.5E$, 0, and $-0.5E$, and V_1 has three levels of βE, 0, and $-\beta E$.
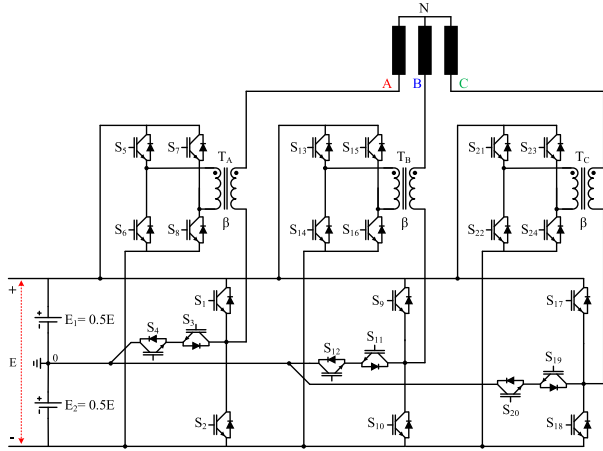
$$V_{A0} = V_0 + V_1 \qquad (1)$$

FIGURE 1. The circuit configuration of the proposed transformer based MLI topology.
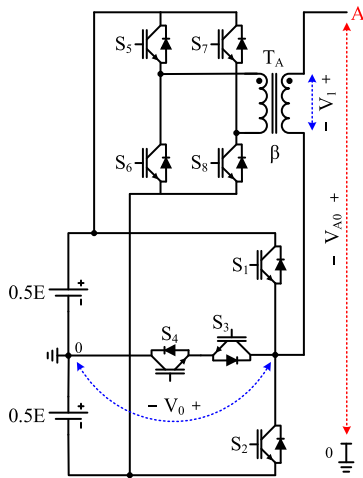

FIGURE 2. Synthesising of the pole voltage V_{A0} in the proposed topology.

The transformer turns ratio β can have different values: A) Case A, $\beta = 1$, producing three voltage levels of E, 0, and $-E$ in the voltage component V_1. B) Case B, $\beta = 1.5$, producing three voltage levels of $1.5E$, 0, and $-1.5E$ in V_1. Although both cases keep producing the same number of voltage levels, the maximum reachable voltage in the case B is higher than that in the case A. Accordingly, the pole voltage can have different voltage level counts: seven levels in the case A (i.e., $1.5E$, E, $0.5E$, 0, $-0.5E$, $-E$, and $-1.5E$) and nine levels for the case B (i.e., $2E$, $1.5E$, E, $0.5E$, 0, $-0.5E$, $-E$, $-1.5E$, and $-2E$).

Fig. 3 shows seven different operating modes of the proposed topology to produce seven voltage levels in the pole voltage V_{A0} when β is equal to 1. For instance, in Fig. 3 (a), mode I describes the required ON/OFF switches for producing $1.5E$ in V_{A0}, in which the switches S_1, S_4, S_5, and S_8 must be ON while S_2, S_3, S_6, and S_7 are OFF. The remaining six voltage levels can be achieved by following the operating modes II to VII, as shown in Figs. 3(b) to (g), respectively. It is worth noting that the mentioned operating modes are selected to produce the targeted voltage level without causing

a short-circuit across the input DC sources. Therefore, some combination of switches cannot be set ON. For example, in phase leg A, the following combinations are not used in the modulation control of the proposed topology: (S_1, S_2), (S_1, S_3, S_4), (S_2, S_3, S_4), (S_5, S_6), and (S_7, S_8).

C. N-LEVEL CONFIGURATION

The proposed topology can be extended to produce N voltage levels by adding more H-bridge cells in each phase leg, being connected through transformers, as shown in Fig. 4. The blocking voltage of the switches is not a function of the voltage levels count, so increasing the voltage level count does not increase the voltage stress across the switches. All H-bridge cells contribute to the pole voltage. For example, the pole voltage V_{A0} is synthesised by adding all the cell voltages V_1, $V_2, \ldots$, and V_n to the base voltage V_0 as expressed in (2).

$$V_{A0} = V_0 + \sum_{i=1}^{n} V_i \quad (2)$$

The N-level configuration of the proposed inverter generates different voltage level counts according to the transformer turn ratio β while keeping the same component count. The generalized configuration has three cases, depending on β: A) symmetrical turns ratio (where $\beta_1 = \beta_2 = \ldots = \beta_n = 1$), B) asymmetrical binary turns ratio (where β_1, β_2, $\beta_3, \ldots$ are 1, 2, 4, $\ldots$), C) asymmetrical ternary turns ratio (where β_1, β_2, $\beta_3, \ldots$ are 1.5, 4.5, 13.5, $\ldots$). The relationships between the transformer count N_{Trf}, switch count N_{SW}, and the voltage level count N are presented in (3-4), (5-6), and (7-8), for symmetrical, binary asymmetrical, and ternary asymmetrical turn ratios, respectively. For example, using six transformers (two per phase leg) produces eleven, fifteen, twenty-seven voltage levels in the pole voltage for symmetrical, binary asymmetrical, ternary asymmetrical turn ratios, respectively. The component counts in (3)-(8) represent the total count in the three legs.

1) SYMMETRICAL RATIOS: $\beta_1 = \beta_2 = \ldots = \beta_n = 1$

$$\underbrace{N = \frac{4N_{Trf}}{3} + 3}_{N_{Trf}=0,3,6,9,12,\cdots} \quad (3)$$

$$\underbrace{\left. \begin{aligned} N_{SW} &= 3N + 3 \\ N_{Trf} &= \frac{3N - 9}{4} \end{aligned} \right\}}_{N=0,3,6,9,12,\cdots} \quad (4)$$
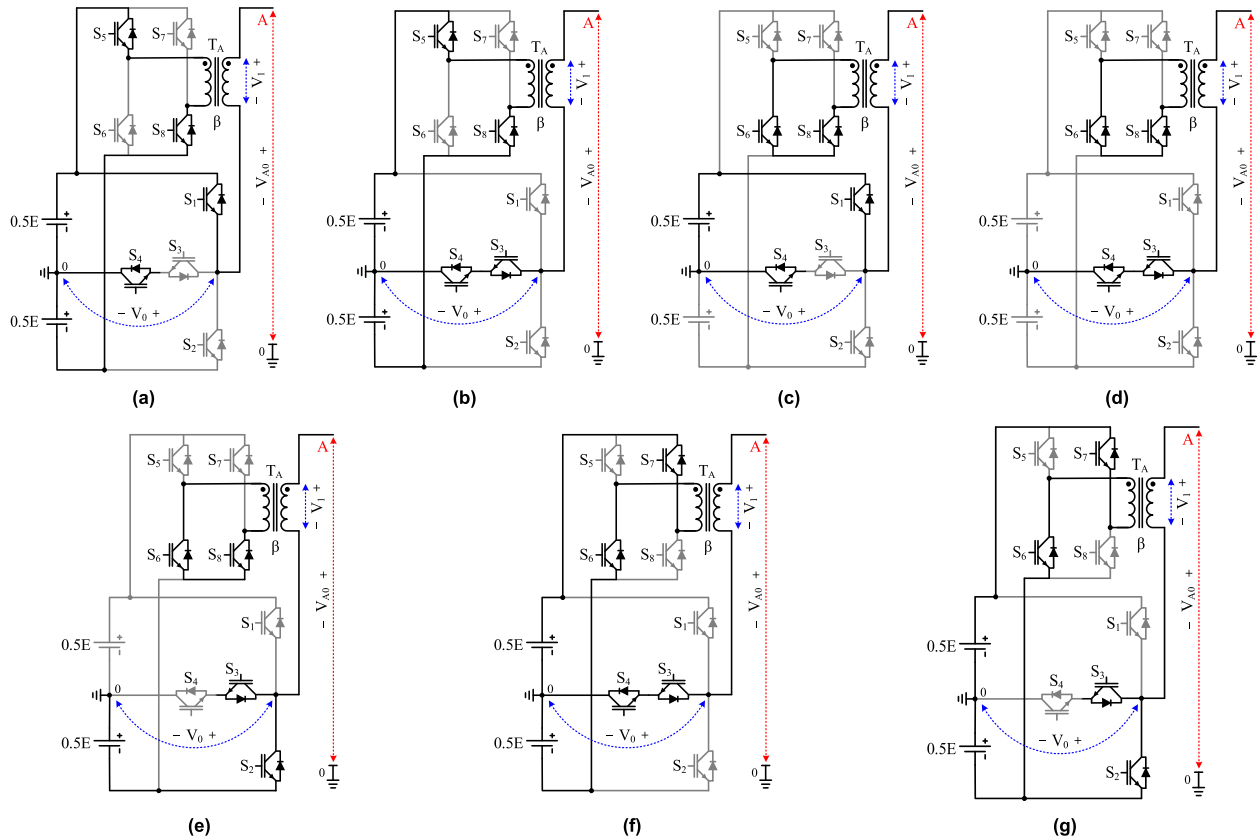
2) ASYMMETRICAL BINARY RATIOS: $\beta_1, \beta_2, \beta_3, \ldots$ ARE 1, 2, 4, $\ldots$

$$\underbrace{N = 2^{\frac{N_{Trf}}{3}+2} - 1}_{N_{Trf}=0,3,6,9,12,\cdots} \quad (5)$$

$$\underbrace{\left. \begin{aligned} N_{SW} &= 12 \left(\frac{\ln(N+1)}{\ln(2)} - 1 \right) \\ N_{Trf} &= 3 \left(\frac{\ln(N+1)}{\ln(2)} - 2 \right) \end{aligned} \right\}}_{N=3,7,15,31,63,127,\cdots} \quad (6)$$

FIGURE 3. Operating modes of the proposed topology when β is 1. (a) Mode I: $V_{A0} = 1.5E$. (b) Mode II: $V_{A0} = E$. (c) Mode III: $V_{A0} = 0.5E$. (d) Mode IV: $V_{A0} = 0$. (e) Mode V: $V_{A0} = -0.5E$. (f) Mode VI: $V_{A0} = -E$. (g) Mode VII: $V_{A0} = -1.5E$.

3) ASYMMETRICAL TERNARY RATIOS: $\beta_1, \beta_2, \beta_3, \ldots$ ARE 1.5, 4.5, 13.5, ...

$$\underbrace{N = 3\left(3^{\frac{N_{Trf}}{3}}\right)}_{N_{Trf}=0,3,6,9,12,15,\cdots} \tag{7}$$

$$\underbrace{\left.\begin{array}{l} N_{SW} = 12\left(\left[\ln\left(\dfrac{N}{3}\right)\Big/\ln(3)\right]+1\right) \\[3mm] N_{Trf} = 3\left(\left[\ln\left(\dfrac{N}{3}\right)\Big/\ln(3)\right]\right) \end{array}\right\}}_{N=3,9,27,81,243,729,\cdots} \tag{8}$$

The H-bridge cells can enlarge the output voltage level count and the output power without increasing the switches blocking voltage. Therefore, from application point of view, the proposed circuit is best suitable for high-power high-voltage applications, in which the component count and inverter footprint are more important than the isolation feature. Other recommended applications for the proposed topology are in constant-frequency applications, including dynamic voltage restorers (DVR), uninterruptible power supplies (UPS), etc. To avoid transformer saturation, like in other transformer-based MLIs, the proposed topology is not suitable for applications where a wide range of frequencies is required, such as motor drives with wide speed ranges.

III. MODULATION STRATEGY

The low-frequency pulse width modulation (LFPWM) scheme is selected to control the proposed topology output voltage due to its simplicity. However, other modulation schemes can be used as well, and selecting the best modulation is outside the scope of this study. Table 1 lists the switching states when β is 1, generating seven voltage levels in the pole voltage. Alternatively, nine voltage levels are generated when β is 1.5, as described in Table 2. The LFPWM scheme is based on these two tables. Moreover, Tables 1 and 2 list the switching states of leg-A switches (S_1-S_8) and the corresponding output voltages V_0, V_1, and V_{A0}.

Fig. 5 shows the generation of the switching signals for the leg-A switches when β is 1. To produce the seven-level pole voltage as shown in the last trace of Fig. 5, a sinusoidal reference signal V_{refA} and six offset signals ($\pm R_1$, $\pm R_2$, and $\pm R_3$) are required. The reference signal can be varied from 0 to the maximum of V_P, while the offset signals can be expressed as in (9) [16].

$$\left.\begin{array}{l} \pm R_1 = V_p \sin(\theta_1) \\ \pm R_2 = V_p \sin(\theta_2) \\ \pm R_3 = V_p \sin(\theta_3) \end{array}\right\} \tag{9}$$

where θ_1-θ_3 are the transition angles between voltage levels as marked in the pole voltage waveform in Fig. 5.
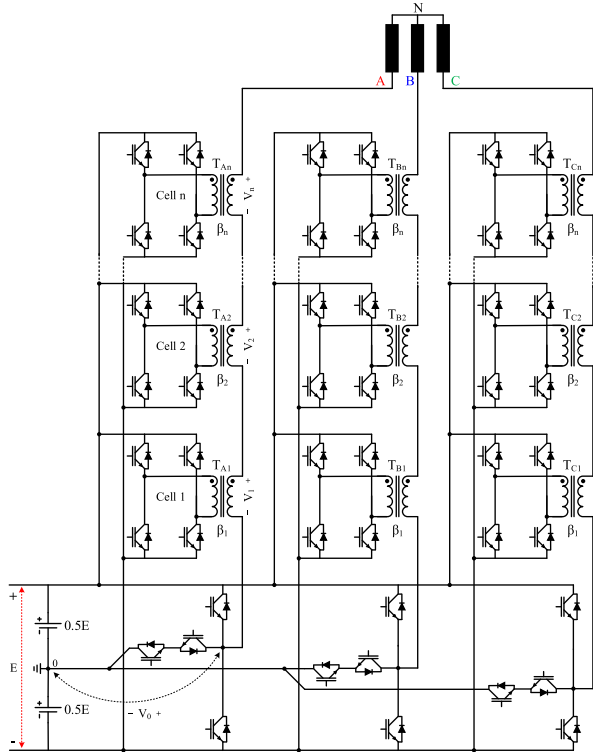
FIGURE 4. The *N*-level configuration of the proposed transformer-based MLI topology.

TABLE 1. Output voltages and the corresponding switching states when B is 1: leg A.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0	V_1	V_{A0}
1	0	0	1	1	0	0	1	0.5E	E	1.5E
0	0	1	1	1	0	0	1	0	E	E
1	0	0	1	0	1	0	1	0.5E	0	0.5E
1	0	0	1	1	0	1	0	0.5E	0	0.5E
0	1	1	0	1	0	0	1	-0.5E	E	0.5E
0	0	1	1	1	0	1	0	0	0	0
0	0	1	1	0	1	0	1	0	0	0
0	1	1	0	0	1	0	1	-0.5E	0	-0.5E
0	1	1	0	1	0	1	0	-0.5E	0	-0.5E
1	0	0	1	0	1	1	0	0.5E	-E	-0.5E
0	0	1	1	0	1	1	0	0	-E	- E
0	0	1	0	0	1	1	0	-0.5E	-E	-1.5E

1=ON, 0=OFF

These transition angles can be calculated using (10) [16]. Further, equation (10) can be used for computing the transition angles of any number of voltage level produced by the *N*-level configuration in Fig. 4. In other words, Fig. 5 can be extended for producing the required switching pulses for *N* voltage levels by using (10) to determine $N-1$ offset signals ($\pm R_1, \pm R_2, \pm R_3, \ldots$ and $\pm R_{(N-1)/2}$).

$$\left. \begin{array}{l} \theta_m = \sin^{-1}\left(\dfrac{2m-1}{N}\right) \\[2mm] m = 1, 2, \ldots, \dfrac{N-1}{2}, \\[2mm] 0 \leq \theta_m \leq \dfrac{\pi}{2} \end{array} \right\} \qquad (10)$$
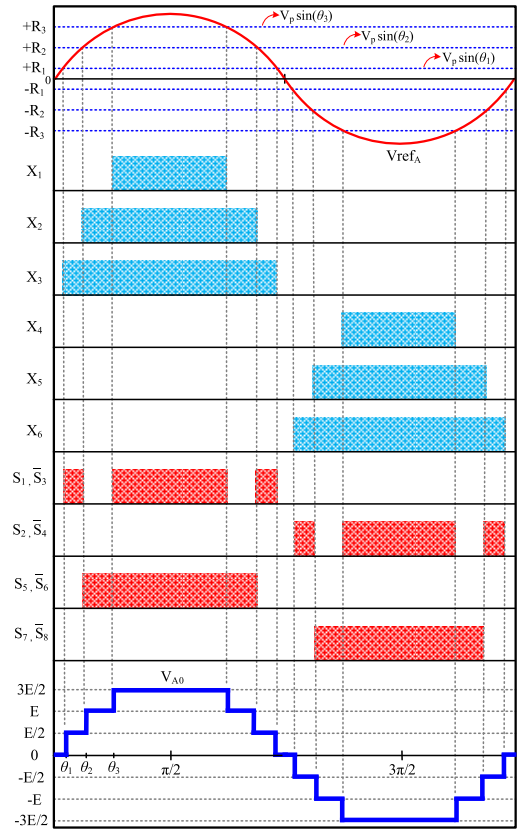

FIGURE 5. Switching signals generation and the leg-A pole voltage V_{A0} when producing seven voltage levels at β of 1.
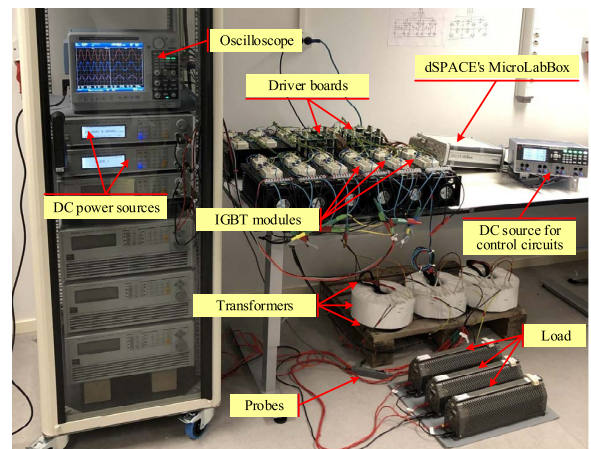

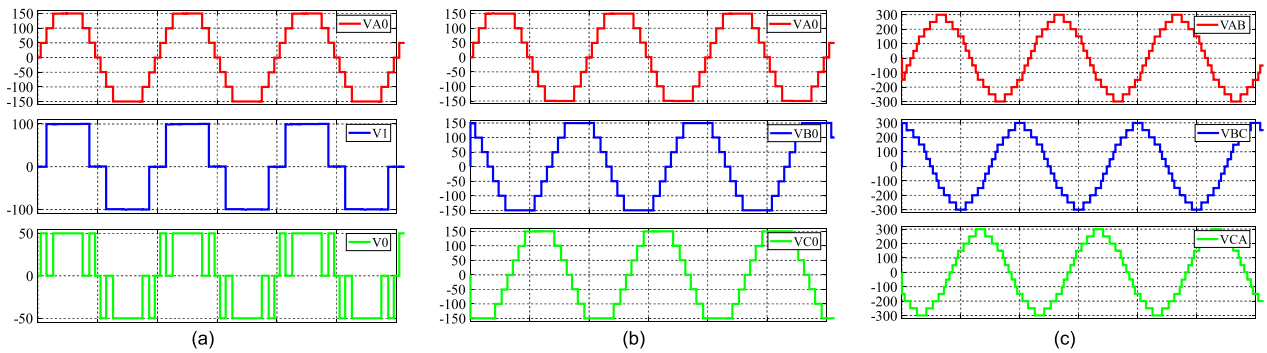**FIGURE 6.** Experimental setup of the proposed topology.

Six primary signals (X_1-X_6) are derived when comparing the reference signal V_{refA} with six offset signals. These six primary signals are the inputs for the Boolean operators in (11)-(14), being used to achieve the switching states in Table 1.

$$S_1, \overline{S_3} = X_1 + (\overline{X_2} \times X_3) \qquad (11)$$
$$S_2, \overline{S_4} = X_4 + (\overline{X_5} \times X_6) \qquad (12)$$
$$S_5, \overline{S_6} = X_2 \qquad (13)$$
$$S_7, \overline{S_8} = X_5 \qquad (14)$$

FIGURE 7. Simulation waveforms of the proposed topology when β is 1. (a) pole voltage V_{A0} synthesizing. (b) pole voltages V_{A0}, V_{B0}, and V_{C0}. (c) line voltages V_{AB}, V_{BC}, and V_{CA}.

TABLE 2. Output voltages and the corresponding switching states when B is 1.5: leg A.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0	V_1	V_{A0}
1	0	0	1	1	0	0	1	0.5E	1.5E	2E
0	0	1	1	1	0	0	1	0	1.5E	1.5E
0	1	1	0	1	0	0	1	-0.5E	1.5E	E
1	0	0	1	1	0	1	0	0.5E	0	0.5E
1	0	0	1	0	1	0	1	0.5E	0	0.5E
0	0	1	1	0	1	0	1	0	0	0
0	1	1	0	0	1	0	1	-0.5E	0	-0.5E
0	1	1	0	1	0	1	0	-0.5E	0	-0.5E
1	0	0	1	0	1	1	0	0.5E	-1.5E	- E
0	0	1	1	0	1	1	0	0	-1.5E	-1.5E
0	1	1	0	0	1	1	0	-0.5E	-1.5E	-2E

1=ON, 0=OFF

TABLE 3. Experimental system specifications.

Description	Value	Unit
DC-link voltage (E)	100	V
Load resistor (R)	50	Ω
Load inductor (L)	100	mH
Output frequency (F_o)	50	Hz
Sampling frequency (F_S)	50	kHz
Number of transformers (N_{Trf})	3	–

voltage probes, digital oscilloscope (Yokogawa, DL850EV), resistive-inductive loads, and the inverter prototype. The inverter prototype is constructed using twenty-four IGBT modules (SEMIKRON, SKM300GA12E4) associated with gate-driver boards (SEMIKRON, SKHI 10/12 R).

A. SIMULATION RESULTS

The transformer turns ratio (β) affects the output voltage level count. The proposed inverter can produce seven and nine voltage levels at β of 1 and 1.5, respectively. Figs. 7-10 show the voltage waveforms of the proposed inverter when changing the turns ratio β from 1 to 1.5. Figs. 7(a) and 9(a) illustrate the synthesized pole voltage V_{A0}, being obtained by adding V_1 to V_0. Figs. 7(b) and 9(b) show the three pole voltages V_{A0}, V_{B0}, and V_{C0}. The output line voltages V_{AB}, V_{BC}, and V_{CA}, are presented in Figs. 7(c) and 9(c). Fig. 7(c) shows that the line voltages can have thirteen different voltage levels of 0, $\pm0.5E$, $\pm E$, $\pm1.5E$, $\pm2E$, $\pm2.5E$, and $\pm3E$ at β of 1. Alternatively, when β is 1.5, seventeen voltage levels of 0, $\pm0.5E$, $\pm E$, $\pm1.5E$, $\pm2E$, $\pm2.5E$, $\pm3E$, $\pm3.5E$, and $\pm4E$ are generated in the line voltages as depicted in Fig. 9(c). The depicted line voltages in Fig. 9(c) have better THD than those in Fig. 7(c) because of having a higher level count, the THD value is 7.14% instead of 8.52%. Further, Figs. 8(a) and 10(a) show the output waveforms when connecting a resistive load (R) of 50 Ω to the inverter outputs, where the line voltage V_{AB}, phase voltage V_{AN}, and load current I_{AN} appear in the first, second, and the third trace, respectively. Figs. 8(b) and 10(b) show the waveforms of V_{AB}, V_{AN}, and I_{AN} when feeding power to a resistive-inductive (R-L) load (R = 50 Ω and L = 100 mH).

The required switching signals for producing nine voltage levels in the pole voltages can be generated by using the same procedures as described in Fig. 5. In this case, eight offset signals are used instead of six. Comparing the eight offset signals and the modulation signals produces eight primary signals Y_1-Y_8. The adequate switching signals are derived by applying the Boolean operations in (15)-(18) on Y_1-Y_8 signals. In (11)-(18), symbols "+" and "X" correspond to the logical operators "OR" and "AND", respectively.

$$S_1, \overline{S_3} = (\overline{Y_6} \times Y_7) + \left(Y_1 + (\overline{Y_3} \times Y_4)\right) \tag{15}$$

$$S_2, \overline{S_4} = Y_5 + \left((\overline{Y_7} \times Y_8) + (\overline{Y_2} \times Y_3)\right) \tag{16}$$

$$S_5, \overline{S_6} = Y_3 \tag{17}$$

$$S_7, \overline{S_8} = Y_7 \tag{18}$$

IV. SIMULATION AND EXPERIMENTAL VALIDATION

This section presents a numerical verification and experimental validation of the proposed topology. The circuit configuration in Fig. 1 is used to evaluate the circuit operation, and Table 3 lists the used system parameters in simulation and experimental tests. Fig. 6 shows the experimental setup, consisting of two programmable DC voltage sources (Chroma, 62024P-100-50), one DC source for control circuits (Rohde & Schwarz, HMP4040), three single-phase transformers (Triad Magnetics, VPM240-20800), dSPACE MicroLabBox controller, current and
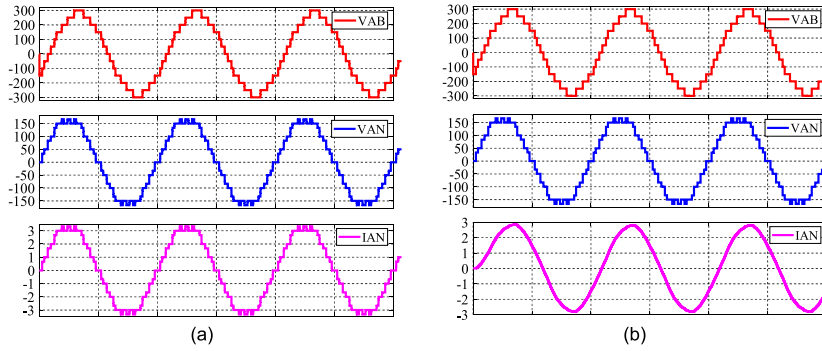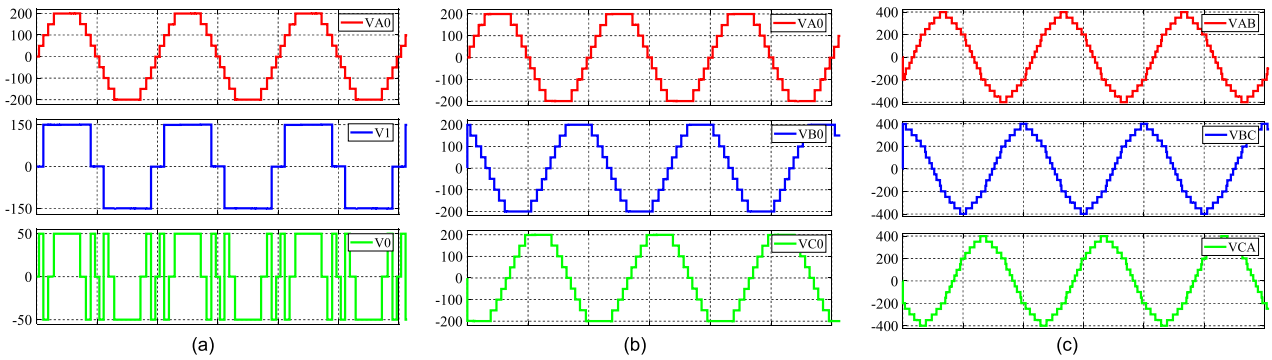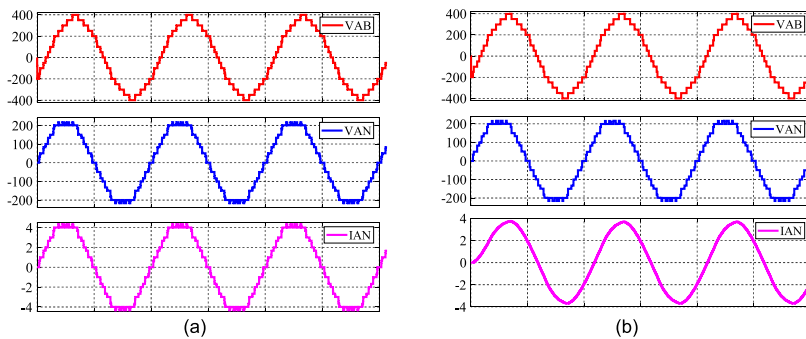
FIGURE 8. Simulation waveforms when β is 1. (a) V_{AB}, V_{AN}, and I_{AN} at resistive load. (b) V_{AB}, V_{AN}, and I_{AN} at resistive-inductive load.

FIGURE 9. Simulation waveforms when β is 1.5. (a) pole voltage V_{A0} synthesizing. (b) pole voltages V_{A0}, V_{B0}, and V_{C0}. (c) line voltages V_{AB}, V_{BC}, and V_{CA}.

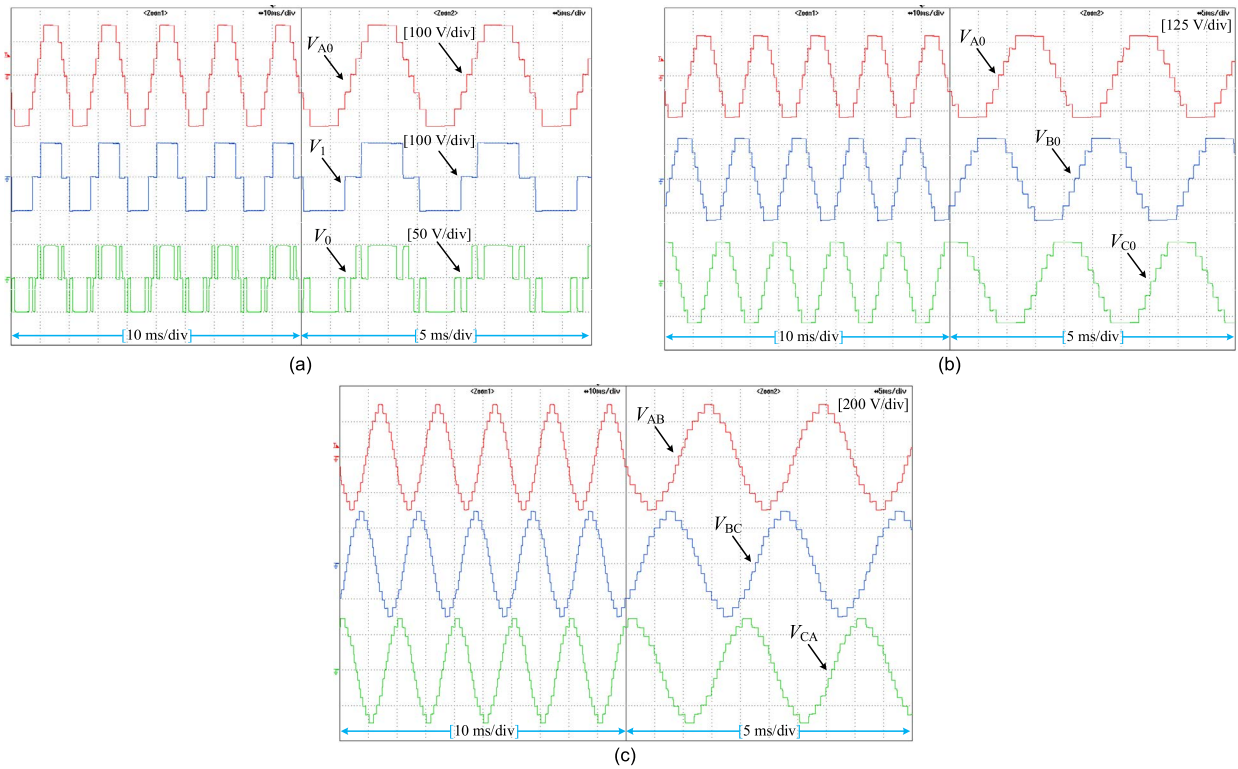
FIGURE 10. Simulation waveforms when β is 1.5. (a) V_{AB}, V_{AN}, and I_{AN} at resistive load. (b) V_{AB}, V_{AN}, and I_{AN} at resistive-inductive load.

B. EXPERIMENTAL RESULTS

The simulation findings are experimentally validated by the in-house inverter porotype in Fig. 6. The proposed topology is tested with one case of β ($\beta = 1$) since we do not have transformers with a turn ratio of 1.5. All the remaining parameters are kept as same as in the simulation verifications. Fig. 11(a) presents the leg-A pole voltage V_{A0} and its two voltage components V_0 and V_1. By setting 100 V as the input voltage of the inverter (E), the waveforms of V_0 and V_1 have voltages of (0 and ± 50 V) and (0 and ± 100 V), respectively, resulting in a seven-level pole voltage as shown in the first trace of Fig. 11(a). Further, Fig. 11(b) shows the seven-level

pole voltages of the three inverter legs V_{A0}, V_{B0}, and V_{C0}. These pole voltages having phase shifts of 120° produce three balanced line voltages of thirteen levels, as depicted in Fig. 11(c). Figs. 12(a) and (b) provide the obtained results when connecting resistive and resistive-inductive loads to the inverter outputs, respectively. The experimental results well validate and confirm the simulations and theoretical analysis of the proposed topology.

The efficiency of the proposed topology is measured experimentally. Fig. 13 shows the obtained values at different output powers while keeping all other system parameters constant. The efficiency increases from 92.69% to 97.76%

FIGURE 11. Experimental waveforms of the proposed topology when β is 1. (a) pole voltage V_{A0} synthesizing. (b) pole voltages V_{A0}, V_{B0}, and V_{C0}. (c) line voltages V_{AB}, V_{BC}, and V_{CA}.
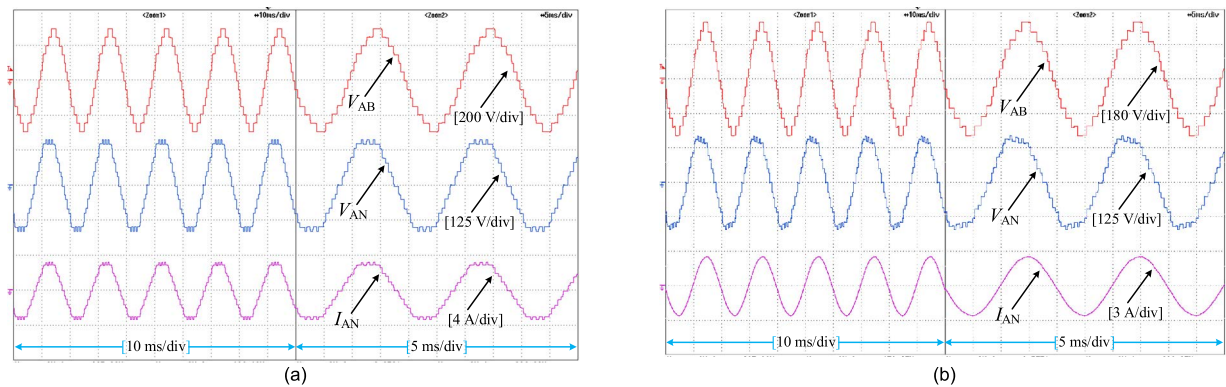
FIGURE 12. Experimental waveforms of the proposed topology when β is 1. (a) V_{AB}, V_{AN}, and I_{AN} at resistive load. (b) V_{AB}, V_{AN}, and I_{AN} at resistive-inductive load.

when increasing the load power from 0.2 KW to 1.5 KW in a step of 0.1 KW. Using low frequencies ($\leq$150 Hz) in the employed switching scheme reduces switching losses and increases the overall efficiency.

V. COMPARATIVE ASSESSMENT OF THE PROPOSED TOPOLOGY

The proposed topology is compared to recent developed transformer-based MLIs at nine-level operation in this section. The proposed topology aims to maximize the output voltage level count while reducing the required components. Therefore, a quantitative comparison is carried out between

the transformer-based counterparts and the proposed topology based on component counts: namely DC voltage source count (N_{DC}), transformer count (N_{Trf}), switch count (N_{SW}), power diode count (N_D), and capacitor count (N_{Cap}). For a fair comparison, the following aspects are considered: A) generating nine levels in the three pole voltages. B) adopting the three-phase configurations. C) equalizing the total voltage of a single DC-link to E volt, e.g., if a topology T_X has a shared DC-link among its three-phase legs, the whole voltage of the DC-link is assumed to be E. D) counting each part based on its primary unit structure, e.g., a unidirectional switch is the counting unit for bidirectional switching devices, and

TABLE 4. Comparison of the proposed three-phase inverter topology with related multilevel inverters for nine-level operation.

Topology	N_{DC}			N_{Cap}				N_{SW}				N_D	N_{Trf}	
				DC-link	Flying capacitors									
	E/4	E/2	E	E/2	E/4	E/2	E	E/4	E/2	E	2E	E	E*	2E*
T_1 [18]	4	0	0	0	0	0	0	24	0	12	0	0	3	0
T_2 [19]	0	0	1	0	0	3	6	0	12	6	6	6	0	3
T_3 [20]	0	0	1	6	3	0	0	12	12	6	0	0	3	0
T_4 [21]	0	0	1	2	3	0	0	12	12	6	0	0	3	0
T_5 [22]	0	0	1	0	0	0	0	0	0	24	0	0	6	0
Proposed MLI	0	2	0	0	0	0	0	0	6	18	0	0	3	0

* The applied voltage across the primary windings, the load current is assumed to be the same for all topologies.
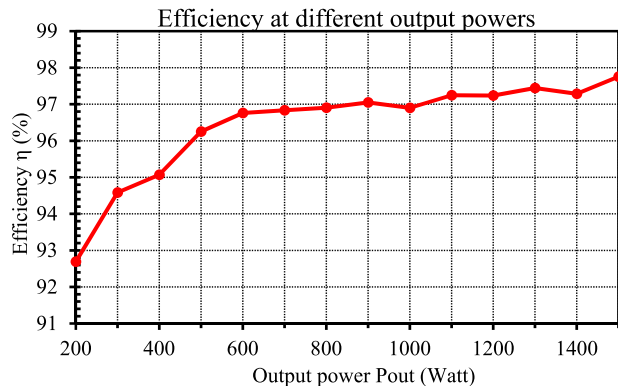
FIGURE 13. Measured efficiency at different load power.

a single-phase transformer is the counting unit for three-phase transformers. Table 4 lists the considered MLI topologies in the comparative study T_1-T_5, and their component counts N_{DC}, N_{Cap}, N_{SW}, N_D, and N_{Trf}. Further, it shows the voltage stress/rating of the necessary parts in each topology. It is noted from Table 4 that the proposed topology and the topologies T_1 and T_5 do not require any capacitor or power diodes, increasing their reliability and conversion efficiency. On the other hand, the topologies T_2-T_4 are capacitor-based circuits, increasing the control complexity, sensor count, and failure rates.

The proposed inverter and topologies T_1-T_4 use the same transformer count, but the proposed inverter has some salient advantages: lowering twelve switches and two DC sources as compared to T_1, eliminating six power diodes and nine capacitors as compared to T_2, removing six switches and nine capacitors as compared to T_3, reducing six switches and five capacitors as compared to T_4. Both T_5 and the proposed topology are capacitor- and diode-free circuits, but T_5 require one DC source while the proposed topology requires two DC sources. However, the proposed topology can save three transformers as compared to the topology T_5. It is worth mentioning that the two DC sources in the proposed topology have a 0.5E voltage rating, while the DC source in the topology T_5 has a voltage rating of E volt. Table 4 confirms that the proposed topology employs the lowest component count among the compared transformer-based MLI topologies [23].

VI. CONCLUSION

This paper proposes a novel three-phase transformer-based nine-level inverter with a reduced component count, having the key features of being capacitor-, diode-free, and low counts of DC sources, switches, and transformers. The proposed circuit can increase the voltage level count to N levels without increasing the voltage stress across the switches, being a promising candidate for high-power high-voltage applications. Further, it has beneficial features of modularity, voltage boosting and simple structure. The working principle of the proposed topology was theoretically demonstrated, numerically verified, and experimentally validated through the in-house setup. Finally, the advantages of the proposed topology, in terms of component counts, are highlighted by a comparative study.

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