A Comparative Study of Two Adaptive Continuous-Time Filters for Decision Feedback Equalization Read Channels

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Abstract - This paper presents a comparative study of two adaptive continuous-time 3rd order allpass equalizers for magnetic disk decision feedback equalization read channels. These are based on adaptive current-mode Gm-C structures employing low-mismatch high bandwidth pseudo-differential balanced transconductors and polarized MOSFET arrays as integrating capacitors. Transistor level simulation results are presented to demonstrate the performance characteristics of both structures.

INTRODUCTION

In recent years various systems based on Decision Feedback Equalization (DFE) [1-3] have been reported for magnetic head read channels. DFE systems using digital FIR filter techniques have been able to meet the increase of data acquisition rates but at the expense of complexity and power dissipation. More recently, however, *low end* drives have prompted considerable efforts [4-7] for developing a low power continuous-time adaptive forward equalizer alternative to the FIR approach. This paper presents a comparative study of two such continuous-time adaptive equalizers designed to work with a sampling frequency of 100 MHz and which consume approximately 3 mW at 3.3 V supply voltage. This is less than one tenth of traditional FIR power needs, and practically independent of the sampling-frequency at the input of the slicer.

EQUALIZER ARCHITECTURE

DFE read channels basically consist of two equalizing filters and a decision element (*slicer*), as shown in the block diagram of Fig. 1. The forward equalizer is used for *precursor* ISI cancellation while the backward equalizer is a non linear *post cursor* ISI remover. It is of considerable interest that both filters operate in current-mode so that the outputs of these filters are added in the current summing node that precedes the sampling switch. The adaptation process depends on the generation of the error signal e_k estimated by the difference between the prediction value at the input of the slicer and the data decision at its output.

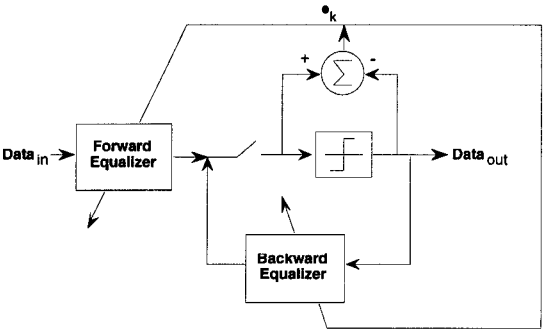

Fig. 1 - Block diagram of a DFE read-head channel.

This paper is concerned with the design of the forward equalizer using adaptive continuos-time structures. For a 100 MHz sampling frequency and the following *a priori* pole location derived from [8]

Real Pole	f = 8 MHz	
Complex Poles	f_0 = 26 MHz	Q = 0.6

the system transfer function is expressed by

$$H(s) = \frac{-S^3 + 3.26 \cdot 10^8 S^2 - 4.1308 \cdot 10^{16} S + 1.3754 \cdot 10^{24}}{S^3 + 3.26 \cdot 10^8 S^2 + 4.1308 \cdot 10^{16} S + 1.3754 \cdot 10^{24}} \cdot \quad (1)$$

ADAPTIVE GM-C ARCHITECTURES

For the above specifications, two Gm-C current-mode structures were designed and compared based on transistor level simulations. Both architectures adapt using LMS modified algorithms [9], and allow the parasitic input capacitance in the Gms to be taken into

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account for very high frequency operation. The automatic tuning of the poles frequency also compensates process tolerances that influence the effective value of the active devices and capacitors. The equalizers linearity is mainly determined by the linearity of the transconductors and integrating capacitors. The DC voltage inherent to the simulated structures biases these transistors well beyond their threshold voltage for enhanced linearity behavior.

Canonical Structure

Firstly, we considered the canonical structure illustrated in Fig. 2. It is composed of four equal value pseudo-differential transconductors embedded in a grounded capacitive network.

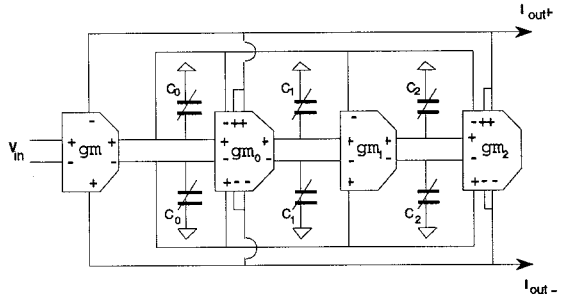


Fig. 2 - Canonical structure.

The corresponding 3rd order state-space system can be expressed as

$$\begin{cases} \dot{[i]} = [A]\cdot[i] + [B]\cdot i_{in} \\ i_{iout} = [C]^T\cdot[i] + D\cdot i_{in} \end{cases} \quad (2)$$

where the system matrices are given by

$$[A]=\begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 & -gm_0/C_0 \\ gm_1/C_1 & 0 & 0 \\ 0 & gm_2/C_2 & 0 \end{bmatrix}, [B]=\begin{bmatrix} gm_0/C_0 \\ 0 \\ 0 \end{bmatrix}, [C]=\begin{bmatrix} 2 \\ 0 \\ 2 \end{bmatrix}, D=-1$$

Notice that matrix [A] assumes the typical *row-shape* characteristic of canonical structures. The system transfer function is thus given by

$$H(s)=\frac{-S^3C_0C_1C_2+S^2C_1C_2gm-SC_2gm^2+gm^3}{S^3C_0C_1C_2+S^2C_1C_2gm+SC_2gm^2+gm^3}. \quad (3)$$

Considering equal-valued transconductors with a nominal transconductance value of 60 µS and after subtracting the effect of the parasitic input capacitance of the Gms we obtain the following nominal values for the integrating capacitors

$C_0 = 0.083$ pF, $C_1 = 0.47$ pF, $C_2 = 1.8$ pF.

Orthonormal Structure

In alternative to the canonical structure described before we also considered the orthonormal structure represented in Fig. 3. Although the design of the orthonormal structure is usually a more complex approach, it can take a rather simplified format for the allpass filter. Moreover, it uses only one of the state variables to build the allpass current output wave and thus making it more immune to noise and offset problems than the previous canonical structure.

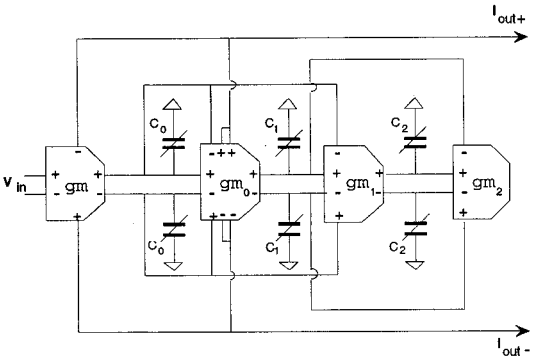


Fig. 3 - Orthonormal structure.

The corresponding 3rd order state-space system is also expressed by matrix equation (2) but the system matrices are now given by

$$[A]=\begin{bmatrix} -gm_0/C_0 & -gm_0/C_0 & 0 \\ gm_1/C_1 & 0 & -gm_1/C_1 \\ 0 & gm_2/C_2 & 0 \end{bmatrix}, [B]=\begin{bmatrix} gm_0/C_0 \\ 0 \\ 0 \end{bmatrix}, [C]=\begin{bmatrix} 2 \\ 0 \\ 0 \end{bmatrix}, D=-1$$

A simple scaling of the system state-variables would transform it in the orthonormal ladder structure proposed in [11]. Hence, since the filter satisfies Lyapunov's equation

$$AK + KA^T + 2\pi bb^T = 0 \quad (4)$$

all the system state-variables are orthogonal and the dynamic range is optimized. The system transfer function for the structure in Fig. 3 is given by

$$H(s)=\frac{-S^3C_0C_1C_2+S^2C_1C_2gm-S(C_0+C_2)gm^2+gm^3}{S^3C_0C_1C_2+S^2C_1C_2gm+S(C_0+C_2)gm^2+gm^3}. \quad (5)$$

Considering again equal-valued transconductors with the same nominal value of 60 µS and after subtracting the effect of the input capacitance of the Gms we obtain the following nominal values for the integrating capacitors

$C_0 = 0.102$ pF, $C_1 = 0.49$ pF, $C_2 = 1.77$ pF.

Adaptive Capacitor Arrays

The adaptation of the Gm-C filters previously described is achieved by means of integrating capacitor structures C_i consisting of a constant *course* MOSFET capacitor C_i' in parallel with an N-bit digitally controlled *fine* tuning capacitor array ΔC_i, as shown in Fig. 4.

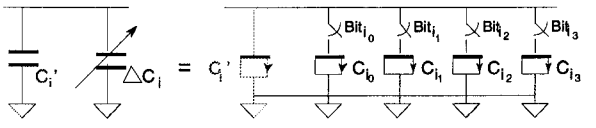


Fig. 4 - Integrating capacitors are formed by a fixed capacitor in parallel with a digitally controlled capacitor-array.

The total integrating capacitance is given by

$$C_i = C_i' + \Delta C_i \ , \tag{6}$$

where

$$\Delta C_i = \sum_{k=0}^{N} C_{ik} \cdot Bit_{ik} \ , \ C_{ik} = 2^k \cdot C_{iN} \ . \tag{7}$$

The minimum value C_i' and the maximum value $C_i'+\max(\Delta C_i)$ of each integrating capacitor C_i are dimensioned to allow the desirable placement of the poles, even under worst case process tolerances that influence the actual value of Gms and of the integrating capacitors. The number of adaptation bits must provide sufficient adaptation precision of the arrays without unduly increasing the circuit complexity. For both structures described before we considered N = 4-bit capacitor arrays made of biased 12.5 fF unit size transistor cells that can be switched on and off by the adaptive control logic. The adaptation process is assumed to be done during the clock recovery preamble and be stable at the decision instants. Alternatively the capacitor array can be loaded in parallel and subsequently adapted to optimum values.

Transconductors

The transconductors employed in the above filters are based on balanced pseudo-differential lossy-C structures, as shown in Fig. 5. Unlike in the circuit used in [10], biasing is provided by the feedback loops established in the filter, yielding improved stability and noise immunity. Moreover, the transistors dimensions determining the biasing voltages were calculated to minimize the allowed mismatch while maintaining maximum frequency performance. Computer simulations showed that such transconductors are capable of maintaining the correct operation of the filter for supply voltages as low as 1.8 V.

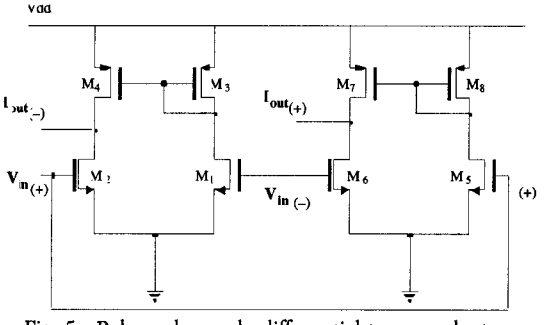
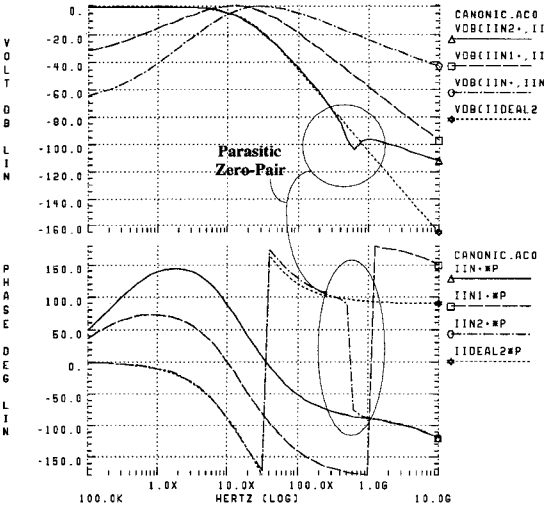


Fig. 5 - Balanced pseudo-differential transconductor.

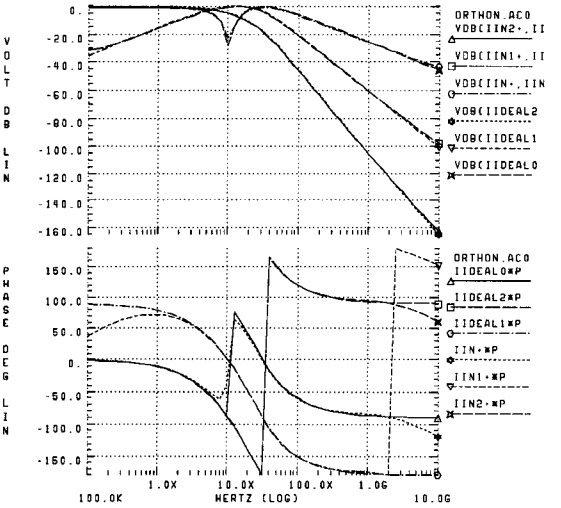
RESULTS AND DISCUSSION

Frequency Response

Transistor level simulations of both structures with nominal integrating capacitance values produce the amplitude and phase versus frequency response characteristics shown in Fig. 6.(a) and Fig. 6.(b), respectively for the canonical and orthonormal structures. Whereas with the response of the canonical structure there is a parasitic zero-pair mismatch in state variable I_{In2} around 450 MHz in the orthonormal structure all state variables I_{Ini} nearly match the ideal I_{Ideali} amplitude and phase characteristics well over 1GHz.



(a)



(b)

Fig. 6 - Frequency response of the (a) canonical and (b) orthonormal filter structures, for nominal integrating capacitance values.

This shows that under identical design conditions the orthonormal structure has a better high frequency performance behavior. Besides, the orthonormal structure has improved adaptability capabilities since it allows independent pole tuning.

Transient Response

The transient response of both structures was analysed using an input corresponding to measured data [*] from the magnetic read head. This waveshape V_{in} represents consecutive transitions, one up and one down, usually mentioned as *dibit* response. The resulting equalized transient response of the orthonormal and canonical outputs are superimposed and are both represented by I_{real} in Fig. 7, showing that both structures practically match the predicted response from the ideal implementation I_{Ideal}.

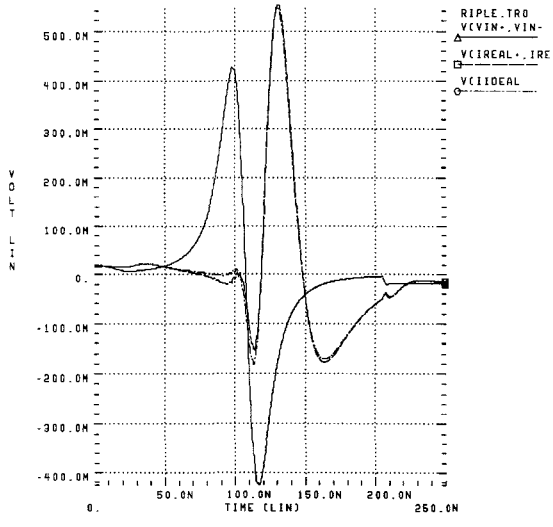


Fig. 7 - Dibit-response of the Allpass Filter.

CONCLUSIONS

This paper presented a comparative study of two continuous-time equalizers for DFE read channels. They can both operate with supply voltages as low as 1.8 V while reducing consumption by a factor of 10 to 100 compared to conventional FIR digital equalizers exhibiting equivelent performance. Besides its improved adaptability, the orthonormal structure shows improved frequency response over the canonical structure and hence suggests that the orthonormal structure is a better realization of the allpass forward equalizer, specially at higher data rates.

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[*] Courtesy of IBM.