AN AUTO-BIASED 0.5 μm CMOS TRANSCONDUCTOR FOR VERY HIGH FREQUENCY APPLICATIONS

Nuno de Figueiredo Garrido, José E. Franca

Department of Electrical and Computer Engineering, Integrated Circuits and Systems Group
Av[a] Rovisco Pais 1, 1096 Lisboa Codex, Portugal
garrido@ecsm4.ist.utl.pt, franca@ecsm4.ist.utl.pt

ABSTRACT*

This paper describes a CMOS transconductance cell for the implementation of very high frequency current-mode gm-C filters. It features simple pseudo-differential circuitry employing small device size transistors and yielding a power dissipation of less than 1 mW/pole at nominal 3.0 V supply voltage. Self-biased common-mode voltage designed to minimize mismatch errors, improves noise and stability behavior. Short channel effects are analyzed and simulation results are presented.

1. INTRODUCTION

Most of the modern high-speed applications requiring continuous-time filtering usually employ current-mode circuit techniques to allow signal processing up to the fundamental limits of MOS devices [1][2]. Moreover, they also allow the use of plain digital CMOS technology working at low supply voltage, which is important for the implementation of mixed analog/digital circuits. This paper proposes a new transconductor cell for the implementation of very high frequency applications. It uses a pseudo-differential topology employing small device size transistors and relies on a self-biased common-mode voltage to achieve improved noise and stability behavior. This DC voltage is designed to minimize mismatch errors and is imposed by the current feedback path.

2. TECHNOLOGY ASSESSMENT

In modern submicron CMOS technologies the long-channel pinch-off model usually described by the square-law relationship is no longer valid [3][4][5]. The use of short-channel devices implies that even simplified analysis should include the influence of gate and source-drain electrical fields on mobility. Moreover, the importance of these parameters has augmented with the consistent shrink in the minimum effective length and gate oxide thickness of MOS transistors inherent to process advancements. The vertical electrical field is modeled by the mobility modulation parameter θ, which depends mainly on the oxide thickness. The critical field for mobility degradation ξ_{crit}, which represents the limit for surface mobility, can be used to model the effect of the longitudinal electrical field. Under these conditions the transistor current can be expressed by [6]

$$I_d = \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{(V_{gs} - V_t)^2}{2(1 + \theta \cdot (V_{gs} - V_t) + \xi_{crit} \cdot \frac{V_{ds_{sat}}}{L})} \cdot (1 + \lambda V_{ds}). \quad (1)$$

Taking the partial derivative of (1) with respect to V_{gs} and assuming $V_{ds_{sat}} \approx V_{gs} - V_t$ we then obtain the following expression for the transistor transconductance

$$g_m = \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{(V_{gs} - V_t)}{2} \cdot \left[\frac{1}{1 + \left(\theta + \frac{\xi_{crit}}{L}\right) \cdot (V_{gs} - V_t)} + \frac{1}{\left[1 + \left(\theta + \frac{\xi_{crit}}{L}\right) \cdot (V_{gs} - V_t)\right]^2} \right] \quad (2)$$

From the above complete expression, two simpler expressions for the transistor transconductance can be derived. On the one hand, the typical simplification for long length devices biased near the week inversion region yield the well-known gm relationship shown in the first branch of (3). On the other hand, mobility reduction due to the combined effect of transverse and longitudinal electrical fields of MOS transistors, is determinant for short length devices biased in the strong inversion. As a result the expression in the second branch of (3) is valid if $(\theta + \frac{\xi_{crit}}{L}) \cdot (V_{gs} - V_t) >> 1$.

$$g_m \approx \begin{cases} \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_t) & \Leftarrow L \geq 2.0\mu m \wedge V_{gs} - V_t \leq 0.3V \\ \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{1}{2 \cdot \left(\theta + \frac{\xi_{crit}}{L}\right)} & \Leftarrow L \leq 0.5\mu m \wedge V_{gs} - V_t \geq 2.0V \end{cases} \quad (3)$$

The transistors achieve their maximum frequency behavior when approaching the velocity saturation region, where gm becomes nearly independent of $(V_{gs} - V_t)$ overdrive inasmuch as mobility is limited by the maximum drift velocity of carriers. Near this region, the

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gm/I_d ratio becomes inefficient since the transconductance barely increases with the biasing current. Considering small values of L we can expect that $\frac{\xi_{crit}}{L} >> \theta$ and hence the transconductance becomes

$$g_m \rightarrow \frac{C_{ox} \cdot V_{sat} \cdot W}{2} \tag{4}$$

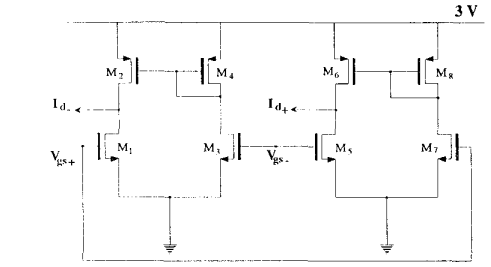
where $V_{sat} = \mu / \xi_{crit}$ is the saturation velocity of carrier at nominal temperature. The gate parasitic capacitance ($C_{gs}=2/3 \cdot C_{OX} \cdot W \cdot L$) and gm define a limit for the transition frequency f_t of the transistor, as given by

$$f_t = \frac{g_m}{2\pi \cdot C_{gs}} \rightarrow \frac{3 \cdot V_{sat}}{8\pi \cdot L} . \tag{5}$$

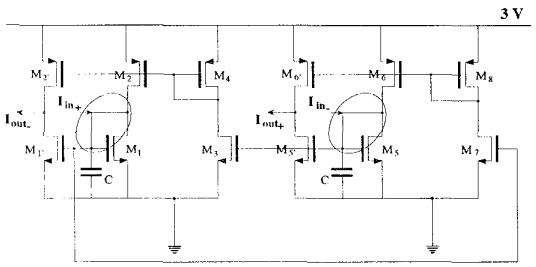
For 0.5 μm devices, this value corresponds to approximately 20 GHz (NMOS) and 15 GHz (PMOS). Therefore, it is expectable that transconductors can work with negligible phase shift up to 1 GHz, and hence active transconductance-C filters operating at very high frequency can be realized.

3. BALANCED TRANSCONDUCTOR WITH SELF-BIASED FEEDBACK

Several transconductor topologies have been presented that are capable of high frequency performance [7][8][9]. The pseudo-differential topology proposed in [8] is particularly interesting for the low supply voltage operation typical of modern submicron CMOS technologies, for two main reasons. First since it does not require the typical tail current of differential pairs it can provide increased headroom for the output voltage swing. Second, the grounded gate parasitic capacitances of the input transistors are easily absorbed in the sizing of the integrating capacitors. This circuit, however, requires additional components for the implementation of the common-mode and damping control networks, therefore it can suffer from additional noise interference and potential common-mode voltage instability due to component mismatches. An interesting solution to overcome the problems of common-mode networks has been proposed in [10] and consists of achieving the required biasing by means of appropriate feedback loops without the use of common-mode circuitry. The implementation given in [10] requires feedback transconductance circuitry that perform the output voltage sensing, in the first place, then a sign inversion and finally the voltage to current conversion for the input comparison. The solution proposed herein is based on a pseudo-differential topology, as given in [8], but whose common-mode voltage is established in a simpler way than is presented in [10]. As we can see in Fig. 1 this consists of a pure current-mode feedback path established between the output nodes (I_{d+},I_{d-}) and the input nodes (V_{gs-}, V_{gs+}), providing exact unity common-mode feedback voltage gain. A simple first order low-pass filter example is given in Fig. 1(b), but the proposed technique is also valid for general purpose filters using more complex structures, as the ones in [11]. As it will be shown next, the sizing of the transistors can be obtained in order to provide an optimum common-mode voltage that minimizes the effects of component mismatches on the operation of the circuit.



(a)



(b)

Fig. 1. (a) Basic transconductor cell and (b) self-biased connection in a first order low-pass filter.

The internal node of the active loads also stabilizes the common-mode of the transconductor, since the drains of M_1,M_2 and M_5,M_6 ideally track the DC drain voltage of M_3, M_4 and M_7, M_8 due to finite g_{ds} conductance. This node imposes a high frequency parasitic pole at approximately

$$f_{node} \approx \frac{g_{m_{PMOS}} // g_{ds_{PMOS}} // g_{ds_{NMOS}}}{2\pi \cdot \left(C_{gs_{PMOS}} + C_{gs_{NMOS}}\right)} \approx \frac{f_{t_{PMOS}}}{2} . \tag{6}$$

The input voltage $v_{in}=V_{gs+}-V_{gs-}$ and the output current $i_d=I_{d+}-I_{d-}$ are fully balanced around the common-mode voltage V_{cm}, thus canceling even-order non-idealities. Hence, considering the balanced inputs $V_{gs+}=V_{cm}+v_{in}/2$ and $V_{gs-}=V_{cm}-v_{in}/2$, the output current can be derived from (1) and be expressed exactly by

$$i_d = (I_{d+} - I_{d-}) = \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{v_{in}}{2 \cdot \left(\theta + \frac{\xi_{crit}}{L}\right)} \cdot \left(1 - \frac{1}{\left[1 + \left(\theta + \frac{\xi_{crit}}{L}\right) \cdot (V_{cm} - V_t)\right]^2 - \left(\theta + \frac{\xi_{crit}}{L}\right)^2 \cdot \frac{v_{in}^2}{4}} \right) . \tag{7}$$

This expression can also be simplified for both long and short channel devices, yielding the expressions shown in

$$i_d \approx \begin{cases} \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{cm} - V_t) \cdot v_{in} & \text{, for L} \geq 2.0\mu\text{m} \\ \mu C_{ox} \cdot \frac{W}{L} \cdot \frac{v_{in}}{2 \cdot \left(\theta + \frac{\xi_{crit}}{L}\right)} & \text{, for L} \leq 0.5\mu\text{m} \end{cases} . \quad (8)$$

Therefore, in both cases, the output current is quasi-linear in respect to the input differential voltage. An estimated large-signal distortion of approximately 0.2% for $v_{in}=1V$ is expected from (7), but real values should increase due to mismatch. Common-mode and supply rejection are only limited by the mismatch between the identical NMOS M_1, M_3, M_5, M_7 and PMOS M_2, M_4, M_6, M_8 transistors.

4. OPTIMUM AUTO-BIASING FOR MINIMUM MISMATCH EFFECTS

Matching properties of MOS transistors show that the variance in both the threshold voltage and gain factor $\beta=\mu \cdot C_{ox} \cdot W/L$ affect the mismatch of I_d according to [12]

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_t)}{(V_{gs} - V_t)^2} + \frac{\sigma^2(\beta)}{\beta^2} . \quad (9)$$

Since the standard deviation parameters $\sigma(V_t)$ and $\sigma(\beta)$ are approximately proportional to $1/\sqrt{W \cdot L}$, minimum size lengths lead to even stronger deterioration of matching, especially in digital technologies. Therefore, although the use of minimum length devices is advisable to achieve maximum frequency performance, a trade-off must be obtained between speed and the amount of allowed mismatch. Fabrication statistical data for both PMOS and NMOS transistors available from similar processes [13] suggest a minimum channel length of $0.8\mu m$ considering a $0.05\mu m$ mask pitch. This data has also been used to estimate the common-mode voltage V_{cm} that minimizes the influence of threshold voltage dispersion on the output current, yielding

$$min \left[\left(\frac{\sigma^2(I_{d_{PMOS}})}{I_{d_{PMOS}}^2} + \frac{\sigma^2(I_{d_{NMOS}})}{I_{d_{NMOS}}^2} \right) (V_{cm}) \right]_{VDD=3.0V}$$
$$\Rightarrow \left. \frac{\sigma^2(I_d)}{I_d^2} \right|_{V_{cm} \approx 1.4V} \approx 0.35\% . \quad (10)$$

The ideal DC common-mode voltage of $V_{cm} = 1.4\ V$ imposes $V_{gs}-V_t \approx 1V$, and thus keeping the PMOS and NMOS transistors in the strong inversion region, although not far from velocity saturation. The self-biasing occurs in the intersection of the DC characteristic of the transconductor with the $V_{in+} = V_{out-}$ and $V_{in-} = V_{out+}$ constrains imposed by the current feedback paths, as illustrated in Fig. 2. The transistors dimensions determining the biasing voltages are calculated to locate the intersect point at $V_{cm} = 1.4\ V$ and thus minimizing mismatch effects while maintaining maximum frequency operation.

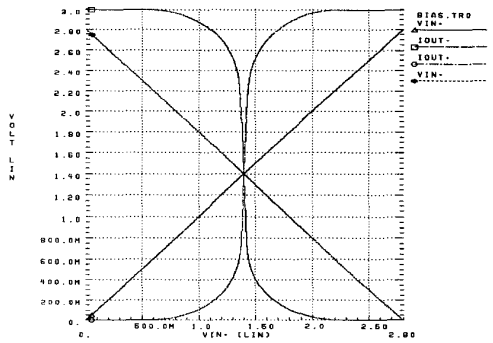


Fig. 2. DC biasing is self imposed by the feedback loops established in a filter implementation.

5. RESULTS AND DISCUSSION

Transistor level simulations of the transconductance voltage output produce the amplitude and phase characteristics depicted in Fig. 3, showing that the high frequency parasitic pole is located around 5GHz and close to the ft of the transistors. Some additional simulation results of the transconductance cell are shown in Table I.

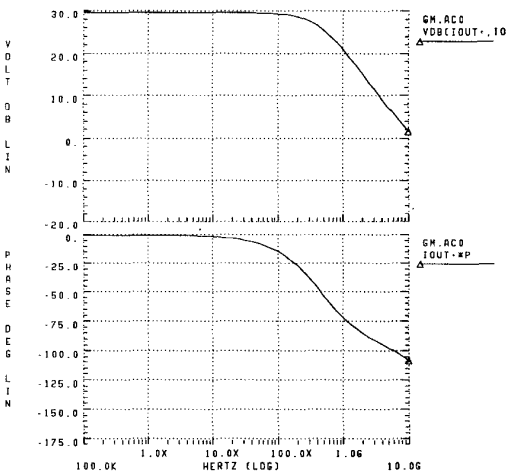


Fig. 3. Frequency response of the pseudo-differential transconductor.

Table I. Characteristics of the MOS transconductor.

Technology	0.5μm Digital CMOS
Supply Voltage	3.0 V
CMRR	80 dB
PSRR, GSRR	60 dB
THD (1Vpp@10MHz)	–50 dB
Power dissipation	350 μW

6. CONCLUSIONS

This paper presented an auto-biased transconductor cell for the implementation of VHF continuous-time current-mode gm-C filters. The auto-biasing is granted by feedback loops, thus avoiding common-mode circuitry and yielding improved stability and noise immunity. The proposed transconductor can operate at low supply voltages for reduced power dissipation. The small feature transistors are designed to allow good high frequency operation while controlling mismatch effects. Computer simulations show that this transconductor is capable of sustaining correct operation for supply voltages as low as 1.8 V.

7. REFERENCES

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