A 1.6Gb/s CMOS LVDS Transmitter with a Programmable Pre-Emphasis System

Benjamín T. Reyes ‡, German Paulina†, Lucas Tealdi†,
Emanuel Labat†, Raúl Sanchez†, Pablo S. Mandolesi*, and Mario R. Hueda‡

‡ Laboratorio de Comunicaciones Digitales - Universidad Nacional de Córdoba - CONICET
Av. Vélez Sarsfield 1611 - Córdoba (X5016GCA) - Argentina
† Fundación Fulgor - Romagosa 518 - Córdoba (5000) - Argentina
* GISEE - LMNE - Universidad Nacional del Sur - Av. Alem 1253 - Bahía Blanca - Argentina
Emails: {breyes, mhueda}@efn.uncor.edu

***Abstract*— A 12 parallel low voltage differential signaling (LVDS) transmitter fabricated in 0.13 μm CMOS is presented. Each LVDS channel can operate over 1.6 Gb/s and includes a programmable pre-emphasis circuit designed to reduce the data-dependent jitter (DDJ) caused by different lengths of PCB traces. Experimental results of the fabricated LVDS confirm the correct operation of the programmable pre-equalization circuit. The power consumption and area per channel is less than 20 mW and 0.084 mm^2, respectively.**

I. Introduction

The low-voltage differential signaling (LVDS) standard has been defined to respond the increasing demand of high-speed chip-to-chip digital interfaces [1]. This standard is usually implemented in digital data interfaces from tens of Megabits per second (Mb/s) up to 3 Gigabits per second (Gb/s) with a relatively low power consumption [2].

On the other hand, it is well-known that a band-limited channel causes inter-symbol interference (ISI) in high-speed interfaces. As detailed in [3], ISI and noise deteriorate the quality of the received signal and causes error in data recovery. Thus, the ISI is usually compensated by channel equalization either on the transmitter (Tx) side, the receiver (Rx) side or both sides simultaneously [3]. In chip-to-chip interfaces, the printed circuit board (PCB) trace is the most common channel. These metallic channels suffer from limited bandwidth due to frequency dependent channel loss that is mainly caused by skin effect and dielectric loss [4]. Furthermore, in high-speed data transmission over FR4 media (PCB traces) the ISI is usually observed in the form of data dependent jitter (DDJ) [2].

In LVDS interfaces, channel equalization is not usually necessary at low data rates (e.g., $<$ 1 Gb/s) and *short* copper channels (e.g., $<$ 6 inches PCB traces on FR4). However, at relative high-speed data rates ($>$ 1.2 Gb/s) and *long* copper channels ($>$ 10 inches), a high DDJ (ISI effect) can be observed in LVDS links [2], [3]. Pre-equalization (or *pre-emphasis*) is the preferred method for channel compensation in LVDS interfaces over FR4 traces due to its low power consumption, reduced silicon area, and simplicity of design [5], [6]. A fixed amount of pre-emphasis is usually adopted in some reported LVDS drivers [5], [7]. However, the amount of pre-emphasis should be adjusted for each Tx chip environment (e.g., different FR4 channel lengths) to effectively equalize the ISI channel.

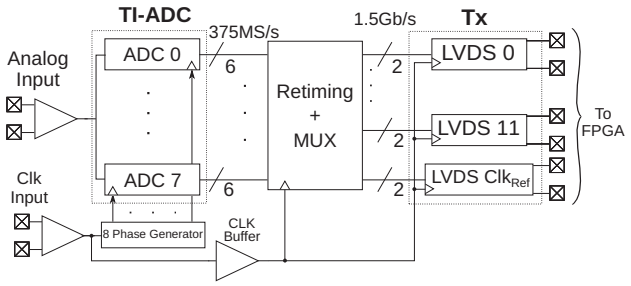

Fig. 1. Chip architecture with LVDS transmitter.

In this work we present an LVDS driver with channel pre-equalization based on a *programmable* pre-emphasis circuit. Unlike most previous LVDS implementations [5], the pre-emphasis circuit is programmable and provides flexibility to adjust the LVDS Tx pre-equalization for different operation environments (e.g. different FR4 trace lengths, board substrate or chip packagings). We highlight that the described LVDS is a part of a 6-bit, 2 Gb/s time-interleaved analog-to-digital converter (TI-ADC) described in [8]. The LVDS interface is required to transmit a data-rate of (at least) 12 Gb/s from the TI-ADC to a field-programmable gate array (FPGA) chip. The TI-ADC chip architecture provides 48 CMOS lines from 250 MHz to 375 MHz each line. Therefore, the LVDS Tx architecture requires a serialization of 48 CMOS lines to 12 LVDS channels to reduce the number of pins of the chip. Then, a data rate of 1 Gb/s to 1.5 Gb/s per channel is required. A careful design to achieve a low time-skew between the LVDS parallel channels has been carried out. Moreover, an extra LVDS clock signal to synchronize a DSP-based receiver implemented in a FPGA platform has been included. Measurements of the fabricated LVDS transmitter demonstrate that the programmable pre-emphasis system is able to equalize different FR4 copper channel lengths.

This paper is organized as follows. Section II describes the LVDS transmitter blocks. Section III presents experimental results, while conclusions are drawn in Section IV.

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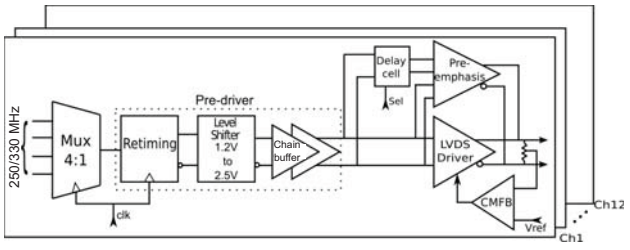


Fig. 2. Tx channel architecture.

II. LVDS TRANSMITTER

A. Overview

Figure 2 shows the proposed architecture for the multichannel transmitter. Each Tx channel consists of a 4:1 multiplexer, a pre-driver circuit and LVDS driver. The pre-driver block includes a retiming circuit, a 1.2 V to 2.5 V CMOS level-shifter and a chain of CMOS buffers. The LVDS driver includes a common-mode feedback (CMFB) block and a programmable pre-emphasis circuit. As mentioned before, the design requires twelve LVDS channels transmitting from 1 Gb/s to more than 1.5 Gb/s per channel. Therefore, a 1.6 Gb/s LVDS Tx design is adopted to meet the specifications.

B. Driver

The LVDS standard [1] defines the electrical requirements for an LVDS driver. For example, typical differential swing voltage (V_{OD}) of 350 mV, common-mode voltage (V_{CM}) of 1.2 V, and a 100 Ω differential impedance at the receiver.

An LVDS driver is basically a current mode differential driver that can be implemented in several topologies. The driver topology used in this implementation is the bridged-switches current source (BSCS) [9], [10]. This topology is simple and has a low power consumption. Moreover, the BSCS topology requires at least 2.5 V supply voltage which is available for this chip project. A BSCS driver acts as a current source with switched polarity. Figure 3 shows the circuit of the driver together with the common mode feedback (CMFB). The driver consists of two current sources (M1 and M6) and four switches MOS (M2 to M5) connected in a bridge configuration. Therefore, applying a logic "1" at the D input and a logic "0" to -D input, the switches M2-M5 are "on" and M3-M4 are "off" and then the terminal $Vout$ sinks the current and the terminal $Vout\_b$ sources the current. Contrarily, when M2-M5 are "off" and M3-M4 are "on", the polarity is changed and the situation is reversed.

On the other hand, the LVDS standard [1] requires a very stable V_{CM}, thus a CMFB loop is used to fix the DC output level at 1.2 V (Fig. 3). The CMFB loop amplifier is a differential pair stage with current mirror load. It is used to compare the output common-mode voltage (sensed from R_{P1}-R_{P2} node) and an off-chip 1.2 V reference. Then, the amplified error is fed back to the current source M1 to close the loop. The CMFB loop includes a Miller compensation over the M1 current source nodes to guarantee enough phase margin. The simulated CMFB open loop response achieves 55 dB DC

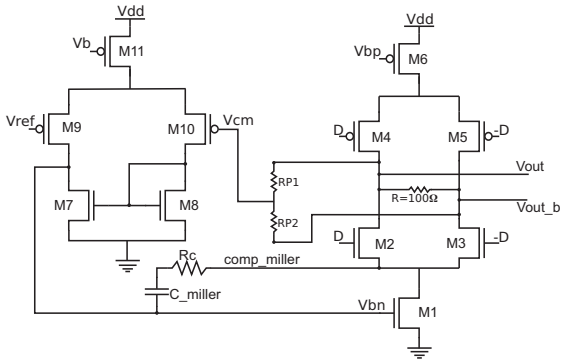


Fig. 3. BSCS driver and CMFB circuit.

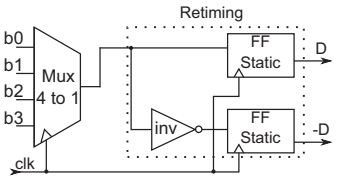


Fig. 4. Mux 4:1 and retiming blocks.

gain and 74 degrees phase margin worst case (corner SS, low V_{DD}, low I_{ref}, and 125°C).

Furthermore, an on-chip 100Ω resistance is added because the source impedance matching minimizes the signal reflections at high-speed data rates [10].

C. Multiplexer and Retiming

Figure 4 shows the 4:1 multiplexer (MUX 4:1) and the retiming diagram. The MUX 4:1 is based on four transmission gate switches that are sequenced by a shift register. The shift-register is clocked by the same retiming clock and synchronized by a signal provided by the ADC block. The retiming circuit is composed of two static D flip-flop (DFF) that clocks the data signal and its complement as shown in Fig. 4. Thus, the DFFs provide the complementary signals D and -D for the level shifter input without phase skew between them. Moreover, since all the LVDS channels (Ch0 to Ch11) are retimed with the same clock signal, a negligible phase skew is also guaranteed between different LVDS input channels.

D. Level Shifter

The ADC, MUX 4:1, and retiming blocks operate at 1.2 V CMOS logic level but a 2.5 V CMOS level is required by the BSCS driver. Therefore, a *conventional* level shifter circuit to convert from 1.2 V CMOS level to 2.5 V CMOS level is used. Figure 5 presents the implemented circuit. It requires of thin-oxide MOS transistors (1.2 V MOS) and thick-oxide MOS transistors (2.5 V to 3.3 V MOS) to translate the switching levels avoiding overvoltage risk on any thin-oxide MOS. Basically, when the level shifter is slightly imbalanced at the NMOS inputs (MN1 and MN2), the PMOS transistors MP1 and MP2 behave as a regenerative charge and hence the outputs will be fully switched at 2.5 V CMOS levels. Besides, the main requirement for this circuit is a high-speed switching

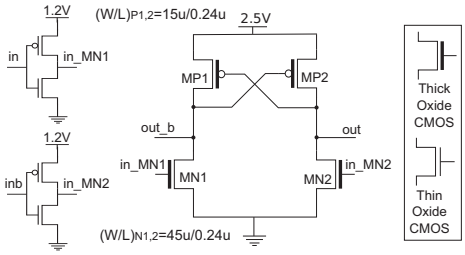
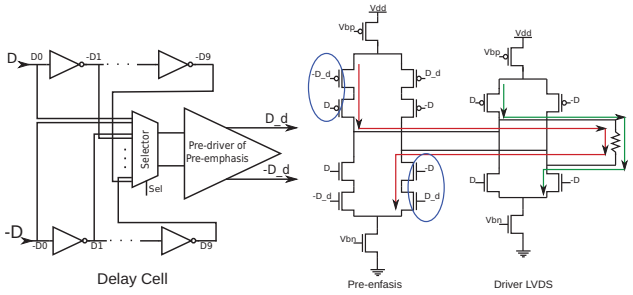


Fig. 5. Level shifter from 1.2 V to 2.5 V.



(a) (b)

Fig. 6. BSCS driver with programmable pre-emphasis circuit: (a) programmable delay circuit (b) pre-emphasis implementation.

(over 1.6 GHz) without time-skew at the outputs. Thus, a detailed transistor sizing (see Fig. 5) to obtain a minimum rise/fall time is required.

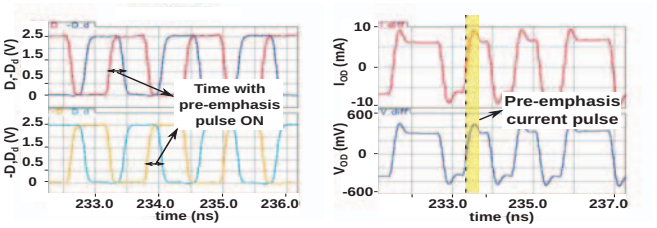
E. Pre-emphasis

A pre-emphasis circuit provides an additional current pulse on each bit transition to speed up rise/fall time, thus overcoming the drawback of different channel lengths. In our implementation, the pre-emphasis circuit proposed in [5] has been used. However, a programmable delay block to control the time duration of the pre-emphasis current-pulse has been added.

Figure 6 shows the delay cell for pre-emphasis control and BSCS driver connection. The programmable delay cells are based on a chain of inverter buffers and a transmission gate selector. The delayed signals, D_d and $-D_d$, are generated from the original signals, D and $-D$, respectively, by means of delay cells. Figure 7(a) depicts the overlapping of the signals D, $-D_d$ and D_d, $-D$ that turn on the pre-emphasis current in each bit transition. Figure 7(b) plots the output driver current with the pre-emphasis current pulses added. Hence, the output V_{OD} shows a *peaking* on each bit transition (see Fig. 7(b)). Moreover, Fig. 8 demonstrates the pre-emphasis effect over a 15" FR4 cooper channel.

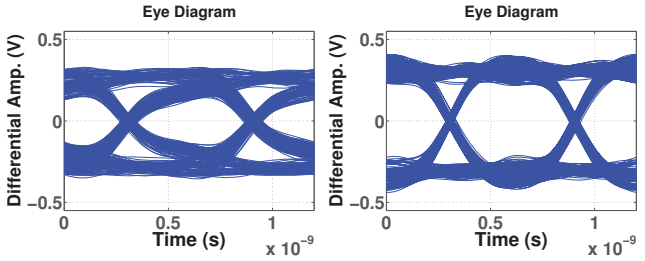
III. Experimental Results

Figure 9 shows the transmission link setting used in both, simulations and experimental measurements. For the simulation results the transmission model includes: complete LVDS driver, electrostatic discharge (ESD) cell, pad model, packaging model, S-parameters copper channel model (s4p files), and simplified Rx model ($R_L = 100\Omega$ and $C_L = 5pF$). For



(a) (b)

Fig. 7. Driver signals: (a) driver and pre-emphasis inputs (b) diff. output driver current (I_{OD}) and diff. output driver voltage (V_{OD}).



(a) (b)

Fig. 8. Eye diagrams after 15" FR4 copper channel model at 1.66 Gb/s: (a) without pre-emphasis (b) with pre-emphasis.

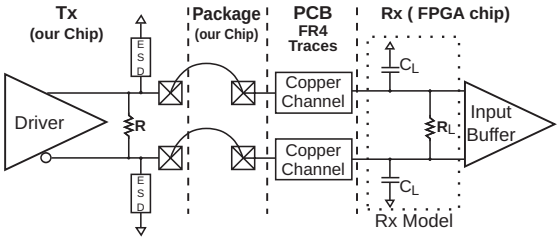


Fig. 9. Chip-to-chip link test setup.

comparison purposes, all the simulation results in the figures are in typical process with nominal power voltage and at room temperature (unless otherwise specified). Moreover, the measured signals have been collected using a 20 GS/s digital oscilloscope from the chip outputs and then re-plotted in the computer. The effectiveness of the fabricated pre-emphasis circuit in the presence of FR4 channels has been verified by processing the captured signal with differential microstrip transmission line models generated with Hyperlynx's *signal integrity tool*.

Figure 10 shows simulated and measured eye diagrams with the pre-emphasis circuit turned on but *without* FR4 channel (in this case, a peaking is caused by the pre-equalization). A good agreement between simulated and experimental can be observed. Figure 11 presents the eye diagram results for two channel length models with different amount of pre-emphasis level. In both cases (6" and 30" copper channel) the eye diagrams show a properly equalization.

Table I summarizes the corner results of several parameters of interest for the LVDS standard compatibility and different channels. Figure 12 depicts the layout of a single LVDS channel, while Fig. 13 shows the microscope view of the

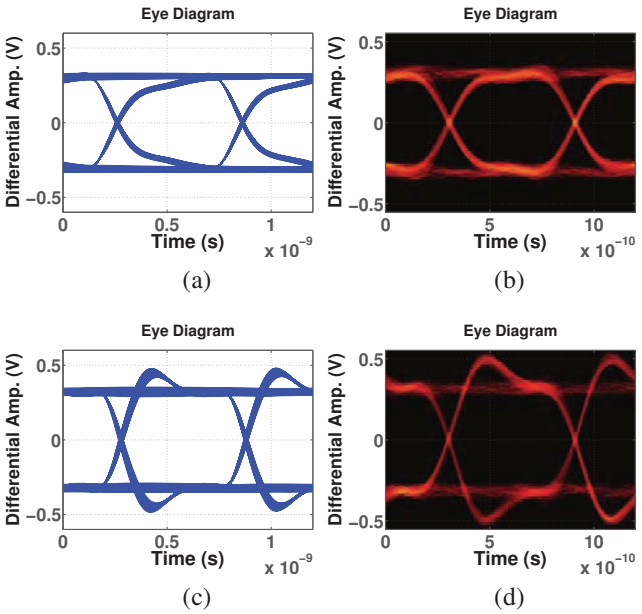


Fig. 10. Eye diagrams (without channel effect) at 1.66 Gb/s: (a) without pre-emphasis (sim.), (b) without pre-emphasis (meas.) (c) with pre-emphasis (sim.),(d) with pre-emphasis (meas.)

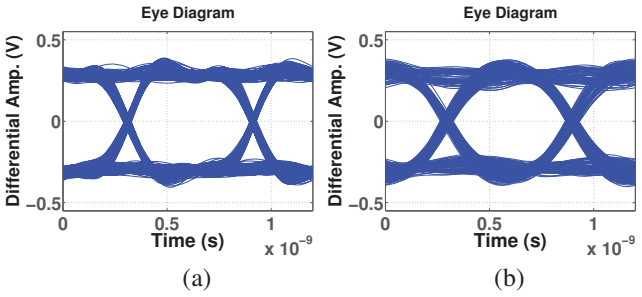


Fig. 11. Eye diagrams output at 1.66 Gb/s: (a) with *minimum* amount of pre-emphasis and after 6" FR4 copper channel model and (b) *medium* amount of pre-emphasis and after 30" FR4 copper channel model

TABLE I

SUMMARY OF CORNER SIMULATIONS.

Proc. N P	VDD [V]	T [°C]	V_{OD} [mV]	DDJ [ps]	Progr. Pre-Emp	I_{Dr} [mA]	Chn [inch]
TT	2.5	25	516	22	None	5.5	1
SS	2.25	125	445	35	None	4.8	1
FF	2.75	0	400	30	None	5.0	1
TT	2.5	25	530	40	D1	5.7	15
SS	2.25	125	480	50	D1	5.1	15
FF	2.75	0	590	18	D1	5.9	15

fabricated chip. The active area per channel is 0.084 mm^2 in a 0.13 μm CMOS process. The total power consumption is 260 mW, including 12 LVDS data channels plus two reference clock channels. The total chip area for data transmission is 2.1 mm^2, including decoupling.

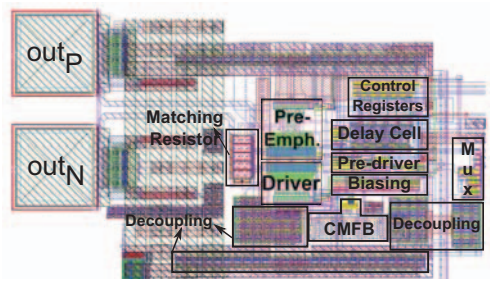


Fig. 12. Layout of a single LVDS channel.

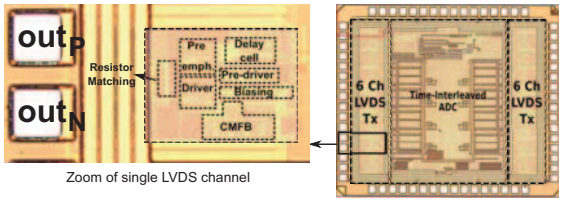


Fig. 13. Chip die photo.

IV. CONCLUSIONS

In this paper, a 12 channel LVDS transmitter fabricated in 0.13 μm CMOS process has been presented. The transmitter is fully compatible with the IEEE LVDS standard, and it is able to operate over 1.6 Gb/s per channel. An important feature of this design is the implementation of a programmable pre-emphasis circuit that can compensate for more than 30-inches of PCB trace with low DDJ and optimal swing. The fabricated LVDS transmitter is a part of a 6-bit, 2 Gb/s time-interleaved analog-to-digital converter [8].

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