Feasibility Study and Design of a Robust Low-Noise Amplifier Operating at Millimeter-Wave for High Reliability Applications

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Abstract-A feasibility study and the corresponding design flow for robust millimeter wave GaN LNAs is provided in this paper. Particular attention is devoted to the selection of the optimum geometry of the first stage active device. A trade-off is shown between noise performance and robustness requirements. The beneficial effects of source degenerative feedback are shown. The LNA's simulated performance are gain > 20B, NF < 1.7dB and power handling capability verified up to +20 dBm input power in CW operation. This design is well suited for operation in high reliability systems, such as space operation on airborne applications.

Index Terms- Millimeter-wave robust low-noise amplifiers, Gallium Nitride, Ka-band, Thermal reliability.

I. INTRODUCTION

The upper part of the K-band, and in particular the spectrum from 26 to 35 GHz, is particularly interesting for the aerospace and defense community since several applications adopt this frequency allocation. A first example of these applications is earth imaging, as the detection of water vapor resonance at 35 GHz. Slightly below, at 33 GHz we have high-resolution, close-range targeting radars, used in seekers or in Electronic Warfare systems [1]. Lastly, the band between 26 and 31 GHz is particularly interesting for satellite telecommunications

Be it spaceborne or airborne, all applications require the handling of high RF power at the operating frequency in conjunction with enhanced circuit reliability – a fundamental aspect in mission critical systems – without excessively burdening the platform's DC power and thermal management system. Form a circuit point of view these two aspects are related to a single crucial point: keeping device operating temperature as low as possible during operation.

Robust receivers represent a key function in this context. Low-Noise Amplifiers (LNA) can either appear either in stand-alone receivers [2] or as part of multi-functional MMICs such as Single-Chip Front Ends [3]–[6]. In all cases the requirements placed upon the LNA are low noise figure, robustness to high interference or received signals and low DC power consumption. Reliability is also an important aspect in these systems. Most applications are critical either because the functionality is crucial (defense) or because maintenance is not feasible (space). Consequently, the power consumption must be reduced as much as possible since it directly impacts the operating channel temperature of the transistor, which in turn affects the reliability of the electronic circuit.

In this paper we provide a feasibility study and the pertinent design flow of a Ka-band robust low-noise amplifier considering also thermal aspects that impact the reliability of the circuit. Section II contains requirements and technology selection indications. Section III contains the analysis to select optimum device geometry when addressing the often-contrasting goals of low-noise performance, survivability and maximum DC power consumption. Section IV contains MMIC design and simulated performance while a comparison with similar designs is provided in Section V.

II.   REQUIREMENTS & TECHNOLOGY SELECTION

The main objective of this study is to verify the feasibility of a MMIC LNA exhibiting simultaneously low-noise performance (i.e. NF < 2 dB) with reduced DC power request (< 150 mW) in conjunction with high-power handling performance capability. The latter parameter is quantified as maximum +20dBm Continuous Wave (CW) incident power or equivalently a strong pulsed (1-ms period with 10% duty cycle) input of +30 dBm at Ka-band 26-31 GHz [7]. All requirements are reported in Table 1. They cover linear, noise, nonlinear, survivability and reliability performance.

Table 1: MMIC LNA design requirements

Requirement	Value	Unit
Operating frequency	27 – 31	GHz
Gain min	20	dB
NF max	1.75	dB
OP1dB	> 15	dBm
I/O return loss	15	dB
Survivability, max input power	+20	dBm
Bias voltage, max	5	V
Current consumption, max	30	mA
Channel temperature	< 160	°C
Max Base-plate temperature	+80	°C

DC power consumption is an important parameter to improve reliability. In fact, as indicated in the eq. (2), there is an exponential relationship between the transistor's operating channel temperature and dissipated DC power. Consequently, the latter parameter shall be minimized in order to increase MMIC Mean Time To Failure (MTTF).

A. Technology Selection

Gallium Arsenide (GaAs) or even more Indium Phosphide (InP) demonstrate unrivaled performance in terms of Noise Figure, especially at millimeter wave operating frequency [8]–[11]. However, these technologies' breakdown voltage is rather low, typically +4V for sub 0.1μm GaAs

[12] and even less (+2V) for InP based technologies [13], [14]. Consequently, while these technologies offer superior noise performance they are discarded for this study since they are unable of fulfilling the robustness requirement.

Gallium Nitride (GaN) is a better wide-bandgap material compared to GaAs This results in a much higher breakdown electric field (one order of magnitude). GaN supports smaller circuits for a given frequency and power levels, allowing higher power densities and efficiencies. As consequence of the above feature, GaN is capable to withstand very strong signals without degradation. Moreover, GaN thermal conductivity is more than three times the thermal conductivity of GaAs. In addition, GaN devices can be operated at higher junction temperature. Currently ESA recommendation is maximum +160°C in derating conditions, but most likely this limit will be set higher in the future [15].

Of course, the power capability of the GaN technology is in general of less relevance for application in LNA unit, but such features can be exploited to simplify the design of the Front End. GaN epitaxy can be grown on both Silicon Carbide (SiC) and Silicon (Si) substrates. SiC features brilliant thermal behavior that greatly mitigates the heat dissipation issue. However, it is rather expensive, considering the limited number of space-grade SiC substrate providers, and is available in smaller radius wafers. On the other hand, the use of Si substrate, while penalizing in terms of thermal behavior and RF losses, leads to lower manufacturing cost with respect to SiC, which is an essential aspect for high volume production: Moreover, Si substrates should allow, in the future, for the integration of RF and digital sub-systems on the same chip

Given these preliminary considerations on the technology and considering the MMIC is designed to be installed in space-borne or avionic systems for European critical missions, we opted to evaluate European technology providers only. The short list is between UMS GaN GH-10 process [16], [17] and OMMIC's D01GH. Both processes have recently demonstrated, at millimeter-wave, low-noise and high-power functionalities [18]–[22] and are able of

operating up to 30 GHz and (slightly) beyond and feature the required power density needed for the demonstrator.

There are also other GaN technologies available in Europe, such as IAF's (Fraunhofer Institute's) GAN10 process [23], [24]. This technology provides exceptional performance in terms of noise, power and frequency behavior. However, it is less suitable for space-qualified operation.

Table 2 European GaN industrial-grade technologies summary

Parameter	GH10	D01GH
V_T (V)	-3.2	-2.0
I_{DSS} (A/mm)	1.2	1.2
$I_{DSS,max}$ (A/mm)	1.4	1.7
g_m (mS/mm)	450	800
NF min @ 30 GHz	1.7	1.4
Recommended V_{DS} (V)	25	< 16
f_T (GHz)	80	110
f_{max} (GHz)	130	160
Power Density (W/mm)	3.5	3.3
Substrate	SiC	Si

As seen in Table *2*, the two processes are quite similar. Anyhow, for this feasibility study, we selected OMMIC's D01GH for the following reasons. First, NF is slightly better. Second, it comes on a Si substrate which reduces production costs and is not sensible to restrictions such as ITAR. Finally, OMMIC is developing a shorter gate length process, namely a 60 nm process, that can be integrated in the future on the same MMIC with the 100 nm gate length technology.

III. DESIGN SOLUTIONS

The design solutions are oriented to satisfy the requirements listed in Table 1. The most critical, in terms of circuit performance are Noise Figure and survivability.

A. Amplifier Topology Selection

Several topologies are available for LNA synthesis. The principal is single ended, cascode, distributed, and balanced. Circuit topology is selected to fulfil one or more key requirements.

Consequently, a detailed analysis is implemented in the first phase of the feasibility study to address initial LNA specifications.

Single ended is by far the most popular topology in mmw-LNA since it is relatively easy to synthesize. At high-operating frequencies, a sensible design strategy consists in keeping circuit complexity at the lowest possible level. Single-ended topology consists in cascading a predetermined number of common source (CS) amplifying stages to obtain the prescribed gain value, obviously within the limitation of a feasible number of stages. A simplified schematic diagram of a 2-stage single-ended LNA is depicted in Fig. 1. At millimeter wave frequencies the inductors are realized with thin microstrip lines.
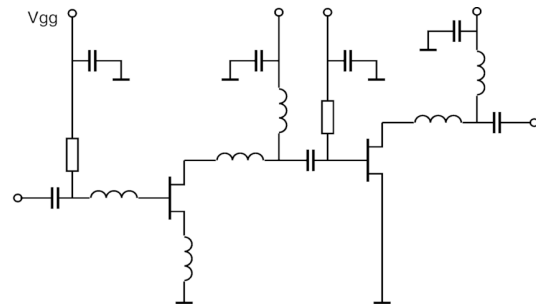

Fig. 1 Simplified schematic of a reactively matched 2-stage single ended low-noise amplifier.

Cascode topology represents an interesting solution when wide operating bandwidth is a design goal in conjunction with low NF and high gain. In this topology, a common source stage is cascaded with a common gate stage acting as a wideband low-input impedance buffer stage for the preceding stage. The balanced topology represents an interesting solution when adequate values of input and output return loss are required over a very wide operating bandwidth. The main downside of this topology is represented by the ohmic losses introduced by the input power splitter that directly affects the mmw-LNA's NF. Another negative side effect resides in the resulting size of this circuit, which practically doubles the single-ended version. Apart from adequate return loss over a wide operating frequency, this topology exhibits another benefit such as very higher power

handling capability, since the incident RF power is halved at the input before the two LNA stages. Distributed amplifier topology is most suited in ultra-wideband applications. Given the relatively small bandwidth, this topology is discarded in the present feasibility study. Therefore, given the LNA requirements, the single-ended topology is selected representing and adequate trade-off between obtainable RF performance and circuit complexity. Three stages are necessary since the associate gain of the transistor at operating frequency is 8 dB.

B. Device Geometry Analysis

In an LNA, the first stage is critical since it fixes the NF of the overall amplifier. Furthermore, in this study, the first stage active device is subject to a survivability requirement expressed as +20 dBm CW incident power.

The two requirements are in contrast for the following reason. Smaller devices, i.e. less number of fingers and shorter gate widths typically exhibit lower noise figure, even if just slightly as depicted in Fig. 2.
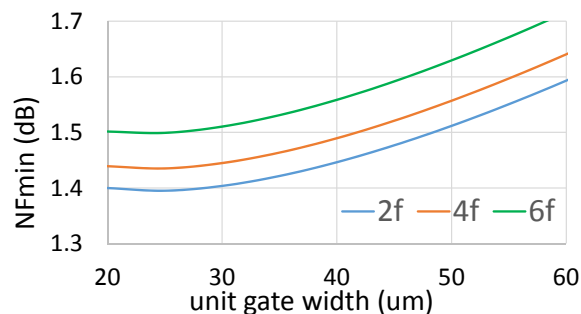

Fig. 2 Minimum Noise Figure for several device geometries, namely 2, 4 and 6 fingers with different gate widths at 30 GHz.

Additionally, at millimeter wave smaller device are more easily matched since the parasitic impedances of a smaller transistor (namely CDS and CDS) are reduced than in larger transistors. Fig. *3* reports the optimum noise termination as a function of device geometry at 30 GHz. Three

device families are analyzed: 2, 4, and 6 finger devices. For each family the gate with is swept from 20 to 60 µm at 5 µm steps. The device is biased at t the low-noise operating point suggested by the foundry, corresponding to VDS +5 V and drain current 100 mA/mm.
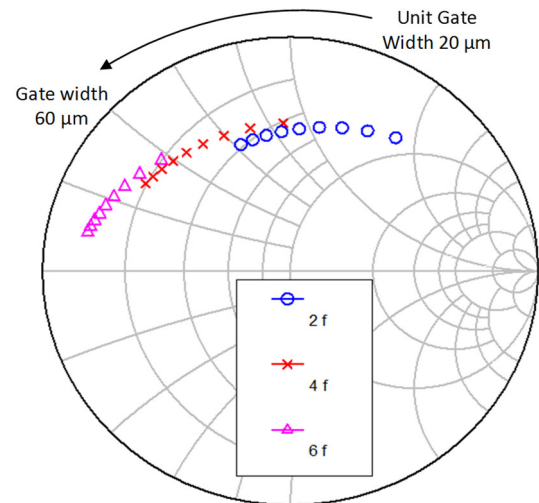

Fig. 3 Optimum noise termination for several device geometries, namely 2, 4 and 6 fingers and different gate widths at 30 GHz.

An analysis of the data in Fig. 3 would lead the designer to opt preliminarily for a small transistor, such as a 2 finger device. In fact, this family of devices is closer to the center of the Smith Chart. The other two families (4 and 6 finger devices) are closer to the low-impedance (short circuit) region entailing a more cumbersome synthesis of the input matching networks.

However, the survivability requirement must also be considered. With respect to this requirement, larger devices are favorable. In fact, OMMIC's design manual, and the maximum rating's section specifies the following limits.

Table 3 Maximum ratings summary for OMMIC's D01GH.

Parameter	Unit	Value
Dissipated Power (DC)	W/mm	4
Rectified DC gate current	mA/finger	2

From the analysis of the data reported in Table 3 it appears that larger devices are favored upon smaller devices since the periphery, and number of fingers is greater, and therefore it is easier to respect the maximum ratings specification. Consequently, we opt for a 4 -finger x 25 μm device representing an adequate trade-off between the contrasting goals of Noise matching, power handling capability and reduced DC power consumption. Accordingly, the drain current on each transistor is 10 mA since they are biased at 100 mA/mm and the total LNA DC power consumption is 150 mW.

C. Inductive Source Degeneration

This circuit technique, applicable to the common source FET configuration, consists in inserting an inductive element (LS) between the FET's source terminal and ground as schematically depicted in Fig.4.
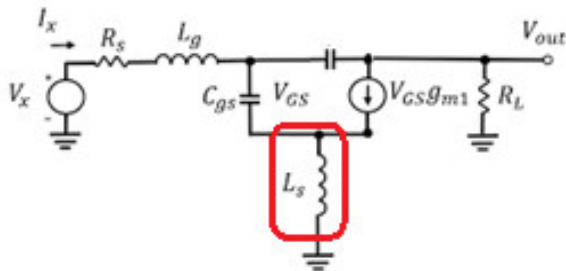

Fig. 4 Simplified equivalent circuit of an HEMT device with source degenerative feedback.

This technique is applied for a variety reasons as briefly explained in the following. First, it lowers the gain of the transistor allowing a wider bandwidth operation. Second, it enables Simultaneous Signal & Noise Matching (SSNM) [25] which is very important since, in general for low-noise devices, the optimum impedances for matching and noise are far from each other [26], [27]. This feature also enables a wider bandwidth operation. Fig. 5 depicts the trajectory of the optimum impedances for matching and noise of a 4 x 25μm transistor as a function of L_S, feedback

inductance value. The active device electrical model is provided by the foundry. It is classical a linear/noise model available in the foundry's PDK rev 1.0.3 [28]. The minimum distance between the two terminations occurs when L_S is around 150 pH. Above this value, the optimum termination for noise moves towards the lower part of the Smith Chart while the optimum termination for gain moves towards the upper border of the Smith Chart making SSNM condition less practical, at least over a broader bandwidth of operation.
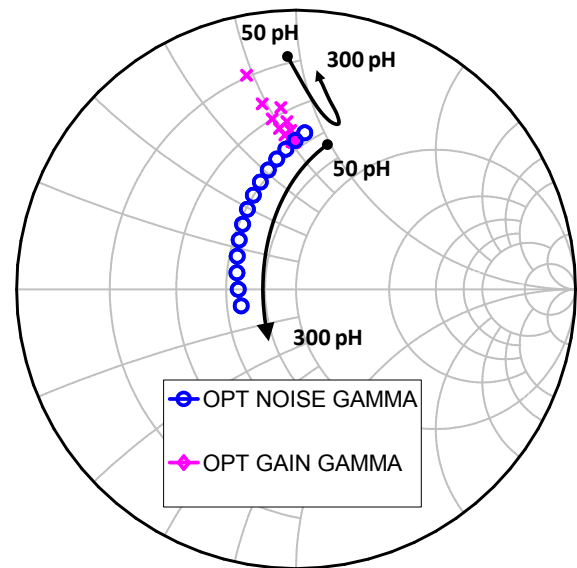

Fig. 5 Optimum noise and gain input reflection coefficient for several feedback values at 30 GHz.

Third, the gain reduction improves the transistor's stability, at least in the operating bandwidth. Fourth, it significantly modifies the output termination that matches the transistor's input to 50 Ω.

The load termination that matches the input of the LNA to 50Ω is defined as Γ_{LCin}, and its formula is reported in (1) where Δ is the determinant of the 2x2 scattering parameter matrix of the active device and Γ_S the source termination that is selected to satisfy a specific minimum noise condition.

$$\Gamma_{LCin} = \frac{s_{11} - \Gamma_S^*}{\Delta - s_{22} \cdot \Gamma_S^*} \qquad (1)$$

Fig. 6 depicts the trajectory of Γ_{LCin} as a function of feedback value at 30 GHz. For low values of feedback source inductance, Γ_{LCin} is in the lower (capacitive) region of the Smith Chart. As the inductive feedback increases, Γ_{LCin} moves towards to Centre and then finally in the upper (inductive) region. If compared to the trajectories reported in Fig.5 we can see that Γ_{LCin} is much more sensible to feedback value since the length of the arc is considerably longer. Consequently, inductive feedback has a higher impact on the output termination that matches the input of the transistor to 50Ω rather than on the optimum for noise/gain input termination.
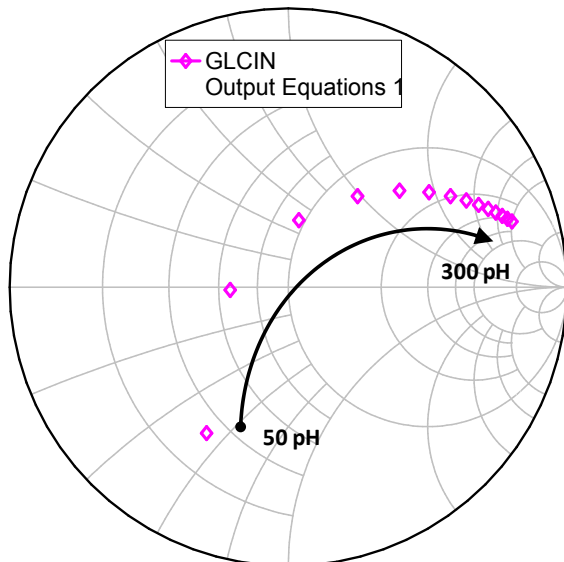

Fig. 6 ΓLCin trajectory, in the output termination plane, as a function of source degenerative feedback at 30 GHz.

If Γ_{LCin} is designed to be relatively close to the centre of the Smith Chart then the SSNM condition is obtained, over a broader operation bandwidth, since the input terminations for gain and noise are closer to each other and the output termination is more easily synthesized. This occurs for feedback values around 150 pH. At lower microwave frequencies, the inductive dipole is realized through a spiral inductor. As the frequency increases, a short and thin microstrip

line replaces the spiral inductor. At very high frequencies, the parasitic inductance of the via-hole to ground through the substrate is often enough to obtain the desired effect. In multi-stage amplifiers, as occurs in mmw-LNAs, there are design guidelines that aid the designer in selecting the inductance value for each stage given a gain / stability constraint, with the aim to obtain an input and output match as close as possible to 50 Ω in conjunction with prescribed gain level.

IV.   IMPLEMENTATION AND EXPECTED RESULTS

A. Integrated Circuit Layout

As expressed previously, the circuit was designed in OMMIC's D01GH technology and following the various design solution provided in section III. Electromagnetic design and analysis were employed to simulate the matching networks (passive structures). The matching networks were designed to provide the appropriate reflection coefficients at the gate and drain terminals of the three transistors as indicated in Fig. 5 and Fig. 6. Matching networks physical layout is depicted in Fig. 8. Series and shunt transmission lines are used for noise/signal matching (at RF) and transistor biasing (at DC). Series DC-block capacitors are inserted also for matching purposes. Details of the input matching network, the most critical for noise and survivability, are reported in Fig. 7.
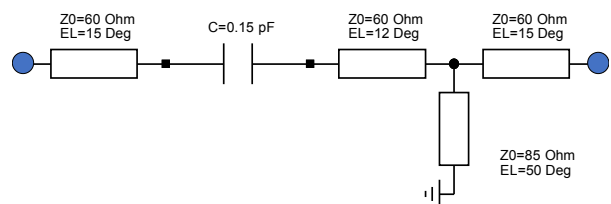

Fig. 7 . Simplified schematic of the Input Matching Network (IMN). Electrical lengths (EL) are given at 30 GHz.

The MMIC's layout is depicted in Fig. 8. The transistors in the first and second stages both have

the same amount of inductive source feedback since they are designed to satisfy the optimum noise performance. The final, (output) stage is matched for gain/noise performance. In fact, the cascade gain of the first and second stage is enough to conceal the noise contribution coming from the final stage [29].

Moreover, Fig. 8. reports also the four matching networks respectively – from input to output – Input Matching Network (IMN), Inter-stage Matching Network #1 (ISMN1), Inter-stage Matching Network #2 (ISMN2), and finally the Output Matching Network (OMN).

Out-band active device unconditional stability is obtained by adding dissipative elements, typically in the biasing structures, whose stabilizing and noisy effects are negligible at operating frequencies but become apparent for frequencies different than operating band. These networks also are depicted in Fig. 8 and an example is identified as "R-C nets". Finally, the inherent stability analysis (i.e., on standard loads) was checked by applying Ohtomo's test [30].
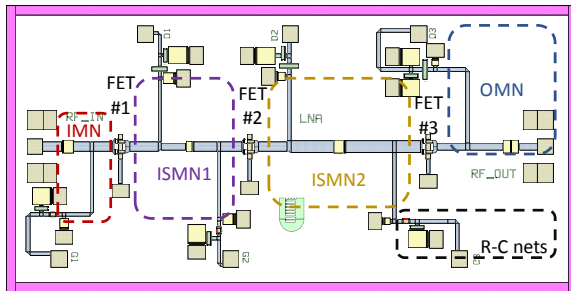

Fig. 8 MMIC layout. Chip size is 3.0 mm x 1.5mm

B. Simulated Performance and Thermal Analysis

Fig. 9 and Fig. 10 report the LNA's simulated gain and noise performance using Momentum EM analysis solver.
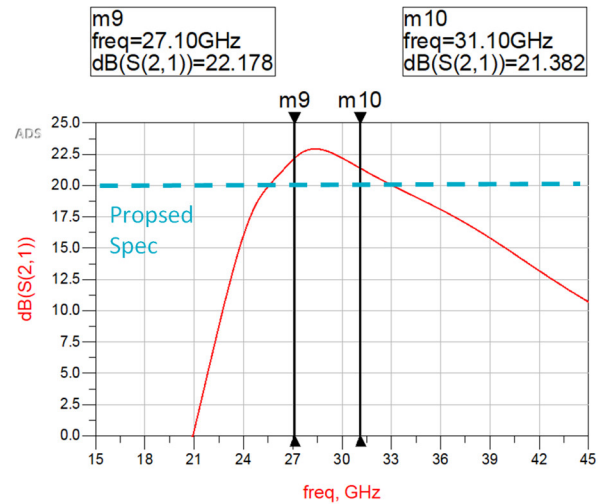

Fig. 9 MMIC LNA simulated (EM) gain

Gain is greater the specified 20dB from 25 to 33 GHz. In the design, bandwidth (27-31 GHz) the gain variation is limited in ± 0.5 dB peak-to-peak.

The noise figure (NF) is smaller than 1.75 dB from 25 to 33 GHz, practically the same bandwidth for which the gain is greater than 20 dB.
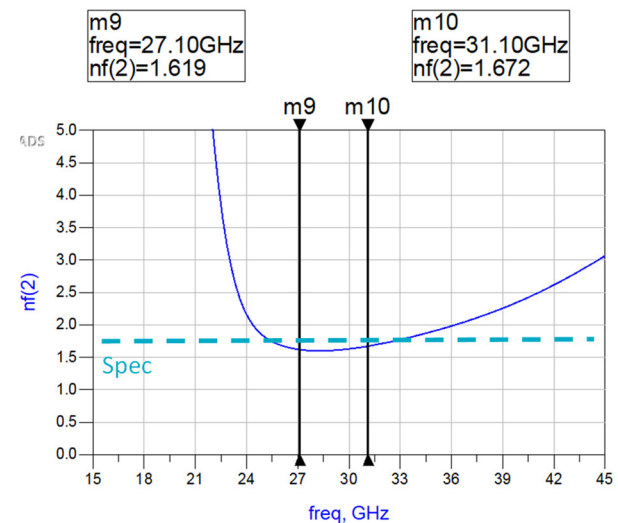

Fig. 10 MMIC LNA simulated (EM) NF

Fig. 11 reports the input and output return loss, IRL and ORL, over frequency.
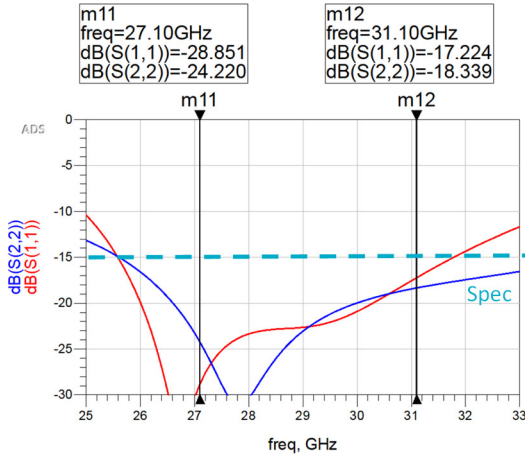
Fig. 11 MMIC LNA simulated (EM) IRL and ORL

The return loss is better than 15 dB from 26 to 32 GHz, therefore in a band slightly larger than the specified one. This result has been obtained by appropriately selecting the feedback inductance value as described in section III.0 "*C. Inductive Source Degeneration*". Non-linear behavior is evaluated in terms of 1dB gain compression point. Fig. 12 depicts the output power to input power relationship of the MMIC LNA at 31 GHz, maximum operating frequency and the corresponding nonlinear gain and gain compression.
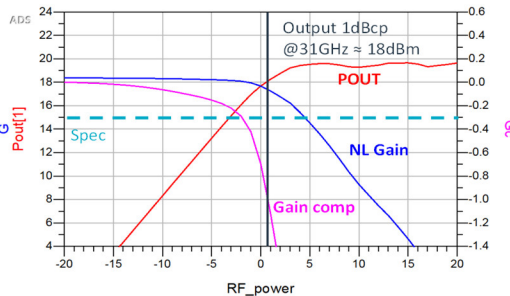

Fig. 12 MMIC LNA simulated (EM) pout-vs-pin (red curve), gain (blue curve) compression (purple curve)

1 dB gain compression point occurs for an input power just over + 2dBm. The corresponding output power level is +18 dBm, well in line with the proposed specification +15 dBm. Finally, the gate DC currents on the three transistors is given as a function of input power in Fig. 13.
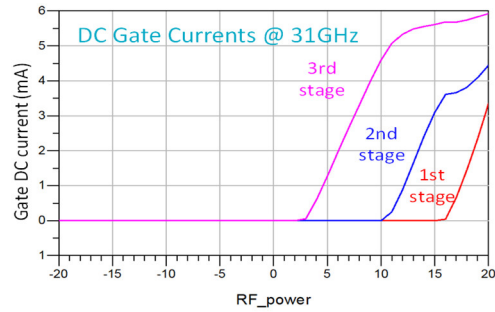

Fig. 13 MMIC LNA simulated (EM) DC

As the input power exceeds the 1dB compression point a DC component in the gate current of the final stage starts to appear. As the input power increases also the second stage (at +10dBm) and the first stage (at +16 dBm) have a DC component in the gate current. At +20 dBm input the final stage's DC gate current is 6mA. The choice of at least 4 finger devices is proved decisive since the limit is maximum 2mA/finger as reported in the maximum rating given in Table 3. A 2-finger device would not respect the maximum rating requirement. An estimation of the transistor's channel junction temperature (Tj) is provided considering the simplified expression reported in (2).

$$T_j = T_{bottom} \exp\left(R_{th@T_0} P_D / T_{ref}\right) \qquad (2)$$

The simplified relation in (2) allows to calculate the transistor's hotspot considering the baseplate temperature (T_{bottom}), the LNA's dissipated power (P_D) and the structure's thermal resistance (R_{th}). T_{ref} is set at +80°C being the maximum specified operative temperature. Considering 0.5W dissipated power in the worse RF condition (+20 dBm) we have an increase in the transistor's temperature of about 25°C with respect to base plate temperature. Consequently, the transistors operate well below the conventional 160°C maximum channel temperature. The thermal resistance (R_{th}) employed for this calculation is 40 °C/W [31], [32].

V.   BENCHMARKING

A performance comparison with recently published GaN robust LNAs operating at 30 GHz is provided in Table 4.

Table 4: Robust GaN LNA comparison table

REF	BW (GHz)	NF (dB)	P1dB (dBm)	PDC (W)	TECH.	Max Pin (W)
[33]	30-39	1.3	11		0.04 um GaN/SiC	
[34]	27-31	3.8			0.15 um GaN/SiC	2W x 6hrs pulsed
[35]	0.1-45	2.6	28	5	0.15 um GaN/SiC	
[7]	22-30	1.5	20	0.20	0.1 um GaN/Si	1W x 1min pulsed 10%
[36]	34-38	2.3	23	1.3	0.1 um GaN/Si	
THIS WORK (*)	25-33	1.7	18	0.15	0.1 um GaN/Si	0.1 CW 1W pulsed 10%

(*) simulations

The interesting performance of the proposed design is the combination of low NF, high survivability and low DC power requirement. Also, channel temperature analysis is reported in this paper to give an additional insight on the predicted reliability of the MMIC LNA. Additionally, it is designed on a Silicon substrate more suitable for high-volume productions.

VI. CONCLUSIONS

A feasibility study and the corresponding design flow for robust millimeter wave GaN LNAs is provided in this paper. Particular attention is devoted to the selection of the optimum geometry of the first stage active device. A trade-off is shown between noise performance and robustness requirements showing that, at this operating band, a 4 x 25 μm device represents a suitable trade-off between the contrasting goals of low-noise, high-power handling requirements and DC power consumption. The beneficial effects of source degenerative feedback are shown. While most designers focus on the effects falling upon the optimum input termination for gain and noise, it is here shown that the most susceptible parameter is the output termination that matches to 50 Ω the input of the transistor , when the transistor's input termination is selected to fulfill an optimum noise condition. The LNA's simulated performance are gain > 20B, NF < 1.7dB, power handling capability analyzed up to +20 dBm input power in CW operation in conjunction with low (150mW)

DC power requirement. A preliminary thermal analysis is provided showing the active devices operate well below the conventional +160°C limit even in the worst operating condition (80°C, +20 dBm input power). This design is well suited for operation in high reliability systems, such as space operation on airborne applications.

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