A Crystal-Less Programmable Clock Generator With RC-LC Hybrid Oscillator for GHz Applications in 14 nm FinFET CMOS

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***Abstract*— This paper presents a crystal-less programmable clock generator. The programmable clock generator takes advantages of both RC and LC oscillators. The frequency reference is generated by the RC oscillator without using expensive external crystals. The sawtooth signal generated from the RC oscillator is sampled by low phase-noise differential clocks which are divided from the LC oscillator. The timing information is then amplified by the sampler which uses hysteresis. An additional block, gain adjuster (GA), reduces lock time and dithering. After the system gets locked, it achieves 0.01 %/V and 25.5 ppm/°C frequency variations for 100 MHz generated clock. The 14 nm FinFET CMOS programmable clock generator draws 28 mA current from a single 1.8 V supply and occupies an active area of 0.12 mm^2. It achieves 163 dBc/Hz FoM for 100 MHz test clock.**

***Index Terms*— Crystal-less, programmable clock generator, RC oscillator, LC oscillator, metastability, FinFET.**

I. Introduction

Various types for the programmable clock generators have been proposed because they directly influence on the performance of core blocks [1]-[5]. Especially, it critically worsens jitter metrics when the jittered clock is applied to high-speed link. DLL-based oscillators are one of the best candidates for the programmable oscillator due to its better accumulating jitter performance than the PLL-based oscillators [1]. Other candidates for the programmable oscillator is based on injection techniques [2] and additional components such as MEMS or NVM [3]. All the oscillators mentioned above generate programmable clock frequency suitable for GHz applications but need an expensive and bulky external crystal oscillator which increases package cost and complexity.

To reduce the phase noise of the oscillator and compensate the frequency inaccuracy due to the temperature and supply variations simultaneously for GHz applications, this work demonstrates the RC-LC hybrid oscillator scheme without utilizing bulky crystals. The RC oscillator takes its role as a fixed reference similar as the previous RC oscillators [4], [5]. For the fixed reference, an external chip resistor is utilized in this work. Since, external chip capacitors are necessary for the clean supply in usual, adding a single chip resistor is much less burden than a crystal. The main difference from the other works is that the RC oscillator locks with the divided LC oscillator (feedback path) and utilizes the multi-modulus divided clock (output path) from the LC oscillator as a programmable clock generator. Since, high-frequency clock can be generated from the LC oscillator, it is suitable for GHz applications unlike other RC oscillators.

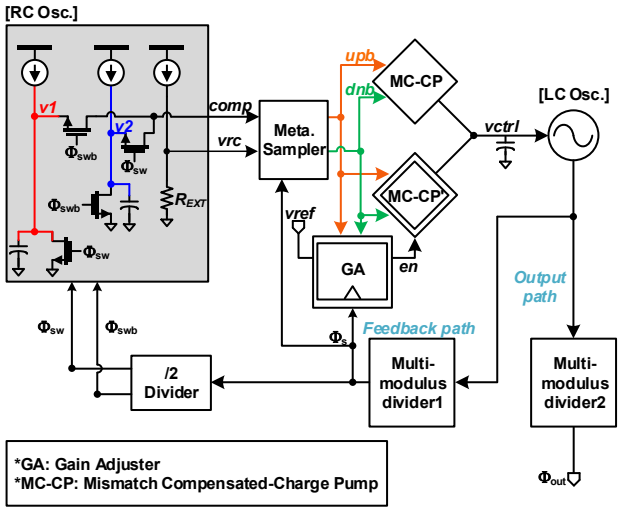

Fig. 1. Overall architecture of the proposed RC-LC hybrid oscillator.

II. Proposed RC-LC Hybrid Oscillator

A. Operating principle of the system

Fig. 1 shows the overall architecture of the hybrid oscillator. It is composed of RC and LC oscillators. As mentioned above, the RC oscillator functions as a frequency generation source and the LC oscillator generates the relatively lower phase-noise reference than the sawtooth wave generated from the RC oscillator. From the frequency difference between the RC oscillator and the divided clock from the LC oscillator, the timing difference is converted to pulses, *upb* and *dnb*, by the sampler with metastable block using hysteresis. The pulse signals, *upb* and *dnb*, are converted to current by the charge pump (CP). Then, the pull-up and pull-down current mismatch is compensated by the mismatch compensation block (MC). Accumulated control voltage, *vctrl*, is then applied to the

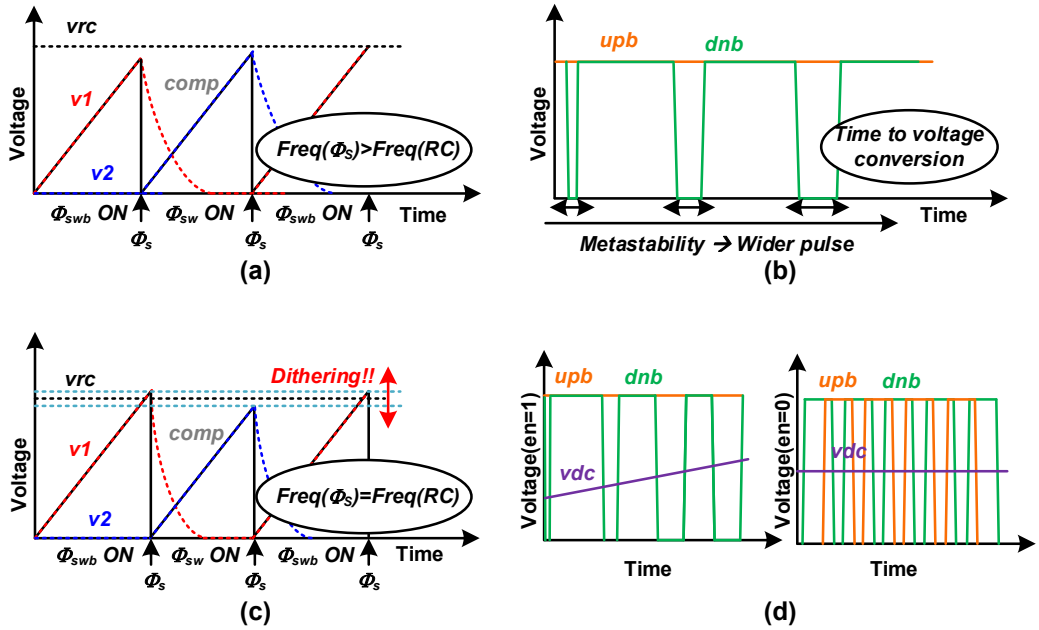

Fig. 2. Locking behavior when the sampling frequency is higher than the RC oscillator: (a) waveform of the node *v1*, *v2*, and *comp*, (b) pulse waveform of the *upb* and *dnb*, (c) dithering phenomenon of the locked oscillator, and (d) function of the GA.

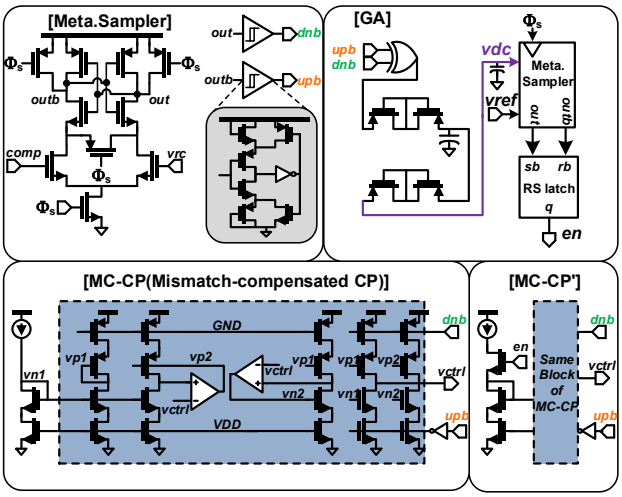

Fig. 3. Schematics of the core blocks (Sampler, GA, MC-CP, and MC-CP').

PMOS varactors of the LC oscillator. In addition, for the less dithering phenomenon and faster lock time, the auxiliary blocks such as the gain adjuster (GA) and the other mismatch-compensated charge pump (MC-CP') for the GA are also designed.

Fig. 2 shows the detailed locking waveform of the RC-LC hybrid oscillator. To eliminate the RC discharging time, divided-by-2 clocks (Φ_{sw}, Φ_{swb}) from the sampling clock (Φ_s) are used similarly with [7]. When Φ_{swb} is on, voltage of the node *comp* becomes *v1*. Voltage of the node *comp* becomes *v2* on the contrary. While the frequency of the sampling clock(Φ_s) is higher than the frequency of the RC oscillator as shown in Fig. 2(a), timing difference is sampled by a strong-arm latch. Since the sampled value is small to offer the timing information, it gets amplified by inverter-based hysteresis blocks. The pulse width gets wider when the sampler and hysteresis blocks enter deeper into the metastable state as described in Fig. 2(b). However, after being locked, dithering phenomenon happens as shown in Fig. 2(c) since the sampler has bang-bang characteristics. Fig. 2(d) shows the function of GA which adjusts the gain efficiently.

B. Circuit implementation

Detailed circuit implementations of sub blocks are illustrated in Fig. 3. For the conversion between phase error and pulse width, strong-arm latch and hysteresis inverter are utilized. Offset calibrating switch transistor is included in the strong-arm latch. In addition, to solve the dithering issue, GA is designed. It gets the dc value of the *upb* and *dnb* by a XOR gate which is then low-pass filtered. The other strong-arm latch in the GA compares the average dc voltage, *vdc* and the reference voltage, *vref*. It gives the GA enabling signal, *en*, using an RS latch. Due to its gain adjusting, it not only reduces dithering after it gets locked but also lock time when the GA enabling signal is on. To get rid of the mismatch between current for *upb* and *dnb*, the charge pump is designed similarly as [6]. For the process variation, a multi-modulus divider is located in the feedback path of the hybrid oscillator. In addition, the other multi-modulus divider is included for various SoC applications.

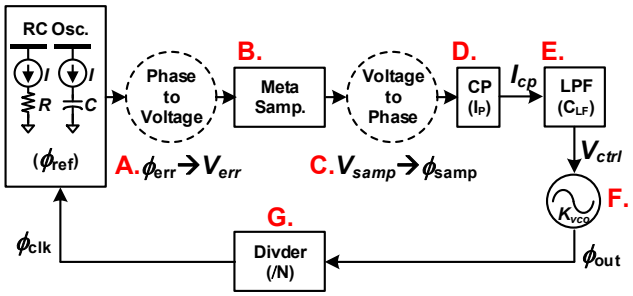

Fig. 4. Modeling for the loop analysis.

TABLE I. FACTORS OF THE TRANSFER FUNCTION

	Factor	Transfer function(s)	Derivation
A	$\frac{V_{err}}{\phi_{err}}$	$\frac{IR}{2\pi}s$	Laplace transform
B	$\frac{V_{samp}}{V_{err}}$	$\frac{1}{s^2\tau_{s1}\tau_{s2}}(\times\frac{\alpha}{s^2})$	Small-signal model Approx.
C	$\frac{\phi_{samp}}{V_{samp}}$	$2\pi\frac{C_{out}V_{TP}/(0.5I_{samp})}{RC}\frac{2}{V_{od}}$	Taylor series Approx.
D	$\frac{I_{cp}}{\phi_{samp}}$	$\frac{I_P}{2\pi}$	Charge pump
E	$\frac{V_{ctrl}}{I_{cp}}$	$\frac{1}{sC_{LF}}$	Loop filter
F	$\frac{\phi_{out}}{V_{ctrl}}$	$\frac{K_{vco}}{s}$	LC VCO
G	$\frac{\phi_{clk}}{\phi_{out}}$	$\frac{1}{N}$	Divider

C. *Loop analysis of the proposed oscillator*

Since the system has two types of oscillator in a feedback loop, the transfer function of the system is analyzed in this part for the stability. Simplified behavioral model is described in Fig. 4. To simplify the analysis, the transfer function is divided into seven factors, A through G. Factor A is derived from Laplace transform of the voltage difference between *comp* and *vrc*. While factor B and C are related to strong-arm latch, they are approximated based on [8]. For simplicity, switch transistor in the strong-arm latch for offset cancellation is not considered in calculation. Furthermore, hysteresis inverter can be also approximated to the second order transfer function or ignored. Lastly, factor D, E, F, and G are easily derived which are commonly used in conventional PLLs. Each factors are derived and summarized in Table I. The overall transfer function of the system is then calculated as

$$\frac{\phi_{clk}}{\phi_{err}} = \frac{f(I, C^{-1}, I_{samp}, I_P, C_{LF}^{-1}, N^{-1}, K_{vco})}{s^3(s^5)}. \quad (1)$$

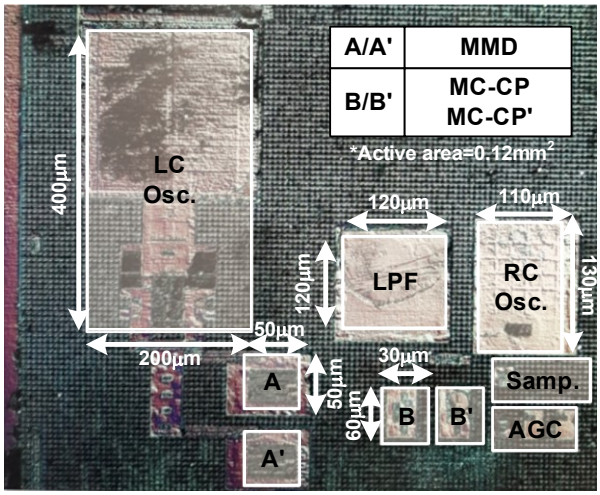

Fig. 5. Chip micrograph of the RC-LC hybrid oscillator with stripped top metal.

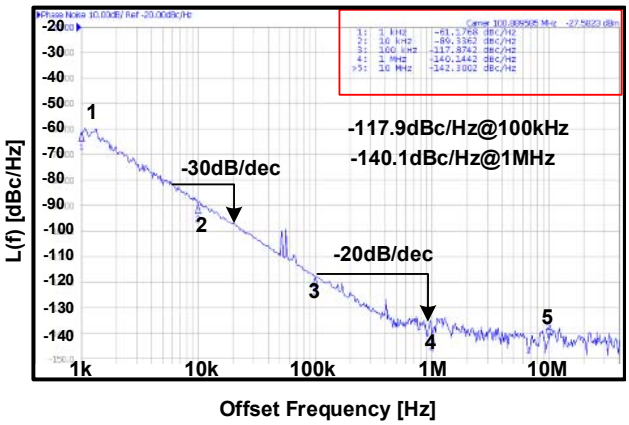

Fig. 6. Measured phase noise for 100 MHz test output.

The open-loop transfer function has three or five poles at the origin which shows that the system is stable for the phase lock.

III. MEASUREMENT RESULTS

The RC-LC hybrid oscillator is fabricated in 14 nm FinFET CMOS and assembled in a QFN package. Fig. 5 shows the chip micrograph of the programmable clock generator. The active area of the chip is 0.12 mm^2 while the LC oscillator occupies 0.08 mm^2 which is much smaller than the other LC-type compensated oscillators. Fig. 6 shows the measured phase noise. The phase noise of the 100 MHz test output is -117.9 dBc/Hz and -140.1 dBc/Hz at 100 kHz and 1 MHz offset respectively with -27.6 dBm carrier power by the E5052B signal source analyzer. Timing metrics, period jitter is also measured for the 100 MHz test clock as described in Fig. 7. It gives 3.7 ps (rms) and 35.9 ps (peak-to-peak) period jitter for 1.15 M hits. Fig. 8 shows frequency variations due to supply and temperature for 3 sample chips. The hybrid oscillator has 0.01 %/V and 25.5 ppm/°C with the range of 1.1~2.0 V and -20~120 °C, respectively. The oscillator consumes the power of

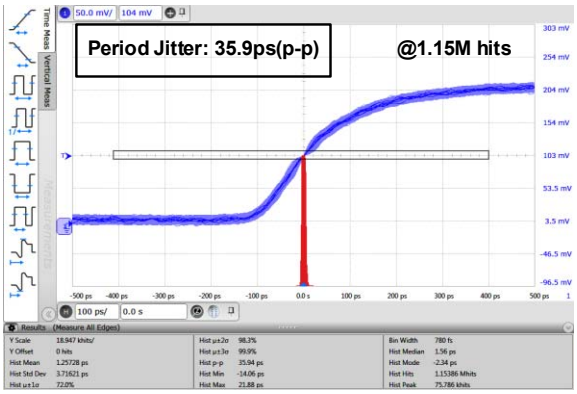

Fig. 7. Measured period jitter for 100 MHz test output for 1.15 M hits.

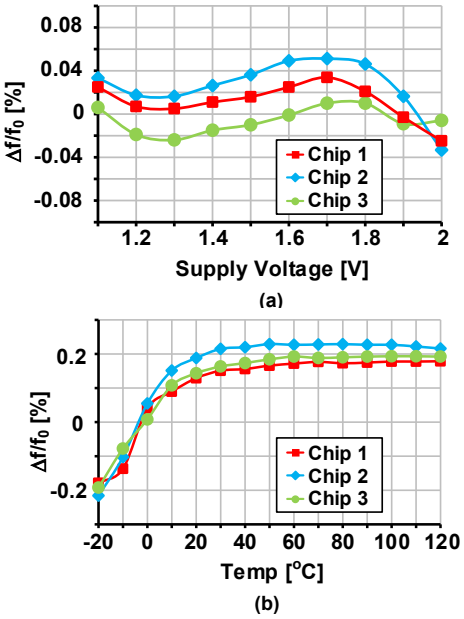

Fig. 8. (a)Measured supply variations and (b) temperature variations for 3 samples.

50.4 mW with a single 1.8 V supply. Table II shows the performance summary and comparisons with the other state-of-the-art programmable clock generators. Compared with the other programmable oscillators, it achieves 163 dBc/Hz FoM_1 and 289 dB FoM_2, respectively.

IV. Conclusions

This paper newly proposes the structure which is RC-LC hybrid oscillator to generate programmable clock. As a result, it is tolerant to supply and temperature variations and has low phase noise. The hybrid oscillator fabricated in 14 nm FinFET CMOS has 0.01 %/V and 25.5 ppm/°C frequency variations for 100 MHz test output. Furthermore, the FoM_1 related to the phase noise and power consumption of the hybrid oscillator is 163 dBc/Hz at 1 MHz offset that is better than the other state-of-the-arts oscillators. Since, all transistors are implemented with thick-gate FETs to prevent leakage from

TABLE II. Performance Comparison

	EL'14 [1]	TCASI'15 [2]	ISSCC'12 [3]	ISSCC'13 [4]	ISSCC'16 [5]	This Work
CMOS Tech. [nm]	130	65	180	65	180	14nm FinFET
Area [mm^2]	0.018	0.062	0.63	0.01	0.015	0.12
Test Freq. [Hz]	1.5G	96M	100M	12.6M	10.5M	100M
Power [W]	9m	1.9m	109m	0.1m	0.22m	50.4m
Temp Variation [ppm/°C]	N/A	N/A	0.008 (-40~85°C)	205 (0~80°C)	137 (-40~125°C)	25.5 (-20~120°C)
Supply Variation [%/V]	N/A	N/A	N/A	0.35 (1.1~1.5V)	4.4 (1.4~2.0V)	0.01 (1.1~2.0V)
FoM1 [dBc/Hz] @1MHz	N/A	169	160	152	162	163
FoM2 [dB]	N/A	N/A	N/A	238	228	289
Type	DLL	INJ	MEMS	RC	RC	RC LC

$$FoM_1 = \left| L(\Delta f) + 20\log(\frac{\Delta f}{f_o}) + 10\log(\frac{P}{1mW}) \right|$$

$$FoM_2 = \left| L(\Delta f) + 10\log\left\{ (\frac{\Delta f}{f_o})^2 \frac{P_{diss}}{1mW} \times \Delta Temp_{ppm} \times (\Delta Volt_{percent})^2 \right\} \right|$$

FETs, FoMs can be further improved for the future prototype. In addition, an external chip resistor can be replaced with low temperature coefficient resistor provided by the process in the future work [7]. Lastly, this work can be further developed by a higher frequency LC oscillator for multi-GHz applications.

Acknowledgment

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