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Reconfigurable Gate Driver Toward High-Power Efficiency and High-Power Density Converters

Thèse

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Résumé

Les systèmes de gestion de l'énergie exigent des convertisseurs de puissance pour fournir une conversion de puissance adaptée à diverses utilisations. Il existe différents types de convertisseurs de puissance, tel que les amplificateurs de puissance de classe D, les demi-ponts, les ponts complets, les amplificateurs de puissance de classe E, les convertisseurs buck et dernièrement les convertisseurs boost. Prenons par exemple les dispositifs implantables, lorsque l'énergie est prélevée de la source principale, des convertisseurs de puissance buck ou boost sont nécessaires pour traiter l'énergie de l'entrée et fournir une énergie propre et adaptée aux différentes parties du système. D'autre part, dans les stations de charge des voitures électriques, les nouveaux téléphones portables, les stimulateurs neuronaux, etc., l'énergie sans fil a été utilisée pour assurer une alimentation à distance, et des amplificateurs de puissance de classe E sont développés pour accomplir cette tâche. Les amplificateurs de puissance de classe D sont un excellent choix pour les casques d'écoute ou les haut-parleurs en raison de leur grande efficacité. Dans le cas des interfaces de capteurs, les demi-ponts et les ponts complets sont les interfaces appropriées entre les systèmes à faible et à forte puissance. Dans les applications automobiles, l'interface du capteur reçoit le signal du côté puissance réduite et le transmet à un réseau du côté puissance élevée. En outre, l'interface du capteur doit recevoir un signal du côté haute puissance et le convertir vers la côté basse puissance. Tous les systèmes mentionés ci-dessus nécessitent l'inclusion d'un pilote de porte spécifique dans les circuits, selon les applications. Les commandes de porte comprennent généralement un décalage du niveau de commande niveau supérieur, le levier de changement de niveau inférieur, une chaîne de tampon, un circuit de verrouillage sous tension, un circuit de temps mort, des portes logiques, un inverseur de Schmitt et un mécanisme de démarrage. Ces circuits sont nécessaires pour assurer le bon fonctionnement des systèmes de conversion de puissance. Un circuit d'attaque de porte reconfigurable prendrait en charge une vaste gamme de convertisseurs de puissance ayant une tension d'entrée V_{IN} et un courant de sortie I_{Load} variables.

L'objectif de ce projet est d'étudier intensivement les causes de différentes pertes dans les convertisseurs de puissance et de proposer ensuite de nouveaux circuits et méthodologies dans les différents circuits des conducteurs de porte pour atteindre une conversion de puissance avec une haute efficacité et densité de puissance. Nous proposons dans cette thèse de nouveaux circuits de gestion des temps mort, un Shapeshifter de niveau plus élevé et un Shapeshifter de

niveau inférieur avec de nouvelles topologies qui ont été pleinement caractérisées expérimentalement. De plus, l'équation mathématique du temps mort optimal pour les faces haute et basse d'un convertisseur buck est dérivée et expérimentalement prouvée. Les circuits intégrés personnalisés et les méthodologies proposées sont validés avec différents convertisseurs de puissance, tels que les convertisseurs semi-pont et en boucle ouverte, en utilisant des composants standard pour démontrer leur supériorité sur les solutions traditionnelles. Les principales contributions de cette recherche ont été présentées à sept conférences prestigieuses, trois articles évalués par des pairs, qui ont été publiés ou présentés, et une divulgation d'invention.

Une contribution importante de ce travail recherche est la proposition d'un nouveau générateur actif CMOS intégré dédié de signaux sans chevauchement. Ce générateur a été fabriqué à l'aide de la technologie AMS de $0.35\mu m$ et consomme $16.8mW$ à partir d'une tension d'alimentation de $3.3V$ pour commander de manière appropriée les côtés bas et haut d'un demi-pont afin d'éliminer la propagation. La puce fabriquée est validée de façon expérimentale avec un demi-pont, qui a été mis en œuvre avec des composants disponibles sur le marché et qui contrôle une charge R-L. Les résultats des mesures montrent une réduction de 40% de la perte totale d'un demi-pont de $45V$ d'entrée à $1MHz$ par rapport au fonctionnement du demi-pont sans notre circuit intégré dédié. Le circuit principal du circuit d'attaque de grille côté haut est le décaleur de niveau, qui fournit un signal de grande amplitude pour le commutateur de puissance côté haut. Une nouvelle structure de décalage de niveau avec un délai de propagation minimal doit être présentée. Nous proposons une nouvelle topologie de décalage de niveau pour le côté haut des drivers de porte afin de produire des convertisseurs de puissance efficaces. Le SL présente des délais de propagation mesurés de $7.6ns$. Les résultats mesurés montrent le fonctionnement du circuit présenté sur la plage de fréquence de $1MHz$ à $130MHz$. Le circuit fabriqué consomme $31.5pW$ de puissance statique et $3.4pJ$ d'énergie par transition à $1kHz$, $V_{DDL} = 0.8V$, $V_{DDH} = 3.0V$, et une charge capacitive $C_L = 0.1pF$. La consommation énergétique totale mesurée par rapport à la charge capacitive de 0.1 à $100nF$ est indiquée. Un autre nouveau décalage vers le bas est proposé pour être utilisé sur le côté bas des pilotes de portes. Ce circuit est également nécessaire dans la partie R_x du réseau de bus de données pour recevoir le signal haute tension du réseau et délivrer un signal de faible amplitude à la partie basse tension. L'une des principales contributions de ces travaux est la proposition d'un modèle de référence pour l'abaissement de niveau à puissance unique reconfigurable. Le circuit proposé pilote avec succès une gamme de charges capacitives allant de $10fF$ à $350pF$. Le circuit présenté consomme des puissances statiques et dynamiques de $62.37pW$ et $108.9\mu W$, respectivement, à partir d'une alimentation de $3.3V$ lorsqu'il fonctionne à $1MHz$ et pilote une charge capacitive de $10pF$. Les résultats de la simulation post-layout montrent que les délais de propagation de chute et de montée dans les trois configurations sont respectivement de l'ordre de 0.54 à $26.5ns$ et de 11.2 à $117.2ns$. La puce occupe une surface de $80\mu m \times 100\mu m$. En effet, les temps morts des côtés hauts et bas varient en raison de la différence de fonctionnement des commutateurs de puissance côté haut et côté bas, qui

sont respectivement en commutation dure et douce. Par conséquent, un générateur de temps mort reconfigurable asymétrique doit être ajouté aux pilotes de portes traditionnelles pour obtenir une conversion efficace. Notamment, le temps mort asymétrique optimal pour les côtés hauts et bas des convertisseurs de puissance à base de Gan doit être fourni par un circuit de commande de grille reconfigurable pour obtenir une conception efficace. Le temps mort optimal pour les convertisseurs de puissance dépend de la topologie. Une autre contribution importante de ce travail est la dérivation d'une équation précise du temps mort optimal pour un convertisseur buck. Le générateur de temps mort asymétrique reconfigurable fabriqué sur mesure est connecté à un convertisseur buck pour valider le fonctionnement du circuit proposé et l'équation dérivée. De plus le rendement d'un convertisseur buck typique avec T_{DLH} minimum et T_{DHL} optimal (basé sur l'équation dérivée) à $I_{Load} = 25mA$ est amélioré de 12% par rapport à un convertisseur avec un temps mort fixe de $T_{DLH} = T_{DHL} = 12ns$.

Abstract

Power management systems require power converters to provide appropriate power conversion for various purposes. Class D power amplifiers, half and full bridges, class E power amplifiers, buck converters, and boost converters are different types of power converters. Power efficiency and density are two prominent specifications for designing a power converter. For example, in implantable devices, when power is harvested from the main source, buck or boost power converters are required to receive the power from the input and deliver clean power to different parts of the system. In charge stations of electric cars, new cell phones, neural stimulators, and so on, power is transmitted wirelessly, and Class E power amplifiers are developed to accomplish this task. In headphone or speaker driver applications, Class D power amplifiers are an excellent choice due to their great efficiency. In sensor interfaces, half and full bridges are the appropriate interfaces between the low- and high-power sides of systems. In automotive applications, the sensor interface receives the signal from the low-power side and transmits it to a network on the high-power side. In addition, the sensor interface must receive a signal from the high-power side and convert it down to the low-power side. All the above-summarized systems require a particular gate driver to be included in the circuits depending on the applications. The gate drivers generally consist of the level-up shifter, the level-down shifter, a buffer chain, an under-voltage lock-out circuit, a deadtime circuit, logic gates, the Schmitt trigger, and a bootstrap mechanism. These circuits are necessary to achieve the proper functionality of the power converter systems. A reconfigurable gate driver would support a wide range of power converters with variable input voltage V_{IN} and output current I_{Load}. The goal of this project is to intensively investigate the causes of different losses in power converters and then propose novel circuits and methodologies in the different circuits of gate drivers to achieve power conversion with high-power efficiency and density. We propose novel deadtime circuits, level-up shifter, and level-down shifter with new topologies that were fully characterized experimentally. Furthermore, the mathematical equation for optimum deadtimes for the high and low sides of a buck converter is derived and proven experimentally. The proposed custom integrated circuits and methodologies are validated with different power converters, such as half bridge and open loop buck converters, using off-the-shelf components to demonstrate their superiority over traditional solutions. The main contributions of this research have been presented in seven high prestigious conferences, three peer -reviewed articles, which have been

published or submitted, and one invention disclosure.

An important contribution of this research work is the proposal of a novel custom integrated CMOS active non-overlapping signal generator, which was fabricated using the $0.35-\mu m$ AMS technology and consumes $16.8mW$ from a $3.3-V$ supply voltage to appropriately drive the low and high sides of the half bridge to remove the shoot-through. The fabricated chip is validated experimentally with a half bridge, which was implemented with off-the-shelf components and driving a R-L load. Measurement results show a 40% reduction in the total loss of a $45-V$ input $1-MHz$ half bridge compared with the half bridge operation without our custom integrated circuit. The main circuit of high-side gate driver is the level-up shifter, which provides a signal with a large amplitude for the high-side power switch. A new level shifter structure with minimal propagation delay must be presented. We propose a novel level shifter topology for the high side of gate drivers to produce efficient power converters. The LS shows measured propagation delays of $7.6ns$. The measured results demonstrate the operation of the presented circuit over the frequency range of $1MHz$ to $130MHz$. The fabricated circuit consumes $31.5pW$ of static power and $3.4pJ$ of energy per transition at $1kHz$, $V_{DDL} = 0.8V$, $V_{DDH} = 3.0V$, and capacitive load $C_L = 0.1pF$. The measured total power consumption versus the capacitive load from $0.1pF$ to $100nF$ is reported. Another new level-down shifter is proposed to be used on the low side of gate drivers. Another new level-down shifter is proposed to be used on the low side of gate drivers. This circuit is also required in the R_x part of the data bus network to receive the high-voltage signal from the network and deliver a signal with a low amplitude to the low-voltage part. An essential contribution of this work is the proposal of a single supply reconfigurable level-down shifter. The proposed circuit successfully drives a range of capacitive load from $10fF$ to $350pF$. The presented circuit consumes static and dynamic powers of $62.37pW$ and $108.9\mu W$, respectively, from a $3.3-V$ supply when working at $1MHz$ and drives a $10pF$ capacitive load. The post-layout simulation results show that the fall and rise propagation delays in the three configurations are in the range of $0.54-26.5ns$ and $11.2-117.2ns$, respectively. Its core occupies an area of $80\mu m \times 100\mu m$. Indeed, the deadtimes for the high and low sides vary due to the difference in the operation of the high- and low-side power switches, which are under hard and soft switching, respectively. Therefore, an asymmetric reconfigurable deadtime generator must be added to the traditional gate drivers to achieve efficient conversion. Notably, the optimal asymmetric deadtime for the high and low sides of GaN-based power converters must be provided by a reconfigurable gate driver to achieve efficient design. The optimum deadtime for power converters depends on the topology. Another important contribution of this work is the derivation of an accurate equation of optimum deadtime for a buck converter. The custom fabricated reconfigurable asymmetric deadtime generator is connected to a buck converter to validate the operation of the proposed circuit and the derived equation. The efficiency of a typical buck converter with minimum T_{DLH} and optimal T_{DHL} (based on the derived equation) at $I_{Load} = 25mA$ is improved by 12% compared to a converter with a fixed deadtime of $T_{DLH} = T_{DHL} = 12ns$.

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To my wife, Fatemeh,
my parents, Mohtaram and
Malekmohammad, and
all members of my family

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Avant-propos

This dissertation is based on materials that are published or under review in prestigious IEEE Journals and Conferences. Chapter 2 includes papers under review for publication in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems. Chapter 3 includes previously published materials in IEEE Transactions on Circuits and Systems I: Regular Papers. Chapter 4 of this thesis includes a material previously published in IEEE International Symposium on Circuits and Systems. Chapter 5 of this thesis includes papers under review for publication in IEEE Transactions on Circuits and Systems I: Regular Papers. The text and the figures were modified to adopt the thesis template. The papers present the core of this research and include the main contributions. However, throughout this dissertation, several conferences and journals have been published in IEEE. I elaborate my contributions to the one conference paper in Chapter 4, and three transactions are reflected in Chapters 2, 3, and 5.

Paper 1: M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, "A 7.6-ns Delay Subthreshold Level-Shifter Leveraging Parasitic Capacitance Data-dependent Current Source," in IEEE Transactions on VLSI Systems, Submitted. This paper presents a novel high-performance level-up shifter, which is convenient for the high side of gate drivers for implementing a power converter. The custom integrated circuit is tested, and the circuit is fully characterized. I personally propose this novel level shifter under the supervision of Prof. B. Gosselin. The measurement and experimental results were obtained at the Smart Biomedical Microsystem Lab. at Laval University under the supervision of Prof. B. Gosselin and the Polystim Neurotechnology Laboratory, Polytechnique Montreal, under the supervision of Prof. Mohamad Sawan. In this work, the measured results verify a shorter propagation delay and lower power consumption than similar works. Prof. Benoit Gosselin, Dr. M. Ali, Dr. A. Hassan, and Prof. Mohamad Sawan extensively revised the paper's content by adding materials and corrections.

Paper 2: M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, "An Active Dead-Time Control Circuit with Timing Elements for a 45-V Input 1-MHz Half-Bridge Converter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 1, pp. 30–41, Jan. 2022. This paper presents a new non-overlapping signal generator to provide appropriate signals for the low- and high-sides of a half bridge. The fabricated chip was validated with an implemented half bridge with off-the-shelf components. I proposed the main idea of the paper

under the supervision of Prof. B. Gosselin. The measurement and experimental results were obtained at Smart Biomedical Microsystem Lab. at Laval University under the supervision of Prof. B. Gosselin. In this work, the reduction of half bridge total loss was proven experimentally through a comparison with a half bridge operation without the fabricated chip. Prof. Benoit Gosselin, Dr. M. Ali, Dr. A. Hassan, and Prof. Mohamad Sawan extensively revised the paper's content by adding materials and corrections.

Paper 3: M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, "A Reconfigurable Single-Supply Multiple-Level Down-Shifter for System-on-Chip Applications," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 2021, pp. 1–5. In this paper, a tunable multi-level down shifter is presented, where only a single supply is required. This novel circuit is utilized as interface between the high-voltage side (data bus network) and the low-voltage side (processors with different supplies). I proposed the main idea of this work under the supervision of Prof. Benoit Gosselin. I prepared the manuscript, and Prof. Benoit Gosselin, Dr. M. Ali, Dr. A. Hassan, and Prof. Mohamad Sawan revised the paper's content by adding materials and corrections.

Paper 4: M. Karimi, M. Ali, A. Aghajani, A. Hassan, M. Sawan, and B. Gosselin, "A 9.2-ns to 1-us Digitally Controlled Multi-Tuned Deadtime Optimization for Efficient GaN HEMT Power Converters" in IEEE Transactions on Circuits and Systems I: Regular Papers, submitted (Invited paper - special issue NEWCAS 2021). In this paper, a multi-tuned deadtime optimization is presented. The fabricated chip is connected to a gate driver that drives two superimposed GaN HEMT power switches. The reconfigurable part of the fabricated chip is controlled digitally to provide asymmetric deadtimes for a buck converter with variable input voltage V_{IN} and output current I_{OUT}. The deadtimes are generated based on an accurate derived equation. I proposed the main idea of the paper under the supervision of Prof. Benoit Gosselin. The measurement and experimental results were obtained at Smart Biomedical Microsystem Lab. at Laval University under the supervision of Prof. B. Gosselin. The measured results show the priority of our presented buck converter over recent published works. Prof. Benoit Gosselin, Dr. M. Ali, Dr. A. Hassan, and Prof. Mohamad Sawan extensively revised the paper's content by adding materials and corrections. Amir Aghajani contributed to the derivation of the mathematical equations and the achievement of the experimental results.

Introduction

Power converters are the key elements of the growing field of power management units that provide different supply voltage and current values to various electronic blocks from various energy sources [10]. Batteries as an energy source example are used in most electronic devices, including laptops, cell phones, and cameras, to power up their internal blocks, such as processors, displays, and analog circuitry, which require different voltages [11]. Figure 0.1 shows various energy sources in different applications where DC–DC conversion is required to provide appropriate power supplies to their internal blocks, such as processors, sensors, and electronic control units [12]. Some blocks require a higher voltage than the battery voltage, and some require a lower voltage than that of the battery. The battery voltage may be $1.5V$, with the digital and analog blocks requiring $1-$ and $3-V$ supplies, respectively. Therefore, DC–DC power converters are essential for providing lower or higher voltages than that of the battery. The converter used to provide a lower voltage than that of the battery is known as a buck converter, while that which provides a higher voltage than that of the battery is called a boost converter [13; 14]. Implantable biomedical devices, such as optical stimulators, are usually supplied by a small coin battery with a low output voltage, ranging from $1V$ to $1.5V$, while the required voltage and current for optogenetic stimulation are approximately $4V$ and $20mA$, respectively. Therefore, a DC–DC boost converter must be employed to meet the requirement [15]. Headphone amplifiers are generally expected to have very low noise levels and high linearity for good audio quality, naturally implying high power consumption. In mobile applications, a trade-off must be made between audio quality and battery life due to limited battery capacity. In these applications, high-efficiency Class D amplifiers are essential to decrease the total loss and consequently address the requirement of providing longer battery lifetime and increase the quality of audio [16].

In wireless power transmission applications, two inductive coils must be mutually coupled for wireless power transfer. The primary coil must be in the transmitter output, and the secondary coil must be in the receiver input. The coil is the output component in the topology of Class E power amplifiers, satisfying the easy coupling requirement with the secondary coil in the receiver side. In addition, the efficiency of Class E power amplifiers makes them suitable for wireless power transmission applications [17]. In sensor interface applications, two sides of low and high powers require an interface to communicate. The suitable interfaces in these

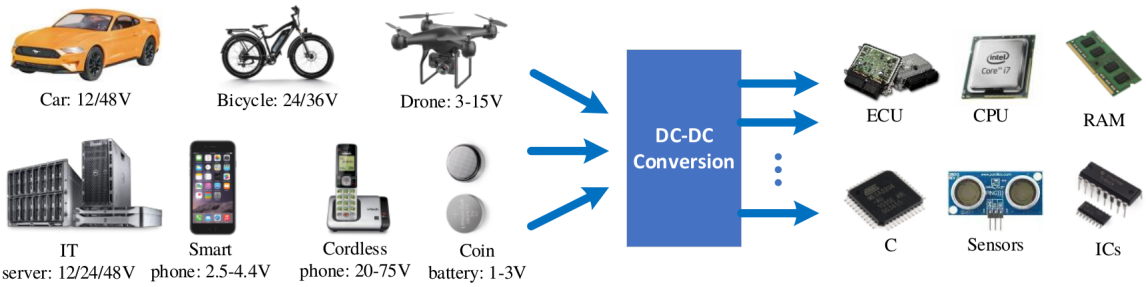


Figure 0.1: Different energy sources, DC-DC conversion, and IC level voltages.

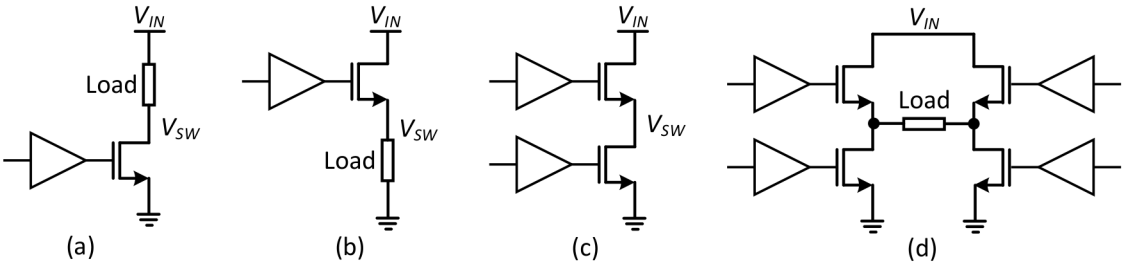


Figure 0.2: Different power switch configurations, (a) Low-Side, (b) High-Side, (c) Half-Bridge, (d) Full-Bridge (H-Bridge).

applications are half and full bridges. The sensor interface is used in automotive applications. In this application, the low voltage side is a processor, and the high voltage side is a network. The equivalent circuit of the network is a R-L load. A half/full bridge would play the role of an interface for receiving the low voltage signal and driving the high voltage side appropriately [18]. The buck–boost configuration is presented to provide a DC voltage that is lower or higher than that of the battery with an opposite polarity (e.g., providing $-2V$ from the $1.5-V$ battery), and the non-inverting flyback converter in which a single circuit provides both higher and lower voltages than the battery's voltage with the same polarity (e.g., providing either 2 or $1V$ from a $1.5-V$ battery) [19].

Various Topologies of Power Converters

Various topologies of power converters are adopted for different applications and purposes. Power converters consist of gate drivers and power switches. Figure 0.2 presents different configurations of power switches. The power transistors can be on-chip (integrated) or discrete (external). To implement integrated power switches for carrying high current, the width (W) of the power switch must be sufficiently large to have a low $R_{DS(on)}$. However, the gate capacitance will be increased when the W increases. Especially for fast switching, the power converter experiences losses. Therefore, a trade-off must be achieved between the $R_{DS(on)}$ and

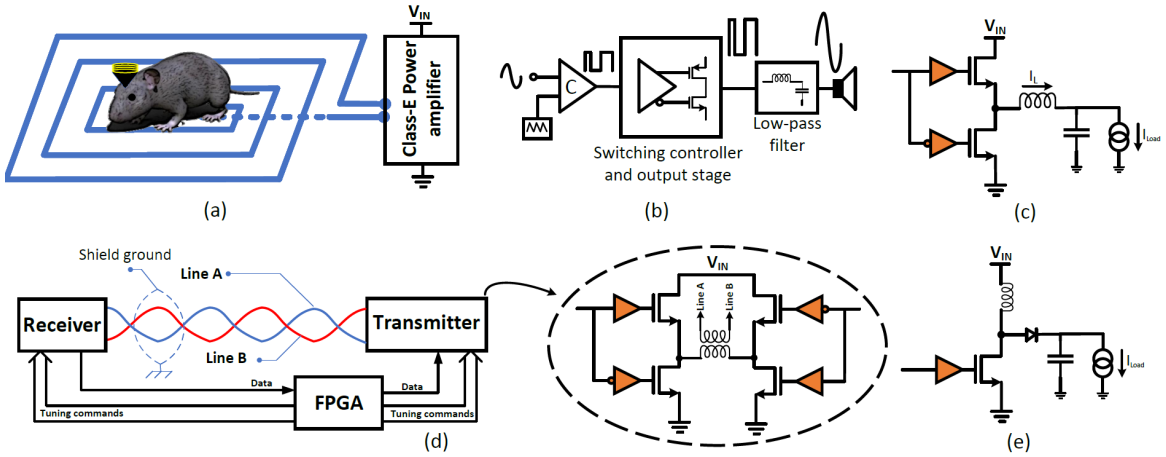


Figure 0.3: General block diagram of different power converters in various applications, (a) Class-E power amplifier for wireless power transmission for freely moving animals, (b) Class-D power amplifier for speaker, (c) Buck converter configuration, (d) Full-Bridge (H-Bridge) for data bus network, (e) Boost converter configuration.

C_{Gate} of the power switch. In high-power and -voltage applications, n-type transistors are preferred due to their low on-resistance $R_{DS(on)}$, but the gate supply should be greater than V_{IN} for high-side n-type power switches for appropriate operation. To elaborate, holes are charge carriers with approximately 2 to 3 times lower mobility than electrons, and to obtain the same On-Resistance $R_{DS(on)}$, the p-type W must be 2 to 3 times larger than that of the n-type, resulting in 2 to 3 times more charge gathering in the transistor gate. Consequently, p-type MOSFETs will have a low thermal resistance and a high current rating, which will affect the dynamic performance. Therefore, a convenient power MOSFET must be selected by considering the appropriate $R_{DS(on)}$ and gate charge. Actually, depending on the switching frequency in different applications, the device on-resistance $R_{DS(on)}$ and the gate charge Q_g are considered in MOSFET selection [20].

$$Q_g = \int_{t_0}^{t_s} \frac{V_{DR}}{R_G} e^{-\frac{t}{R_G C_{eff}}} dt \tag{1}$$

Equation 1 shows the gate charge, where V_{DR} is the peak value of the gate drive voltage, and Ceff is the effective gate input capacitance. $R_{ds(on)}$ is obtained by $R_{ON} = R_{silicon} + R_{wire} + R_{lead}$, where $R_{silicon}$ = inherent resistance from silicon process, R_{wire} = bond wire resistance, and R_{lead} = resistance of the lead frame. Texas Instrument released a detailed application report on June 2016 to explain the importance of $R_{ds(on)}$ [20].

In Parts (a) and (b) of Figure 0.2, the power switch is used in the low and high sides of the converter, respectively. Figure 0.2.c shows the half-bridge configuration, and Figure 0.2.d presents the full-bridge (H-bridge) configuration, which consists of two half-bridges. Fig. 3

presents the general block diagram of different power converters in some applications. Figure 0.3.a shows a wireless power transmission (WPT) system that is used for freely moving animals. For the part of the system that is implanted in the head-stage of the animal for brain stimulation study, the WPT system must continuously transfer power wirelessly. For WPT implementation, a printed spiral coil would be used to propagate the magnetic flux for the receiver coil inside the head-stage. A Class E power amplifier with a specific gate driver is utilized to perform the functionality appropriately and deliver the power to a given distance [21]. Figure 0.3.b presents the general block diagram of a Class D power amplifier, which is mostly applicable for headphones and speakers. In this design, the weak sinewave of the input signal is compared with a sawtooth waveform, and the results are applied to the switching controller and output stage (SCOS) block. In the SCOS part, a particular gate driver is designed to generate a high-amplitude pulse for the low pass filter. Finally, the extracted high-amplitude sinewave signal is applied to the speaker [22]. Figure 0.3.c shows the general block diagram of a buck converter. In the last stage of this topology, two power switches are used. Afterward, a LC low pass filter is used. Recall that the current through an inductor is an integral of its applied voltage with a proportionality constant of $1/L$. This will create a triangular waveform for $i_L(t)$. The average of this current, $i_{L(avg)}$, is delivered to the load because the capacitor is an open circuit for this DC current. In the configuration in Figure 0.3.c, the gate driver is required for power switches to handle the switches when they are working under high power operation. Figure 0.3.d shows the application of power converters in data bus networks. In the Figure 0.3.d, the enlarged view of transmitter T_X is presented. As shown, a full bridge would be used to drive the network appropriately. The equivalent circuit of the network is a R-L load, which depends on the length of lines A and B, and the resistance and inductance values are different, consequently requiring various power switches to drive the line conveniently. A level down shifter can be adopted for the receiver R_X to receive the high amplitude pulse signal from the line and convert down the amplitude to be compatible with the controller in the low power side. In this application, T_x and R_x connect to the network through a digital isolating transformer. Figure 0.3.e presents the simplified schematic of a boost converter. In this topology, the combination of a power switch, a diode, an inductor, and a capacitor can create a DC voltage that is higher than the input voltage. The operation of this converter relies on the fact that in one phase, the inductor current reaches its maximum level and will be released to the capacitor from the beginning of the second phase. The power switch used in this converter needs a gate driver to function properly [13; 14].

Gate Driver Requirements

In power converters with a single power switch, gate drivers are used to reduce the switching loss by quickly charging the parasitic capacitance. In a converter with two superimposed power switches, gate drivers are responsible for receiving a pulse signal from the controller

Table 0.1: Ideal switch characteristics.

	I_F	R_{ON}	V_{ON}	V_{BR}	I_{OFF}	R_{OFF}	P_G	V_G	I_G
On-State	High (infinity)	Low (zero)	Low	–	–	–	Low	Low	Low
Off-State	–	–	–	High	Low	High	Low	Low	Low

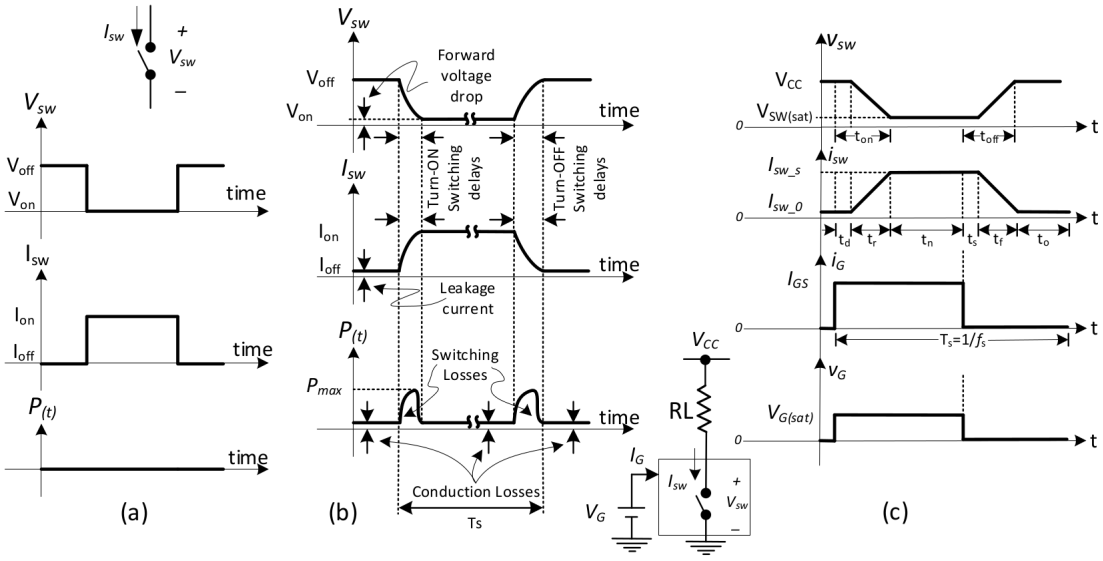


Figure 0.4: (a) Ideal switch waveforms, (b) practical switch waveforms, and (c) timing parameters of power switch operation and gate driver waveformes.

and providing two appropriate driving signals for the low and high sides. Furthermore, a gate driver is required to protect the power switches for secure operation for converters. In addition, in converters with various input voltages V_{IN} and output loads I_{Load}, a reconfigurable gate driver is required to tune the internal circuit of the gate driver to implement a high-performance power converter at different V_{IN} and I_{Load} values.

To deepen the understanding of the gate driver requirement for power switches in a power converter, the characteristics and specifications of switches must be investigated. The common motivation among different switching devices, which are designed for specific applications, is to obtain the characteristics of a "super device." The characteristic of an ideal super device is a suitable reference for designing a real device. Table 0.1 summarizes the characteristics of an ideal switch where I_F, R_{ON}, V_{ON}, V_{BR}, I_{OFF}, and R_{OFF} are the forward current, the on-state resistor, the forward voltage drop, the forward or reverse voltage, the leakage current, and the off-state resistor, respectively. Notably, a low R_{ON} causes a low on-state loss P_{ON}, and a similar phenomenon occurs for R_{OFF} and P_{OFF} . The voltage and current of an ideal power switch during operation and the corresponding power loss are illustrated in Figure 0.4.a. P_G, V_G, and I_G are the power, voltage, and current of the gate driver, as shown in Figure 0.4.c [20].

Table 0.2: Internal capacitances for a power MOSFET.

	Internal Capacitances	Values	Conditions
$C_{iss} = C_{gs} + C_{gd}$	Input Capacitance	$1350pF$	drain and source terminal shorted
$C_{oss} = C_{gd} + C_{ds}$	Output Capacitance	$58pF$	gate and source shorted
$C_{rss} = C_{gd}$	Reverse Transfer Capacitance	$3pF$	source connected to ground

For proper operation in high frequencies, the device must be completely turned on and off instantaneously during the turn-on and -off process. Thus, it must have low t_d, t_r, t_s, and t_f which are the delay, rise, storage, and fall times, respectively (Figure 0.4.c). The other parameters of power switching devices are dv/dt and di/dt, which characterize the rapid changes in the voltage across and the rapid increase of the current through the devices. Finally, R_{0JA} as thermal impedance from the internal junction to the ambient must be low to transmit heat easily to the ambient. The characteristic of a practical switch is shown in Figure 0.4.b with typical waveforms. In this figure, as device current I_{SW} rises during turn-on, the voltage across the device V_{SW} falls. The other important parameters shown in Figure 0.4.b are the turn-on time t_{on} (the sum of the delay and rise times) and turn-off time t_{off} (the sum of the storage and fall times) of the switching device [20].

A practical switching device requires finite delay time t_d, rise time t_r, storage time t_s, and fall time t_f. In Figure 0.4.b, the corresponding power losses of the power device are illustrated.

Unlike the ideal switch, which has no losses, practical switches suffer from conducting and switching losses, which are shown in Figure 0.4.b. The switching parameters as inconvenient effects are the objectives of any new device, which should exhibit improvement. For example, the dropped voltage across a conducting power device is usually in the order of $1V$ or higher in some cases up to several volts. P_{ON} as the average conduction power loss is equal to $f_s(\int_0^{t_{on}} pdt)$ where f_s is the conduction frequency, and "P" is the instantaneous power loss (product of V_{sw} and I_{sw}). is the instantaneous power loss (product of Vsw and Isw).

During the transition from one conduction state to another, the current and the voltage have substantial values. Thus, the power losses increase during the switching and can be calculated as $P_{sw} = f_s(\int_0^{t_r} pdt + \int_0^{t_s} pdt + \int_0^{f} pdt)$, where f_s is the switching frequency, and t_r, t_s, and t_f are the rise, storage, and fall times, respectively. Therefore, the power dissipation of a switching device is expressed as $P_D = P_{ON} + P_{SW} + P_G$, where P_G is the gate driver power consumption [20].

Power MOSFETs, which are practical power switches, are used for power converter implementation. When a significant power level must be handled, a power MOSFET as a particular type of transistor must be designed. The main advantages of a power MOSFET over other power components include high switching speed and good efficiency at low voltages. The inherent specifications of power MOSFETs constrain the exchange speed. The limitation is caused by

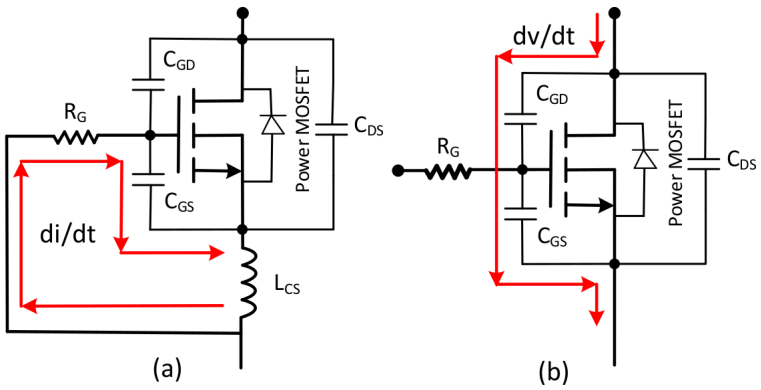


Figure 0.5: (a) Source parasitic inductance and (b) parasitic capacitances of power MOSFET.

the internal capacitances of the MOSFETs. When the transistor switches, these capacitances must be charged or discharged. Given that the current flow through the mentioned capacitances is restricted by the outer gate driver, charging and discharging can be a slow process. The gate driver will really force the transistor's switching speed [23]. Table 0.2 summarizes the internal capacitances of C3M0075120K as a power MOSFETs to serve as evidence over internal capacitances [24]. These capacitances are shown in Figure 0.3. The comparison in Table 0.2 indicates that the largest capacitance is Cgs, that for a specific power transistor the value of $1347pF$ is reported.

In addition to internal capacitance, parasitic inductance can be along with each the MOSFETs pins. Parasitic inductance has adverse effects, which are summarized as follows:

The parasitic inductance in any given circuit is actually caused by current gradients. Thus, among the three pins of power MOSFETs, the gate parasitic inductance would be the smallest. However, because of the large input internal capacitance in the gate, a resonance circuit might be created between these two undesirable internal components. Oscillation would occur and lead to the devastation of the power MOSFETs. In very high switching, the internal inductance must always be low enough to avoid this phenomenon [25]. The most effective parasitic inductance is in the source because this inductance creates feedback in the source and tends to consume increased switching time, thereby boosting switching losses. Figure 0.4 shows the source parasitic inductance and its equivalent feedback. These voltages and current fluctuations in Figures 0.3 and 0.4 that are respectively caused by the parasitic capacitances and inductances unintentionally turn on power MOSFETs when they are expected to be turned off. That is, dv/dt and di/dt would charge the C_{gs}, and the transient response of main switching causes the VGSV_{GS} to be higher than the V_{th}. Eventually, the power MOSFETs would be turned on accidentally [26].

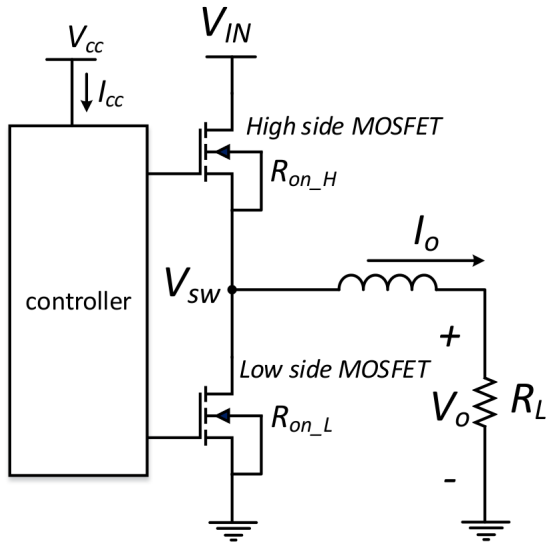


Figure 0.6: Simplified power converter circuit for calculating different kinds of loss.

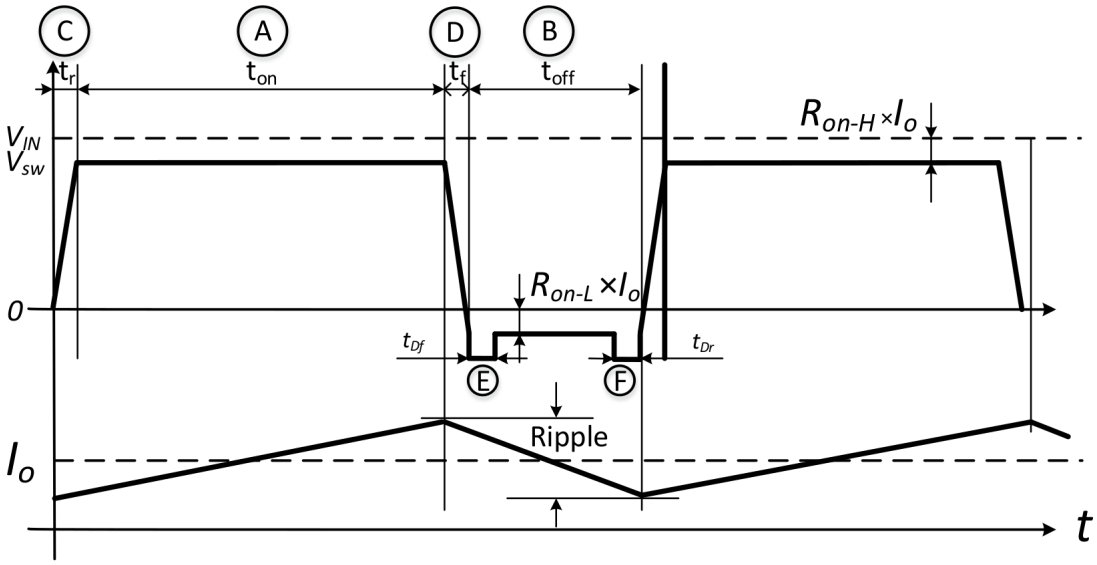


Figure 0.7: Provided waveform for calculating different losses.

Converter's Different Losses

Designing efficient converters requires minimizing losses through appropriate design practices and circuit techniques. Figures 0.6 and 0.7 are provided for calculating the different kinds of losses of a given power converter. The losses in a power converter include conduction, switching (commutation), dead-time, gate charge, and IC operating losses [27].

Important parameters are tagged in waveform in Figure 0.6 as requirements for calculating different losses and summarized as follows:

Conduction Loss

This loss is calculated in sections of "A" and "B" of the Figure 0.7 waveform. The important parameters of this loss are the on-resistances of the high/low sides (H/L Sides) of the MOSFET [28]. The following equation is employed to calculate this type of loss:

$$\begin{aligned} P_{ON-H} &= I_O^2 \times R_{On-H} \times \frac{V_O}{V_{IN}} \\ P_{ON-L} &= I_O^2 \times R_{On-L} \times (1 - \frac{V_O}{V_{IN}}) \end{aligned} \tag{2}$$

where V_{IN}, V_O, I_O, R_{On-H}, and R_{On-L} are the respective input voltage, output voltage, and high and low sides of the power MOSFET on-resistance, which are tagged in Figures 0.6 and 0.7. For the calculation of the H/L on-resistances, the drop voltages ($V_{drop} = R_{on-H} \times I_O$) in the waveform of Figure 0.4 are measurable. Then, the on-resistances can be calculated as V_{drop}/I_O.

Switching loss

This loss is calculated in Sections "C" and "D" of the waveform, and the required parameters for calculation are the rise t_r and fall t_f times.

$$P_{SW-H/L} = \frac{1}{2} \times V_{IN} \times I_O \times (t_r + t_f) \times f_{SW} \tag{3}$$

where f_{SW}, t_r, t_f are the switching frequency, the high-/low-side MOSFET turn-on rise time, and the high-/low-side MOSFET turn-off fall time, respectively, and V_{IN} and I_O are tagged in Figure 0.6.

Dead Time Loss

This loss is calculated in Sections "E" and "F" of the waveform, and the required parameters for calculation are the body-diode forward voltage and the dead times in rising t_{Df} and falling t_{Dr}. Although this loss is not great in this well-designed half bridge, it is the cause of shoot through and will burn the power MOSFETs in the half bridge because a short circuit is occurring between V_{IN} and GND in this short time (t_{Dr}, t_{Df}) (Figure 0.6). In this design, the amount of current through power MOSFETs is approximately $60mA$, while in high voltage application, this current would be around some decades of Amperes. Therefore, the proposed dead time circuit is practical and useful for high voltage application in protecting expensive power MOSFETs and guaranteeing the functionality of converters.

$$P_D = \frac{1}{2} \times V_D \times I_O \times (t_{Dr} + t_{Df}) \times f_{SW} \tag{4}$$

where V_D, t_{Dr}, and t_{Df} are the low-side MOSFET body-diode forward voltage parameters, which are tagged in Figures 0.6 and 0.7.

Gate Charge Loss

This loss is due to the left charge in the gate during the switching in which the important parameters are C_{g-H} and C_{g-L} (high- and low-side power MOSFET gate capacitances).

$$\begin{aligned} P_G &= (Q_{g-H} + Q_{g-L}) \times V_{gs} \times f_{SW} \\ P_G &= (C_{g-H} + C_{g-L}) \times V_{gs}^2 \times f_{SW} \end{aligned} \tag{5}$$

where $Q_{g-H}, Q_{g-L}, C_{g-H}+C_{g-L}, V_{gs}, f_{SW}$ are the high-side MOSFET gate electric charge [C], the low-side MOSFET gate electric charge [C], the high-side MOSFET gate capacity [F], the low-side MOSFET gate capacity [F], the gate drive voltage [V], and the switching frequency [HZ].

IC Operating Loss

This loss is due to the IC consumption current, which is denoted as I_{CC} in Figure 0.6.

$$P_{IC} = V_{CC} \times I_{CC} \tag{6}$$

where V_{IN} and I_{CC} are the input voltage and the IC consumption current tagged in Figure 0.6.

Various Topologies of Gate Driver for Different Power Converters

In [1] , an integrated Class E power amplifier (PA) is presented, and the operating frequency is $2.45GHz$. This PA is implemented in a $0.18\mu m$ CMOS process. Figure 0.8 shows the topology of this differential cascode Class-E PA with driver stages. In this design, the inductors are designed on-chip.

The measured efficiency of the presented differential PA is as high as 43.6%. Figure 0.9.a shows the die micrograph of the PA, while Figure 0.9.b presents the simulated and calculated output powers, the drain efficiency, and the power-added efficiency against $V_{DD,PA}$ with and without a dynamic cascode bias (DCB). The circuit includes one output and two driver stages, where the output supply and the driver stages are different. In Figure 0.8, the L_{d1} and L_{d2} are on-chip inductors whose quality factor (Q) at $2.45GHz$ is 13. In this design, L_{s1} and L_{s2}

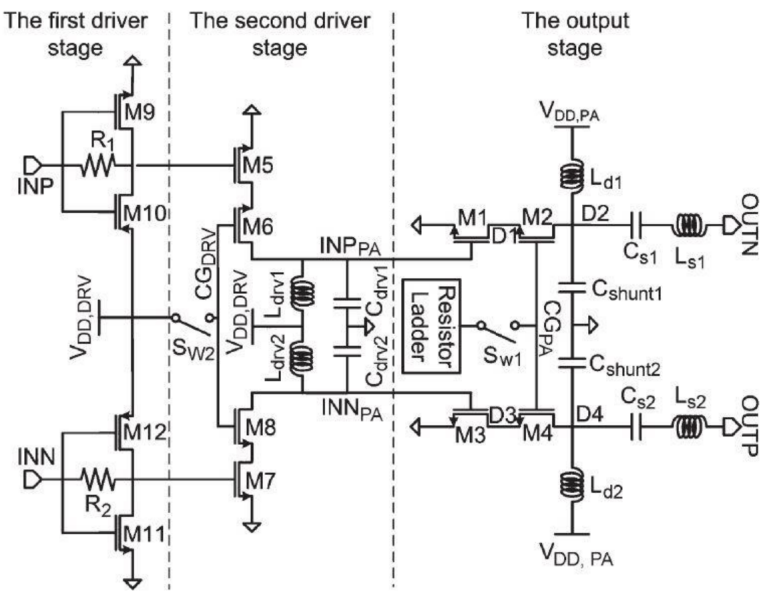


Figure 0.8: Topology of the differential cascode Class-E PA with driver stages [1].

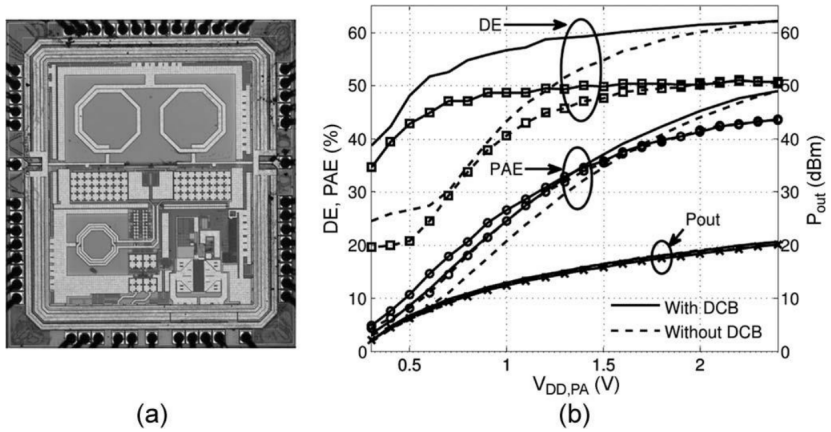


Figure 0.9: (a) Die photo of the PA. (b) Simulated and calculated output power, drain efficiency (DE), and power-added efficiency (PAE) against V_{DD}, PA with and without dynamic cascode bias (DCB) [1].

are implemented partly with bond-wire and off-chip inductances. To implement the driver of this Class E PA, the first stage is realized by two inverters with resistive feedback. The second driver stage is implemented by leveraging a LC tank-loaded cascode amplifier to minimize power consumption and allow a sufficient high supply voltage, which is 2.0 V, to drive the Class E stage.

A Class D PA is presented in [2], and its topology is shown in Figure 0.10. In this design, the PA adaptively regulates its switching frequency to achieve optimal power efficiency across the

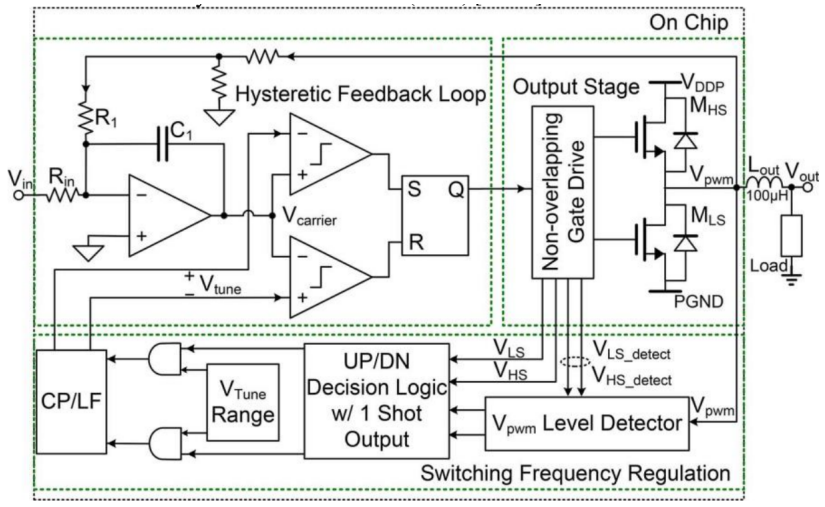


Figure 0.10: Topology overview of the class-D amplifier with f_{SW} regulation [2].

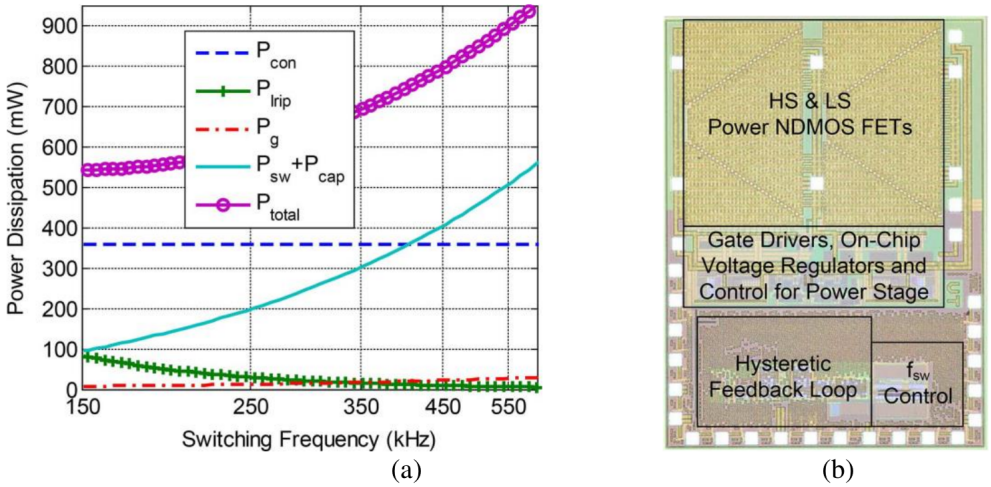


Figure 0.11: (a) Measured different types of losses of designed Class-D PA, (b) Chip photograph of the class-D amplifier, the die measures $3.4mm \times 2.5mm$ [2].

full output power range. The PA is implemented in a $0.14 - \mu m$ SOI BCD process. The PA achieves 93% efficiency at a $45W$ output power and $> 80\%$ power efficiency down to $4.5W$. In this design, all types of loss are calculated based on the measured parameters, while the power output stage works with $80V$ (V_{DDP}). The gate driver is supplied by an on-chip $3.3V$ regulator V_{DD}. The gate drivers include a two-step level shifter, which can handle a supply bounce higher than the internal supply.

As shown in Figure 0.10, the proposed Class-D PA design includes a non-overlapping gate driver, which is controlled by peripheral circuits of switching frequency regulation and hysteretic feedback loop sections. Figure 0.11.a shows the different power losses versus the switch-

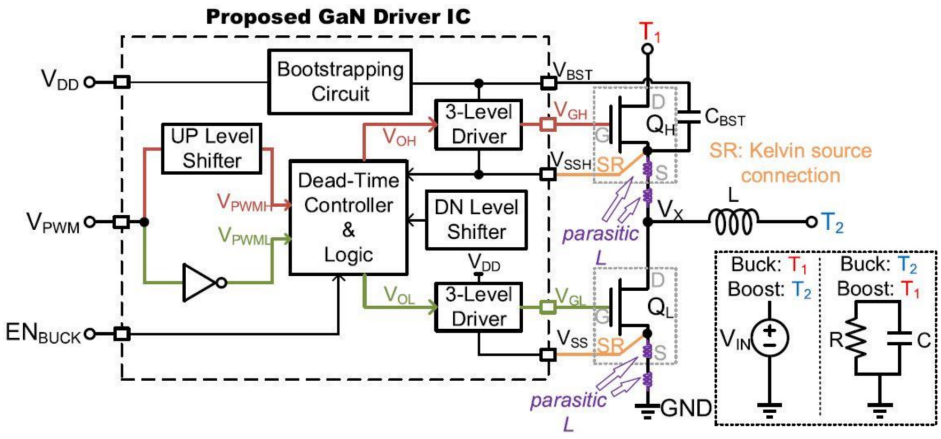


Figure 0.12: Block diagram of the proposed gate driver for GaN power switches [3].

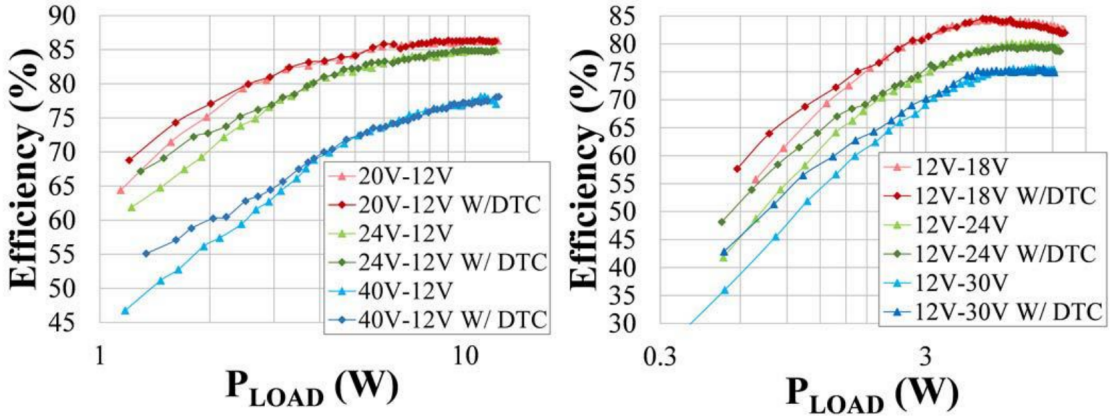


Figure 0.13: Efficiency versus load power for the proposed driver in a (a) buck converter; (b) boost converter [3].

ing frequency. Among these losses, the gate driver loss (P_g) results from charging/discharging the gate capacitance of MHS/MLS when turning MHS/MLS on/off. In [Buck/Boost], the gate driver for a buck/boost converter with optimal-point tracking dead-time control is presented in Figure 0.12. In this gate driver topology, two 3-level drivers, an up-level shifter, a down-level shifter, a dead-time control circuit, and a bootstrapping circuit are used to provide the appropriate functionality. This gate driver of GaN power switches is implemented with a $0.18-\mu m$ BCD process. The designed dead-time control circuit would tune the required delay for driving the GaN power switch depending on the load. The efficiency is respectively improved by 8.33% and 6.78% at light load in the buck and boost converter configurations due to the proper deadtime control circuit. The peak efficiencies of the $20\tilde{}12V$ (buck) and $12\tilde{}18V$ (boost) conversions are 86.37% and 84.39%, respectively. Figures 0.13.a and 0.13.b show the efficiency versus load power for the proposed driver in the buck and boost converter topologies, respectively.

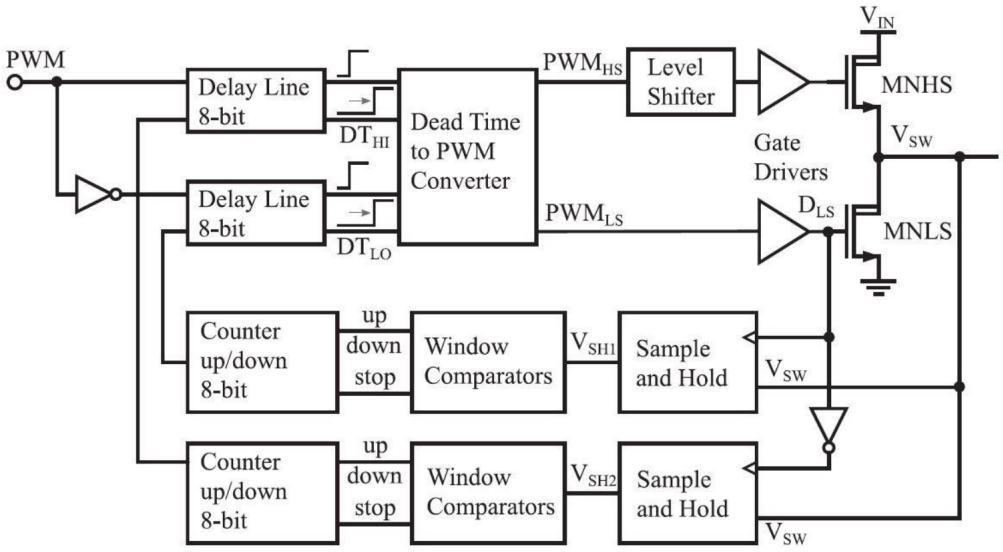


Figure 0.14: Detailed overview of the proposed mixed-signal dead time control [4].

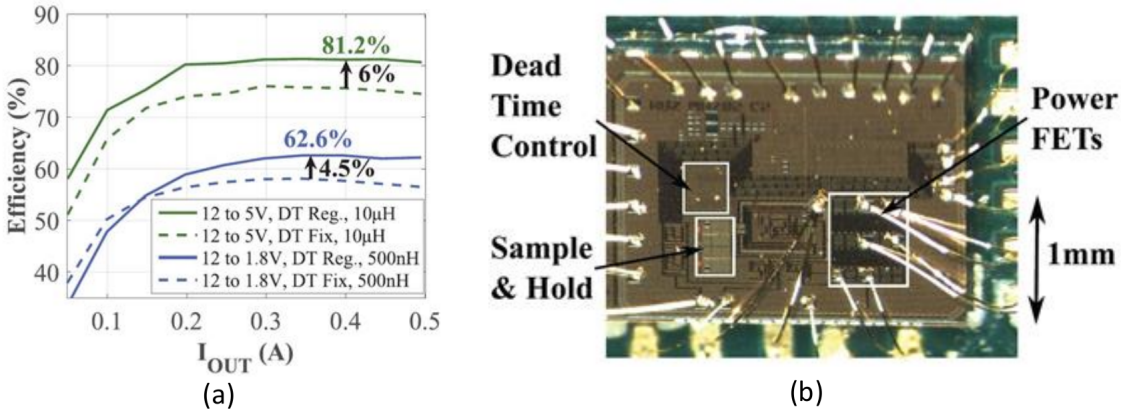


Figure 0.15: (a) Measured efficiency of the synchronous buck converter for a $12V$ to $5V$ conversion with an inductor of $10\mu H$ and conversion from $12V$ to $1.8V$ with an inductor of $500nH$ (b) Microphotograph of the testchip, directly bonded to the PCB [4].

In [4], a buck converter with a predictive mixed-signal deadtime control at an 18-V input voltage and a 10-MHz operating frequency is presented. The peripheral block diagrams of the level shifter, the gate driver, and the PWM generator are included in the gate driver to obtain great performance from the buck converter. The converter is implemented in $180-nm$ high voltage BiCMOS technology. The proposed deadtime circuit reduces the total losses of the buck converter by 31%, which results in a 5.3% efficiency improvement at $V_{IN} = 18V$, $V_{OUT} = 5V$, and $I_{Load} = 0.45A$. The measured peak efficiency of the implemented buck converter is as high as 81.2%, with an efficiency improvement of 6% with deadtime control.

Figure 0.15.a presents the measured efficiency of the synchronous buck converter for a $12-V$

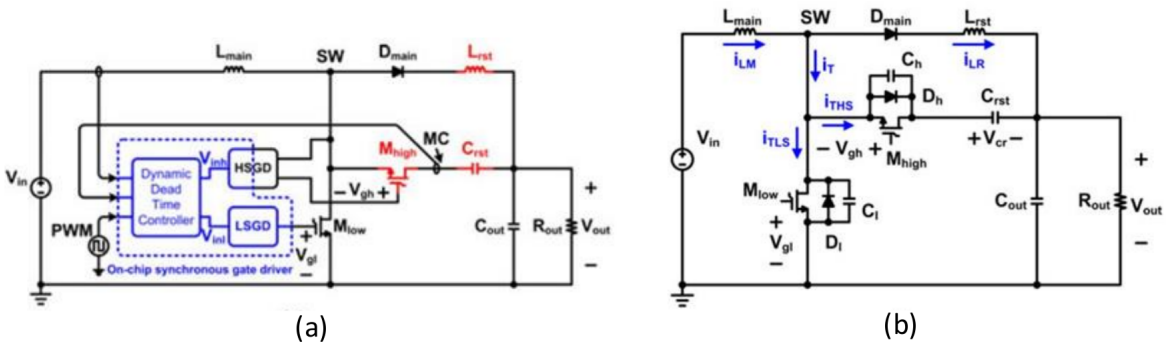


Figure 0.16: Schematic of the proposed QSW-ZVS boost converter with a custom-designed dynamic dead-time-controlled synchronous gate driver, and (b) equivalent circuit of the proposed boost converter [5].

Table 0.3: Examples of different power converter leveraging their gate drivers.

	[1]	[2]	[3]	[4]	[5]
Results	Measured	Measured	Measured	Measured	Measured
Process	$0.18\mu m$ CMOS	$0.14\mu m$ SOI BCD	$0.18\mu m$ BCD	$0.18\mu m$ BiCMOS	$0.50\mu m$ CMOS
Power amplifier type	Class-E	Class-D	Buck/Boost	Buck	Boost
Switching frequency	$2.45GHz$	$0.5MHz$	$9MHz$	$1MHz$	$1MHz$
Input Voltage V_{IN}	$2.4V$	$80V$	Buck:$20-40V$ Boost:$12-20V$	$18V$	$48-60V$
Output current/power	$--/20dBm$	$--/45W$	–	$45A/--$	$0.86A/--$
Power device	Si	Si	GaN	Si	Si
Efficiency	43.6%	93%	Buck:86.37% Boost:84.39%	81.2%	92.7%
Efficiency Improvement	–	–	Buck:8.33% Boost:6.87%	6%	–

to $5-V$ conversion with an inductor of $10\mu H$ and a conversion from $12V$ to $1.8V$ with an inductor of $500nH$. Fig. 15 (b) shows the microphotograph of the test chip, which is directly bonded to the PCB. In [5] presents a gate driver for a boost converter with an on-chip dynamic dead-time controller, as shown in Figures 0.16.a and 0.16.b. In this topology, the on-chip dynamic deadtime controller is developed to provide near-optimum dead time for the power FETs during switching transitions under different output voltage and load current conditions to achieve zero voltage switching (ZVS) with minimal body diode conduction loss for the power FETs. The gate driver is implemented with a $0.5-\mu m$ high voltage CMOS process.

The proposed boost converter provides an output voltage of $150V$. The peak power efficiency of the proposed converter is 92.7% at the switching frequency of $1MHz$.

Contributions

In this research, we proposed, designed, and implemented different required building blocks of drivers for power converters, including a level-up shifter, a level-down shifter, and a deadtime generator circuit, to address various challenges of power converters. Conventional power converters suffer from different types of losses in addition to the low- and high-side propagation delay mismatch. Therefore, new schemes must be proposed and novel circuits must be designed to achieve an efficient power converter, which can be achieved by overcoming different losses and reducing the propagation delay mismatch between the low and high sides. Designing high density converters with high-efficiency performance will reduce the size and cost in addition to the power loss. In this work, the necessary circuits for the gate driver in power converter applications are designed toward increasing the power efficiency and density. Power converters have seven types of losses, and four of them, including the switching, dead-time, power switch output capacitance, and gate charge losses, are time-dependent. The deadtime circuit is an essential part of the gate driver that could reduce or remove time-dependent losses. In power converters, dead-time loss becomes a serious issue as the operating frequency increases. Sufficient deadtime is required to avoid short circuit between the converter's supply V_{IN} and GND to decrease the loss and increase the reliability and stability of power converters. Meanwhile, a large deadtime leads to high reverse conduction loss, which is critical in GaN high-electron-mobility transistors (HEMTs) due to the high voltage drop of the reverse conduction through the 2-D electron gas (2DEG). In some conventional applications, a fixed deadtime is utilized. However, the amount of deadtime depends on the I_{Load} or V_{IN} of the power converters. The deadtime required by the power converter increases with the VIN and decreases as the I_{Load} increases. Thus, in applications exploiting fixed deadtimes with varying I_{Load} or V_{IN}, the fixed deadtime must be long enough at the lowest I_{Load} or high V_{IN} to avoid short circuit, which will produce a large reverse conduction loss at high I_{load} or low V_{IN}. Meanwhile, power converters with symmetric tunable deadtimes show a higher efficiency than fixed deadtime-based converters. However, the required deadtimes for the low and high sides of converters vary because the high-side power switch is under hard switching while the low-side one is under soft switching operation. Indeed, the asymmetric tunable deadtimes for the low and high sides of converters must be efficiently designed for power converters. In this research, we propose and designed an asymmetric deadtime generator for half bridges that reduces the total loss of the implemented half bridge by 40%. In addition, we mathematically proved that an optimum deadtime exists for power converters and derived the equation for optimum deadtime for a typical buck converter. The deadtime obtained by the derived equation is compared with the simulation and experimental results in the implementation of a buck converter, showing high consistency. Level-up and -down shifters are two other essential blocks of gate drivers that must be well designed for power converters to function correctly. High-performance level shifters with minimized propagation delay, static, and dynamic power consumptions must have energy-efficient power converters.

The summary of this dissertation's contributions are as follows:

- Proposal of a novel topology of a high-performance level-up shifter for the gate drivers of power converters. In our design, the main parameters of the level shifter, including propagation delay, static and dynamic power consumptions, and conversion range, are improved significantly compared to those of other solutions.
- Introduction of a new low loss half bridge using a custom integrated CMOS non-overlapping signal generator and off-the-shelf electronic components. The total loss of the implemented half bridge with our proposed circuit is decreased by 40% compared to that of the half bridge without our chip. The fabricated chip is successfully validated with a 45-V input 1-MHz half bridge with a RL load where the efficiency is 82% and input power is $7.2W$.
- Development of a new structure for a single-supply reconfigurable multiple-level down-shifter to receive the signal from the high voltage side of the data bus network and provide the appropriate signal that is compatible with the low voltage side circuits, such as FPGA and MCU. The output of this design is reconfigurable to provide a signal with amplitudes of $1.2-V, 1.8-V$, and $2.5-V$ for different families of processors with different core supplies.
- Proposal and realization of an energy-efficient buck converter with variable V_{IN} and I_{Load} using a custom integrated CMOS reconfigurable asymmetric optimum deadtime generator and off-the-shelf components. In this design, the efficiency of the designed buck converter is improved by 12% at $P_{OUT} = 50mW$ compared to that of a fixed deadtime generator. In addition to the novel circuit, the new approach to providing optimum deadtime for a typical buck converter relies on mathematical analysis.

Thesis Outline

The thesis is organized as follows. In Chapter 2, the proposed 7.6-ns delay subthreshold level-shifter leveraging parasitic capacitance voltage-controlled current source is introduced by describing the design, implementation, and experimental results. Chapter 3 presents an active dead-time control circuit with timing elements for a 45-V input 1-MHz half-bridge with $P_{IN} = 7.2W$ converter to achieve a low-loss power converter. Chapter 4 describes a reconfigurable single-supply multiple-level down-shifter for system-on-chip applications, which is practical for the realization of a receiver for a data bus. In Chapter 5, a 9.2-ns to 1-us digitally controlled multi-tuned deadtime optimization for efficient GaN HEMT power converters is presented, elaborating on the circuit implementation, mathematical analysis, and experimental results as proof of concept. Finally, conclusions are drawn in the last chapter, and the aspects that require further exploration and improvement are presented.

Chapter 1

Methodology

1.1 Data-bus Requirements Summary

This research and development project is a collaborative work with an industrial partner. The partner requires a reconfigurable data bus for the implementation of a compact sensor interface. To implement the tunable data bus, a reconfigurable transmitter (T_x) and a tunable receiver (R_x) must be proposed to communicate with a FPGA for data processing. Figure 0.3.d shows a simplified data bus and its connection with the FPGA using a T_x and a R_x. These types of generic data buses[1], presented in 1966 and then revised in 1983, provides some different wiring topologies; consist of a serial, twisted shielded pair interface. In one of these data buses, the standard low and high transmission bit-rates are $12.5kbps$ and $100kbps$ respectively. Since in the transmission data bus the equivalent impedance of shielded twisted pair cable is around 78Ω, the T_x output impedance should be $75\Omega \pm 5\Omega$ and equally divide between Line A and Line B for getting a proper matching between the lines and T_x. In the other side, the R_x must have an equivalent input impedance of $8k\Omega$ minimum. Twisted lines A and B provide a RL equivalent circuit that depends on the length of the lines, and various R and L values will be loaded (variable I_{load}) in the T_x output. In addition, the industrial partner requires the supply (V_{IN}) of T_x to be variable ($12V - 24V$). Therefore, a reconfigurable T_x must be designed to accommodate variable V_{IN} and I_{load}. The R_x is responsible for receiving data from the bus as the high-voltage side and delivering the data to the FPGA, which is in the low-voltage side. The R_x output must be reconfigurable to deliver data with different amplitudes to be able to communicate with different families of the FPGA with various core supplies.

[1]The names of data buses standard have been omitted due to the industrial partner request.

1.2 Links between Chapters and Contributions

For the T_x implementation, we propose and fabricated a custom integrated circuit with novel circuit techniques to present an energy-efficient power converter. A critical challenge in the gate drivers of power converters is the propagation delay mismatches between the high- and low-side gate drivers that lead to additional loss in power converters. This challenge is encountered because the number of blocks for realizing the high side of gate drivers is more than that for the low side blocks. Furthermore, the high-side circuits are working under a higher voltage than the low-side circuits. Thus, the high voltage transistors in the high-side circuits are associated with a large parasitic capacitance, which increases the propagation delay. Therefore, providing a high-performance level shifter for the high-side blocks with a minimized propagation delay would help minimize the effect of propagation delay mismatches. We proposed a novel scheme which is uses a voltage controlled current source, a circuit with three n-channel MOSFETs, one CMOS input inverter, and one CMOS output buffer to provide a fast response time. Chapter 2 describes the proposed level shifter and proof of the concept with mathematical analysis and experimental results. Power converters in which superimposed power switches are employed for their topologies suffer from an adverse phenomenon named shoot-through, which produces a large switching loss and consequently decreases the power efficiency significantly. Indeed, addressing this deleterious issue would boost the performance of power converters. Our proposed non-overlapping signal generator for the T_x part removes shoot-through and consequently decreases the total loss significantly. This custom integrated circuit is validated by a half bridge and presented in Chapter 3 by details.

For realizing the tunable R_x, we proposed and implemented a reconfigurable single-supply multiple-level down shifter to serve as an appropriate interface between the data bus and the FPGA. The proposed technique uses a diode connected circuit structure, a current source, five transmission gates, a diode-supercapacitor combination, and input/output buffers to implement this reconfigurable level-down shifter. Given the interface role of this circuit, a short propagation delay and a low power consumption are advantageous. Chapter 4 reflects the implementation of the proposed novel level-down shifter as Rx part of data bus network.

A reconfigurable gate driver to support power converters with variable input voltage V_{IN} and output current I_{OUT} is one of the asked parameters by our industrial partner to be used for Tx part of data bus network. The most frequently used power switches for implementing power converters are Si MOS, SiC MOS, and GaN transistors. A Figure of Merit $(FoM) = Q_{OSS}.R_{ON}$ is recommended as the advantage of GaN over Si or SiC (Q_{OSS} and R_{ON} are the output capacitor charge and on-resistance of the power switch, respectively). Furthermore, the GaN transistor does not suffer from reverse recovery loss due to the absence of a body diode and has lower gate charge and output capacitance than Si or SiC. In addition, the power density of the GaN power switch is significantly higher than that of Si or SiC. For example, EPC2012 as a part number of the GaN power switch can tolerate up to $200V$ and $3A$ in

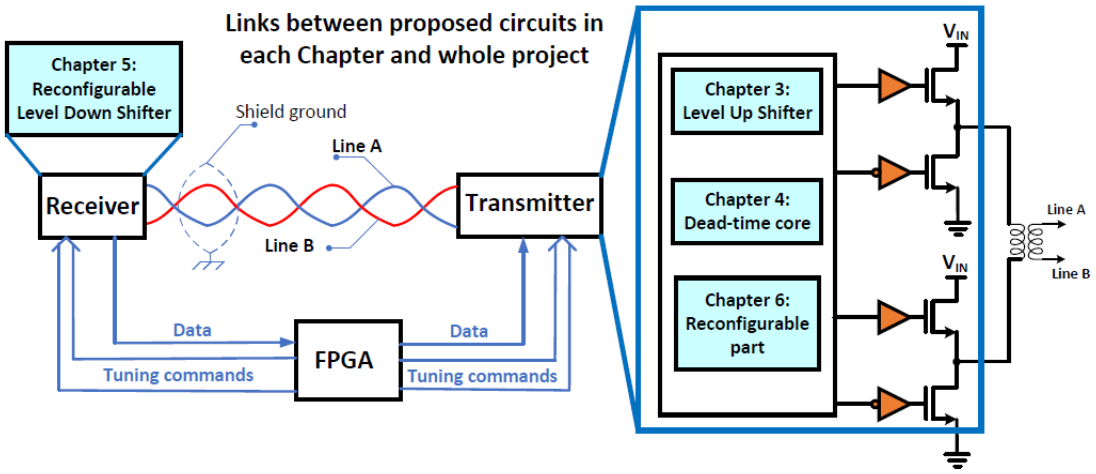


Figure 1.1: Links between proposed circuits in each chapter and whole project.

the $0.9mm \times 1.7mm$ dimension. However, GaN devices typically exhibit a higher power loss during deadtime than Si or SiC due to their higher reverse conduction voltage (e.g., V_{SD} of $2.0V$ at $10A$ for LMG5200 compared to $\sim 1V$ for Si MOSFETs). Therefore, employing GaN power switches is reasonable for achieving high power density in power converter design.

To satisfy this requirement, a tunable deadtime circuit is proposed and included in conventional gate drivers. Indeed, when the V_{IN} or I_{OUT} of a power converter is variable, different deadtimes for the high and low sides are needed to produce an efficient converter. Chapter 5 presents a 9.2-ns to 1-us digitally controlled multi-tuned deadtime optimization for efficient GaN HEMT power converters with variable V_{IN} and I_{Load} as T_x part. Figure 1.1 shows the role of each paper in the project and their connections together.

1.3 Conclusion

In each chapter of this dissertation, one building block of T_x or R_x is discussed in detail. Post-layout simulation, mathematical analysis, and experimental results are provided as proof of the concept of the proposed circuit functionality. Literature review is performed for each building block in the beginning of each chapter in addition to the literature review of the different power converter applications in the introduction of this dissertation. All the building blocks of T_x and R_x are implemented in AMS $0.35\mu m$ technology with novel circuits. The achieved results are presented in highly ranked conferences and journals. The specifications and characteristics of some of the different power converters for various applications are compared in Table 0.3 at the end of the thesis introduction. Furthermore, at the end of each chapter, the performance of the proposed novel circuit for the different T_X and R_X parts is compared with that of state-of-the-art circuits.

Chapter 2

A 7.6-ns Delay Subthreshold Level-Shifter Leveraging Parasitic Capacitance Voltage-Controlled Current Source

2.1 Résumé

Une nouvelle méthode de décalage de niveau qui utilise une nouvelle approche basée sur une source de courant commandée en tension à capacité parasite est présentée pour minimiser le délai de propagation et maximiser la plage de conversion de tension. Ce nouveau schéma utilise un circuit optimisé comprenant une source de courant dépendante, un circuit composé de trois MOSFET à canal N interconnectés (TnM), un inverseur d'entrée CMOS et un tampon de sortie CMOS pour fournir un temps de réponse rapide. Notre méthode utilise les capacités parasites équivalentes d'un circuit TnM pour augmenter le niveau d'un signal d'entrée avec une amplitude allant de niveaux de tension sous-seuil à $+3.0V$. Le circuit de décalage de niveau (LS) fabriqué en technologie CMOS à $0.35\mu m$ occupe une surface de silicium de seulement $25\mu m \times 25\mu m$. Le LS présente des délais de propagation de montée et de descente mesurés de 4 et $11.2ns$, respectivement. Les résultats mesurés démontrent le fonctionnement du circuit présenté sur une large gamme de fréquences allant de 1 à $130MHz$. Le circuit fabriqué consomme $31.5pW$ de puissance statique et $3.4pJ$ d'énergie par transition à $1kHz$, $V_{DDL} = 0.8V$, et une charge capacitive de $C_L = 0.1pF$.

2.2 Abstract

A novel level shifting method that uses a new approach based on a parasitic capacitance voltage controlled current source is presented to minimize the propagation delay and maximize the

voltage conversion range. This new scheme uses an optimized circuit including a dependent current source, a circuit made of three interconnected n-channel MOSFETs (TnM), one CMOS input inverter, and one CMOS output buffer to provide a fast response time. Our method utilizes the equivalent parasitic capacitances of a TnM circuit to increase the level of an input signal with an amplitude ranging from subthreshold voltage levels to $+3.0V$. The level shifter (LS) circuit fabricated in $0.35\mu m$ CMOS technology occupies a silicon area of only $25\mu m \times 25\mu m$. The LS shows measured rising and falling propagation delays of 4 and $11.2ns$, respectively. The measured results demonstrate the operation of the presented circuit over a wide frequency ranging from 1 to $130MHz$. The fabricated circuit consumes $31.5pW$ of static power and $3.4pJ$ of energy per transition at $1kHz$, $V_{DDL} = 0.8V$, and capacitive load of $C_L = 0.1pF$.

2.3 Introduction

Level shifters (LSs) are key circuits in numerous microelectronic systems including system-on-chip (SoC) and complex system-in-package (SiP) devices [29; 30; 9; 31]. These circuits are used to translate one signal level to another, allowing signals to be properly transferred across supply voltage domains [32; 33; 34]. High-performance telecommunication systems require high-speed level shifter circuits consuming as low power as possible. Low-power applications, such as peripheral modules for the Internet of Things or implantable medical devices, working at medium or low frequency, often use subthreshold circuits to decrease static and dynamic power consumption by orders of magnitude [35; 36; 37]. Energy-efficient circuit designs using subthreshold operations are well suited for these applications that do not need fast circuits operation [38; 39]. High-performance subthreshold LSs are necessary in these low-power applications [40; 41].

Different voltage levels are frequently used inside the various building blocks of SoCs [17; 42; 43; 9]. Using multiple technologies operating at various supply voltages within the same SiP decreases the fabrication cost and the power consumption [44; 45; 46]. Emerging technologies are highly optimized to improve performance; hence, using them in SiP is advantageous but expensive [47; 48]. Therefore, robust technologies using higher supply voltage technologies can cohabit with lower supply voltages to accommodate both high-speed high-performance and low-power non-critical blocks in the same SiP [49; 50; 51; 52; 53; 54].

Figure 2.1.a illustrates the basic structure of a conventional current mirror-based LS (CBLS). Different techniques and innovations have been proposed to improve the main parameters of CBLSs, including propagation delay (Figure 2.1.b), static and dynamic power consumption, and dynamic conversion range [55; 56; 57; 58; 59; 60; 6; 61]. This circuit has less contention than the latch-based LS [54]. However, it can exhibit a large static short-circuit current when the input pulse intensity is high (Figure 2.1.a), which can significantly increase the power

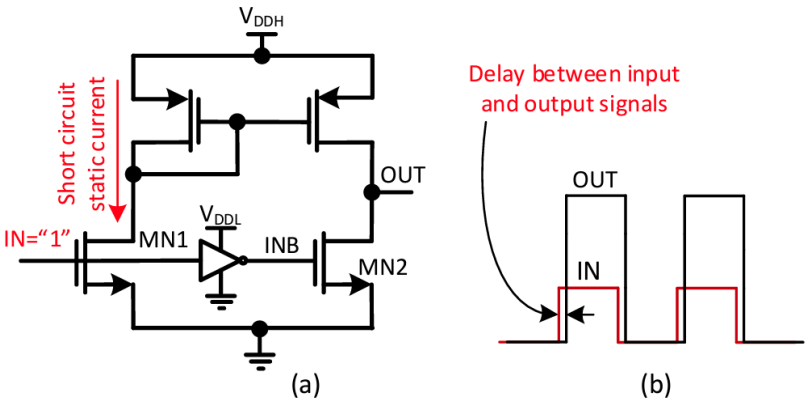


Figure 2.1: Simplified level shifter circuit schematic: (a) basic structure of current source-based LS, (b) propagation delay between input and output signals.

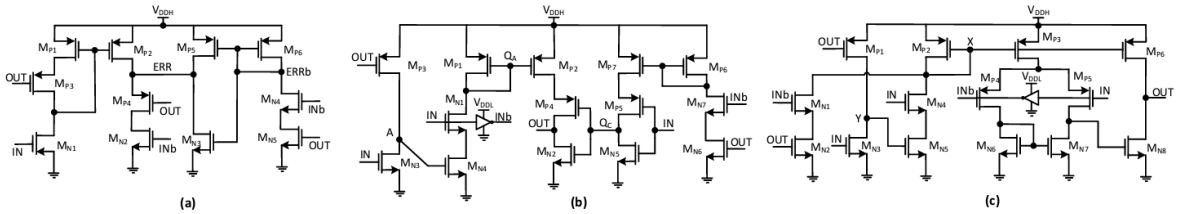


Figure 2.2: Different CBLS: (a) CBLS Current source with logic error detection circuit [6], (b) Two stage CBLS [7], (c) CBLS with correction circuit [8].

consumption.

In [6], a logic error detection circuit for near-threshold operation is used to enhance the performance of CBLS as shown in the Figure 2.2.a. In this schematic, the level shifting part includes $M_{P1} - M_{P4}$, M_{N1}, and M_{N2}, while the logic error detection part consists of M_{P5}, M_{P6}, and $M_{N3} - M_{N5}$. Although this LS was implemented in a CMOS $14 - nm$ process using minimum transistor sizes, a two-stage topology resulted in a rather long propagation delay and narrow conversion range.

The CBLS reported in [7] (Figure 2.2.b) uses the n-type MOSFET M_{N4} to minimize the static current. However, utilizing 15 transistors to implement the LS can result in a larger circuit area. This CBLS also uses a substantial amount of power, and the feedback loop lengthens the propagation delay.

The CBLS presented in [8] uses a digital circuit based on error correction, as shown in Figure 2.2.c, to overcome the limitations of conventional LSs. However, the presented LS suffers from significant contention in nodes OUT and Y. The contention is due to the superimposition of M_{P6} with M_{N8} at the output node on the right-hand side and M_{P1} with M_{N3} on the left-hand side. The circuit in [8] also suffers from a similar problem like the LS circuit in [7]. The

drawbacks associated with this topology are a long propagation delay due to the feedback loop and a bulky area. Since the circuits shown in Figures 2.2.b and 2.2.c operate as dual-stage circuits, their total speed is limited due to the resulting long propagation delay.

In this paper, a novel subthreshold LS circuit based on a voltage controlled current source (VCCS) combined with the equivalent parasitic capacitance of three interconnected n-channel MOSFETs (TnM) is presented to shift the signal level up with a shorter propagation delay, a wider conversion range, and a lower power consumption in low-power subthreshold building blocks compared to other solutions. In this circuit, the current source supplies the needed current to the TnM within the given operating period, while the TnM converts the obtained current from the VCCS to a voltage level greater than the input pulse level. A feedback mechanism is designed to provide the amount of current for the TnM and keep the LS in the sleep mode after the transition times which minimizes the total power consumption (TPC). The efficient design of TnM helps in fast charge/discharge of its equivalent parasitic capacitance, resulting in minimized propagation delay (PD). Developing the VCCS and TnM also maximizes the conversion range (CR) compared to other LS circuit solutions.

The remaining sections of this article are organized as follows. The configuration and the operating principle of the proposed LS circuit is presented in Section 2.4. The implementation of the circuit, mathematical discussion, and the post-layout simulation results are brought in Section 2.5. The measured performance of the LS chip prototype is arranged in Section 2.6. The obtained results are discussed and compared with that of similar designs in Section 2.7, and the conclusion is given in Section 2.8.

2.4 Proposed LS Architecture and Operation

The proposed LS is constructed based on a current mirror structure, so it benefits from the high impedance of its output node and good matching capability. A feedback network circuit is employed to control the current supplied to a modified current mirror-based LS (MCLS) (Figure 2.3.a). The latter realize the main part of the level shifting section, which consists of three MOSFETs that are efficiently connected to each other to provide an equivalent parasitic capacitance C_p at node V_A (Figure 2.3.c). This topology reduces the consumed energy, propagation delay, and the expansion of the conversion range.

In Figure 2.3.a, the variable V_A corresponds to the voltage of an important circuit node that is later used to produce the control voltage V_C, as illustrated in Figure 2.3.c. The voltage variation (ΔV_A) is measured by the feedback network and converted into a current variation (ΔI_A). Then, ΔI_A is subtracted from the main mirrored current I. Finally, the rest of the current I_1 is delivered by the MCLS. Therefore, when $\Delta I_A = I$, the feedback network completely shuts down the system. Consequently, the average corresponding power consumption of the area shown in green in Figure 2.3.b is saved.

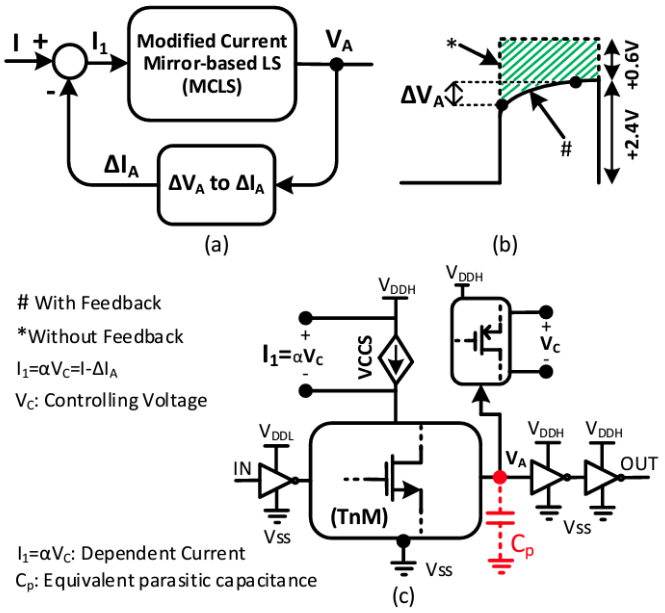


Figure 2.3: General block diagram of the proposed CBLS: (a) Operation of the feedback part, (b) Potential of V_A with and without feedback network, and (c) Simplified proposed LS.

However, converting V_A to V_{DDH} using a buffer can consume as much power as the energy saved by the feedback mechanism, as shown in Figure 2.3.b. The equivalent parasitic capacitances in node V_A are significantly bigger than those in the subsequent stages due to the TnM subblock (Figure 2.3.c). Therefore, the feedback network must control the voltage of this critical node V_A. The controlled charge/discharge of the large parasitic capacitance in node V_A gradually shifts the level of the applied signal. Then, the output buffer in the lower-strength nodes transforms the enhanced signal at node V_A into V_{DDH} with minimal contention. The TnM provides a simplified topology designed to efficiently exploit the parasitic capacitance of the MOSFETs. Accordingly, this process of converting the input signal into V_{DDH}, thanks to TnM and the feedback network, significantly improves PD, TPC, and the conversion range compared with other implementations. Furthermore, the closed-loop negative feedback regulates the current delivered to the TnM to minimize any unnecessary power consumption.

The circuit operation is illustrated in Figure 2.3.c. The voltage-controlled current source (VCCS) supplies a variable current to the TnM and produces a voltage V_A, which helps to generate the control voltage V_C of the feedback circuit. Finally, V_A is amplified through two inverters to buffer the signal and generate V_{DDH}. In Figure 2.3.c, the equivalent parasitic capacitance at node A is denoted C_p.

The advantages of the presented wide conversion range LS are summarized as follows:

1. A VCCS and a TnM are used to progressively increase the input signal level. Therefore,

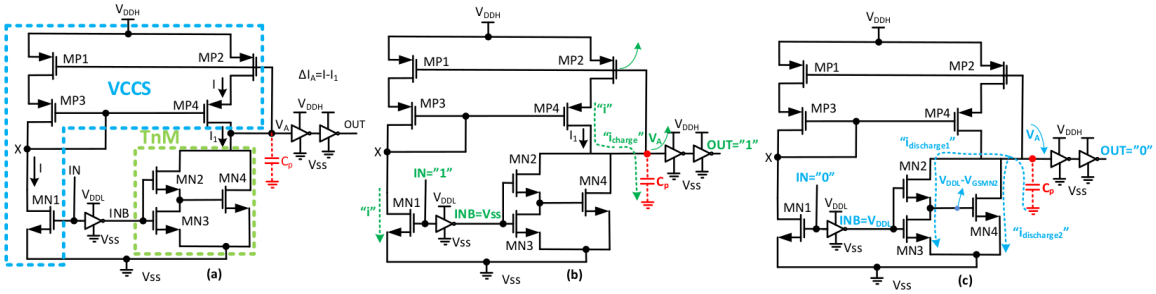


Figure 2.4: Implementation and operation of the proposed LS: (a) Transistor level realization, (b) LS operation when IN="1", and (c) LS operation when IN="0".

the opposition between the strong pull up and the weak pull down is completely removed, resulting in significant improvements in PD, CR, and TPC.

2. In contrast with the conventional current mirror-based LS, wherein the quiescent current harms the LS performance, the feedback part of the circuit in this presented LS design permits the circuit to work only during the necessary time intervals. During off periods, the LS is placed in stand-by mode, thereby significantly decreasing the leakage current and the static power.

3. Our topology uses one effective stage to raise the signal intensity, rather than two or more, resulting in reduced propagation latency.

4. The presented circuit utilizes a large transistor on the low side of the current mirror to address the weak pull down issue associated with the low V_{DDL}. This allows converting the low amplitude signal into a pulse of amplitude V_{DDH}. Consequently, the circuit is suitable for use in the subthreshold region.

5. The presented circuit uses fewer transistors compared with conventional CBLS circuit implementations, resulting in area saving.

2.5 Circuit Implementation and Simulation

The detailed description of the proposed LS circuit implementation is presented in Figure 2.4.a. It consists of several subblocks, including a TnM, a feedback network, a VCCS, an input inverter, and an output buffer.

2.5.1 Circuit Description

In the presented LS circuit illustrated in Figure 2.4.a, the input signal (IN) is applied to the n-channel MOSFET MN1, and the voltage V_A, which is in-phase with IN, is applied to the gates of MP1 and MP2 (p-type MOSFETs, superimposed with MN1 to cut off the static current).

Accordingly, this circuit is allowed to operate only within the duration of the delay between the input and output signal (propagation delay). Otherwise, V_A turns off MP1 and MP2 to avoid the flow of current I_1 to TnM (standby).

The role of the TnM composite MOSFET made of MN2, MN3, and MN4 is to shift the level of the input voltage upward by providing a dynamic equivalent capacitor, the value of which depends on the value of IN, charged by VCCS at node V_A . When IN="1", the VCCS charges C_p . When IN="0", the TnM discharges C_p without the need for extra switches. In contrast of using a fixed capacitor (e.g. a metal-to-metal capacitor or a fixed parasitic capacitor) to charge V_A , this scheme provides a dynamic capacitor value at node V_A , the value of which depends on the operating region of MP2, MP4, MN2, MN3, and MN4. When IN="1", the voltage V A increases and puts MP2 and MP4 in the triode region. In this case, the value of C_p decreases and so do the dynamic power consumption and the delay. When IN="0", the voltage V_A decreases and puts MN2, MN3, and MN4 in the triode region. In this case, the value of C_p reduces and so do the dynamic power consumption and the delay [37]. In contrast to using a fixed capacitor at node V_A, the TnM dynamically controls the value of the distributed parasitic capacitance C_p according to the transient value of the input pulse (IN) when it is charged by VCCS and discharged through the MN2, MN3, and MN4. It will be shown in the next sections that using a dynamic parasitic capacitor provided by the TnM at node V_A , compared to a fixed capacitor, allows this LS design to operate in subthreshold region while providing same delay and a wide conversion range compared to a LS working in strong inversion and consuming more power.

When IN is high, the current flows through the p-channel transistors (MP2 and MP4) to charge the equivalent parasitic capacitance in node A. Accordingly, the voltage node V_A changes meanwhile. The voltage node V_A changes till MP1 and MP2 enter the cutoff region. Consequently, the flowing current "I" decreases. Eventually, the voltage node V_A is conveyed to V_{DDH} by the output buffer. The circuit operation when IN="1" is illustrated in Figure 2.4.b. In contrast, MN2 and MN3 turn on, and MN4 turns off when IN="0". Consequently, the available charged equivalent parasitic capacitance from the latter state at node A is discharged by the branch made by MN2 and MN3. Thus, the voltage V_A instantly discharge nearly to zero. The circuit returns to sleep mode when MN1 is turned off. The circuit operation when IN="0" is illustrated in Figure 2.4.c.

The produced current from MN1 must be mirrored to TnM in the proposed topology to shift up the output voltage. However, the current flowing into MP2 and MP4 depends on the V_{SG} of MP2. The gate voltage of MP2 increases when the V_A increases gradually, whereas the drain of MP2 decreases. Accordingly, the V_{SG} and V_{SD} of MP2 and MP4 decrease, respectively. The dependent current of VCCS flows into TnM. Consequently, the voltage node A increases. This way, the V_{SG} of MP2 and the V_{SD} of MP4, which corresponds to V_C (Figure 2.3.c), create a well-controlled voltage to turn-off MP2 and MP4, preventing extra current delivery to TnM,

Table 2.1: Transistor sizes of the Proposed LS in Figure 2.4.

Parts	Components	Values (μm)
Input inverter	PMOS	W/L=1.5/0.35
	NMOS	W/L=1.5/0.35
	MN1	W/L=10/0.35
	MP1	W/L=10/0.35
VCCS	PM2	W/L=0.4/0.35
	PM3	W/L=0.4/0.35
	PM4	W/L=0.4/0.35
	MN2	W/L=1.5/0.35
TnM	MN3	W/L=1.5/0.35
	MN4	W/L=0.4/0.35
Output buffer	PMOS	W/L=0.4/0.35
	NMOS	W/L=0.4/0.35

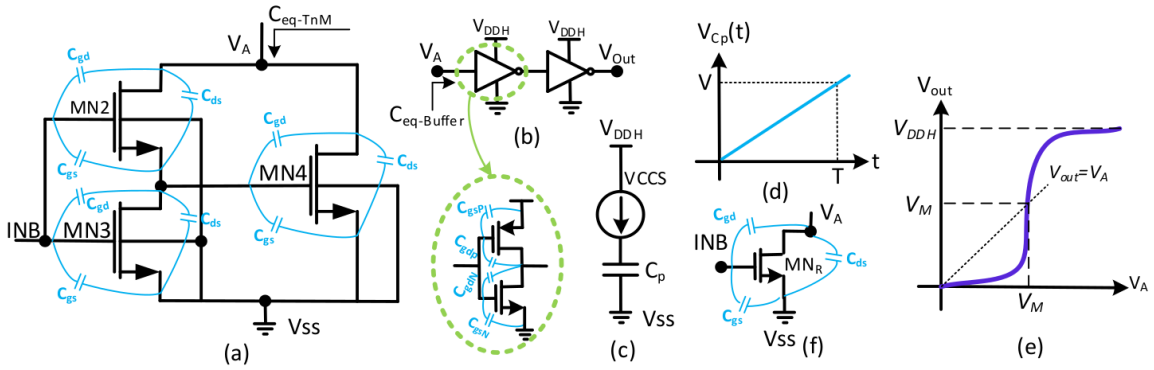


Figure 2.5: The circuit diagram of the TnM with all its parasitic capacitances, (b) The equivalent parasitic capacitance charged by a current source, (c) Voltage across C_P, (d) Simplified circuit of output buffer, (e) Transfer function of a buffer.

and decreasing extra power consumption. The feedback network saves a considerable amount of energy at each cycle, as highlighted in Figure 2.3.b. Table 2.1 shows the dimensions of all transistors used in the presented LS circuit shown in Figure 2.4.a.

2.5.2 TnM Circuit Analysis and Equivalent Capacitor

The circuit diagram of the TnM with all its parasitic capacitances is illustrated in Figure 2.5.a. The effective equivalent parasitic capacitance C_p at node "A" is the sum of the capacitance seen from the drain of TnM (C_{eq-TnM} in Figure 2.5.a)), the drain of MP4 C_{dMP4}, and the input capacitances of the output buffer $C_{eq-Buffer}$. Thus, the total equivalent parasitic capacitor seen at node "A" is nonlinear and depends on the region of operation of the MOSFET. Figure 2.5.b presents the simplified circuit of the output buffer and the schematic of an inverter with

its parasitic. C_{dMP4}, $C_{eq-Buffer}$, and C_{eq-TnM} are detailed in 2.1. C_p is the summation of these capacitances.

$$
\begin{aligned}
C_{dMP4} &= C_{dsMP4} + C_{dgMP4} \\
C_{eq-Buffer} &= C_{gsp} + C_{gdp} + C_{gdN} + C_{gsN} \\
C_{eq-TnM} &= C_{dsMN4} + C_{gdMN4} + C_{dsMN2} + C_{gdMN2} \\
C_p &= C_{eq-TnM} + C_{eq-Buffer} + C_{dMP4}
\end{aligned}
\tag{2.1}
$$

Overall, simulations are necessary to obtain an accurate estimation of the total parasitic capacitance seen at a specific node. A model is based on the equation of the capacitance charged by a current source, as shown in Figure 2.5.c. In this model, the voltage across the capacitance C_p is given by 2.2, where V is the voltage developed across capacitor C p during the time interval T, as shown in Figure 2.5.d, and i_{Cp} is the current flowing through C_p .

$$
V = \frac{1}{C_P} \int_0^T i_{C_P}(t)dt \tag{2.2}
$$

Simulation can be performed to precisely determine the value of the equivalent parasitic capacitance at node "A" in the circuit shown in Figure 2.4.a.

In the proposed circuit, the capacitance value seen at node "A" can vary because the amount of current delivered to node "A" depends on the operating region of MP2 over different time intervals. When V_A is zero, MP1 and MP2 are in their saturation regions. Therefore, the values of C p can be obtained by

$$
I = i_{SD_{MP2}} = \mu_P C_{OX} \frac{W}{2L} (V_{SG_{MP2}} - |V_{thp}|)^2 (1 + \lambda V_{SG_{MP2}}) = C_P \frac{dV_A}{dt} \tag{2.3}
$$

Equation 2.3 is valid only at startup. Afterward, when IN changes to "1", the gate voltage of MP2 and the drain voltage of MP4 boost by increment of V_A gradually, forcing MP2 to enter in the triode region. Therefore, $i_{SD_{MP2}}$ in 2.3 is substituted by

$$
i_{SD_{MP2}} = \mu_P C_{OX} \frac{W}{L} \left[(V_{SG_{MP2}} - |V_{thp}|) V_{SG_{MP2}} - 0.5 (V_{SG_{MP2}})^2 \right] (1 + \lambda V_{SG_{MP2}}) \tag{2.4}
$$

Finally, MP2 enters the cutoff region, $i_{SD_{MP2}}$, and the circuit shuts down when V A further increases. The current delivered to TnM by MP2 and MP4 follows three steps. At the beginning, the current is modeled by the equation of the drain current of MP2 when it is in the saturation region. Then, the current is modeled by the equation of the drain current of MP2 when it is in the linear region. Finally, the delivered current is equal to zero in the

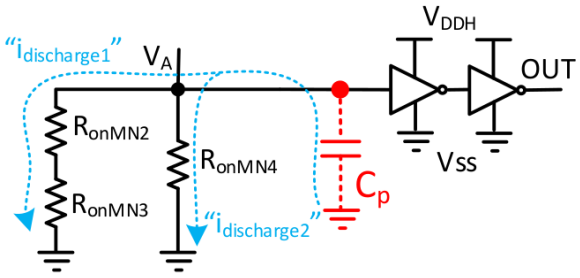


Figure 2.6: Equivalent circuit of the presented LS circuit when IN="0".

cutoff region of MP2. However, the current flowing through TnM during these three regions produces a Gaussian waveform described by:

$$I_{TnM}(t) = \frac{1}{\sigma\sqrt{2}} e^{\frac{-(t-m)^2}{2\sigma^2}} \tag{2.5}$$

where σ is standard deviation, m is mean value, and t represents the time. The amplitude of the flowing current equals $\frac{1}{\sigma\sqrt{2}}$, and the operating time of the circuit equals approximately $m/2$. The LS circuit operation during the transition times and the transfer function of the output buffer must be analyzed to derive the propagation delay formula. The V_O as a function of V_A (input of buffer voltage) is plotted in Figure 2.5.e. In this voltage transfer characteristic, V_M is the switching threshold. Thus, the output of the presented LS changes when V_A reaches V_M. Therefore, when IN="1", to extract the rising propagation delay t_{pr} from 2.2, we replace $i_{Cp}(t)$ by $I_{TnM}(t)$ describe by 2.4. In this way, 2.2 can be rearranged as follows where $V = V_A$.

$$V_A = \frac{1}{C_P} \int_0^T \frac{1}{\sigma\sqrt{2}} e^{\frac{-(t-m)^2}{2\sigma^2}} (t)dt \tag{2.6}$$

The proposed LS is allowed to work only during the propagation delay; therefore, the integral bounds of 2.6 are from t_0 to $t_0 + t_{pr}$, where t_0 indicates the exact start time of the LS input signal (IN) going up and the $t_0 + t_{pr}$ shows the moment that the V_A increases to reach V_M . Thus, replacing V_A by V_M in 2.6 and evaluating this integral over the rising propagation delay t_{pr} yields

$$V_A = V_M = \frac{1}{C_P} \int_0^{t_0+t_{pr}} \frac{1}{\sigma\sqrt{2}} e^{\frac{-(t-m)^2}{2\sigma^2}} (t)dt \tag{2.7}$$

Which can be approximated using Simpson's rule.

$$V_M = \frac{1}{C_P} . \frac{(t_0 + t_{pr}) - t_0}{6} . \left[I_{TnM}(t_0) + 4I_{TnM}\left(\frac{2t_0 + t_{pr}}{2}\right) + I_{TnM}(t_0 + t_{pr}) \right] \tag{2.8}$$

Replacing dt by a time interval Δt in 2.3 yields

$$\Delta t.i_{SD_{MP2}} = C_P.\Delta V_A \tag{2.9}$$

where ΔV_A is the variation of V_A over the time interval Δt. The value of C_p is determined by

$$C_P = \frac{\Delta t.i_{SD_{MP2}}}{\Delta V_A} \tag{2.10}$$

In 2.10, the value of $i_{SD_{MP2}}$ depends on the region of operation of MP2. $i_{SD_{MP2}}$ can be calculated using 2.3 when the MP2 is in saturation and using 2.4 when it is in triode regions. The propagation delay t_p is then derived as follows:

$$t_{pr} = \frac{6C_P V_M}{I_{TnM}(t_0) + 4I_{TnM}\left(\frac{2t_0+t_{pr}}{2}\right) + I_{TnM}(t_0 + t_{pr})} \tag{2.11}$$

when IN goes down, the MN1 is turned off and C_p , which was charged at the previous step when IN="1" starts to discharge through MN2, MN3, and MN4. Figure 2.6 shows the equivalent circuit of the presented LS when IN="0". In this case, to extract the falling propagation delay t_{pf}, the equation of the discharging capacitor must be used. Based on Figure 2.6, we have:

$$V_{C_P}(t) = V_A.e^{\frac{-t_{pf}}{R_{onT}C_P}} \tag{2.12}$$

where R_{onT} equals to $(R_{on2} + R_{on3})||R_{on4}$ (Figure 2.6) and C_p is described by 2.10, while $i_{SD_{MP2}}$ is a discharging currents, as illustrated in Figure 2.6:

$$C_P = \frac{\Delta t.(i_{discharge1} + i_{discharge2})}{\Delta V_A} \tag{2.13}$$

In 2.12, the falling propagation delay of t_{pf} equals the time interval between the input signal (IN), when it goes down and the moment that $V_{C_P}(t)$ decreases to reach V_M . Therefore, by replacing $V_{C_P}(t)$ by V_M in 2.12, t_{pf} is estimated by:

$$V_{C_P}(t) = V_M \rightarrow e^{\frac{-t_{pf}}{R_{onT}C_P}} = \frac{V_M}{V_A} \rightarrow -t_{pf} = R_{onT}.C_P.Ln(\frac{V_M}{V_A}) \rightarrow t_{pf} = R_{onT}.C_P.Ln(\frac{V_A}{V_M}) \tag{2.14}$$

Finally, the propagation delay is estimated by the average of t_{pr} and t_{pf} as follows:

$$t_P = \frac{t_{pr} + t_{pf}}{2} \tag{2.15}$$

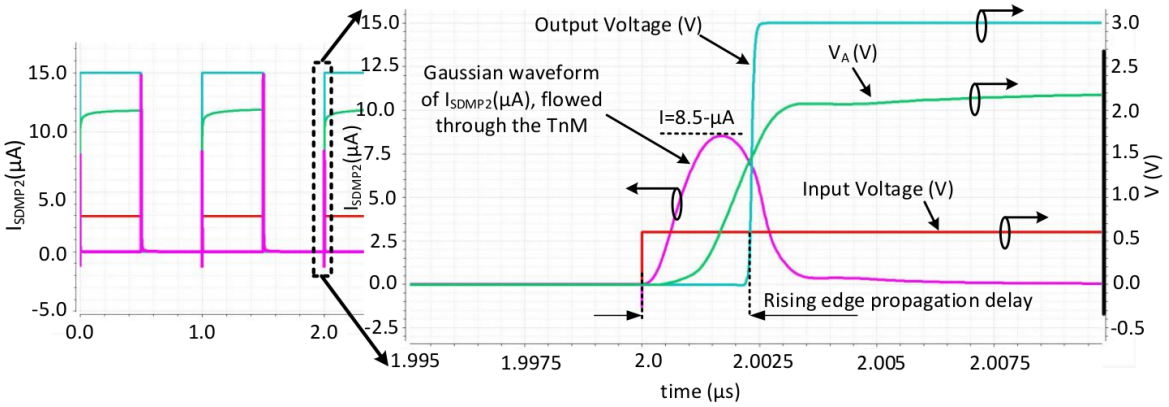


Figure 2.7: Simulated $0.6V$ input pulse, $3.0V$ pulse output, voltage V_A, and current flowing through the TnM signals of the proposed LS at $1MHz$.

2.5.3 Simulated Performance

The simulation results of the presented LS are illustrated in Figure 2.7. It shows an input voltage of $0.6V$, a current "I" flowing through TnM, a V_A gradually increasing, and the output voltage of $3.0V$ with an operating frequency of $1MHz$. In the inset of Figure 2.7, the propagation delay of the rising edge is $1.99ns$. The current flows in the TnM only during a limited time interval within the propagation delay, which provides the current I with a Gaussian wave shape (Figure 2.7). The figure also shows V_A, which is controlled by the feedback network increases smoothly. The peak current flowing inside the TnM during the rising edge of the input/output pulses duration is constrained to $8.5\mu A$. The current in the rising edge is reduced by half, thanks to the utilization of a feedback network, which minimizes any contention and speeds up the operation of the circuit, as shown by the limited duration of this current waveform.

Figure 2.8.a and 2.8.b shows the simulated C_p and voltage at V_A at the transitions, during the rising and the falling propagation delays, respectively, where the LS circuit is permitted to work. Figure 2.8.a presents the simulated C_p and V_A when IN goes up. In this case, V_A is close to zero in the beginning and put the MP2 and MP4 in saturation region. This is when, the variable C_p has its highest parasitic capacitance. Then, when the V_A increases gradually, the MP2 and MP4 goes in the triode region which decreases the parasitic capacitance at node A. Thus, C_p follows a descending curve when the V_A increases when IN="1". As shown in Figure 2.8, C_p can vary from $30fF$ to $7.0fF$ when V_A increases from $0.0V$ to $1.3V$.

Figure 2.8.b illustrates the simulated C_p and V_A when IN goes down. In this case, the voltage V_A is around $1.35V$ in the beginning assuming it was charged previously, the gate voltages of MN2 and MN3 are equal to V_{DDL} , which turned them on. A shown in Figure 2.6, the TnM creates two different branches between V_A and ground for discharging of C_p when IN="0": 1)

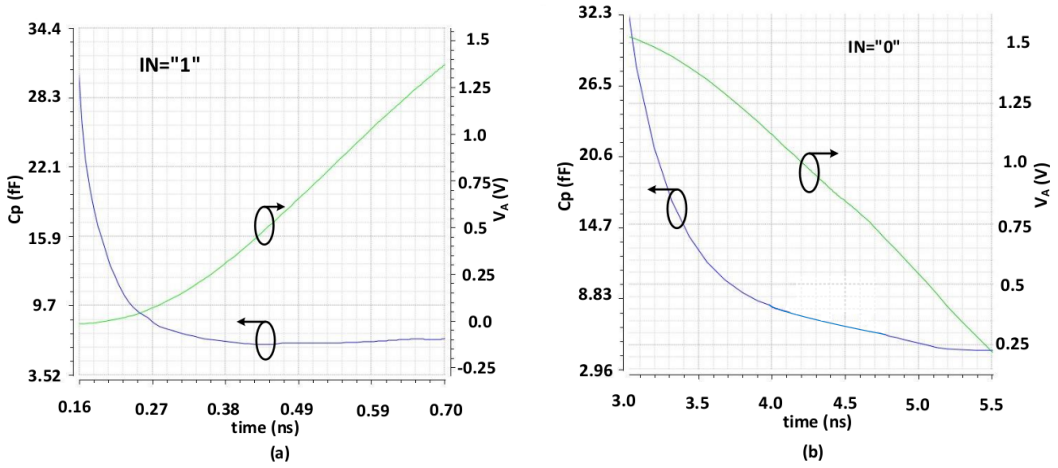


Figure 2.8: Simulated C_p and voltage of V_A during the (a) rising (IN="1") and (b) the falling propagation delay (IN="0").

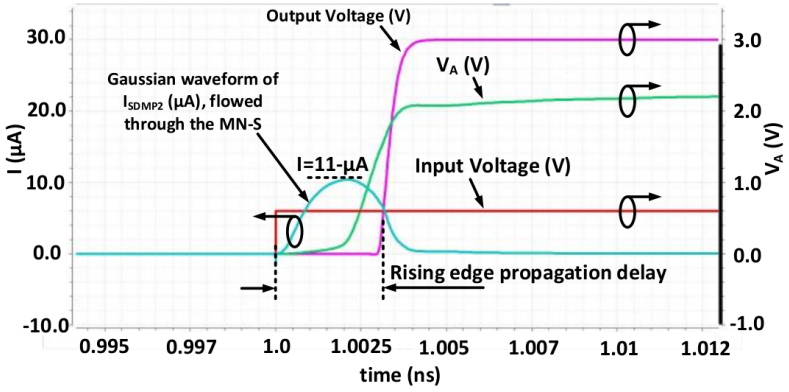


Figure 2.9: Enlarged view of simulated $0.6V$ input pulse, $3.0V$ pulse output, voltage V_A, and current flowing through the single transistor signals of the LS at $1MHz$.

through MN4, and 2) through MN2 and MN3 in series. In the beginning, the V_A is large which puts MN4 and MN2 in the saturation region, significantly increasing the parasitic capacitance at node A. At this moment, C_p can be as high as $32fF$ according to the simulation (Figure 2.8.b). When V_A decreases, the voltage across TnM decreases, and consequently, MN4 and MN2 goes to the triode region, which decreases the parasitic capacitance at Node A. Then, when IN="0" and V_A starts decreasing, C_p decreases as shown in Figure 2.8.b. The value of C_p varies from $32fF$ to $5fF$ when V_A decreases from $1.40V$ to $0.20V$ for IN="0".

We compare the LS operation with a single transistor (Figure 2.5.f) instead of using the TnM. Figure 2.9 presents an input voltage of $0.6V$, a current "I" flowing through a single transistor (replacing the TnM), a V_A gradually increasing, and the output voltage of $3.0V$ with an operating frequency of $1MHz$. In the inset of Figure 2.9, the PD of the rising edge is $3.18ns$.

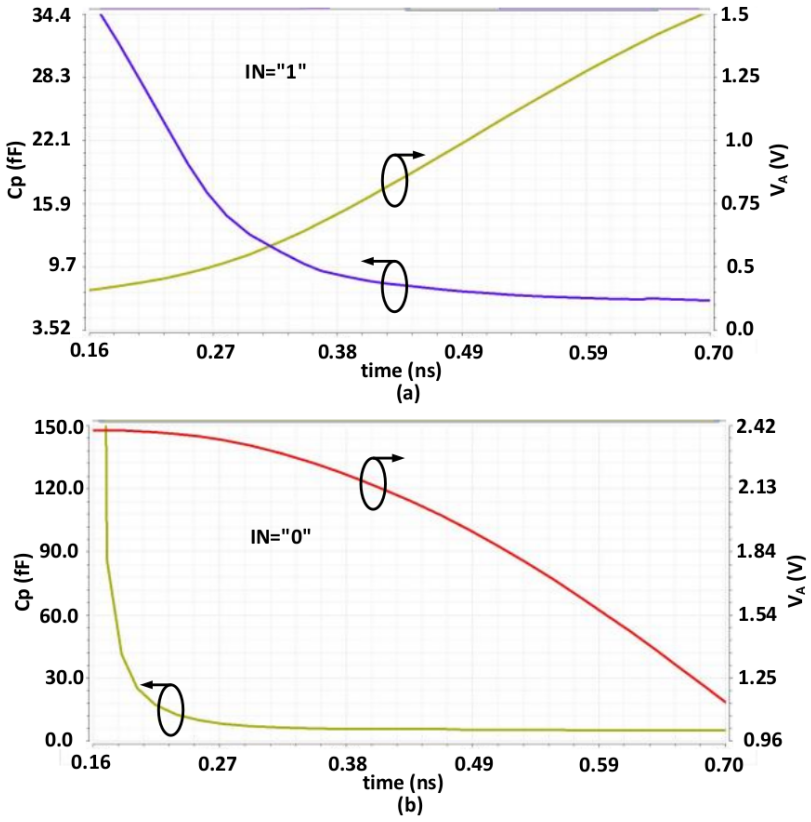


Figure 2.10: Simulated C_p and voltage of V_A when a single transistor is used instead of the TnM during the (a) rising (IN="1") and (b) the falling PD (IN="0").

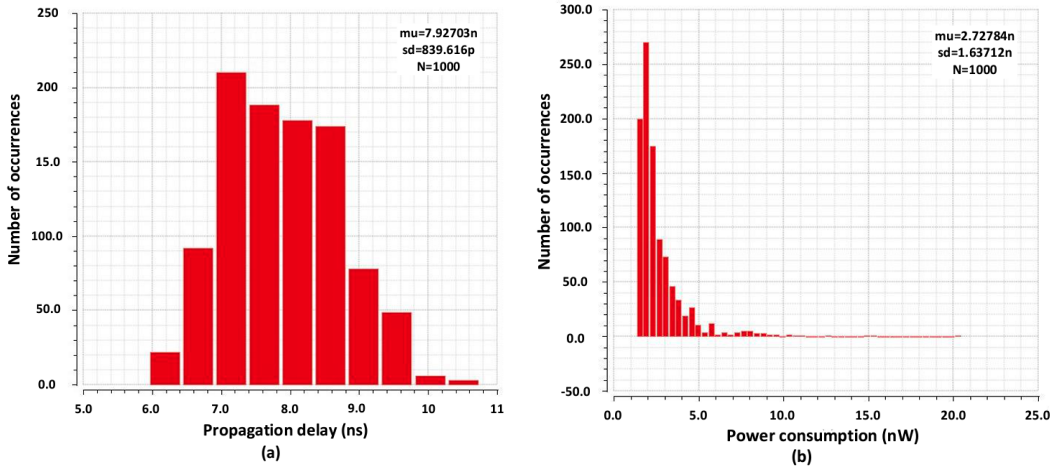


Figure 2.11: Evaluation of the proposed LS operation with a Monte–Carlo simulation: (a) Propagation delay, (b) power consumption.

In this setting, the simulated PD was 1.6 times longer than with the proposed LS circuit, which is using the TnM. The amplitude of the current is $I = 11\mu A$, compared to $I = 8.5\mu A$

when the TnM was used. To elaborate, when a single transistor is used instead of the TnM, the low side of the presented LS design (Figure 2.4.a) performs like a conventional LS circuit (Figure 2.1) that suffers from contention. Consequently, the power consumption and the PD of this LS increase compared to our solution, as simulated and shown in Figure 2.9. Figs. 2.10.a and 2.10.b show the simulated C_p and voltage V_A during the, respectively, rising and the falling transitions in which the LS circuit (using a single transistor instead of the TnM) is permitted to work. In Figure 2.10.a, the input of the single transistor (used instead of the TnM) is "0" and the single transistor is turned off. So, the variation of C p in node A depends on the parasitic capacitances of MP2 and MP4 (Figure 2.4.a) where C_p varies from $35fF$ to $7fF$ during the transition of the LS output from "0" to "1". During this transition, V_A varies from $0.2V$ to $1.5V$. When IN="1" the operation of the LS is independent of the parasitic capacitance of the low side of the LS. Therefore, the variation of C_p and V_A in Figure 2.10.a and Figure 2.8.a are the same. Figure 2.10.b illustrates the simulated C_p and V_A when IN goes low. In this case, the input of the LS, which is using a single transistor rather than the TnM, is "1" and the single transistor is turned on. Since V_A has reached its maximum voltage after the previous step (IN="1"), it places MP2 and MP4 in their cutoff region. Therefore, C_p depends on the parasitics of a single transistor and is independent of the parasitic of MP2 and MP4. When V_A becomes large, the single transistor (i.e. MN2 in Figure 2.1) is put in the saturation region, significantly increasing the parasitic capacitance at node A. At this time, C_p can be as high as $150fF$ according to the simulation (Figure 2.10.b). When V_A decreases, the voltage across the single transistor decreases, and consequently, the single transistor goes into the triode region, which decreases the parasitic capacitance at node A. Then, when IN="0" and V_A starts decreasing, C_p decreases as shown in Figure 2.10.b. The value of C_p varies from $150fF$ to $5fF$ when V_A decreases from $2.4V$ to $1V$ for IN="0". Comparing Figure 2.10.b with the Figure 2.8.b, the equivalent parasitic capacitance at node A of the LS with the single transistor is greater than with the TnM, due to the generated contention in this node, which consequently increases the PD. When the PD increases, the voltage of V_A reaches V_M, showing that the variation of $V_A(dV_A/dt)$ is slow. The equivalent capacitance at node A is, therefore, large ($C_p = i_{MP4}/(dV_A/dt)$), as shown in Figure 2.10.b.

Validating the operation of the proposed design against mismatch and process corners is critical because the current delivered to TnM is closely related to the V_{SG} and V_{SD} of MP2 and MP4, respectively. MP2 and MP4 shown in Figure 2.4.a are responsible for adjusting the current delivered to the TnM; hence, they must be designed and be laid out to be robust against process variations. The design is simulated for the typical case corner using typical NMOS and PMOS transistor parameters, $V_{DDH} = 3.0V$, $V_{DDL} = 1.6V$, capacitive load (C_L) = $100fF$, and operating frequency of $1MHz$. The simulation yields a value of the propagation delay (average of rising and falling PD) of $7.86ns$ for the presented LS. A worst-case simulation is performed to assess the effects of process variations. In the AMS design kit, "worst power" (WP) means "fast NMOS/fast PMOS" whereas, "worst speed" (WS) means "slow NMOS/slow

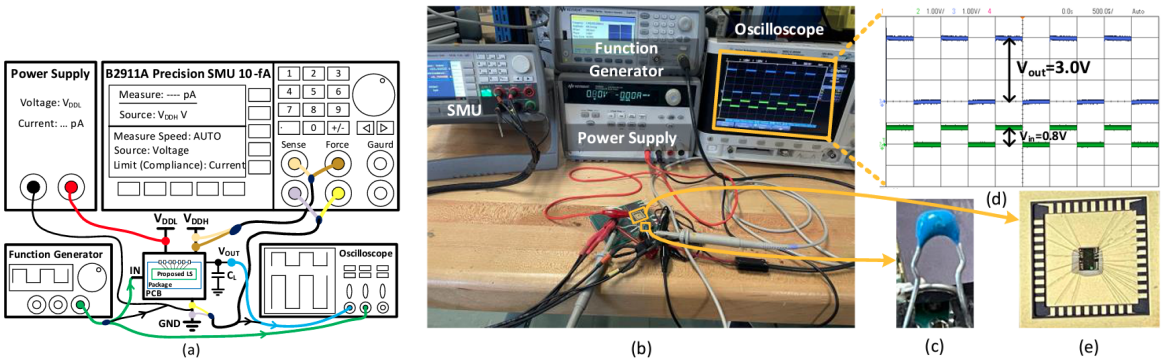


Figure 2.12: Test setup, (a) Setup block diagram, (b) Fabricated chip under test, (c) $10pF$ capacitive load, (d) Input and output measured waveforms, (e) Wire-bonded die.

PMOS". The WP and WS represent the worst operating conditions due to process variations. The simulated values of the propagation delay for the WP and WS cases are 6.46 and $12.41ns$, respectively.

The WS case has the longest delay, while the WP yields the shortest delay. A Monte–Carlo simulation is performed for $V_{DDH} = 3.0V$, $V_{DDL} = 1.6V$, capacitive load $(C_L) = 100fF$, and an operating frequency of $1MHz$ to further examine the influence of process variations on the operation of the presented LS. The resulting propagation delay and its log-normal distribution of variance of 0.105, mean propagation delay (mu) of $7.92ns$, and standard deviation (sd) of $0.839ns$ are presented in Figure 2.11.a. The power consumption of the LS is also assessed to validate the operation of the proposed circuit against mismatch and process corners. The design is simulated for the typical case corner using typical NMOS and PMOS transistor parameters, $V_{DDH} = 3.0V$, $V_{DDL} = 0.8V$, capacitive load $C_L = 100fF$, and an operating frequency of $1kHz$. The simulation yields a total power consumption of $1.89nW$ for the presented LS. A worst-case simulation is performed to assess the effects of process variations on power consumption. The simulated values of the power consumption for the WP and WS cases are 12.16 and $1.565nW$, respectively. A Monte–Carlo simulation is performed for $V_{DDH} = 3.0V$, $V_{DDL} = 0.8V$, capacitive load $C_L = 100fF$, and an operating frequency of $1kHz$ to further examine the influence of process variations on the operation of the presented LS. The resulting power consumption and its log normal distribution of variance of 0.6, mean power consumption (mu) of $2.7278nW$, and standard deviation (sd) of $1.6371nW$ are presented in Figure 2.11.b.

2.6 Experimental Results

Figure 2.12 shows the test setup used to perform the experimental validation of the fabricated LS circuit. As shown in the block diagram of Figure 2.12.a, a capacitive load is used to perform the measurement. A source measurement unit (SMU) with a resolution of $10fA$ (KEYSIGHT-

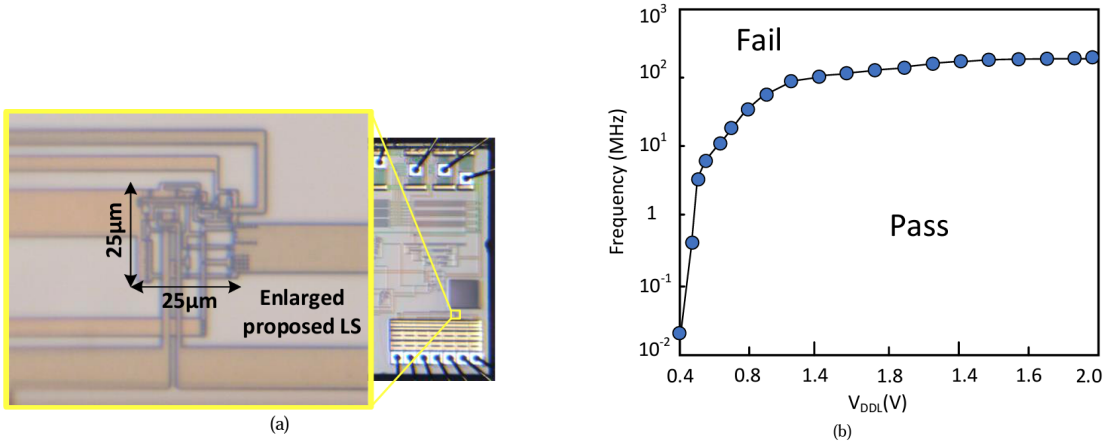


Figure 2.13: Experimental performance: (a) Micrograph of the fabricated LS in CMOS AMS $0.35\mu m$ and partially enlarged view (area: $25\times25\mu m^2$), (b) Shmoo plot for operating frequency versus V_{DDL}.

B2911A) is utilized to accurately measure the power consumption. Figure 2.12.b shows the test equipment and the fabricated chip under test mounted on a custom printed circuit board (PCB). Figure 2.12.c presents the enlarged view of one $10-pF$ capacitive load for the test. Figure 2.12.d shows the screenshot of the oscilloscope and the measured input and output waveforms of the fabricated LS in parallel with amplitudes of $0.8V$ and $3.0V$, respectively. Figure 2.12.e shows the enlarged view of the wire-bonded fabricated chip.

The presented LS circuit was fabricated in an AMS $0.35\mu m$ CMOS process. A photograph of the fabricated chip prototype is shown in Figure 2.13.a. The fabricated LS occupies an area of $25\times25\mu m^2$. The performance of the fabricated LS is measured over a wide range of frequencies. The maximum operating frequency of the circuit is shown for different input signal amplitudes while the V_{DDL} change from $0.4V$ to $2.0V$ and $V_{DDH}=3.0V$. The proposed LS successfully works up to $130MHz$ (at $V_{DDL}=1.6V$) as shown in Figure 2.13.b, while similar LS circuits are limited to $100MHz$, like in [61].

The total power consumption is another important parameter that must be considered. The measured power consumption of the fabricated LS circuit is presented in Figure 2.14.a as a function of the frequency of the input pulse. Power consumption is measured experimentally for input signal amplitudes and V_{DDL} of $0.6, 0.7, 0.8, 1.0, 1.4$, and $1.8V$, a fixed $V_{DDH}=3.0V$, and a capacitive load $C_L=20pF$. The consumed power increases with the frequency of the input pulse. Except the input inverter, which is supplied by V_{DDL}, the other parts of the presented LS circuit are supplied by V_{DDH}, as shown in Figure 2.4.a, and they consumes the main power. V_{DDL} is only connected to the input inverter that consumes a negligible amount of power. Accordingly, the measured power consumption shown in Figure 2.14.a is the result of the product of V_{DDH} and the current drained from V_{DDH} measured by the SMU. Among

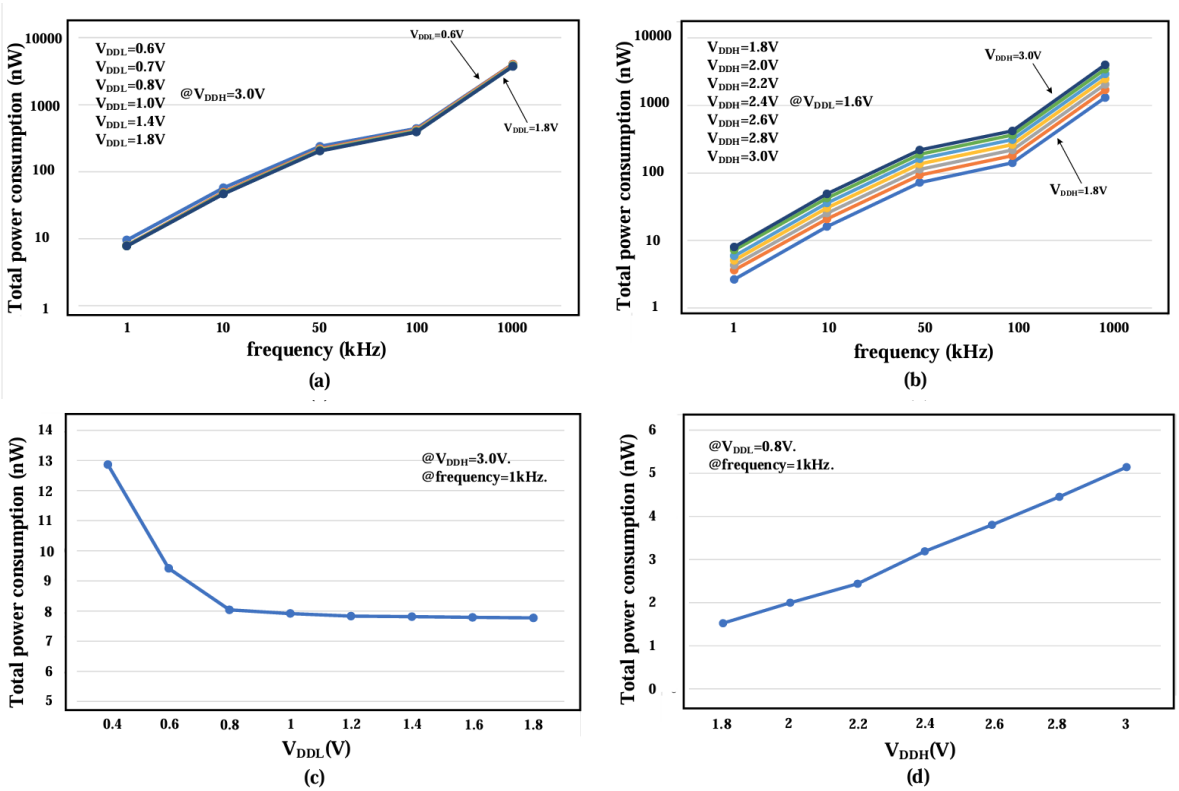


Figure 2.14: Measured power consumption variation with used $C_L = 20pF$: (a) Across frequency for different V_{DDL}, (b) Across frequency for different V_{DDH}, (c) for different V_{DDL} at $V_{DDH} = 3.0V$ and a frequency of $1kHz$, and (d) for different V_{DDH} at $V_{DDL} = 0.8V$ and a frequency of $1kHz$.

the six measured curves, the highest power consumption variation occurs when the circuit converts the input signal with the lowest amplitude into $3.0V$ (from $0.6V$ to $3.0V$). While the lowest power consumption variation is obtained when the circuit converts the input signal with the highest amplitude into $3.0V$ (from $1.8V$ to $3.0V$). The circuit needs more power to provide a higher conversion gain. Since in all six measured curves presented in Figure 2.14.a the V_{DDH} is fixed, the variation of measured consumed power versus V_{DDL} are close to each other.

The variation in power as a function of the input frequency over several values of V_{DDH} ($1.8, 2.0, 2.2, 2.4, 2.6, 2.8$, and $3.0V$) is shown in Figure 2.14.b. The results are obtained for a fixed V_{DDL} and a capacitive load $C_L = 20pF$. In this set of measured curves, the power consumption also increases with the frequency. In these seven curves, the highest measured power occurs at $V_{DDH} = 3.0V$ while the lowest one is observed at $V_{DDH} = 1.8V$.

The measured consumed power variation of the LS circuit is presented in Figure2.14.c for different values of V_{DDL} at $V_{DDH} = 3.0V$, capacitive load $C_L = 20pF$, and an operating frequency of $1kHz$. In this descending curve, when V_{DDL} increases (i.e. the amplitude of the

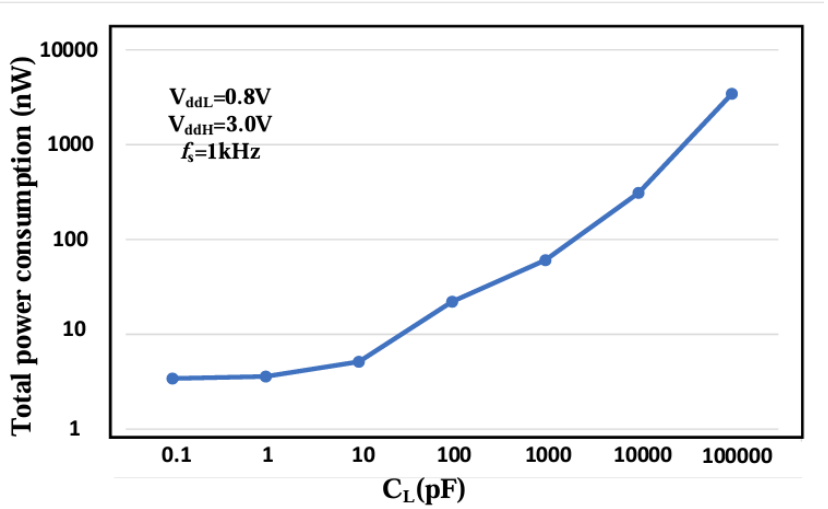


Figure 2.15: Measured power consumption versus capacitive load for a $1-kHz$ input pulse, $V_{ddL} = 0.8V$, and $V_{ddH} = 3.0V$.

input signal increases), the implemented LS requires a lower amount of energy to convert the input signal to a signal with an amplitude of $3.0V$, because V_{DDH} is fixed at $3.0V$. The total power consumption of the LS circuit versus V_{DDH} for a fixed $V_{DDL} = 0.8V$, capacitive load $C_L = 20pF$, and an operating frequency of $1kHz$ is shown in Figure 2.14.d. The measured power consumption that is within a range of a few nW increases with V_{DDH}.

The static power consumption (P_S) of the presented LS circuit is measured for different input signal values. The P_S measured for these DC input values, without applying any input pulse, is within a few pW. When the input of the LS is connected to GND ("0") or V_{DDL} ("1"), the measured P_S are 31.5 or $260pW$, respectively. The power consumption versus capacitive load (C_L) at $1kHz$ pulse shaped input, $V_{DDL} = 0.8V$, and $V_{DDH} = 3.0V$ is measured and presented in Figure 2.15. In this measurement, the C_L is changed from $0.1pF$ to $100nF$ and the power is measured at each step. As the C_L increases, the power consumption increases.

The propagation delay of the LS circuit is measured for an input pulse signal of a frequency of $1MHz$ and a duty cycle of 50% while an inverter, integrated in the chip, is used as a load. As shown in Figure 2.16.a, the LS shows a rising propagation delay of $4ns$, while it shows a falling propagation delay of $11.2ns$ (see Figure 2.16.b). Thus, the average propagation delay of the presented LS after a transition is $7.6ns$.

Given that the propagation delay is an essential parameter of a LS circuit, Figures 2.16.c and 2.16.d are provided to evaluate the variation of the propagation delay versus the voltage variation in V_{DDL} and V_{DDH}. The rising and falling propagation delays versus V_{DDL} at a fixed $V_{DDH} = 3.0V$, and while using an integrated inverter as load, is presented in Figure 2.16.c. The propagation delay, especially the rising edge delay for $V_{DDL} < 0.8V$, is long because

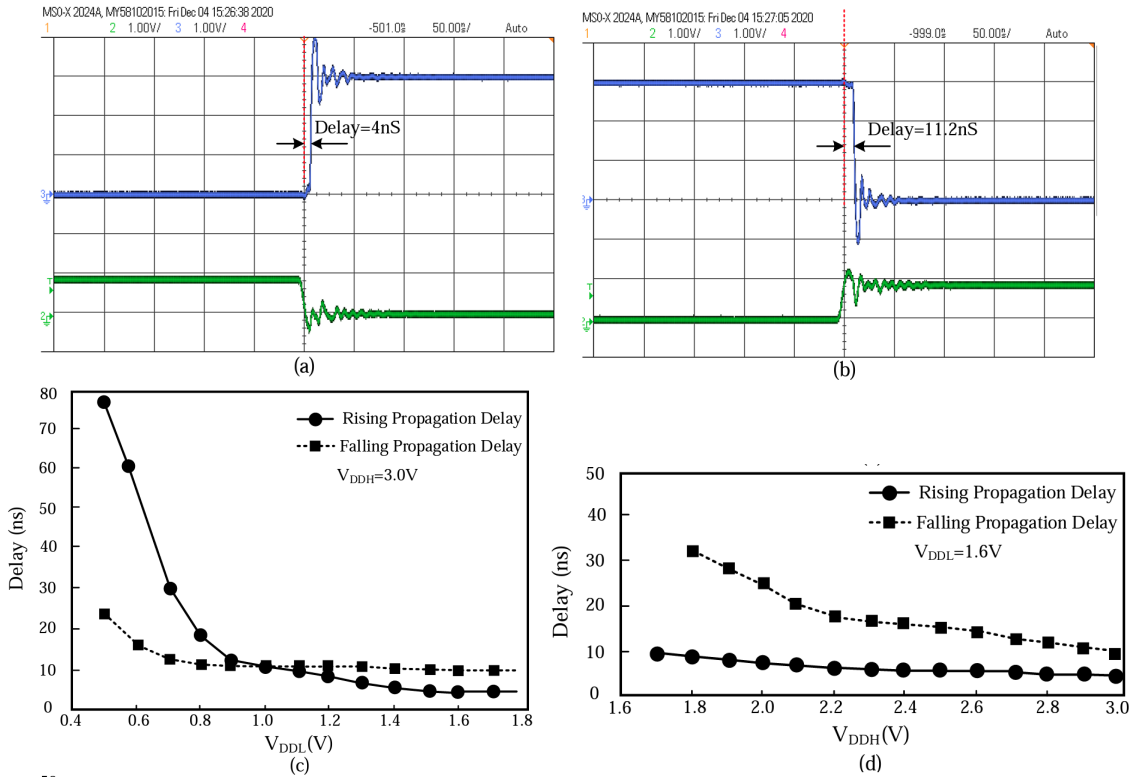


Figure 2.16: Measured propagation delay when an integrated inverter is used as load: (a) Rising edge at the output for a $1-MHz$ input pulse with an amplitude of $0.8V$, and $V_{DDH} = 3.0V$ (b) Falling edge at the output for a $1-MHz$ input pulse with amplitude of $0.8V$, and $V_{DDH} = 3.0V$ (c) Variation of rising and falling propagation delay versus V_{DDL} at $V_{DDH} = 3.0V$, and (d) Variation of rising and falling propagation delay versus V_{DDH} at $V_{DDL} = 1.6V$.

of the larger conversion gain of the circuit when it is converting a low-amplitude signal into a high amplitude signal of $3.0V$. The measured delay variation curve, especially the falling propagation delay, is almost flat for $V_{DDL} > 0.8V$. The measured variations of the rising and falling propagation delays versus V_{DDH} at fixed $V_{DDL} = 1.6V$, while an integrated inverter is used as load, are shown in Figure 2.16.d. In this figure, the propagation delay is measured when the LS converts a pulse shaped signal with a $1.6V$ amplitude into $3.0V$. In Figure 2.16.d, the propagation delay of the circuit is almost flat, especially the rising propagation delay, which shows that the circuit provides good performance at lower conversion gain (converting 1.6 to $3.0V$).

Designing circuits to work in subthreshold is essential for low-power budget applications, such as in biomedical implants [62; 63]. The results in Figure 2.17 show that the operation of the circuit in subthreshold meets the requirements of high performance operation, thanks to the TnM and feedback network of the proposed LS (Figure 2.4.a). Figure 2.17 presents the measured waveforms of the implemented LS for an $80mV$ and $50kHz$ input pulse converted into a $3.0V$ waveform. As can be seen, a clean $3.0V$ pulse is extracted at the output of the

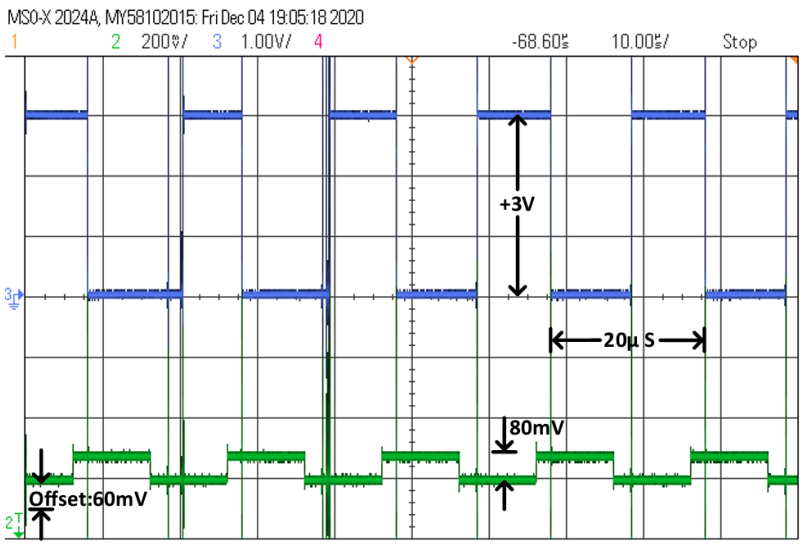


Figure 2.17: Measured waveforms of LS at $50kHz$ input pulse with amplitude of $80mV$ into $3.0V$, while an integrated inverter is used.

Table 2.2: Performance Summary and Comparison with other solutions. E_c: Energy consumption; P_s: Static power consumption; FoM=Range/delay

References	Range(V)	CMOS Process (nm)	Delay (ns) ($@V_{DDL}(V)$ $f_{in}(MHz)$)	$E_C(J)$ ($@V_{DDL}(V)$ $f_{in}(MHz)$)	$V_{DDH}(V)$	$P_s(pW)$	FoM	Result
TVLSI'17 [36]	$0.20-1.10$	40	$11.57(@0.4, 1.0)$	$67.4f(@0.4, 1.0)$	1.1	90.1	0.060×10^9	Simulated
TVLSI'15 [59]	$0.10-1.0$	90	$16.60(@0.2, 1.0)$	$77.0f(@0.2, 1.0)$	1	8700	0.048×10^9	Simulated
TCAS-I'17 [60]	$0.33-1.80$	180	$29.0(@0.4, 0.50)$	$61.5f(@0.4, 0.500)$	1.8	330	0.048×10^9	Measured
JSSC'21 [6]	$0.32-1.20$	14	$8.30(@0.5, 1.0)$	$0.1p(@0.8, 1.0)$	1.2	–	0.084×10^9	Measured
JSSC'12 [61]	$0.40-3.0$	350	$15.0(@0.8, 0.01)$	$5.8p(@0.4, 0.010)$	3	230	0.146×10^9	Measured
TVLSI'16 [7]	$0.40-1.80$	180	$30.0(@0.4, 1.0)$	$150.0f(@0.4, 1.0)$	1.8	300	0.026×10^9	Simulated
This work	$0.08-3.0$	350	$7.60(@1.6, 1.0)$	$3.4p(@0.8, 0.001)$	3	31.5	0.184×10^9	Measured

presented LS circuit from an ultra-low amplitude input pulse. Therefore, the proposed LS provides a convenient interface between a weak signal and a digital processor.

2.7 Discussion and Performance Comparison

The achieved experimental validation revealed that the utilization of TnM remarkably improves the performance of the proposed LS. The TnM relies on the equivalent parasitic capacitances of the MOSFET utilized in the LS circuit. The feedback network prevents the LS circuit from consuming a large amount of power during the transitions. This minimizes the propagation delay, allows operation in subthreshold, and minimizes static and dynamic power consumption. Table 2.2 summarizes and compares the performance of the presented LS circuit with other solutions. The experimental results show an improvement of approximately 8.5% of the propagation delay compared with [6], which uses a current mirror-based LS. In addition, the proposed circuit can successfully convert a pulse signal over a wide range of conversion $(0.08-3.0V)$ and with an amplitude as small as $80mV$ into $3.0V$ while working in subthresh-

old and consuming only $28nW$. Moreover, the measured maximum operating frequency of the fabricated circuit improved by 30% improvement compared to the other solutions. The static and dynamic power consumptions is comparable with those of the recently published papers in this field. A reasonable criterion to consider the performance of a LS design is to measure the propagation delay while the circuit is working over a given conversion range. Indeed, the more conversion range results in more propagation delay. Therefore, a Figure of Merit (FoM) is recommended to assess the performance of the propagation delay over the conversion range. In our presented LS, the propagation delay of $7.6 - ns$ is measured while the LS was converting a pulse with an amplitude of $1.6V$ to a pulse with an amplitude of $3.0V$. Thus, a $FoM = (3.0 - 1.6)V/(7.6ns) = 0.184 \times 109$ is achieved. With this FoM, the larger value is the better. A FoM is used in [64] to compare the different LS designs together. This FoM uses the multiplication of the total power consumption with the propagation delay ($nW.ns$). However, all design compared with this FoM must use the same V_{DDL} which is not applicable for the results presented in Table 2.2.

2.8 Conclusion

A new high-performance LS circuit topology is presented in this work. The presented current mirror-based structure offers wide-range and fast LS conversion. This structure can convert subthreshold input signal levels into above-threshold levels with minimum propagation delays. The operation of the proposed circuit is efficient, especially in the case of contention on high-impedance nodes, owing to the utilization of a feedback network and a voltage controlled current source (VCCS). The utilization of an equivalent parasitic capacitance of three interconnected n-type MOSFETs (TnM) circuit to implement the level-shifting scheme of the circuit is sound and optimized. The advantageous effect of this TnM minimizes the propagation delay and dynamic power consumption, leveraging its equivalent parasitic capacitance as the level shifting part of LS. In addition, this approach enhances the conversion range compared to the other mechanism. The measured performance of the test chip implemented in a $0.35\mu m$ AMS design process outperforms other solutions. The discussion and the measured performance of the presented LS illustrated the numerous advantages of this solution, namely wide conversion range, low power consumption, and short propagation delay.

Chapter 3

An Active Dead-Time Control Circuit With Timing Elements for a 45-V Input 1-MHz Half-Bridge Converter

3.1 Résumé

Dans cette étude, un circuit de contrôle du temps mort est proposé pour générer des délais indépendants pour les côtés haut et bas des commutateurs des convertisseurs en demi-pont. En plus de réduire considérablement les pertes des convertisseurs de puissance à transistors GaN, la méthode proposée atténue le courant de fuite par l'application de commutateurs de puissance superposés. Le circuit présenté ici comprend une architecture à condensateurs commutés et est mis en œuvre dans la technologie AMS $0.35\mu m$. Dans sa mise en œuvre, le circuit de contrôle du temps mort proposé occupe une surface de silicium de $70\mu m \times 180\mu m$. Pour réaliser cette technique, une source de courant à large oscillation est utilisée des deux côtés. Chaque côté de la source de courant est équipé de deux condensateurs, de deux déclencheurs de Schmitt et de trois portes de transmission. Les résultats montrent que les côtés bas et haut des commutateurs du convertisseur en demi-pont projeté nécessitent respectivement des délais de 35 et $62ns$. Les performances du circuit à temps mort proposé sont évaluées en l'assemblant avec le convertisseur en demi-pont. Le prototype du circuit de gestion du temps mort proposé permet de réduire de 40% les pertes de puissance dans le circuit en demi-pont.

3.2 Abstract

In this study, a dead-time control circuit is proposed to generate independent delays for the high and low sides of half-bridge converter switches. In addition to greatly decreasing the losses of power converters, the proposed method mitigates the shoot-through current through the application of superimposed power switches. The circuit presented here comprises a switched

capacitor architecture and is implemented in AMS $0.35\mu m$ technology. In the implementation, the proposed dead-time control circuit occupies a silicon area of $70\mu m \times 180\mu m$. To realize the technique, a two-sided wide swing current source is employed. Each sides of the current source comes with two capacitors, two Schmitt triggers, and three transmission gates. Results show that the low and high sides of the projected half-bridge converter switches respectively require delays of 35 and $62ns$. The performance of the proposed dead-time circuit is evaluated by assembling it with the half-bridge converter. The proposed dead-time prototype achieves a 40% drop in power losses in the half-bridge circuit.

3.3 Introduction

Different applications require various types of power converters, including DC–DC boost/buck converters [65; 66; 67], class-D power amplifiers [68], half-bridge converters [69], and switched-capacitor circuits [70]. These converters are mainly applied to system basis chips in automation, including those used in airbag squib drivers, braking valve drivers, and power steering integrated circuits [71; 72; 73; 74]. Power converters are also widely used in neural stimulation and wireless power transmission in implantable biomedical microsystems [17; 75; 76; 32].

Dense and miniaturized power converters comprising small passive components are useful in high-frequency application, but the switching losses of power switches limit the operating frequency of these devices [77; 78; 79]. In addition to switching losses, power converters suffer from conduction and gate charge losses that affect their efficiency [80; 81]. Their safety also tends to be affected by power switches' false or immature ON-state [82]. These drawbacks are mainly attributed to the parasitic inductances and capacitances of power switches [83]. A half-bridge output stage is shown in Fig. 3.1 along with the equivalent circuit of a power switch with the associated parasitic inductance. The figure also demonstrates the power switch's input capacitance C_{iss}, output capacitance C_{oss}, and reverse transfer capacitance C_{rss}. These elements cause electromagnetic interferences and parasitic oscillations and are thus undesirable [84].

In implementing gate drivers, several techniques are used to accelerate the charge/discharge of unwanted elements of C_{iss} and C_{oss} and to mitigate the switching and gate charge losses of power switches. A soft-switching technique was proposed in [85; 86; 87] to reduce switching losses. The resonant gate driver approach is also widely used to reduce gate charge losses [88]. In [82], a specific double-pulse test was conducted to study the hard switching of power switches. Moreover, the high-voltage energy storing (HVES) approach was utilized to increase the gate driving speed [89]. In the HVES methodology, the authors aimed to decrease the adverse effects of parasitic gate loop inductance by embedding an on-chip resonant LC tank.

Standard high-voltage automotive data buses often require operating voltage from $-27V$ to $+45V$ to drive hydraulic actuators with power converters [90]. The power converters mainly

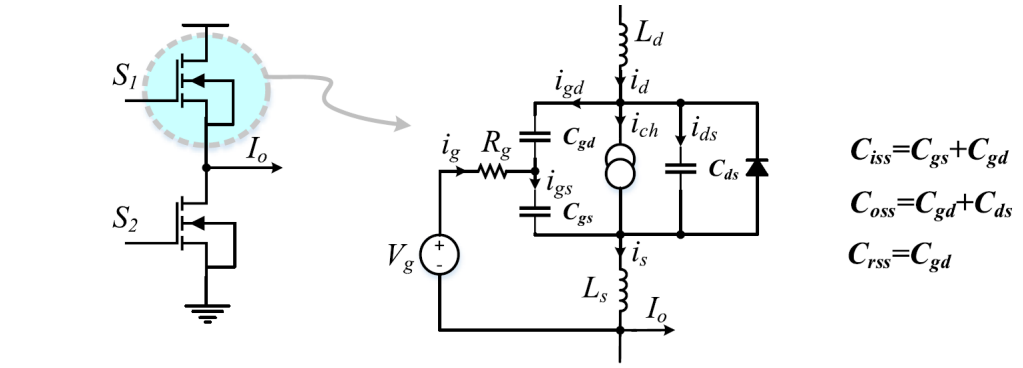


Figure 3.1: Half-bridge output stage and equivalent circuit of power switch during operation.

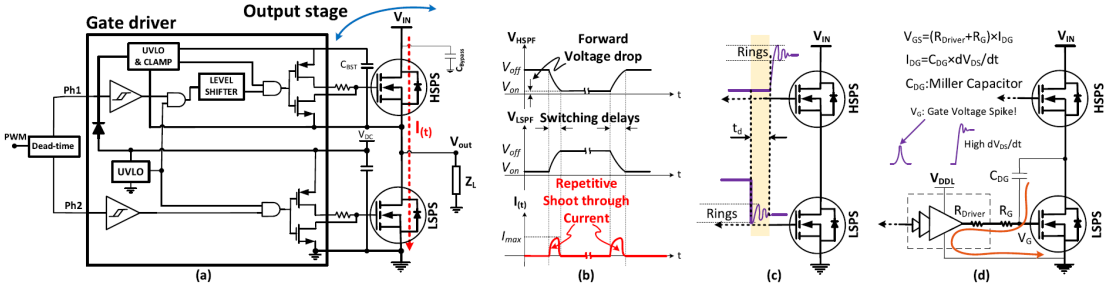


Figure 3.2: Power converter and the different sources of shoot-through: (a) half-bridge circuit with simplified dead-time circuit, (b) impact of switching delays, (c) ringing effect due to the output parasitic capacitance C_{oss} of HSPS, and (d) Miller capacitor effect.

operate with dead-time control circuits (DTCCs) [91]. These circuits have two main structures. Logic gates are sometimes used to create delays and thereby implement a dead-time between the activation of complementary conductive paths and avoid overlap [92; 93; 9; 94]. In other cases, time constants are used and implemented with resistors, capacitors, current sources, etc. [95]. The latter is preferred for high voltage applications that require long delays [96]. In the use of logic gates, a fixed circuit that is not changed during operation is typically implemented. In the use of time constants, the controlling signals and switching techniques should be regulated to control the current source and capacitors and thereby create the dead-time.

A set of two superimposed complementary power switches makes up a power converter [97]. Half-bridge converters, in particular, utilizes two superimposed complementary power switches as the output stage to drive a given load (Figure 3.2.a). Most of the power budget in a half-bridge circuit is consumed in the output stage, during which shoot-through and losses occur. Shoot-through arises when two power switches are inadvertently closed at the same time, thereby causing unnecessary power losses and potential damages [98]. Such phenomenon can be avoided by creating a dead-time interval between the control signals of power switches

[99]. Figure 3.2.a shows the circuit of a half-bridge convertor, including a dead-time part, gate driver, high-side power switch (HSPS), and low-side power switch (LSPS). Figure 3.2.b shows that in the scenario in which one of the superimposed complementary switches is turned on before or while the other switch is turned off, a shoot-through current can flow from the supply rail to the ground during the overlap time interval. In this case, non-overlapping driving signals should be provided to the power switches via a DTCC [100].

Shoot-through may also result from ringing in the driving circuit; such phenomenon increases the gate-to-source voltage V_{GS} of the high-side switches above the threshold voltage V_{TH} of the power transistor (Figure 3.2.c) [101]. This issue is commonly observed in gallium nitride (GaN) high electron mobility transistors (HEMTs) because of their low $V_{TH} \sim 1V$ [102] relative to other types of power switches, such as silicon carbide and conventional silicon (V_{TH} of $\sim 2.5V$) [4]. This property of GaN HEMTs is attributable to the output parasitic capacitance C_{oss} of the high-side power switch. GaN HEMTs are commonly applied to power converters because of their various advantages, including their low on-resistance and parasitic capacitance, high operating temperature, and small package size. Furthermore, small junction capacitance, and no reverse recovery loss are three advantages of GaN transistors over Si or SiC MOS. While, in the Si or SiC MOS, in addition to reverse recovery, there is also forward bias losses V_F of the body diode.

As for the ringing effect in the driving circuit, the issue can be addressed by adjusting the damping ratio or by providing enough dead-time interval between the driving signals of complementary switches. The transient response of the main switching circuit can cause the formation of Miller capacitance at the gate of the low-side complementary switch. This condition results in the V_{GS} of the switches to exceed V_{TH} (Figure 3.2.d). In this scenario, the switching frequency of the circuit should be fine-tuned to handle the high dv/dt and di/dt without exceeding V_{TH} [34]. Non-overlapping signal generators and dead-time controllers are therefore important in guaranteeing the safe and efficient operations in half-bridge circuit power converters. These solutions are effective in addressing shoot-through and ringing and can thus decrease losses.

The presented DTCC design enhances the performance of half-bridge power converters. It uses a two-sided wide swing current source, a switched capacitor structure, and a particular signaling technique to generate precise delays between the required non-overlapping gate driving signals, and accurately drive a half-bridge circuit and avoid losses or excessive power consumption due to shoot trough, etc. Compared to other dead-time circuit solutions, our DTCC circuit has the key advantage of generating two asymmetric delays, the operating parameters of which are independent of the half-bridge circuit parameters, for the high side and the low side of the converter. Additionally, the presented solution allows to generate required long delays between the high-side and low-side driving signals, which is highly desirable in high voltage applications. Such design reduces the imperfections in the entire signal prop-

agation process in the half-bridge converter to achieve lower power consumption and better signal quality. In Section 3.4, we describe the main idea and advantages of the proposed dead-time structure. The circuit implementation is also discussed. In Section 3.5, we detail the experimental results. In Section 3.6, we summarize our conclusions.

3.4 Proposed Dead-Time Circuit

Cross-connected NAND/NOR gates and a chain of inverters in feedback loops are used in conventional dead-time circuits to generate non-overlapping signals with delays [34]. The propagation delay of these inverters provides the delays in the non-overlapping signals. This configuration of integrated circuits produces typical pico second delays and is thus not useful in various power applications requiring long delays in the range of nanoseconds (e.g., high-voltage circuits, high currents, and highly reactive loads) [95].

3.4.1 Proposed Architecture

The proposed DTCC enables the generation of nanosecond delays and mitigates shoot-throughs at the same time. This property of the proposed DTCC decreases the power losses in power converters. Figure 3.3.a shows the presented scheme. Specifically, the scheme comprises two-sided wide swing current sources (TS-WSCS) for linearly charging two capacitors C_1 and C_2 on each side of the circuit. Each side of the circuit also has three switches for controlling the charging and discharging processes. Moreover, the right and left branches of the circuit are equipped with two Schmitt triggers (STs) with defined comparison hysteresis windows. These STs restrict the values of the generated delays between the two non-overlapping driving signals.

Figure 3.3.b shows the predefined state machine that reflects the originality of the proposed idea. Specifically, the figure illustrates the non-overlapping timing methodology for the low- and high sides of half-bridge converters. The states in this machine are change polarity "CP", close switch "CS", charge capacitors "CC", and Schmitt trigger "ST". The presented active dead-time circuit is controlled by a finite state machine (FSM) to generate the required half-bridge control delays. The circuit operation based on the FSM is clarified according to Figure 3.3.b. The circuit operation is illustrated according to Figure 3.3.b. Given an operating high-side power switch (operating HS), the polarity of the signal at its output is supposed to change (CP HS) instantly when the deactivating signal arrives at its gate (deactivating HS). However, the process is time consuming because of the large parasitic capacitance of the HSPS. In meeting the required time, the Φ_1 signal should close the corresponding controlling switch before the LSPS is activated (CS LS). The TS-WSCS then charges the capacitor C_2 linearly (CC LS) to reach the upper bound of the utilized ST (ST LS). At this point, the HSPS is deactivated completely (deactivated HS). This process should generate t_{d2}. In Figure

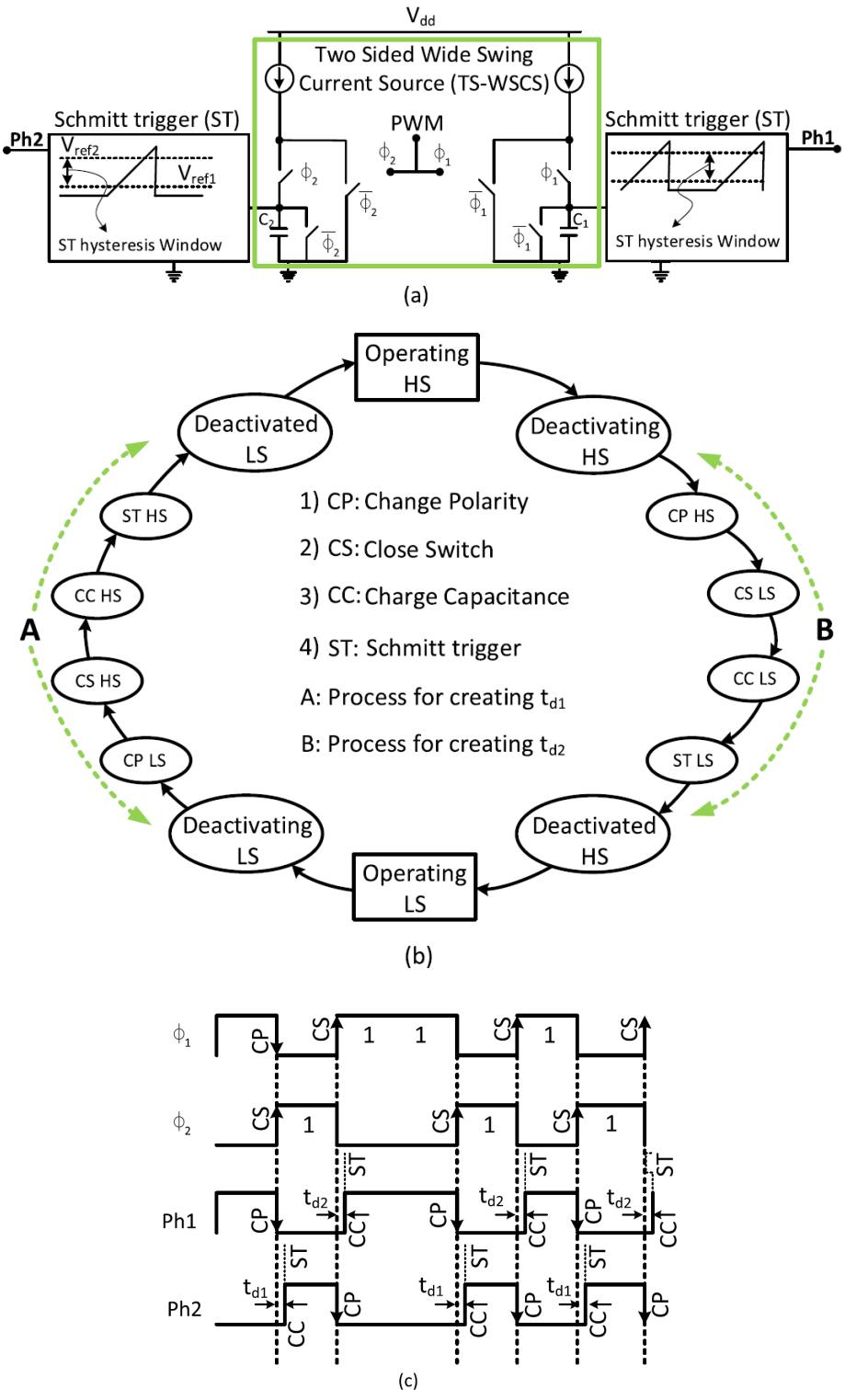


Figure 3.3: Proposed dead-time control circuit: (a) simplified schematic, (b) state machine representation, and (c) timing diagram.

3.3.b, the process is labeled as the "B" process. The activation of the LSPS (operating LS) is provided similar to "B" process which is named "A" process. This process should also generate the time required to completely deactivate the LSPS before the activation of the HSPS again. Figure 3.3.c presents the timing diagram, which includes four curves tagged by t_{d1}, t_{d2} and the different working states of the proposed DTCC [95].

The proposed DTCC approach offers the following benefits:

1. The amount of current delivered by the TS-WSCS, the values of the capacitors, and the comparison levels of STs determine the generated delay of the circuit. Adjusting these parameters thus helps obtain the long delays needed in high-voltage and power applications, including those requiring large parasitic capacitances (e.g., power switches).

2. To set the delays between non-overlapping signals independently, the proposed circuit generates different time delays t_{d1} and t_{d2}. Such capability facilitates the adjustment of the delays of the low- and high-side parts. In particular, the driving signals of the HSPS go through more stages (i.e., level shifter and gate driver) than those of the LSPS. Thus, ensuring the absence of any overlap between switch operations calls for a longer t_{d2} than t_{d1}.

3. The signals for arranging the capacitors and current source in the presented circuit are based on a predefined FSM. Specifically, this FSM is used to charge/discharge the capacitors and utilize/remove the current source and thereby produce a suitable dead time. This property reflects the originality of the presented circuit.

A gate driver with two independent inputs serves as the interface between the proposed DTCC and output stage of the half-bridge converter. This interface helps fulfill the practical operation of the proposed dead-time circuit for the half-bridge converter. Specifically, the gate driver receives non-overlapping signals from the proposed DTCC and then delivers them to the HSPS and LSPS. It also provides the power switches with an adequate amount of driving current from its supply.

3.4.2 Circuit Implementation

Our dead-time circuit prototype chip fulfills the R-L load requirements of a standard high-voltage data bus [90], having $V_{IN} = 45V$ and driving a R-L load of $R = 100\Omega$ and $L = 150\mu H$ with a half-bridge converter. The presented dead-time circuit prototype can provide high-side and low-side delays of $35ns$ and $62ns$ to such a half-bridge converter. The transistor-level implementation of the proposed DTCC is shown in Figure 3.4.a. The TS-WSCS supplies the charging current of capacitors C_1 and C_2. The sources are formed by nine MOSFETs (MP1–MP7 and MN1, MN2). MN1 and MN2 are two diode connected transistors that serve

Table 3.1: Aspect ratios of TS-WSCS transistors.

	MP1, MP2	MP3	MP4-MP7	MN1, MN2
W(μM)	10	5	10	0.4
L(μM)	0.35	0.35	0.35	5

as current sources for respectively generating I_{in} and I_{bias}. MP1, MP2, and MP3 are used to bias the cascaded transistors MP4, MP5, MP6, and MP7. The following design strategies are considered to ensure that the TS-WSCS circuit functions:

1. Currents I_{bias} and I_{in} are set to be equal for MP1–MP7 to be in their saturation region.
2. The width of MP3 is set to half of that of MP1, MP2, and MP4–MP7. The setting should bias MP1, MP4, and MP6 properly in the active region.
3. Minimum gate lengths are adopted for MP1, MP4, and MP6 to maximize the frequency response.

The aspect ratios of the transistors used for the TS-WSCS are listed in Table 3.1. A ramp signal is generated using the timing elements MN3–MN8 (i.e., transmission gates), $C_1 - C_2$, and control signals $\Phi_1 - \Phi_2$. Driven by Φ_1 and Φ_2, MN3–MN8 are utilized to linearly regulate the charging and discharging times of C_1 and C_2. The TS-WSCS circuit can be quickly turned on and off. Therefore, a $0.6V$ offset resulting from the residual charges (Figure 3.4.a) in C_1 and C_2 after one transition is added to the generated ramp signal at nodes 1 and 2 (Figure 3.4.a). In this case, MN3 and MN6 are added to remove the residual charge and cancel the generated offset. The addition is possible if MN3 and MN6 are activated in phase with MN5 and MN8, respectively. The required delays are generated using two STs. In setting the STs'hysteresis windows, their reference voltages are adjusted to $V_{ref1} = 0.76V$ and $V_{ref2} = 1.74V$. Following the adjustment, the STs can then generate a non-overlapping signal that provides enough dead-time to avoid shoot-throughs in the converter resulting from the ramp signals generated across the capacitors C_1 and C_2. Figure 3.4.a shows that the ST circuits are surrounded by two boxes. Figure 3.4.b illustrates the effect of the offset added to the ramp signals of node 1 with and without the addition of MN3 and MN6. The slope of the ramp signals decreases because of the added offset without the use of MN3 and MN6. The generated delay is thus $5ns$ longer than expected.

The following equations are arranged to show the relation between the generated delays t_{d1} and t_{d2} and the circuit parameters. The equation for the capacitor is:

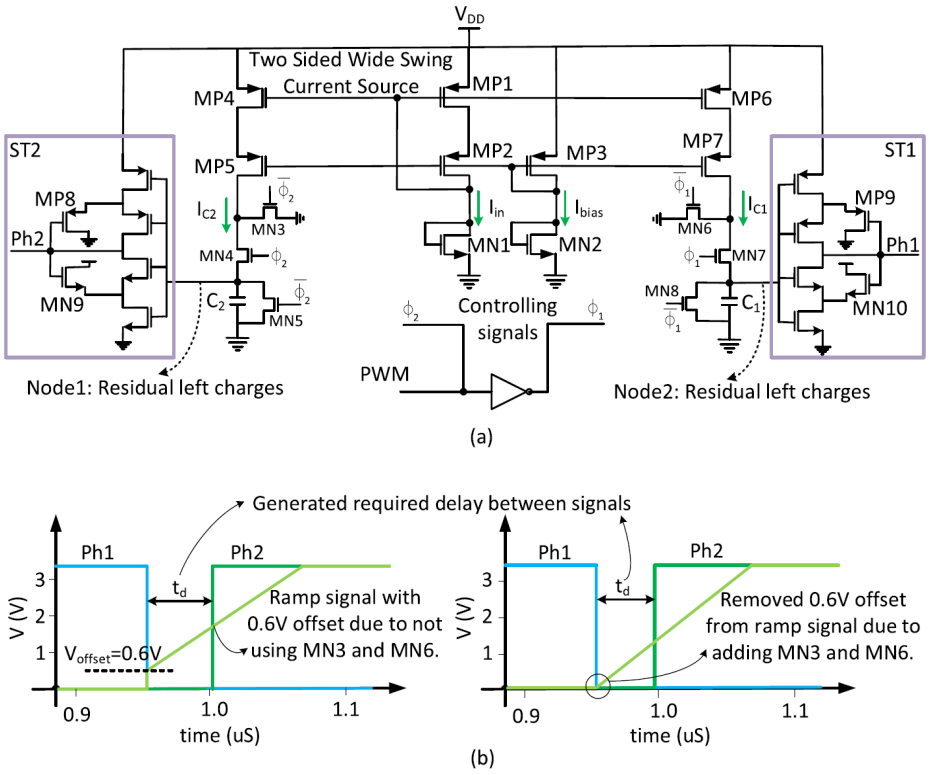


Figure 3.4: (a) Transistor-level implementation of proposed DTCC, (b) added offset to the ramp signal with and without MN3 and MN6.

$$i_c(t) = C.\frac{dV_c(t)}{dt}, (t_0 \leq t \leq t_1) \Rightarrow i_c(t).dt = C.dV_c(t), (V_0 \leq V_c(t) \leq V_1) \tag{3.1}$$

Constant current is delivered to the capacitors. Hence, the following equation is obtained through the integration from t_0 to t_1 and from V_0 to V_1, with the upper and lower bounds of the integrals being ST reference voltages and their corresponding start and stop times:

$$\int_{t_0}^{t_1} i_C(t)dt = C.\int_{V_0}^{V_1} dV_c(t) \Rightarrow I \times [t_1 - t_0] = C \times [V_c(t_1) - V_c(t_0)] \Rightarrow I \times [t_1 - t_0] = C \times [V_1 - V_0] \tag{3.2}$$

where $V_C(t_0) = V_0 = 0$ as the capacitors are reset after each period and $t_0 = 0$ is the time at which the capacitors start charging at the beginning of each period. Assume that t_1 is the time at which the ramp signal ($ramp = k.t$, where $k = I/C$ and "t" is the time) reaches the high level of the ST window. In this case, t_{d1} and t_{d2} can be expressed as:

$$t_{d1} = (C_1/I_{C_1}) \times V_{ref2},$$
$$t_{d2} = (C_2/I_{C_2}) \times V_{ref2}, \tag{3.3}$$

where V_{ref2} is the trigger voltage of the STs located on each side of the TS-WSCS. The generated delays in the proposed DTCC rely on the values of the I_{C_1} and I_{C_2} currents (Figure 3.4.a) that the TS-WSCS delivers to the capacitors. Given the relation between the output current and the values of I_{in} and I_{bias}, the operation of the proposed design against mismatch and process corners should be validated. Specifically, MN1 and MN2 (Figure 3.4.a) that are used to adjust the biasing current should be made robust against process variations. The operations on both sides of the proposed DTCC during the generation of t_{d1} and t_{d2} are the same. A different t_d is due to the different parameter values on each side of the circuit. Therefore, the circuit is evaluated to be robust against process variations for one of the delays (i.e., t_{d2}). For the designed circuit of the typical case corner, i.e., typical NMOS and PMOS transistors and $V_{DD} = 3.3V$, the simulated dead-time value t_{d2} is $67ns$. A worst-case scenario is simulated to cope with process variations. In the AMS kit, "fast NMOS/fast PMOS" corresponds to "worst power" (WP) while "slow NMOS/slow PMOS" corresponds to “worst speed” (WS). In this study, we evaluate the operation of the proposed circuit in the WP and WS cases. The WP and WS cause process variations and are thus the worst conditions of component operations. The simulated dead-time values t_{d2} for the WP and WS cases are 50.0 and $90.0ns$, respectively. Obviously, the WS case yields the longest dead-time while the WP has the shortest dead-time. In this work, the impact of the process variations on the performance of the proposed DTCC is studied using a Monte Carlo simulation. A supply voltage of $V_{DD} = 3.3V$ is set for the simulation. The results for t_{d2} are shown in Figure 3.5. Specifically, the simulated t_{d2} shows a log-normal distribution with a variance of 0.14. The average delay of t_{d2} is $67.36ns$, and the standard deviation is $9.59ns$. This work aims for a robust design against process variations with the lowest standard deviation. Therefore, the dimensions of MN1 and MN2, which are responsible for biasing the circuit, should be increased. At the same time, the same aspect ratio "W/L" should be maintained. However, both tasks lead to a trade-off between the chip area and the sensitivity of the generated delay to process variations.

The impact of the parasitic inductance on the produced dead-time delays is examined through post-layout simulations. The relevant voltages, including the non-overlapping signals (Ph1, Ph2), and the ramp signal across capacitors C_1 and C_2 are shown in Figure 3.6. The figure also presents the parameters of $t_{d1} = 35ns$, $t_{d2} = 67ns$, $V_{ref2} = 1.74V$, and $V_{ref1} = 0.76V$. After the addition of the MN3 and MN6 transmission gates at high and low STs, the $0.6V$ offset is effectively removed from the ramp signal. As observed in Figure 3.6, the generated delays between the non-overlapping signals rely mainly on the slope of the ramp signals. Moreover,

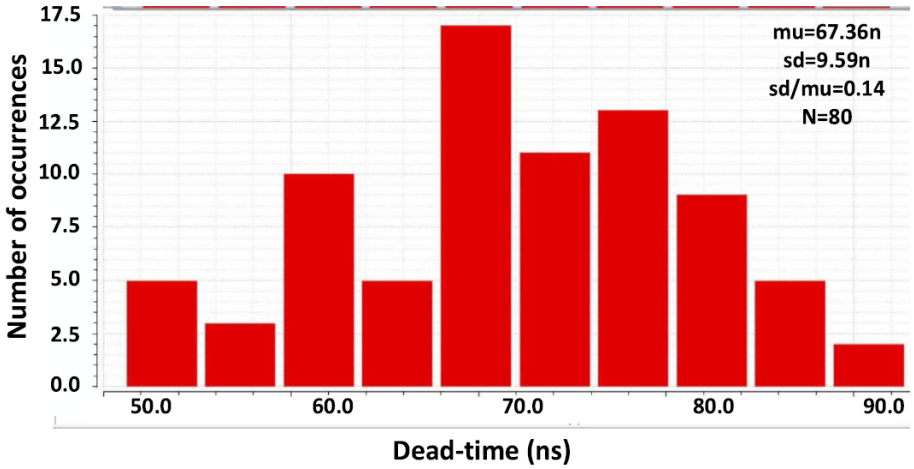


Figure 3.5: Evaluation of DTCC operation with a Monte-Carlo simulation.

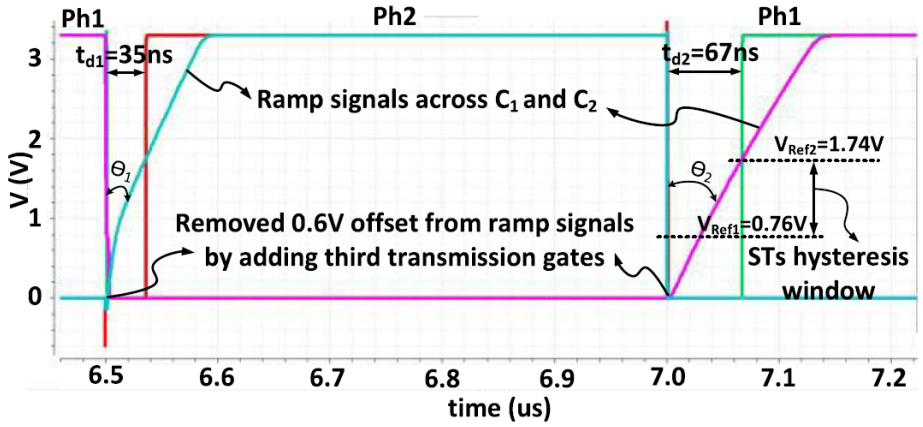


Figure 3.6: Simulated dead time between signals.

the hysteresis windows of the STs differ (as the capacitance of C_2 is relatively large, the slope of the ramp signals is slow). Therefore, the upper bound of the Schmitt trigger V_{ref2} on the corresponding side of C_2 meets the ramp signals later. The generated t_{d2} is thus longer than t_{d1}. The delays in the design could be set in other ways. For example, the amount of the current delivered to the capacitors can be set. Another option is to set the STs' hysteresis window parameters by the upper and lower bounds on the basis of the sizes of MP8, MP9, MN9, and MN10 in the design (Figure 3.4.a).

In Figure 3.6, Θ_1 and Θ_2 respectively denote the angles between the generated ramp signals and the falling edges of the non-overlapping signals. A ramp signal with a sharp slope yields a small angle. A small angle in this case results in a short dead-time because the ramp signal produced meets V_{ref2} of the corresponding ST early. At this point, the proposed DTCC is

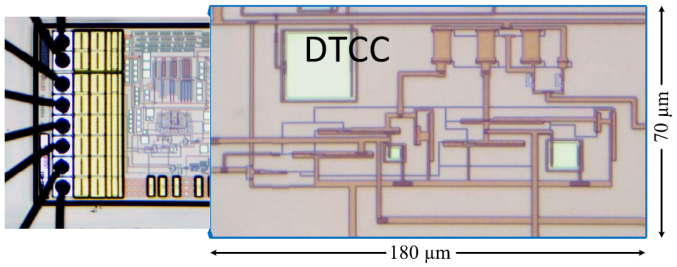


Figure 3.7: Chip micrograph of fabricated DTCC in CMOS AMS $0.35\mu M$.

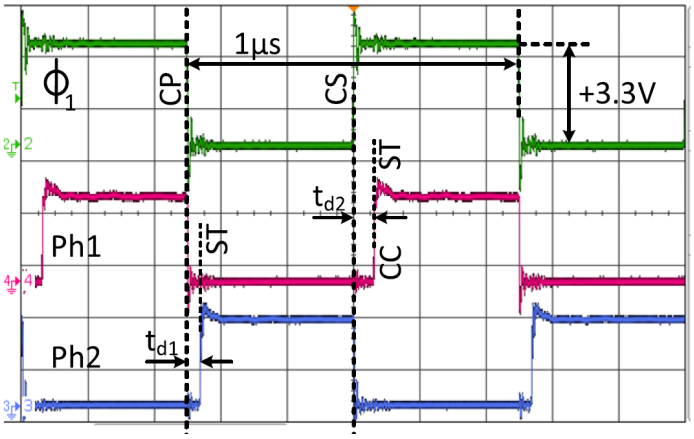


Figure 3.8: Measured generated dead-time delays between non-overlapping signals.

implemented to produce fixed t_{d1} and t_{d2} for a specific power converter. In the post-layout simulation, the proposed DTCC without PADs consumes $190\mu W$ of power under no load conditions.

3.5 Measured Performance

We fabricate the proposed DTCC in AMS $0.35\mu m$ CMOS. The micrograph of the integrated chip prototype is shown in Figure 3.7. The proposed circuit occupies an area of $180\mu m \times 70\mu m$. The integrated DTCC is designed to generate $t_{d1} = 35ns$ and $t_{d2} = 62ns$ for the LSPS and HSPS, respectively, by using $C_1 = 30fF$ and $C_2 = 55fF$. The lower and upper bounds for both STs on each side are 0.76 and $1.74V$, respectively. The delays meet the requirements of a projected power converter. The dead-time required by a power converter is contingent on the supply voltage V_{IN} and the current delivered to the load [67].

3.5.1 Results of DTCC measurement

The measured non-overlapping signals produced by the DTCC prototype for a $1MHz$ input square wave signal Φ_1 and a supply voltage of $3.3V$ are shown in Figure 3.8. The figure

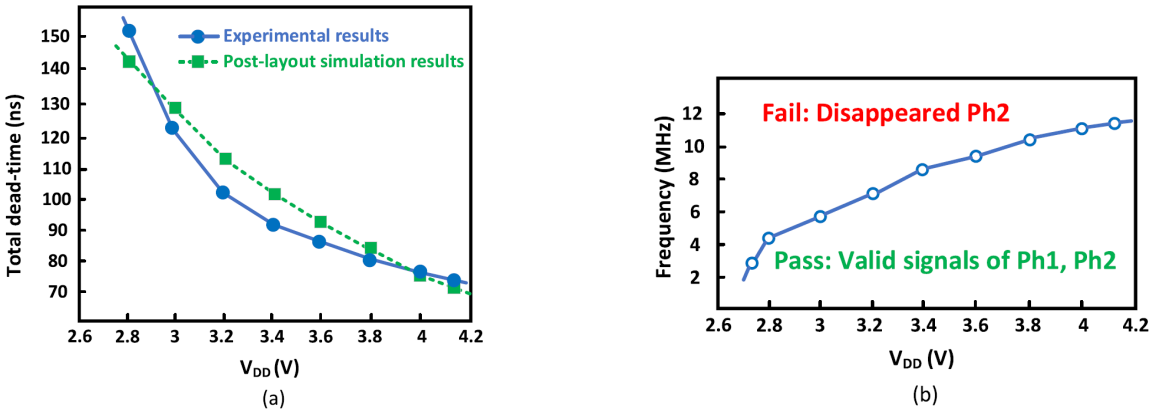


Figure 3.9: Measured DTCC performances: (a) Comparison of the experimental and post-layout simulation results of the dead-time delays variation versus the power supply voltage V_{DD}. (b) The effect of V_{DD} on the maximum operating frequency of DTCC.

also presents the four states (i.e., CP, ST, CS, and CC), delays (i.e., t_{d1} and t_{d2}, and signals (i.e., Ph1 and Ph2). A good agreement is reached between the experimental results and the projected timing diagram (Figure 3.3.c). Moreover, the measured results agree well with the post-layout simulation results (Figure 3.9.a). The measured and simulated delays with a precision of 0.01% and a supply voltage of $3.3V$ are equal to $t_{d1} = 35ns$ for $C_1 = 30fF$. However, the measured results $62ns$ and simulated results $67ns$ present a difference in t_{d2} values for $C_2 = 55fF$. The results are presented in Figure 3.9.a. An increase in the supply voltage V_{DD} causes a decrease in the generated dead-time between the non-overlapping signals according to a second-order function. In particular, the second-order effect is more distinct in the measurement than in the simulation (Figure 3.9.a). An increase in V_{DD} boosts the V_{SG} values of MP1, MP4, and MP6 (Figure 3.4.a). Moreover, the second-order function relates to the V_{SG} values of the MOSFETs biased in the saturation region and their drain current charge the capacitors C_1 and C_2. As presented in Equation 3.3, the I_{C_1} and I_{C_2} currents delivered to the capacitors are inversely related to the amount of generated dead-time (i.e., a large charging current results in a steep ramp signal, which in turn produces a short dead-time). Therefore, the generated dead-time is associated with V_{DD} by a second-order descending curve. This work experimentally validates the operation of the proposed DTCC.

The validation is performed at different supply voltages V_{DD}, over a frequency range of $10Hz - 11MHz$, and square input signals. Herein, t_{d1} and t_{d2} determine the frequency limitation $11MHz$ at different V_{DD}. The delays produced by the non-overlapping control signals are independent of the input signal frequency. Therefore, the frequency of the input signal can be increased up to $fp \leq 1/(t_{d1}+t_{d2})$. Such a condition represents the extreme case in the proposed design. The effect of changes in V_{DD} on the maximum operating frequency is illustrated in Figure 3.9.b. The limitation is observed to only affect Ph2 of the non-overlapping signals

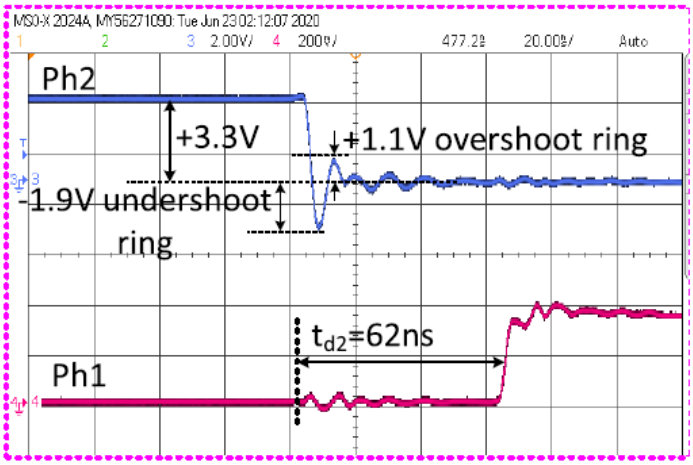
generated. This result is due to the fact that an increase in frequency with a specific value of V_{DD} causes the values of t_{d1} and t_{d2} to be close. Therefore, Ph2 disappears while Ph1 is available. As mentioned previously, dead-time delay drops when V_{DD} increases. A reduced dead-time delay in turn increases the maximum operating frequency (Figure 3.9.b).

The amplitudes of the undershoot and the overshoot ringing near the edge of the measured signals are -1.9 and $+1.1V$, respectively (Figure 3.10). In Figure 3.10.a, the red and blue curves mark Ph1 and Ph2, respectively. Ph1 reaches a high state when the ringing of its complimentary signal Ph2 becomes totally damped. The results reveal slight variations in the ringing observed in the non-overlapping parts of control signals which are provided for the gates of the HSPS and LSPS, respectively. The differences may be explained as follows: avoiding any overlap between the on-states of the superimposed complimentary switches of the power converter requires the generation of adequate dead-time t_d between the control signals. Figures 3.10.a and 3.10.b respectively present the measured t_{d2} ($62ns$) and t_{d1} ($35ns$).

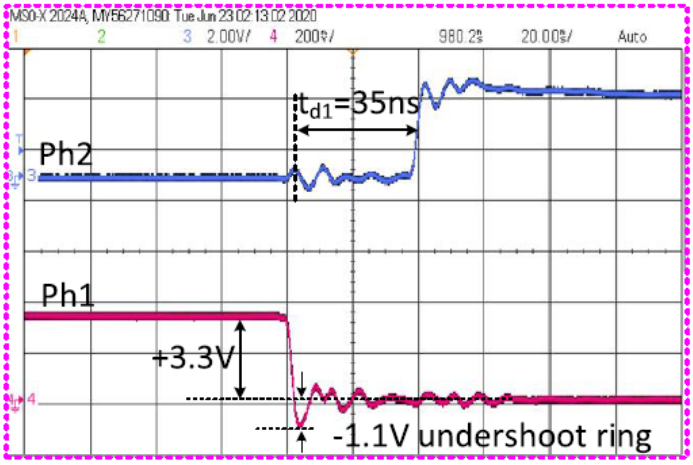
In Figure 3.11, the measured power consumption of the proposed DTCC is shown as a function of the input frequency for different values of V_{DD}. The power indicated refers to static and dynamic power. Dynamic power is consumed by the charge and discharge of the capacitive load in the outputs of Ph1 and Ph2 of the fabricated chip connected to the half-bridge converter. Additional losses may also be incurred in the active PADs because of the internal CMOS stages used to buffer the I/O signals.

The capacitive load is estimated by measuring the slew rate of the non-overlapping signals generated when the DTCC is connected to the half-bridge converter, that is, $C_L = i_{dynamic}/(slewrate)$. The slew rate is equal to $0.16V/ns$ when the signals at the output of the DTCC range from $0.5V$ to $3.0V$; the corresponding dynamic current is $2.5mA$. The circuit has two outputs, namely, Ph1 and Ph2. Dynamic current is consumed to drive the capacitive loads at the outputs of Ph1 and Ph2. Therefore, the total capacitive load of the DTCC is $C_{Lph1} + C_{Lph2} = 2.5mA/(0.16 \times 109) = 15.62pF$. Given the inputs of the gate driver having the same circuit, the capacitive load at each output is $C_{Lph1} = C_{Lph2} = 7.81pF$.

As shown in Figure 3.11, the power consumption varies with frequency. This relationship is attributed to the switching losses of the MOSFETs that increase almost linearly with the operating frequency. In the proposed DTCC, the output currents I_{C_1} and I_{C_2} increase with V_{DD}. The same is true for the power consumption. Figure 3.11 also presents the variations of power consumption with the operating frequency given eight specific V_{DD} values. The maximum frequency of the circuit changes in line with V_{DD}. As the generated dead-time decreases with V_{DD}, the upper curve ($V_{DD} = 4.1V$) achieves the highest maximum frequency with $11.4MHz$. As the frequency of the non-overlapping signal further increases and exceeds $1/(t_{d1} + t_{d2})$, Ph2 drops and then disappears completely. For a valid non-overlapping signal, the power consumption varies from $16.8mW$ to $41mW$ on the basis of V_{DD}, which can vary



(a)



(b)

Figure 3.10: Measured outputs of Ph1 and Ph2: (a) generated delay t_{d2} for the high side of half-bridge converter, (b) produced delay t_{d1} for the low side of half-bridge converter, and the amplitude of individual ringing at the edges of each phase.

from $2.8V$ to $4.1V$, and the operating frequency, which ranges from $100kHz$ to $11.4MHz$.

3.5.2 Validation with Half-Bridge Circuit

The DTCC prototype is validated by implementing a half-bridge circuit with commercial components. The block diagram of the implemented half-bridge circuit with the fabricated DTCC is illustrated in Figure 3.12. The eGaN HEMTs are driven by the LM5113 gate driver (Figure 3.12). The power eGaN FET can work at voltages of up to $100V$ and deliver currents as high as $5A$ to the load. Two independent high-side and low-side TTL logic inputs comprise the gate driver. These inputs are compatible with the fabricated DTCC chip. The LM5113

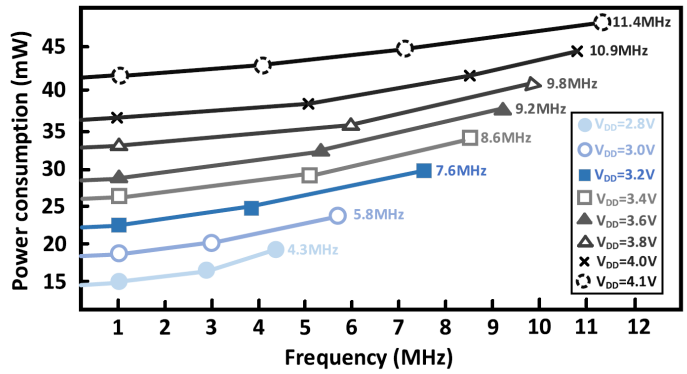


Figure 3.11: Measured power consumption variation with respect to the input frequency for different values of V_{DD} for $7.81pF$ estimated capacitive load in each output of Ph1 and Ph2.

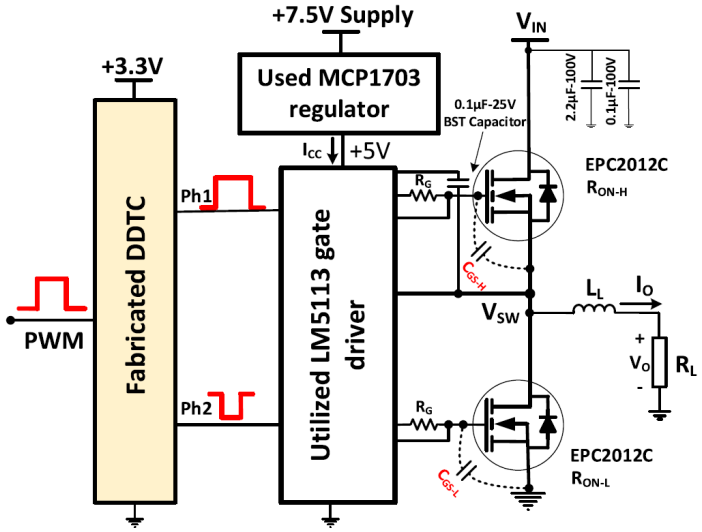


Figure 3.12: Block diagram of the test half-bridge circuit with the fabricated DTCC.

contains the required bootstrap (BST) diode. The commercial regulator MCP1703 supplies the gate driver with $5V$ (Figure 3.12). For the output stage of the half-bridge circuit, we utilize two eGaN HEMTs from EPC (EPC2012C), two freewheeling diodes (SDM03U40-7) placed in parallel with each power switch to reduce spikes in the inductive load, and a BST capacitor (C1005X5R1E104K050BC). The BST capacitor provides the gate charge for the HSPS, dc bias power for the half-bridge under-voltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The minimum on-time of low-side transistor affects the value of the bootstrap capacitor; a value of over $0.1\mu F$ is deemed satisfactory. Any power supply noise is removed by connecting two bypass capacitors in parallel between the input voltage V_{IN} and GND [34; 103].

The basic operations of the half-bridge circuit with inconvenient and convenient dead-time

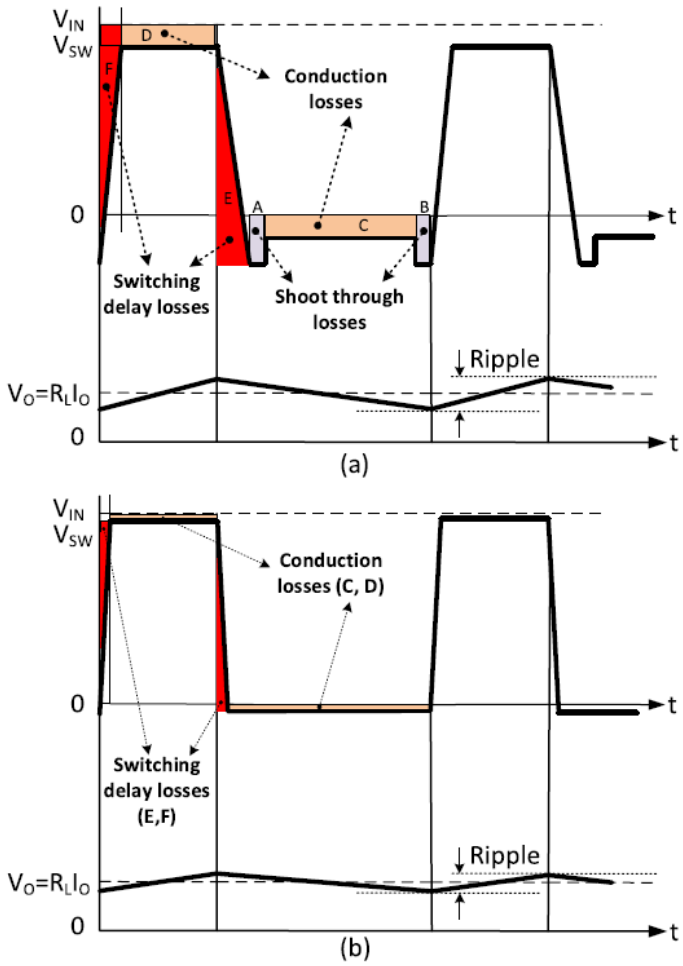


Figure 3.13: Relevant waveforms of half-bridge circuit (a) with inconvenient amount of dead-time, showing the dead-time dependent losses of A, B, C, D, E, and F; and (b) with a convenient amount of dead-time, showing a significant dead-time dependent loss reduction.

are respectively shown in Figures 3.13.a and 3.13.b. Regardless of the operation, three critical power losses heat up the power switches and substantially affect the safety of the power converter. These power losses depend on the overlap between the activation of the power switches. Hence, they can be minimized using a convenient DTCC. The dead-time dependent power losses (DDPLs) include conduction loss, switching delay loss, and shoot-through loss. These DDPLs are illustrated in Figure 3.13.a with different colors and names (A, B, C, D, E, and F) [104; 105; 106]. Given a convenient amount of dead-time, losses A and B in the half-bridge circuit are totally eliminated, and the volumes of C–F are greatly minimized (Figure 3.13.b).

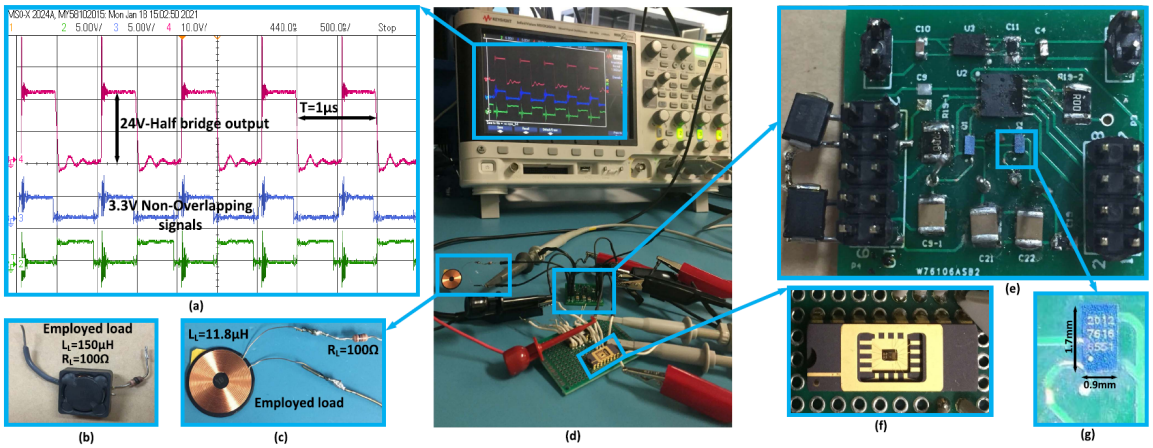


Figure 3.14: Experimental setup of the half-bridge circuit. (a) Measured signals. (b) R_L load with $R = 100\Omega$ and $L = 150\mu H$ load. (c) R_L load with $R = 100\Omega$ and $L = 11.8\mu H$ load. (d) Test bench. (e) Custom printed circuit board. (f) Packaged fabricated chip. (g) Power GaN transistor.

3.5.3 Power Loss Analysis

The total power losses in the designed power converter should be calculated on the basis of the measured parameters from the implemented converter [107; 108] to identify the effects of the proposed DTCC on the implemented half-bridge circuit.

The first DDPL is the conduction loss (Figure 3.13). The conduction loss of the HSPS (P_{ON-H}) depends on the switch's on-resistance (R_{ON-H}) and the amount of current delivered to the load during the operation. The same description applies to the LSPS, that is, P_{ON-L} depends on R_{ON-L}. The second DDPL is the switching loss. The switching loss is due to the rise and fall times of the switching voltage VSW (Figure 3.13). The switching loss of the HSPS (P_{SW-H}) depends on the operating frequency of the power converter. It also relies on V_{IN} and I_O [34]. The third DDPL is the body diode loss (P_D), particularly in the Si or SiC MOSFETs. It is mainly caused by the reverse recovery of the inductor current (L_L current) by the body diode of the LSPS. P_D depends on the operating frequency of the converter and the forward voltage (V_D) of the LSPS' body diode [48]. For a half-bridge circuit, the gate charge loss (P_G) results from the gate charging of the power switches, and the gate driver loss is caused by gate charging (P_{GD}). The loss of the fabricated DTCC (P_{DTCC}) must be added to the attained DDPLs, P_G, and P_{GD} losses to achieve the total power loss of the implemented half-bridge circuit [109; 110; 111; 90; 112].

The experimental setup for characterizing the implemented half-bridge circuit with the DTCC prototype is presented in Figure 3.14. The required dead-time for a power converter depends on the values of the load and V_{IN}. In this work, we measure the performance of the half-bridge circuit with the fabricated DTCC under two conditions. In the first condition, the

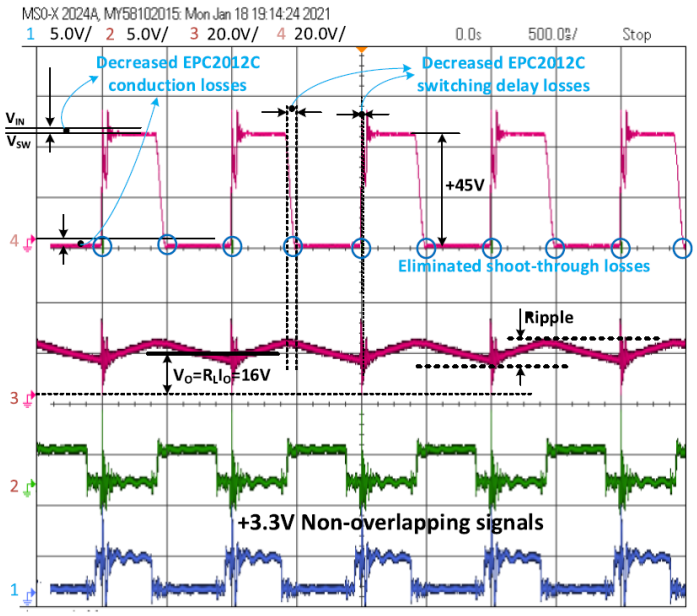


Figure 3.15: Measured waveforms of the test half-bridge circuit with the fabricated DTCC circuit.

input voltage (V_{IN}) is $24V$, and the half-bridge circuit is configured to drive a 100Ω resistor in series with a $11.8\mu H$ inductor. In the second condition, V_{IN} is $45V$, and the load is a 100Ω resistor in series with a $150\mu H$ inductor. Figure 3.14.a shows a screenshot of the circuit in the first condition ($V_IN = 24V$, $R_L = 100\Omega$, $L_L = 11.8\mu H$) taken by an oscilloscope. Meanwhile, Figures 3.14.b and 3.14.c present the output loads in the experimental setup for the two conditions. Figure 3.14.d illustrates the measurement setup. Figure 3.14.e shows the test's printed circuit board, including the half-bridge circuit. The size of the custom printed circuit board (PCB) used to characterize the half-bridge is $2.54cm \times 3cm$ and the size of the power switches are $1.7mm \times 0.9mm$. Figures 3.14.f and 3.14.g respectively demonstrate the fabricated wire-bonded chip (DTCC) and one tiny power switch.

Figure 3.15 plots the measured waveforms of the half-bridge circuit with the DTCC under the second condition. As shown in Figures 3.14.a and 3.15, the DDPLs decrease significantly. The switching loss of the power switches is associated with the rise and fall times (t_r, t_f) of the V_{SW} (Figure 3.13). The same is illustrated in Figure 3.15. In the ON-state, the conduction loss of the power switches varies with the differences between the high levels of V_{IN} and V_{SW}. In the OFF-state, the conduction loss depends on the differences between the zero and low levels of V_{SW} (Figure 3.13.a). As for the shoot-through loss, it is attributed to the A and B parts of the V_{SW} waveform (Figure 3.13.a). These parts are eliminated in the presented experimental results in Figure 3.15.

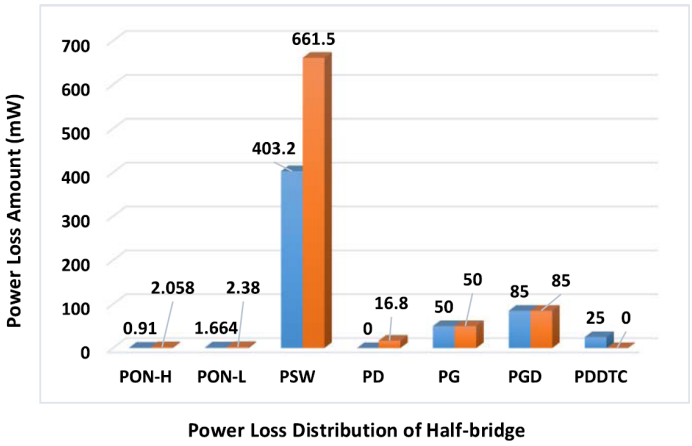


Figure 3.16: Histogram of the calculated power losses of the test half-bridge circuit with and without the fabricated DTCC.

3.5.4 Calculation of Power Losses

Figure 3.16 shows the histogram of the losses of the half-bridge circuit with and without the DTCC prototype. The blue and orange colors in the figure respectively represent the calculated losses of the half-bridge circuit with and without the fabricated DTCC. The power losses associated with the DDPLs of the half-bridge circuit with and without the DTCC prototype are 403.774 and 682.738mW, respectively. This result implies a 40% improvement with the use of the proposed DTCC. The half-bridge circuit with the fabricated DTCC consumes 563.774mW of total power; without the DTCC prototype, it consumes 834.538mW. This result implies a 32% improvement in total power consumption when the proposed DTCC is utilized.

The maximum operating temperatures of the sensitive devices with and without the proposed DTCC are calculated. The results highlight the significance of the improvement of the power losses in the operation of the components of the half-bridge circuit. Figure 3.16 shows that the highest power loss corresponds to the switching loss of the HSPS (P_{SW}). The total power losses of the HSPS (i.e., $P_{ON-H} + P_{SW}$) with and without the proposed DTCC are 663.558 and 404.11mW, respectively. According to the equations in [109; 110; 111; 90; 112] and the specifications of EPC2012C, the calculated operating temperatures of the HSPS with 3.4 and without 3.5 the DTCC are

$$T_{Ja} = 404.11mW \times 85°C/W + 85°C = 119.3°C \tag{3.4}$$

$$T_{Jb} = 663.558mW \times 85°C/W + 85°C = 141.4°C \tag{3.5}$$

The calculated T_{Ja} and T_{Jb} remain below the absolute maximum rating of $T_J = 150°C$ of EPC2012C. Nonetheless, the $22.1°C$ improvement in the maximum temperature greatly enhances the safety of the half-bridge circuit. Table 3.2 presents the measured performance of

Table 3.2: Performance comparison with previous works.

	[4]	[107]	[110]	[111]	This work
Results	Measured	Measured	Measured	Measured	Measured
Tech(.nm)	180	65	350	350	350
$f_p(MHz)$	10	10	10	0.1	1
$t_d(ns)$	0.125	1	Analog	200	35 and 62
$I_O(mA)$	200	120	600	500	210
$V_{IN}(V)$	12	5	3.6	250	45
$\Delta P_{loss}(\%)$	30.5	-	-	-	32
Efficiency	81.2%	76.4%	-	77%@20W	82%

the half-bridge circuit with the proposed DTCC. The switching frequency (f_p), dead-time delay (t_d), output current (I_O), input voltage (V_{IN}), technology (Tech.), total loss improvement (ΔP_{loss}), and efficiency are compared with the reported measurement (Measured) results of other solutions. The proposed DTCC circuit obviously provides the low and high sides of the half-bridge circuit with independent dead-time delays of 35 and 62ns, respectively. These dead-times are robust and able to reduce the dependent losses of the half-bridge circuit by 40%. They also enhance the total power consumption by 32%. Meanwhile, the losses greatly decrease the maximum operating temperature of the half-bridge circuit. With the application of the proposed DTCC, the maximum operating temperature is considerably improved, thereby boosting the safety of the half-bridge circuit. A convenient dead-time can decrease the values of t_r, t_f, and the average delivered current. However, the values of V_{IN} and the operating frequency are fixed. That is why the amount of improvement of switching loss is limited.

3.6 Conclusion

This study puts forward a circuit for generating dead-time delays to realize the proper non-overlapping operation of power converters. In traditional dead-time circuits, logic gates and inverters are used to create delays. Such scheme is prone to variations and limitations. By contrast, the proposed DTCC uses timing elements that integrate precise capacitors and current sources. The proposed DTCC can produce relatively long and independent time delays for HSPS and LSPS. The generated delays between the non-overlapping control signals meet the general requirements of half-bridge power converters. The proposed DTCC occupies a silicon area of $70\mu m \times 180\mu m$. It is validated using a test half-bridge circuit supplied at $45V$ and $1MHz$. The half-bridge circuit is implemented with discrete off-the-shelf components. The effects of the proposed DTCC on the losses of the test converter are evaluated herein. The results show that the proposed DTCC improves the dead-time dependent converter losses by 40%. The measured performance of the presented DTCC is also compared with that of

previous solutions.

Chapter 4

A Reconfigurable Single-supply Multiple-level Down-shifter for System-on-Chip Applications

4.1 Résumé

Un nouveau décaleur abaisseur de niveau destiné à la conversion de signaux d'amplitudes différentes dans des applications de système sur puce (SoC) est présenté. Cette nouvelle architecture de décaleur abaisseur à alimentation unique, mise en œuvre dans une technologie CMOS AMS de $0.35\mu m$, fournit plusieurs niveaux reconfigurables. Une structure de circuit connectée par diode, une source de courant, cinq portes de transmission, une combinaison diode-supercondensateur et des tampons d'entrée/sortie sont utilisés pour mettre en œuvre ce décaleur de niveau reconfigurable. Le circuit reçoit un signal en forme d'impulsion avec une amplitude de $3.3V$, et fournit trois signaux différents avec des amplitudes nominales de $1.2V$, $1.8V$ et $2.5V$ selon la configuration du circuit. Le circuit proposé pilote avec succès une gamme de charges capacitives entre $10fF$ et $350pF$. Le circuit présenté consomme une puissance statique et dynamique de $62.37pW$ et $108.9\mu W$, respectivement à partir d'une alimentation de $3.3V$, à une fréquence de fonctionnement de $1MHz$ et une charge capacitive de $10pF$. Les résultats de la simulation post-layout montrent que les délais de propagation de chute et de montée des trois configurations sont respectivement de l'ordre de $0.54ns$-$26{,}5ns$ et de $11.2ns - 117{,}2ns$. Il occupe une surface de $80\mu m \times 100\mu m$.

4.2 Abstract

A novel level down shifter intended for translation of signals with different amplitudes in System-on-Chip (SoC) applications is presented. This new single supply down-shifter architecture, implemented in a $0.35\mu m$ AMS CMOS technology provides multiple reconfigurable

levels. A diode connected circuit structure, a current source, five transmission gates, a diodesupercapacitor combination, and input/output buffers are employed to implement this reconfigurable level shifter. The circuit receives a pulse shaped signal with an amplitude of $3.3V$, and provides three different signals with nominal amplitudes of $1.2V$, $1.8V$, and $2.5V$ depends on the circuit configuration. The proposed circuit successfully drives a range of capacitive loads between $10fF$ and $350pF$. The presented circuit consumes a static and a dynamic power consumptions of $62.37pW$ and $108.9\mu W$, respectively from a $3.3V$ supply, at an operating frequency of $1MHz$ and a capacitive load of $10pF$. Post-layout simulation results show that the fall and rise propagation delays of the three configurations are in the range of $0.54ns$-$26.5ns$ and $11.2ns$-$117.2ns$, respectively. It occupies an area of $80\mu m \times 100\mu m$.

4.3 Introduction

Level shifters, whether up or down, are key building blocks in integrated electronic systems, including System-on-Chip (SoC), and System-in-Package (SiP) applications [63; 113; 34; 114; 115; 17]. Figure 4.1.a shows an example of a SoC module including various building blocks integrated inside a single chip [116; 117; 118]. SiP systems are very dense devices combining separate chips implemented in different process and packaged together using a two-dimensional (2-D) or three-dimensional (3-D) substrate, as depicted in Figure 4.1.b. Dense integrated systems regrouping many building blocks like SoC and SiP require different voltage supply levels. For example, CPU can operate between $0.9V$ to $1.2V$, while USB interfaces may require up to $+5V$ for proper operation [119; 120]. Moreover, analog I/Os with higher voltages ($1.8V$, $2.5V$, and $3.3V$) are inevitable to allow proper interface between many different chips [121]. Thus, level shifters are essential circuits in both SoCs and SiPs to allow signal compatibility between all building blocks [32; 122; 60; 123].

Both level down and level up-shifter are important. A level down-shifter (LDS) receives a signal from a circuit operating at a higher supply voltage, and converts it to drive a circuit operating at a lower supply voltage [124]. A simple method for down converting the level of a signal is using a resistive voltage divider circuit. However, this technique is very slow ($< 1MHz$), and consumes a considerable amount of power. Level-down shifting can also be achieved using a single MOSFET with the drain connected to the high-voltage side and the source connected to the low-voltage side, while the gate is activated, and the source is pulled up by a resistor. This method is also power hungry and is limited to a few MHz [64].

Designing a high-performance level down-shifter with low power consumption and short propagation delay is challenging. Many SoCs include power transistors using thick oxide layers, generating large parasitic capacitances [125; 126; 127]. The level shifters employed in these systems must drive large capacitive loads [9]. In [124], a high-performance level shifter in which the energy consumption is decreased by a bootstrap input stage is presented to improve the

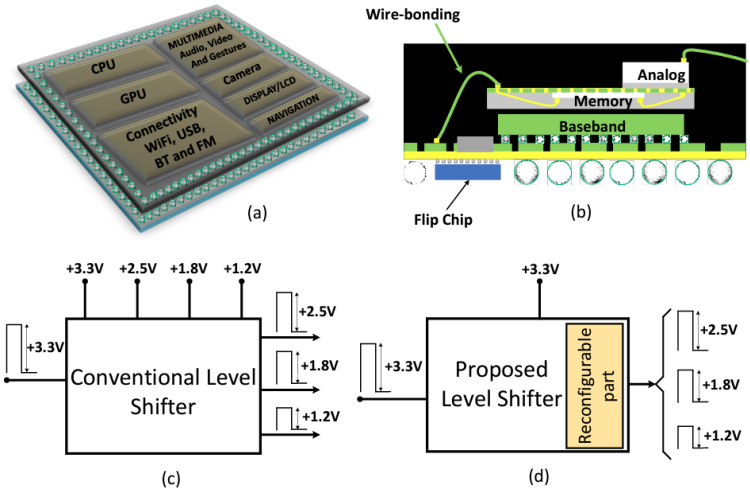


Figure 4.1: Conceptual diagrams for: (a) SoC module, (b) SiP module cross section, (c) The conventional LDS, and (d) The proposed LDS.

fan-in load. This level down converting structure can drive a capacitive load between $0.1pF$ and $1pF$. A dual supply level down shifter driving a $2-pF$ capacitive load was presented in [113]. This topology reduces the active area and the resulting energy-delay, but it is not optimized in the aspect of the power consumption. Besides, it is not a single supply structure.

It is worth noting that conventional LDS circuits need the whole lower supply voltage when down shifting a higher voltage signal to multiple lower signals [128; 129; 130]. Such a configuration is illustrated in Figure 4.1.c. An example of a $3.3-V$ module communicating with other modules at $1.2V$, $1.8V$, and $2.5V$ and the three required voltage supplies is shown. Therefore, the number output connections of such a multiple voltages SoCs increases, which increases the power consumption [122]. Designing a high-performance single-supply LDS to drive large capacitive loads is a challenging task.

In this paper, we present a reconfigurable structure of a novel LDS that uses a single supply voltage of $3.3V$ to down shifting a $3.3V$ signal to one of the three levels; $2.5V$, $1.8V$, and $1.2V$ as shown in Figure 4.1.d. The main idea of this work comes from combination of a diode-connected feature and a current source. The diode connected part is controlled dynamically by the input signal that has the higher amplitude. The connection point of diode-connected circuit and the current source provide the output signal with the lowest amplitude. The rest of this paper is organised as follows. In Section 4.4, the main concept and the beneficial advantages of proposed LDS are discussed. Section 4.5 presents the implementation of the LSD's building circuits. The post-layout simulation results are presented and discussed in section 4.6, and the conclusion is given in section 4.7.

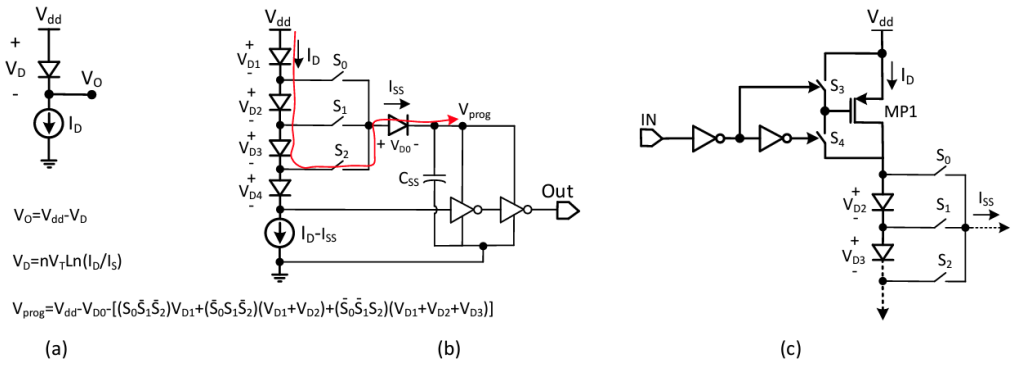


Figure 4.2: The proposed RSS-LDS: (a) Main concept, (b) General explanation of system reconfigurability scheme, and (c) Realization of the controller circuit.

4.4 Proposed Reconfigurable Level Down Shifter

The proposed LDS circuit is based on the particular operation of a diode, the anode of which is connected to the supply (V_{dd}) and the cathode of which is sunk by a current source. As shown in Figure 4.2.a, the amount of dropped voltage across the diode (V_D) depends on the amount of sunk current from its cathode (I_D). In Figure 4.2, we have $V_O = V_{dd} - V_D$. The proposed LDS is leading to a reconfigurable single supply level down shifter (RSS-LDS). Figure 4.2.b illustrates the reconfigurable scheme ($S_0S_1S_2$), and how a single supply is used to multiple voltages ($V_{D1}, V_{D2}, ...$) and V_{prog} to the output buffers. An offchip supercapacitor (C_{SS}) is charged by an on-chip diode to deliver the I_{SS} to provide the floating supply V_{prog} to the output buffer (Figure 4.2.b). The voltage value provided at node V_{prog} by this bootstrap mechanism involving I_{SS} and C_{SS} can be change. Consequently, the amplitude of the output signal can be selected. To provide reconfigurability, three switches S_0, S_1, and S_2 are employed to change the number of diode voltages contributing to node V_{prog}. The following equation describes the resulting voltage at V_{prog}.

$$V_{prog} = V_{dd} - V_{D0} - [(S_0\bar{S}_1\bar{S}_2)V_{D1} + (\bar{S}_0S_1\bar{S}_2)(V_{D1}+V_{D2}) + (\bar{S}_0\bar{S}_1S_2)(V_{D1}+V_{D2}+V_{D3})] \quad (4.1)$$

The direction of current flowing between V_{dd} to V_{prog} is shown by a red arrow when the S2 is closed ($\bar{S}_0\bar{S}_1S_2 = 1$). In this configuration, there are three diodes (V_{D1}, V_{D2}, V_{D3}), in addition to the main diode (V_{D0}), in the path for delivering I_{SS}. As a result, the V_{prog} node provides the lowest supply voltage to the output buffer, providing a low-voltage pulse at the output. Figure 4.2.c shows how the diode connected architecture is controlled dynamically by the input signal with the highest voltage. For this purpose, MP1 is controlled by two switches (S_3, S_4) and has two operating modes (diode-connected mode and sleep mode). The activation signals of S_3 and S_4 comes from the outputs of two series inverters. Since the input pulse is

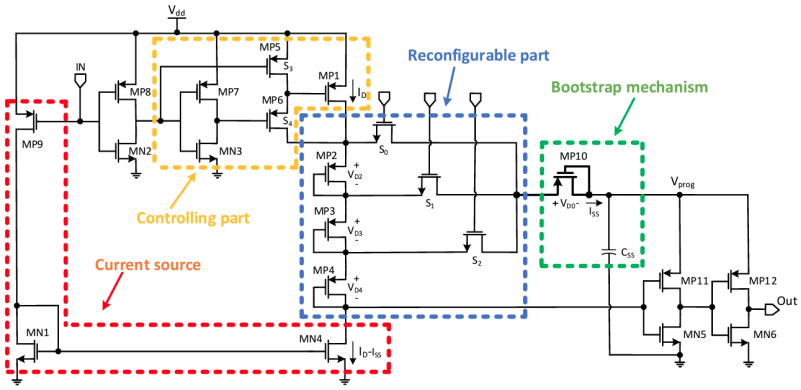


Figure 4.3: Circuit diagram of the proposed RSS-LDS.

connected to the first inverter, each switch is activated by one of the levels of the input pulse, respectively. When S_4 is closed, MP1 works in the diode-connected mode and delivers current to the circuit. In the opposite mode, when S_3 is closed, MP1 is turned off and the system is put in sleep mode.

The essential benefits attained by the proposed RSS-LDS are:

- Contrary to the traditional LDS, the proposed RSS-LDS needs only one voltage supply (V_{dd}) while it can generate an output signal of three different amplitudes. For communicating with the other building blocks of a multiple voltages SoC, the proposed RSS-LDS does not require three separated DC-DC convertors and regulators. Thus, a sheer amount of power and area can be saved in the multiple voltage SoCs using the presented RSS-LDS.

- Compared with the conventional LDS, the proposed RSS-LDS employs diode-connected structure and a current source for realizing the presented concept. Therefore, depending on the number of superimposed diode-connected structure and the selected point between the diodes, the value of floating V_{prog} node can be adjusted. This provides a reconfigurable scheme to provide different voltage levels at the output.

- Finally, the proposed RSS-LDS, due to the utilization of the diode-connected and the bootstrap mechanisms, can drive large capacitive loads, which is an important requirement of an SoC in which high-voltage and low-voltage modules communicating with each other are combined in the same chip.

4.5 Circuit Implementation

Figure 4.3 shows the transistor level implementation of the proposed RSS-LDS circuit. It is composed of different subblocks including input inverters, controlling circuits to provide a

Table 4.1: Components specifications of the proposed RSS-LDS.

Controlling part	Components	MP1	MP5	MP6	MP7,MN3
	W(μm)	75	15	15	5
	L(μm)	0.45	0.35	0.35	0.35
Current source	Components	MP9	MN1	MN4	
	W(μm)	75	15	15	
	L(μm)	0.45	0.35	0.35	
Reconfigurable part	Components	MP2	MP3	MP4	$S_0S_1S_2$
	W(μm)	28	20	0.5	45
	L(μm)	0.35	0.35	0.5	0.35
Bootstrap mechanism	Components	MP10	Cap.	C_{SS}	
	W(μm)	45	Value	$2.2\mu F$	
	L(μm)	0.35			
Input inverter/ Output buffer	Components	MP8, MN2	MP8, MN2	MP6	MN12
	W(μm)	1	5	10	10
	L(μm)	0.35	0.35	0.35	0.35

bimodal operation for MP1, reconfigurable part, current source, bootstrap mechanism, and output buffer. The supply voltage of the proposed RSS-LDS is $V_{dd} = 3.3V$. It receives a input pulse signal of an amplitude of 3.3V and can generate three output signal levels of nominal amplitudes of $1.2V$, $1.8V$, and $2.5V$, depending on the states of the controlling switches. The presented circuit is using a floating voltage node at V_{prog}, which allows the circuit to be reconfigurable, thanks to a bootstrap mechanism.

Since V_{prog} is supplying the output buffer, the voltage value at node Vprog must be lower than the gate voltage of MP11, when the input signal level is high. Indeed, in this state, the requirement of $V_{SG} \leq V_{TH}$ of MP11 must be met to avoid MP11 from being turned on. This requirement can be difficult to meet when the circuit is configured to generate a pulse of $1.2V$ because the V_{SG} of MP11 is equals $V_{D4} - V_{D0}$, and must be lower than the V_{TH} of MP11, when the input signal is high. To achieve this essential requirement, the width of MP10 must be made a few times larger than the width of MP4.

In addition, in all settings, the circuit must be able to deliver enough driving current from V_{dd} to V_{prog} to drive a considerable load value with the output buffer. Therefore, the width of S_0, S_1, S_2, and MP10 must be made large enough to meet this requirement. It should be noted that the width of MP2, MP3, and MP4 must be made a few times smaller than the width of the switches and MP10 to meet this requirement and allow proper operation of MP11 in the worst case scenario. Table 4.1 shows the aspect ratios of the utilized transistors and the capacitance value of the off-chip capacitor used to implement the RSS-LDS.

In this circuit, when the input signal is low, MP5 is turned off. In the same condition, MP6 is turned on to put MP1 in a diode-connected transistor configuration, so it can deliver the current I_D to the lower side diode-connected transistors (MP2-MP4). Similarly, MP9 is turned

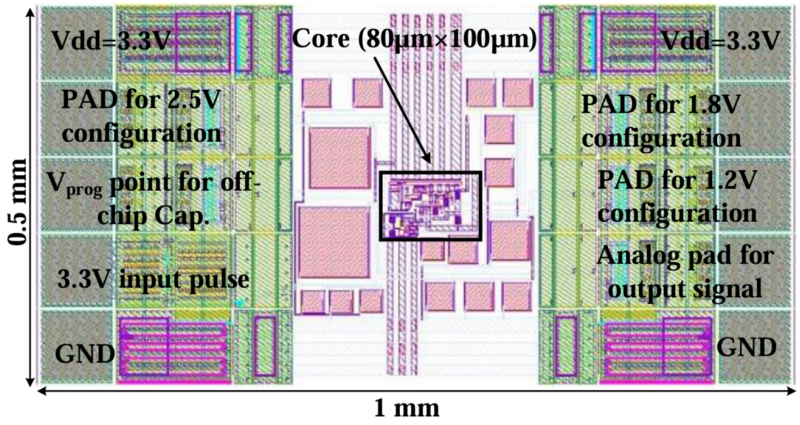


Figure 4.4: Layout view of the proposed RSS-LDS implemented in 0.35 µm CMOS process.

on to allow the current source mirroring the current of MN1 to the diode-connected transistors. In this case, assuming the circuit is configured to generate a pulse level of $1.8V$ at the output (S_1 is closed), the current of I_{SS} (the difference of I_D and the current of MN1) pass from S_1 and MP10 to charge the C_{SS} and create the needed voltage at node V_{prog} to supply the output buffer. In contrast, when the input is high, MP5 is turned on to force MP1 to be shut down. MP9 dictates the shutdown of the current source.

4.6 Post-Layout Simulation Results

The proposed RSS-LDS circuit was designed and implemented in a standard $0.35\mu m$ AMS CMOS technology. It occupies only $80\mu m \times 100\mu m$ of silicon area as shown in Figure 4.4. Figure 4.5 shows the post-layout simulation of the presented RSSLDS when it is configured to provide a pulse level of $2.5V$. The top part of this figure shows the results for a $1-MHz$ input frequency at $3.3V$, and a $10-pF$ capacitive load. In these conditions, the falling and the rising edge propagation delays are $0.8ns$ and $40.2ns$, respectively. The bottom part of Figure 4.5 presents the performance of the circuit with a $350-pF$ capacitive load. The rise time becomes long at such big loads. However, the output signal could reach $2.5V$. In this case, an output buffer should be utilized to regenerate the output pulse. It should be noted that the rising edge propagation delay (r_{pd}) happens when the signal goes above the V_{TH} of n-type MOSFET of inverter. Similarly, the falling edge propagation delay (f_{pd}) happens when the V_{SG} of p-type MOSFET of inverter pass the condition of $V_{SG} \geq V_{TH}$.

Table 4.2 presents the post-layout simulation results of the presented RSS-LDS at a $3.3-V$ supply voltage and an operating frequency of $1MHz$ for three output level ($1.2V$, $1.8V$, and $2.5V$). The important parameters of this design are the static power consumption (P_S) and the dynamic power consumption (P_{dyn}), which is equal to $C_L f_p (V_{dd})^2$, the rising edge propagation delay (r_{pd}), and the falling edge propagation delay (f_{pd}). The performance of the circuit is

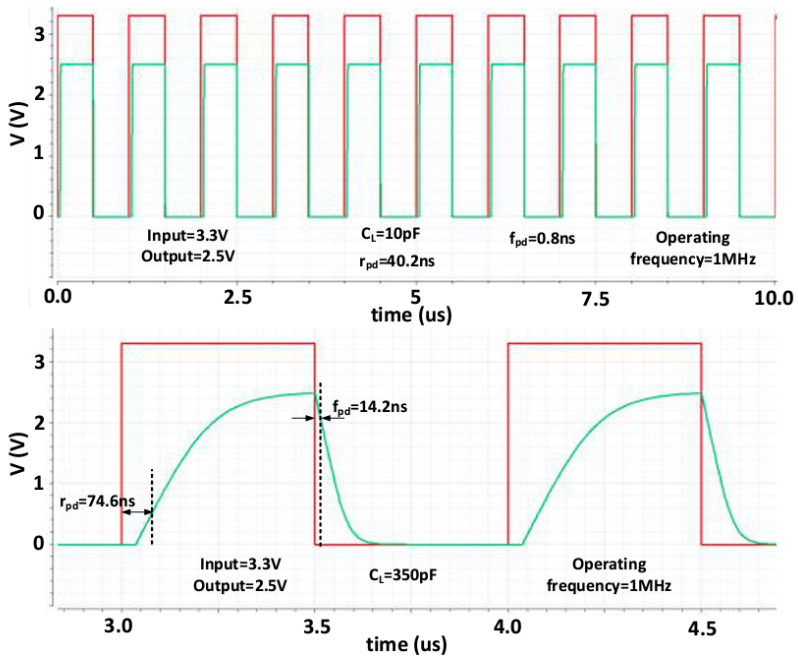


Figure 4.5: Resulting performance of the RSS-LDS at the three configurations at $V_{dd} = 3.3V$ and operating frequency $= 1MHz$.

Table 4.2: Internal capacitances for a power MOSFET.

Output Level	$1.2V$	$1.8V$	$2.5V$
C_L	$10fF - 100pF$	$10fF - 150pF$	$10fF - 350pF$
P_S	$58.87pW$	$60.78pW$	$62.37pW$
P_{dyn}	$108.9nW - 1.08mW$	$108.9nW - 2.72mW$	$108.9nW - 3.81mW$
r_{pd}	$11.2ns - 117.2ns$	$24.2ns - 78.8ns$	$37.5ns - 74.6ns$
f_{pd}	$1.7ns - 26.5ns$	$0.7ns - 19.8ns$	$0.54ns - 14.2ns$

evaluated across the frequency of the input signal. For $1.2V, 1.8V$, and $2.5V$ output levels, reasonable output signals are achieved to up to $100MHz$ for a $10 - pF$ capacitive load.

The performance comparison of the RSS-LDS with the recently published circuits when configured to generate a $2.5V$ pulse level is presented in Table III. A Figure-of-Merit (FoM) is defined to provide a fair comparison. The used FoM is the result of the multiplication of C_L, f_P, NC (Number of Configuration), V_{dd}, and square of process divided by the multiplication of the total power (P_{total}), the total delay (D_{total}), and the NS (Number of Supply):

$$FoM = \frac{C_L \times f_P \times NC \times V_{dd} \times (\text{Procsess})^2}{P_{\text{total}} \times D_{\text{total}} \times N_S} \tag{4.2}$$

As shown in the defined FoM, the inconvenient circuit parameters are put in the denominator of equation. Therefore, the circuit with higher power consumption, longer propagation delay,

Table 4.3: Performance comparison of the proposed RSS-LDS configured to generated $2.5V$.

References	[131]	[113]	[124]	[125]	This work
V_{dd}	1.8	1.2	1.2	1.8	3.3
Tech. (nm)	180	65	65	180	350
Typ.	Up	Down	Down	Up	Down
$f_P(MHz)$	1	500	500	1	1
$C_L(pF)$	0.023	0.45	1	0.043	10
$P_S(W)$	$92p$	$0.65m$	$1.28m$	$0.99n$	$62.37p$
$P_{dyn}(W)$	$76.24n$	324μ	720μ	$470n$	108.9μ
$r_{pd}(ns)$	6.1	0.4	0.25	1.4	40
$f_{pd}(ns)$	6.1	0.8	0.5	1.4	0.8
NS	2	2	1	2	1
NC	1	1	1	1	3
FoM($\times 10^{-6}$)	0.73	0.48	1.66	0.94	2.72

and more NS, could achieve smaller score. On the other hand, according to the parameter of nominator of the defined equation, the circuits with more NC, where could drive bigger capacitive loads, while is working in higher frequency at a specific supply and process, would attain larger score. So, the best FoM is the largest one. As it is shown in the Table III, the presented RSS-LDS achieves larger FoM compared to the prior works. This ensures the better performance of the presented design.

4.7 Conclusion

This paper proposes a new level down shifter to be an convenient interface between high-voltage and low-voltage parts in SoC applications. The presented Reconfigurable Single Supply Level Down Shifter (RSS-LDS) employs diode-connected structures, current sources, and bootstrap technique to realize the idea. The privilege of the proposed methodology is being single supply, reconfigurable, and capable of driving large capacitive loads. The defined FoM involved eight parameters of proposed RSS-LDS to implement a fair comparison where achieved the best score. To prove the concept, the results of post-layout simulation are presented in the tables and figures.

Chapter 5

A 9.2-ns to 1-us Digitally Controlled Multi-Tuned Deadtime Optimization for Efficient GaN HEMT Power Converters

5.1 Résumé

Cet article présente un nouveau circuit de contrôle du temps mort ajustable fournissant un délai optimal pour l'optimisation des convertisseurs de puissance. Notre méthode peut réduire les pertes liées au temps mort tout en améliorant l'efficacité et la densité de puissance d'un convertisseur de puissance donné. Le circuit présente un élément de retard reconfigurable pour générer une large gamme de temps mort pour différentes applications de conversion de puissance avec des charges et des tensions d'entrée variables. L'équation du temps mort optimal pour les convertisseurs buck est dérivée, et sa dépendance à la tension d'entrée et à la charge est discutée. Les résultats expérimentaux montrent que le circuit présenté peut fournir une large gamme de délais de temps mort, allant de $9.2ns$ à $1000ns$. La consommation d'énergie du circuit présenté est mesurée pour différentes charges capacitives C_L et fréquences de fonctionnement f_s. Le circuit a consommé une puissance comprise entre $610\mu W$ et $850\mu W$ sur les plages de temps mort mesurées alors que $C_L = 12pF$, $V_{dd} = 3.3V$, et $f_s = 200kHz$. Le générateur de temps mort proposé peut fonctionner jusqu'à $18MHz$ lorsque le temps mort minimum de $9.2ns$ est sélectionné. Le circuit présenté occupe une surface de $150\mu m \times 260\mu m$. La puce fabriquée est connectée à un convertisseur buck pour valider le fonctionnement du circuit proposé. Le rendement d'un convertisseur buck typique avec un T_{DLH} minimum et un T_{DHL} optimal à $I_{Load} = 25mA$ est amélioré de 12% par rapport à un convertisseur avec un temps mort fixe de $T_{DLH} = T_{DHL} = 12ns$.

5.2 Abstract

This paper presents a tunable new deadtime control circuit providing an optimal delay for power converter optimization. Our method can reduce the deadtime loss while improving the efficiency and power density of a given power converter. The circuit presents a reconfigurable delay element to generate a wide range of deadtime for different power conversion applications with varying loads and input voltages. The optimal deadtime equation for buck converters is derived, and its dependency on the input voltage and load is discussed. Experimental results show that the presented circuit can provide a wide range of deadtime delays, ranging from $9.2ns$ to $1000ns$. The power consumption of the presented circuit is measured for different capacitive loads (C_L) and operating frequencies (fs). The circuit consumed a power between $610\mu W$ and $850\mu W$ across the measured deadtime ranges while $C_L = 12pF$, $V_{dd} = 3.3V$, and $f_s = 200kHz$. The proposed deadtime generator can operate up to $18MHz$ when the minimum deadtime of $9.2ns$ is selected. The presented circuit occupies an area of $150\mu m \times 260\mu m$. The fabricated chip is connected to a buck converter to validate the operation of the proposed circuit. The efficiency of a typical buck converter with minimum T_{DLH} and optimal T_{DHL} at $I_{Load} = 25mA$ is improved by 12% compared to a converter with a fixed deadtime of $T_{DLH} = T_{DHL} = 12ns$.

5.3 Introduction

Efficient power converters are essential circuits used in System-in-Packages (SiP) modules for distributing power to the different building blocks [132]. Many high-performance applications, such as video processing [133], are particularly power-hungry. Power converters are ubiquitous in industrial and consumer electronics. They are employed in so many applications, from smartphones, tablets, and headphones [16; 134], to TV sets, car electronics, wireless power chargers for electric vehicle [135; 17], public fitness equipment [136], and wearable medical devices [137]. Power converters, such as DC–DC converters, bridges (half and full), and class-D power amplifiers, must present high efficiency and power density [138; 139; 30; 140]. A thorough analysis of losses must be performed, so a power converter design can meet these key criteria [141; 142; 143]. Losses must be examined at the component and peripheral circuits levels to improve converter performance. Si MOS, SiC MOS, and GaN transistors are the most frequently used power switches in power converters [144; 145; 146; 147; 148]. A Figure of Merit (FoM) $= Q_{OSS}R_{ON}$ is recommended in [149] to the advantage of GaN's over Si or SiC (Q_{OSS} and R_{ON} are the output capacitor charge and the on-resistance of the power switch, respectively). Furthermore, the GaN transistor does not suffer from reverse recovery loss due to the absence of a body diode, has a lower gate charge, and a smaller output capacitance than with Si or SiC [150; 151]. The carrier mobility in the 2D electron gas (2DEG) channel is considerably faster in the GaN transistor, and the breakdown voltage is higher due to its large acute electric field [152; 153]. Hence, GaN transistors are excellent candidates for ultra-high-power density operation. Figure 5.1 shows the different types of losses found in power

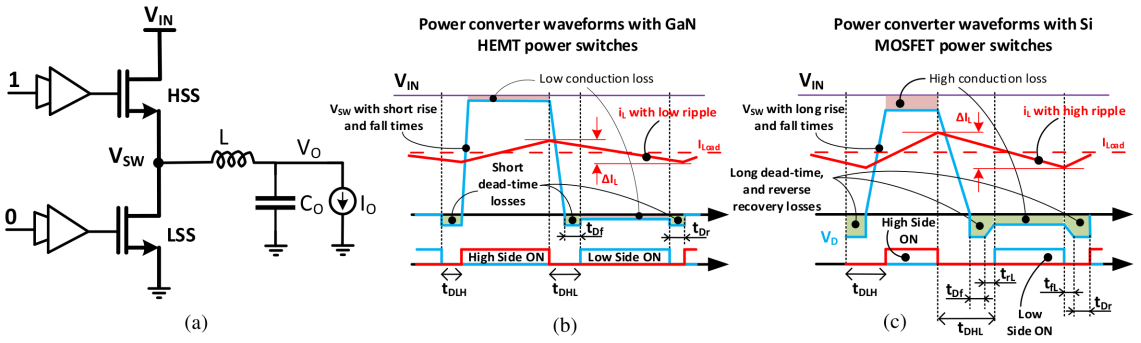


Figure 5.1: Conventional power converter (a) Simplified schematic, (b) Waveforms with GaN HEMT power switches, and (c) Waveforms with Si MOSFET power switches.

converters. Figure 5.1.a depicts a simplified schematic of a conventional power converter. Figure 5.1.b illustrates the power converter's essential waveforms needed for the case of GaN transistors. In contrast, Figure 5.1.c shows the needed power converter's waveforms when the power switches are implemented with Si MOSFETs.

The rise and fall times (t_r and t_f) of the main curve of the power converter (V_{SW}) are shorter when GaN transistors are used, as shown in Figures 5.1.b and 5.1.c. In the same condition, the switching time of the GaN transistors is six times faster than for Si MOSFET [152]. Accordingly, the switching losses P_{SW} of the GaN transistors are minimized because the overlap of I_{DS} and V_{DS} of the high-side power switch (HSS) is minimized when the t_r and t_f of V_{SW} are shorter [152]. Figures 5.1.b and 5.1.c show that the power converter using GaN transistors has a significantly lower conduction loss (P_{CON}). The P_{CON} equals the value of R_{ON} times the value of the RMS current of the power switches (see the Appendix for more details). GaN transistors achieve lower conduction loss because their R_{ON} is smaller than that of Si MOSFETs. Another type of loss in power converters is due to the reverse recovery charge Q_{RR} in the freewheeling of the low-side switch (LSS). This loss equals the multiplication of Q_{RR}, V_{IN}, and the operating frequency f_S of the converter (see the Appendix).

Moreover, this loss can be significant in power converters with Si MOSFETs. However, the loss is almost zero in GaN-based converters because the GaN is a majority carrier device, and it does not have reverse recovery-based loss. This point is clarified in Figures 5.1.b and 5.1.c for Si and GaN-based converters, respectively. Another factor that contributes to the switching loss is the stored energy in the output capacitance of the power switch, which is dissipated during the turn-on time. This loss (P_{CAP}) depends on the output charge of the power switch (Q_{OSS}) and equals the multiplication of Q_{OSS}, f_S, and V_{IN} (see the Appendix). GaN devices also have small output capacitances compared with Si MOSFETs. Accordingly, they exhibit a much smaller P_{CAP}. The LSS body diode in power converters can conduct during the deadtime, resulting in a power loss associated with the forward voltage of the

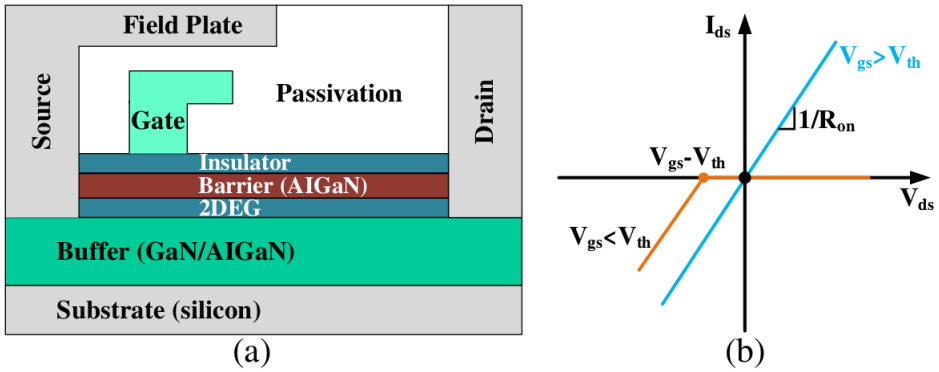


Figure 5.2: GaN transistor: (a) Cross section of the lateral structure (b) simplified behavior in 1^{st} and 3^{rd} quadrant.

diode. Although GaN devices have no body diode, their symmetry helps in conducting in the third quadrant with a diode-like behavior. The lateral GaN structure is comprised of a source and drain that are linked by a 2DEG channel, with the Gate controlling the conductivity of the 2DEG. 5.1.a and 5.1.b illustrate the cross-sectional view of the lateral structure of a GaN transistor and its behavior in the first and third quadrants, respectively. When the current flows in reverse conduction in GaN devices, the drain and source terminals can swap the termination. GaN transistors have a high third quadrant conduction (e.g., V_{SD} of $2V$ at $10A$ for LMG5200 compared to $\sim 1V$ for Si MOSFETs). Hence, GaN devices typically exhibit a higher power loss during deadtime P_{DT}. This power loss can be calculated as follows:

$$P_{DT} = f_S \times V_{SD} \times I_{out} \times (T_{DLH} + T_{DHL}) \tag{5.1}$$

where I_{OUT} is the output current of the power converter; and T_{DLH} and T_{DHL} are the required deadtimes, as shown in Figures 5.1.b and 5.1.c. Accordingly, an adjustable deadtime control circuit is necessary to select the optimal deadtime for different power converter applications to achieve maximum efficiency. When the optimum deadtime is tuned, the signal of V_{SW}(Figure 5.1.a) has sufficient time to reach zero, but does not cross it. Then, the buck converter can work at its maximum operating frequency and maximum efficiency. The other power converter losses to consider include those resulting from the gate driver P_G, output inductor DC resistance P_{DCR}, equivalent series resistance of the output capacitance P_{ESR}, and power switch packaging losses (see Appendix) [154; 155; 156; 157; 158].

The gate driver supply voltage V_{DC} is usually separated from the power switches supply V_{IN} inpower converter implementation where two n-channel bootstrapped power switches are usedas HSS and LSS(Figure 5.3.a). The VDC is fixed to $+5V$, while the V_{IN} is between $12V$ and $200V$ depending on the application. Accordingly, the same gate driver design would support different power converter applications. The amount of deadtime delay required to

activate the HSS and LSS switches, which depends on the value of V_{IN}, must be set to longer values because the operation of power switches is known to be slower at higher V_{IN}. A gate driver with a reconfigurable deadtime control circuit allows to finetune and find the optimal the required deadtime for various V_{IN}. This mechanism ensures a power converter design with a sound efficiency performance for a wide range of applications with different V_{IN} values [159; 160].

The needed power converter deadtime depends on the type of load (RLC, RL, and LC) and the values of the used off-chip passive components. The primary distinction among most converter types (DC–DC, Class-D power amplifiers, and bridges, including half and full) is the kind of load. Accordingly, adopting a single implementation of a gate driver with a tunable deadtime delay for the various power converter topologies has several benefits. Figure 5.3.a shows a power converter with variable input voltage (V_{IN}), variable load (Z_L), and reconfigurable deadtime control fulfilled with a gate driver [161; 162; 34; 101; 163; 90]. In this configuration, a field-programmable gate array (FPGA) sends the tuning commands to the deadtime control circuit. Figure 5.3.b shows the timing diagram of the gate driver with a PWM signal under no load condition where the switching specifications are illustrated, including the turn-off delay T_{PHL}, turn-on delay T_{PLH}, output rise time T_{OR}, output fall time T_{OF}, low-to-high transition deadtime T_{DLH}, and high-to-low transition deadtime T_{DHL}.

The deadtime control circuit is a key circuit in gate drivers that enables high-quality switching to drive the HSS and LSS power switches [164; 9]. Figure 5.3.a presents a general building block of a power converter that includes a gate driver associated with an integrated deadtime control circuit [165]. Although the gate driver implementation frequently has a fixed deadtime, a reconfigurable gate driver with the ability to adjust the deadtime delay is desirable to provide an optimal deadtime to reduce P_{DT}, thereby increasing the efficiency and power density [166; 32; 167; 168].

Several tunable deadtime control circuits were discussed in the literature. The use of a gate driver with adjustable deadtime delay used for tuning a half-bridge with a high supply voltage ($V_{IN} = +86V$) is discussed in [101]. This gate driver configuration generates a variable deadtime delay between $4.5ns$ and $58ns$ for a variable load with a current ranging from $200mA$ to $2A$. However, this deadtime circuit does not generate enough delays (i.e. longer delays are required) to support power converters with high V_{IN} and wider load range. A commercial gate driver integrated circuit with tunable deadtime delay is presented in [163]. It drives a half-bridge that can operate up to $V_{IN} = 200V$ and supply up to $3A$ to a load. However, the deadtime control involved in this gate driver uses two off-chip resistors to allow a tunable operation. This situation increases the power dissipation of the gate driver. Moreover, the reliability of the gate driver circuit can be affected, and the resolution of the deadtime delay can be degraded.

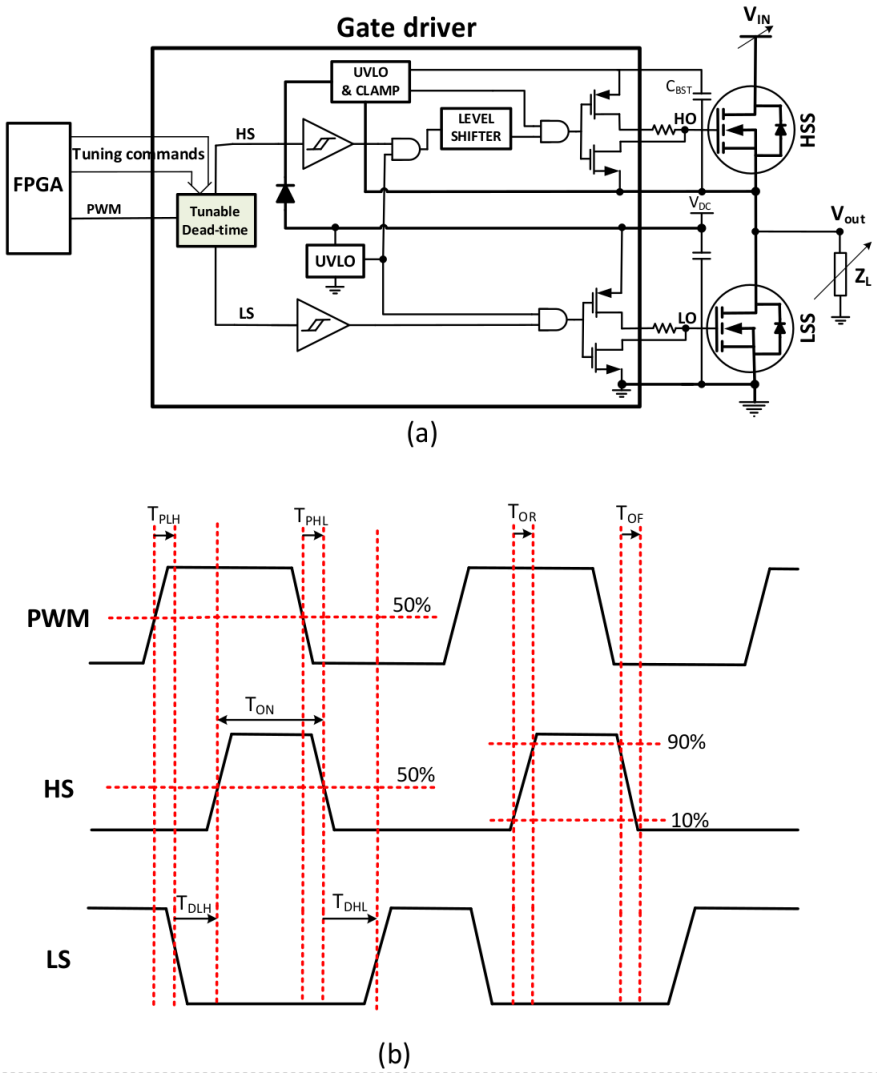


Figure 5.3: A power converter with a tunable dead-time generator, and (b) timing diagram of gate driver in PWM mode under no load condition.

A deadtime optimization method for GaN-based buck converters is described in [166]. In this paper, the optimization relies on mathematical analysis and the derived equations for both T_{DLH} and T_{DHL}. In [166], an efficiency improvement of up to 4.5% is achieved compared to using a fixed deadtime, but one drawback with the derived equations is a lack of accuracy. A digital deadtime correction wherein the deadtime can be tuned during a power converter operation is reported in [169]. In this technique, the deadtime circuit measures the voltages of V_{SW} and LSS gate and tunes the deadtime. An adaptive deadtime control methodology wherein a digital circuit was used to optimize the required deadtime through measuring the voltage of V_{SW} is presented in [67]. Comparator-based, dual-edge modulation deadtime optimization, and adaptive deadtime controller techniques, are presented in [66], [170], and [171], respectively. An issue with the deadtime control circuits presented in [168; 169; 67; 66; 170; 171]

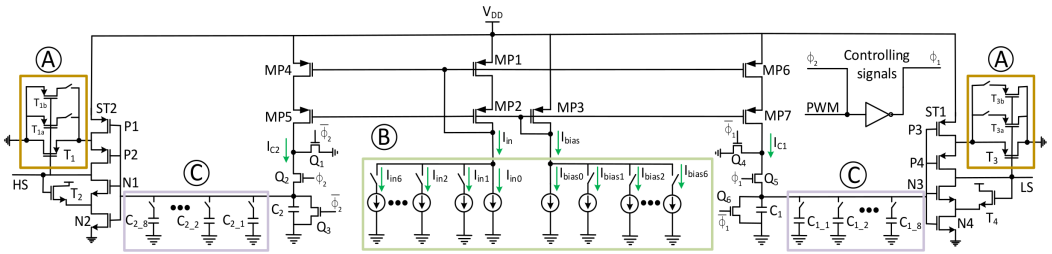


Figure 5.4: Schematic of the proposed Multi-Tuned-Dead-Time Generator. Three tunable parts of A, B, and C can receive tunning commands from the FPGA to reconfigure the circuit for creating different required delays between the generated non-overlapping signals on the outputs of HS and LS [9]. All the components of the proposed circuit will be integrated as a part of gate driver for different power converter applications.

is that the sensing voltage V_{SW} for estimating the required deadtime needs a few switching cycles of the power converter operation because the V_{SW} signal has the longest rise and fall times (t_r and t_f) in the power converter. This is decreasing the performance of the deadtime control circuit. The additional circuit required to measure the potential of V_{SW} can also affect the power density and increase the cost. A dynamic deadtime optimization technique for a power converter is presented in [172]. In this approach, an additional circuit was placed in parallel with the LSS, which affects the performance of LSS. Another circuit is also needed to sense the voltage of V_{IN}, which increases the overall power consumption of the converter and reduces the efficiency.

In this work, we propose a novel circuit for deadtime control that provides a wide range of delays to the power converter HS and LS by utilizing three independent reconfigurable analog modules. The tunable modules can receive digital commands from a controller to tune the required deadtime. In contrast with what is usually accepted, i.e. the values of T_{DHL} and T_{DLH} must be minimized as much as possible according to Equation 5.1 to decrease the deadtime loss, we show that this applies only for T_{DLH}, while an optimal value can be reached for T_{DHL} to decrease the power converter's deadtime loss. Indeed, if the T_{DHL} is made shorter or longer than the optimal value, the deadtime loss increases degrading the converter efficiency. The remaining of this paper is arranged as follows. Section 5.4 presents the proposed building blocks, circuit implementations, and mathematical analyses. Section 5.5 presents the experimental results. Section 5.6 discusses the performance comparison with other solutions. Section 5.7 provides the conclusion.

5.4 Proposed Tunable Deadtime Circuit

5.4.1 Proposed Architecture

Figure 5.4 illustrates the configuration of the proposed Wide Range Multi-Tuned-Deadtime Control Circuit (WRM-TDC). Three adjustable parts (A, B, and C) are utilized to allow a wide range of deadtime delays. The controller command can be used to set up these parts (32 dedicated switches are used for both sides). The presented WRM-TDC uses two initial capacitors (C_1 and C_2), which are linearly charged by I_{C_1} and I_{C_2}, respectively, to produce two rectangular signals.

These rectangular waveforms are applied to two Schmitt Triggers (ST_1 and ST_2). Two pulse signals are generated at the output of ST_1 and ST_2 when the rectangular signals are applied because the hysteresis windows of ST_1 and ST_2 are initialized (switching thresholds of STs are set with initial values). The two pulse-shaped signals produced at the output of STs do not overlap each other due to the created deadtime between T_{DLH} and T_{DHL} thanks to the presented WRM-TDC. A wide swing current source (MP1-MP7) is employed to mirror the currents of Iin and Ibias (for producing I_{C1} and I_{C2}). In addition, the switches of $Q_1 - Q_6$ are closed/opened with controlling signals Φ_1 and Φ_2 to charge/discharge C_1 and C_2. The gate driver with the adjustable deadtime receives a PWM signal from the controller and generates two waveforms for HS and LS power switches with optimal T_{DLH} and T_{DHL} to allow for high power conversion efficiency with minimized deadtime loss.

The advantages of the presented WRM-TDC are:

- Digital commands are sent to the WRM-TDC to adjust the required deadtime of the gate driver. Accordingly, off-chip components or digital-to-analog converters are not needed. Therefore, the communication between the FPGA and the gate driver is facilitated, the power consumption of the gate driver is decreased, and the reliability of power converters is increased. In addition, the strategy for generating different deadtimes is simple and fast.

- To tune the proposed deadtime control circuit, we use three different current/capacitor-based tuning circuits (A, B, and C). Hence, producing a wide range of T_{DLH} and T_{DHL} is possible. This potential procedure is essential for power converters with various loads and V_{IN}.

- The type of circuits used to design each reconfigurable part is different. Accordingly, the attained resolution from each part is different. ST has the highest resolution, while the capacitor-based parts have the lowest resolution. This situation allows the allocation of the least significant bits (LSBs) of the controlling code to ST-based tuning circuit. Meanwhile, the most significant bits (MSBs) are dedicated to the capacitor-based parts.

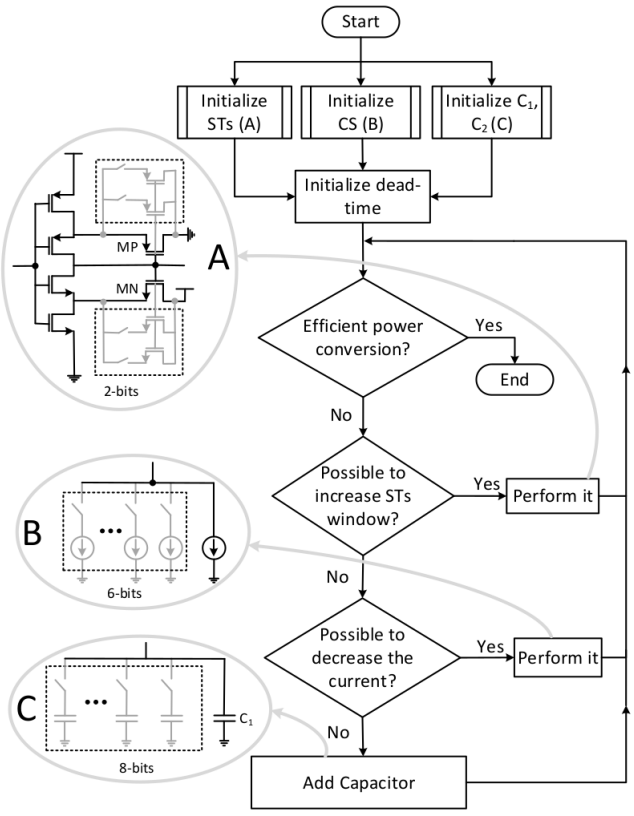


Figure 5.5: Flowchart of the operation of proposed deadtime control circuit.

Therefore, when large deadtimes is required, the proposed WRM-TDC can support power converters with a wide range of V_{IN} and load.

5.4.2 Circuit Programming and Optimization Approach

Figure 5.5 clarifies the flexibility and the reconfigurability of the presented WRM-TDC. The involved parameters and the methodologies used to realize the projected objectives are illustrated. Three sections of A, B, and C must be initiated to start the deadtime. Then, the power conversion must be verified according to the decision steps of the flowchart (i.e. decision 1, decision 2, and decision 3) to achieve maximum efficiency in a given power converter. According to [145], an efficient conversion occurs when the power converter output waveform V_{SW} meets the following conditions: $t_{Df} = 0$, $t_{Dr} = 0$, $t_{rL} = 0$, and $t_{fL} = 0$. The power dissipation (conduction loss) of the transistor increases with V_{DS}. During t_{Df} and t_{rL} (t_{fL} and t_{Dr}) the voltage drop across the low side transistor V_{DS} and is larger than that when the low side transistor is ON. This increases the conduction loss of the low side transistor during the t_{Df} and t_{rL} (t_{fL} and t_{Dr}). Thus, by minimizing the t_{Df} and t_{rL} (t_{fL} and t_{Dr}), the conduction loss of the low-side transistor will be minimized, and the power conversion efficiency will be maximized.

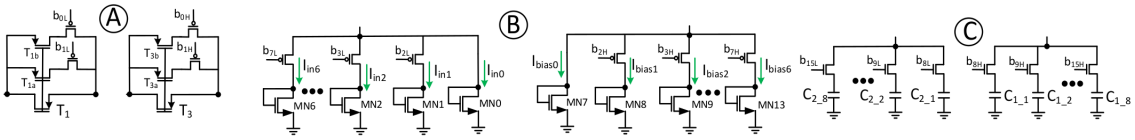


Figure 5.6: Transistor level implementation of the tunable A, B, and C parts.

Then, the power conversion must be verified in the decision stage to see if it is efficient. The waveform of the power converter output (V_{SW}) confirms the efficient conversion [145]. The conditions of $t_{Df} = 0, t_{Dr} = 0, t_{rL} = 0$, and $t_{fL} = 0$ in the waveform of V_{SW} can be achieved for an efficient operation.

If the conversion is efficient, then the configured WRM-TDC is convenient for the application. Otherwise, the first tuning part (A) must be reconfigured to achieve more delays if there is still some bit available for the reconfiguration of part A. Then, the status of the power converter must be verified again to determine if the target efficiency has been met. To reconfigure part A, 2 bits are dedicated to change the values of T_{DLH} and T_{DHL}. As shown in Figure 5.5 (part A), MOSFETs are adding in parallel with MP step by step and the same for MN to change the deadtimes. Consequently, the V_{refs} of STs will be modified, resulting in a broader hysteresis window being applied to the ramp signals over the main capacitors. Finally, the deadtime is increased to reach the optimal deadtime.

If the conversion is still inefficient when both bits of part A are used, then part B must be configured, as shown in Figure 5.5. Part B utilizes a tunable current source that is controlled by 6 bits. The amount of delivered current to the main capacitors must be decreased to obtain more deadtime. For this purpose, the number of paralleled current sources must be decreased step by step, with the condition of "efficient conversion" being verified at every step. If all the 6 bits of part B were used, then the third part (C), which contains a capacitive bank, must be included in the circuit. The capacitive bank is controlled with 8 bits to adjust the capacitor value and tune the adequate deadtime for the power converter based on the values of V_{IN} and the load. If all the 16 bits of parts A, B, and C were used, and the converter still needed longer deadtime, then the values of V_{IN} and the load should be fixed. Specifically, the proposed reconfigurable deadtime can be useful over specified ranges of V_{IN} and loads. Notably, cases where I_{OUT} is high,and V_{IN} is low require short deadtimes.

5.4.3 Circuit Implementation

Figure 5.6 shows the circuit implementation of the reconfigurable parts (A, B, and C) of the proposed WRM-TDC. In part A, T_1 and T_3 are the key transistors to configure the hysteresis windows of ST2 and ST1, respectively. These hysteresis windows of ST1 and ST2 depend on the dimensions of T_1 and T_3, respectively. Two p-channel MOSFETs of T_{1a} and T_{1b} (T_{3a}

and T_{3b}) are included in parallel with T_1 (T_3) to design an adjustable part on the STs. The hysteresis windows of the STs can be expanded if their adjusting transistors are excluded from the STs. Hence, the p-channel MOSFETs (T_{1a}, T_{3a}, T_{1b}, and T_{3b}) are enabled to achieve the shortest possible deadtime as the initial configuration. Then, this adjusting part A must be excluded from the circuit by active low switches (p-type transistors) to obtain the longer deadtime. T_{1b} and T_{3b} which are tunable parts of ST2 and ST1, respectively, are controlled with the activating bits of b_{0L} and b_{0H}) to change the values of the delays of T_{DLH} and T_{DHL} (the same for T_{1a} and T_{3a}).

The second tunable parts are I_{in} and I_{bias}. The parallel diode connected n-channel MOSFETs of MN0–MN13 are implemented to fulfill this part with real circuits. The values of the produced T_{DLH} and T_{DHL} are inversely related with currents I_{in} and I_{bias}. Accordingly, all the diodes connected must be added in the circuit to achieve the minimum T_{DLH} and T_{DHL}. Then, the MN1–MN6 and MN8–MN13 must be removed from the circuit with the active low switches (p-type transistor) to provide longer delays.

The third reconfigurable part of the proposed WRM-TDC is shown in part C. The value of the produced T_{DLH} and T_{DHL} are in direct relation with the sizes of the capacitors used. Accordingly, one capacitor is utilized in the circuit as initialization to attain the shortest T_{DLH} and T_{DHL}. Then, the integrated capacitors ($C_{1-1} - C_{1-8}$ and $C_{2-1} - C_{2-8}$ in Figure 5.6) are included in the circuit to be in parallel with the main capacitors (C_1 and C_2 in Figure 5.4) for creating longer T_{DLH} and T_{DHL}. The integrated switches in this part must be active high type (n-type MOSFET).

The aspect ratios of the transistors and the values of the passive components used to implement each part of the presented circuit are listed in Table 5.1. These components are needed for implementing one side of the circuit (generating T_{DHL}). The other side of the circuit uses the same components to generate T_{DLH}. 32 bits b_{0L} to b_{15L} and b_{0H} to b_{15H} are devoted for controlling the 32 switches used to realize the tunable parts in both sides of Figure 5.4. Among these 32 bits, four LSB bits of $b_{0L} - b_{1L}$ and $b_{0H} - b_{1H}$ are allocated to the ST-based parts (in the right and left of Figure 5.4), 12 bits of $b_{2L} - b_{7L}$ and $b_{2H} - b_{7H}$ are earmarked to current source part (I_{in} and I_{bias}), and the 16 MSB bits of $b_{8L} - b_{15L}$ and $b_{8H} - b_{15H}$ are assigned to capacitor-based tunable part.

The created delays in the presented WRM-TDC depends on the amounts of currents I_{C1} and I_{C2} (Figure 5.4) delivered by the current source to the integrated capacitors. Given the relation between the output current and the values of I_{in} and I_{bias}, the operation of the proposed design against mismatch and process corners should be validated. Specifically, MN0–MN13 (Figure 5.6, part B), which are used to adjust the biasing current, must be made robust against process variations. The operations on both sides of the proposed WRM-TDC are the same during the production of T_{DHL} and T_{DLH} (deadtime). A different deadtime is due to the

Table 5.1: Dimensions of all components adopted for realizing the circuit. N/A=Non-Applicable; ST:Schmitt Trigger; MP,P,N,T,MN: are Tagged on Figures 5.4, 5.6; CS: Wide Swing Current Source.

A,ST	Comp.	P1,2;N1,2	T2	T1	T1a	T1b
	W(μm)	0.4	0.6	0.6	0.8	1
	L(μm)	0.45	0.35	0.35	0.35	0.35
C	Comp.	C_2	C_{2-1}	C_{2-2}	C_{2-3}	C_{2-4}
	Value(fF)	10	15	30	60	120
	Comp.	C_{2-5}	C_{2-6}	C_{2-7}	C_{2-8}	
	Value(pF)	0.24	0.5	1	1.5	
B	Comp.	MN0	MN1	MN2	MN3	MN4
	W(μm)	0.4	0.6	0.8	1	1.2
	L(μm)	0.45	0.35	35	0.35	0.35
	Comp.	MN5	MN6	N/A	N/A	N/A
	W(μm)	1.4	1.4	N/A	N/A	N/A
	L(μm)	5	5	N/A	N/A	N/A
C	Comp.	MP1, MP2	MP3	MP4-MP7	All switches	
	W(μm)	0.8	0.4	0.8	0.4	
	L(μm)	0.35	0.35	0.35	0.35	

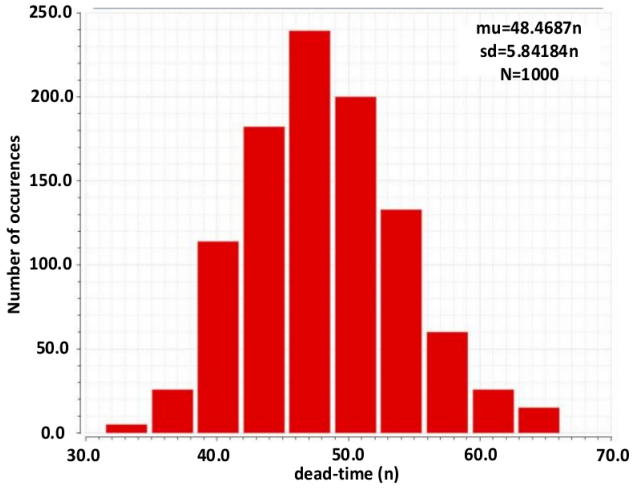


Figure 5.7: Evaluation of the proposed WRM-TDC operation with Monte Carlo simulation.

various parameter values on each side of the circuit. Accordingly, the circuit is evaluated to be robust against process variations for one of the deadtimes (i.e., T_{DHL}). The simulated deadtime value T_{DHL} is $47.5ns$ for the designed circuit and associated typical case corner (i.e., typical NMOS and PMOS transistors and $V_{DD} = 3.3V$). A worst-case scenario is simulated to anticipate the effect of process variations. Using the AMS kit, “fast NMOS/fast PMOS" yields the highest power consumption or Worst power (WP), whereas "slow NMOS/slow PMOS” yields the slowest speed or Worst speed (WS). In this study, we evaluate the operation of the proposed circuit in the WP and WS cases for one of the tuning commands (i.e., 0FFF). The

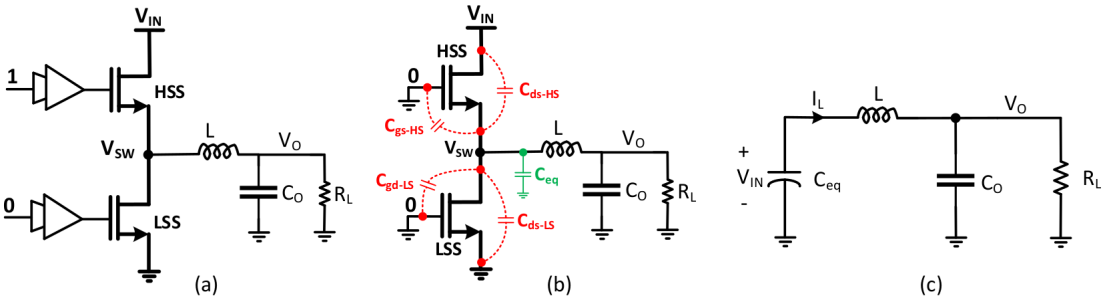


Figure 5.8: Buck converter operation evaluation (a) Simplified circuit while the HSS is turned on and the LSS is turned off (b) operation in the beginning of deadtime with effective parasitic capacitance, and (c) equivalent circuit during deadtime operation with the charged equivalent capacitor in the node V_{SW}.

WP and WS are the worst operating conditions of the circuit (Figure 5.6). The simulated deadtime values T_{DHL} for the WP and WS cases are 35.8 and 72.92ns, respectively. The WS case yields the longest deadtime, while the WP has the shortest deadtime. The impact of the process variations on the performance of the proposed WRM-TDC is studied using a Monte-Carlo simulation. A supply voltage of $V_{DD} = 3.3V$ is set for the simulation. The results for T_{DHL} are shown in Figure 5.7. Specifically, the simulated T_{DHL} shows a log-normal distribution with a variance of 0.12. The average delay of T_{DHL} is 48.46ns, and the standard deviation is 5.84ns. To increase robustness against process variations and decrease the standard deviation, the dimensions of MN0–MN13, which are responsible for biasing the circuit, can be increased while maintaining the same aspect ratio "W/L". But, a trade-off must be made between the chip area and the sensitivity of the generated deadtime to process variations. The operation of the proposed circuit is evaluated under different programming commands (i.e., 0FFF) and temperatures ($-40°$ to $80°$). Figure 5.7.b presents the simulated results. The value of $T_{DHL} = 50ns$ is selected by the command "0FFF", and varies from 42 to 52ns for the above temperature range

5.4.4 Optimal Deadtime Mathematical Analysis

A simplified power converter circuit is illustrated in Figure 5.8 to derive the equation of the optimum required deadtime for a buck converter. Figure 5.8.a shows the converter circuit when the HSS is turned on and the LSS is turned off. The HSS and LSS are in their 'off' states within the deadtime duration. Meanwhile, Figures 5.8.b and 5.8.c show the operation at the beginning of the deadtime with the effective parasitic capacitance and the equivalent circuit of the converter during the deadtime operation with the charged equivalent capacitor in node V_{SW}, respectively. Within the deadtime duration, the HSS and LSS are turned off. In this condition, the total equivalent capacitance in node V_{SW} is given by

$$C_{eq} = C_{gd-LS} + C_{ds-LS} + C_{gs-HS} + C_{ds-HS} + C_{par} \tag{5.2}$$

where C_{par} is the parasitic capacitance of the power switch packaging and wire-bonding. Figure 5.1.b shows that the deadtimes T_{DLH} and T_{DHL} are set asymmetrically to ensure a secure operation against shoot-through and provide efficient conversion of the power converter. To increase the buck converter efficiency, the T_{DHL} must be set in its optimal state, which is when the charged C_{eq} is totally discharged ($V_{Ceq}(T_{DHL}) = 0$), then the LSS must be activated. Otherwise, if T_{DHL} is set longer or shorter than the optimal time, the loss is increased, and the buck converter will not be efficiently designed. The optimal duration condition for T_{DLH} is determined to avoid shoot-through. The value of T_{DLH} can be reduced as long as shoot-through does not occur. The equivalent circuit of the buck converter is shown in Figure 5.8.c where C_{eq} is charged in advance by V_{IN} at the beginning of the deadtime. The analysis of the deadtime generation begins with:

$$V_L(t) = L\frac{dI_L(t)}{dt} \tag{5.3}$$

which can be rearranged as follows when evaluated within a given time interval:

$$V_L \Delta T = L \Delta I_L \tag{5.4}$$

where V_L equals to $V_{IN} - V_{OUT}$. In this buck converter, ΔT is for the time duration of the HSS operation for one cycle of the input PWM, which is obtained by the product DT_s. Thus, in Equation 5.4, ΔT must be replaced by DT_s as follows:

$$(V_{IN} - V_{OUT})DT_s = L\Delta I_L \tag{5.5}$$

where D and T_s are the duty cycle and period of the input PWM, respectively. In the buck converter, D is equal to V_{OUT}/V_{IN} [169]. The value of ΔI_L is evaluated by substituting the V_{OUT}/V_{IN} instead of D in 5.5 as follows:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})\frac{V_{OUT}}{V_{IN}}\frac{1}{f_s}}{L} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{LV_{IN}f_s} \tag{5.6}$$

In Figure 5.1.b, the red curve shows the currents flowing into the circuit during the deadtime, in which $I_{L(peak)}$ is equal to $I_{Load} + \frac{\Delta I_L}{2}$. According to Equation 5.6, $I_{L(peak)}$ can be defined by

$$I_{L(peak)} = I_{Load} + \frac{\Delta I_L}{2} = I_{Load} + \frac{V_{OUT}(V_{IN} - V_{OUT})}{2LV_{IN}f_s} \tag{5.7}$$

After setting an optimal deadtime for the buck converter, the zero-voltage switching condition would occur [172]. In this condition, the available charge in the C_{eq} is discharged by converter's inductance before turning-on the LSS. According to the equation of the equivalent capacitance in node V_{SW} at a given time,

$$I_{Ceq} = C_{eq}\frac{dV_{Ceq}(t)}{dt} \Rightarrow I_{Ceq} = C_{eq}\frac{\Delta V_{Ceq}(t)}{\Delta t} \tag{5.8}$$

During the discharge of the equivalent capacitance, $I_{Ceq-discharge} = I_L$. Hence,

$$\Delta t = \frac{C_{eq}\Delta V_{Ceq}(t)}{I_L} \tag{5.9}$$

As shown in Figure 5.1.b, I_L is approximately equal to $I_{Lpeak}(I_L(t) \approx I_{Lpeak}(t))$ within the deadtime duration, and $\Delta V_{Ceq}(t)$ is equal to $V_{IN} - V_{Ceq}(T_{DHL}) = V_{IN} - 0 = V_{IN}$ in the optimal deadtime conditions ($V_{Ceq}(T_{DHL}) = 0$). This condition holds for all Δt equal to T_{DHL}, specifically at its optimal value. From the equation of I_{Lpeak} in Equation 5.7, the optimal deadtime is given by

$$\Delta t_{opt} = \frac{C_{eq}V_{IN}}{I_{Lpeak}} = \frac{C_{eq}V_{IN}}{I_{Load} + \frac{V_{OUT}(V_{IN}-V_{OUT})}{2LV_{IN}f_s}} = T_{DHL} \tag{5.10}$$

where $I_{load} = \frac{V_{OUT}}{R_L}$. The deadtime T_{DLH} must be minimized as much as possible to avoid shoot-through. An efficient buck converter design must address this requirement.

5.5 Measured Performance

5.5.1 Experimental results of proposed WRM-TDC

Figure 5.9 shows the experimental test bench. The experimental results of the proposed WRM-TDC are measured by soldering it on a printed circuit board (PCB) in the laboratory. Two 16-bit flat ribbon cables are utilized to send the digital commands to the proposed circuit to program the different T_{DHL} and T_{DLH} at the circuit output. A pulse-shaped signal was generated with a function generator as input signal. The deadtimes T_{DHL} and T_{DLH} are measured with an oscilloscope between the non-overlapping signals. Different capacitive loads of $1pF - 10nF$ was used at each output of under test chip to measure the performance of fabricated chip.

The chip micrograph of the proposed WRM-TDC fabricated in $0.35\mu m$ CMOS process is presented in Figure 5.10. A wire-bonded die micrograph is presented in Figure 5.10.a. The enlarged cores of the fabricated chip, which includes the different parts of A, B, C, and CS and occupies $150\mu m \times 260\mu m$ of silicon area, are shown in Figure 5.10.b. Figure 5.11

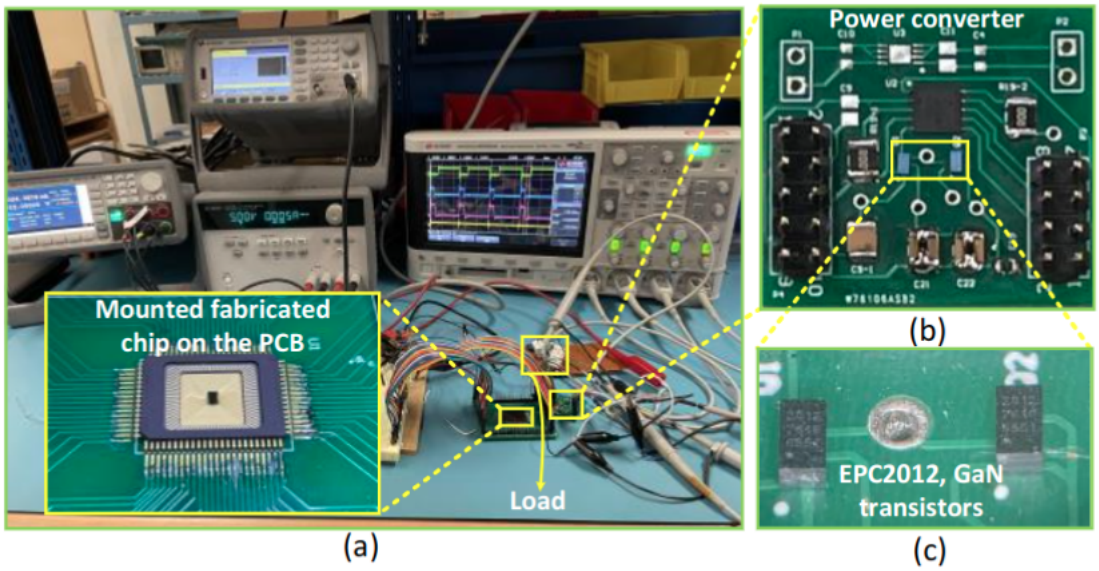


Figure 5.9: Experimental setup: (a) equipment to measure the performance of fabricated WRM-TDC, (b) enlarged power converter, and (c) enlarged power GaN transistors of EPC2012.

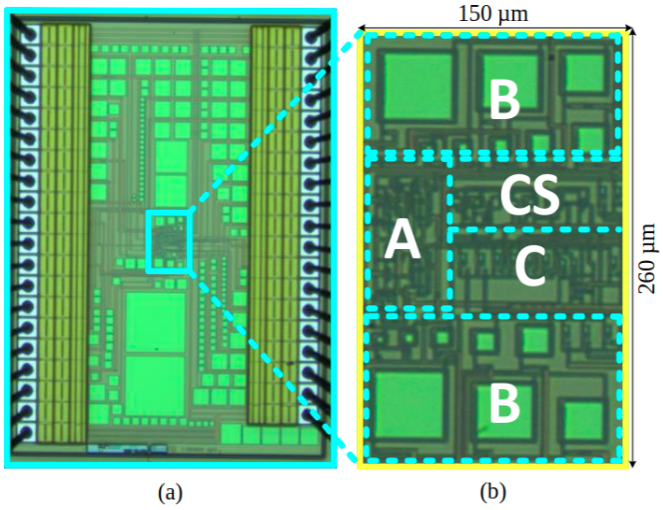


Figure 5.10: Chip micrograph of the proposed WRM-TDC fabricated in 0.35μm CMOS process (a) die micrograph, (b) enlarged core including different circuit parts of A, B, C, and CS.

shows the measured deadtimes generated by the WRM-TDC. The measured minimum and maximum selectable deadtimes corresponding to programing commands of 0000 and $FFFF$ are presented in Figure 5.11.a and 5.11.b, respectively. A minimum deadtime of $T_{DLH} = 9.2ns$ is measured for the proposed WRM-TDC, while the circuit was supplied with $V_{DD} = 5.0V$, and the operating frequency was $f_s = 1MHz$. A maximum deadtime of $T_{DHL} = 1\mu s$ is measured, while the fabricated prototype was supplied with $V_{DD} = 3.3V$, and the operating

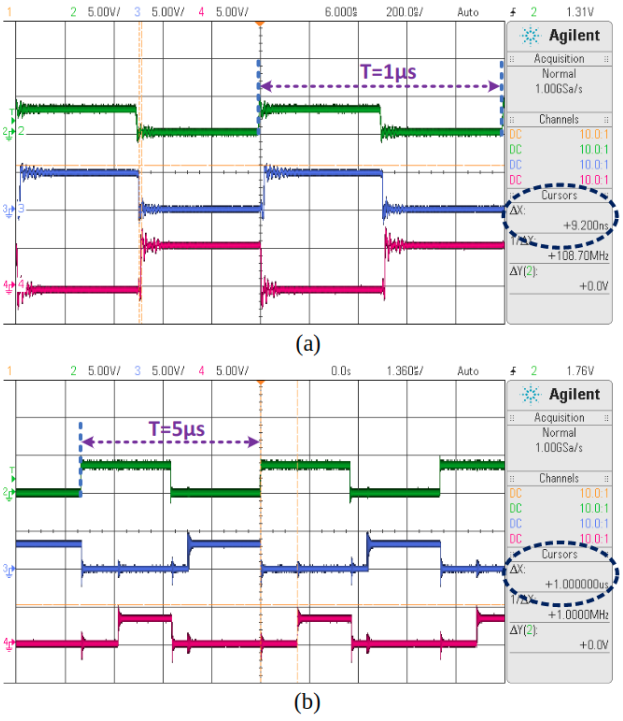


Figure 5.11: Measured generated dead-times by WRM-TDC:(a) minimum produced dead-time of $T_{DLH} = 9.2ns$ at $C_L = 1pF$, $V_{dd} = 5.0V$, and $f_s = 1MHz$;(b) maximum attained dead-time of $T_{DHL} = 1\mu s$ at $C_L = 5pF$, $V_{dd} = 3.3V$, and $f_s = 200kHz$.

frequency was $f_s = 200kHz$. In Figure 5.11, the green waveform corresponds to the input pulse signal applied to the chip. The signals in blue and red correspond to the output of the chip, which can be used as appropriate driving signals for the HS and LS of the buck converters. The measured T_{DLH} and T_{DHL} are shown in blue an and red correspond to the output of the chip, which can be used as appropriate driving signals for the HS and LS of the buck converters.

The measured T_{DLH} and T_{DHL} are shown in blue and red in Figure 5.12.a, respectively. The circuit is connected to $V_{DD} = 5.0V$, a capacitive load $C_L = 1pF$ was used, and the operating frequency was set to $f_s = 1MHz$. The measured results are categorized based on the operation of the circuit in four different regions. In the first region, the proposed WRM-TDC is initialized to produce the shortest possible deadtime. In this configuration, parts A and B are enabled, and part C is disabled (MN0-MN13, T_{1a}, T_{1b}, T_{3a}, and T_{3b} are in the circuit, while the integrated capacitors are disabled). In this first region, the measured T_{DLH} and T_{DHL} are 9.2 and 10.8ns, respectively. The circuit can be programed to work in the other regions to increase the deadtime. In Region 2, part A is disabled step by step by received commands, part B is enabled, and part C is disabled. The LSB b0 is set to "1" to increase the delay whereas the other bits are kept at "0" (i.e., the command of "0001",

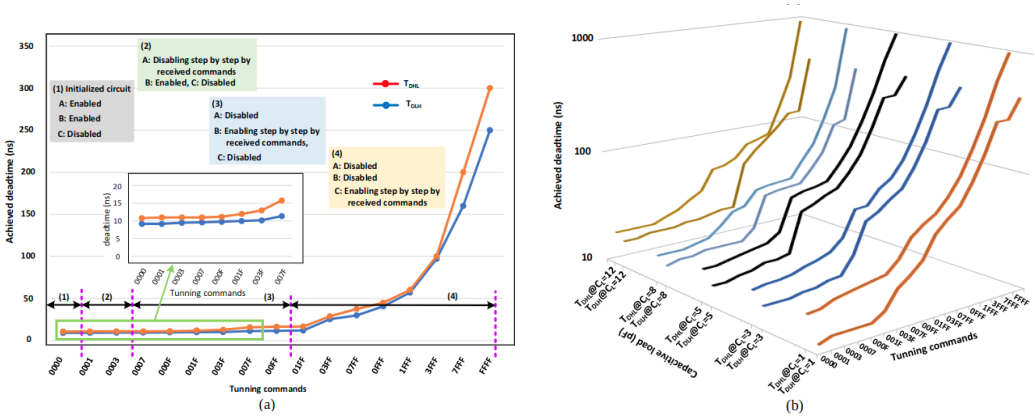


Figure 5.12: Measured T_{DLH} and T_{DHL} from the fabricated chip in the various conditions:(a) different configurations of circuit at $V_{dd} = 5.0V$, capacitive load $C_L = 1pF$, and $f_s = 1MHz$;(b) different configurations of the circuit at $V_{dd} = 3.3V$, capacitive between $C_L = 1pF$ to $C_L = 12pF$, and $f_s = 400kHz$.

which is the hexadecimal code corresponding to the controlling switches status, is sent to the WRM-TDC). Two bit are dedicated to Region 2. In this part, the measured deadtime resolution is $0.2ns$ with 1% precision. Accordingly, the maximum achievable deadtimes for Region 2 are $T_{DLH} = 9.6ns$ and $T_{DHL} = 11.2ns$ under $V_{DD} = 3.3V$ and $f_s = 1MHz$. The circuits of Region 3 are activated step by step by the commands to achieve longer deadtimes than what is attained in Region 2. In Region 3, parts A and C are disabled, and part B is enabled. The measured resolutions of the circuit in Region 3 for T_{DLH} and T_{DHL} are measured at approximately 0.3 and $1ns$ (the difference between two measured deadtimes corresponds to two commands), respectively, while the number of bits dedicated to this region is 6 bits. Accordingly, the maximum measured T_{DLH} and T_{DHL} are 12 and $16.6ns$, respectively. Parts A and C are disabled, while part B is enabled by the commands to measure the results in Region 3. A longer deadtime can be achieved in Region 4 where the circuit is using a capacitive bank as delay element. In Region 4, eight different values of integrated capacitors (Table 5.1) that correspond to eight controlling bits are embedded. The longest $T_{DLH} = 250ns$ and $T_{DHL} = 300ns$ are measured in Region 4 for commands of $01FF$ to $FFFF$. Parts A and B are disabled, and part C was enabled by the commands to measure the results in Region 4. The measured results in Figure 5.12.b show the performance of the circuit in various conditions. The circuit is configured by the different commands while it is connected to $V_{DD} = 3.3V$, the capacitive load was changed from $C_L = 1pF$ to $C_L = 12pF$, and the operating frequency was set to $f_s = 400kHz$. In this condition, the measured T_{DLH} and T_{DHL} are $11ns$ to $450ns$ and $16ns$ to $1000ns$, respectively, depending on the configuration, as shown in Figure 5.12.b. The presented experimental results in Figure 5.12.b demonstrate that the configured circuit can produce stable T_{DHL} and T_{DLH} for different capacitive loads at a fixed V_{dd}.

Figure 5.13.a shows that the measured power dissipation of the fabricated chip corresponds

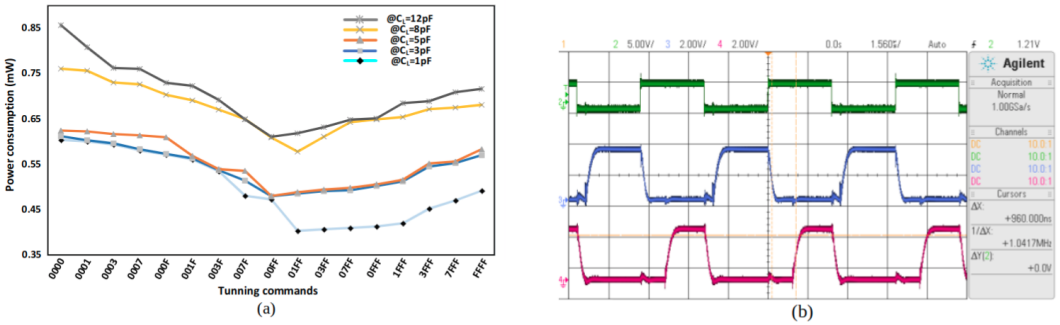


Figure 5.13: a) Measured power consumption versus tuning commands at different capacitive loads (b) Measured waveforms of proposed circuit at $V_{dd} = 3.3V$, $f_s = 200khz$, and capacitive load of $C_L = 10nF$ at each output of chip.

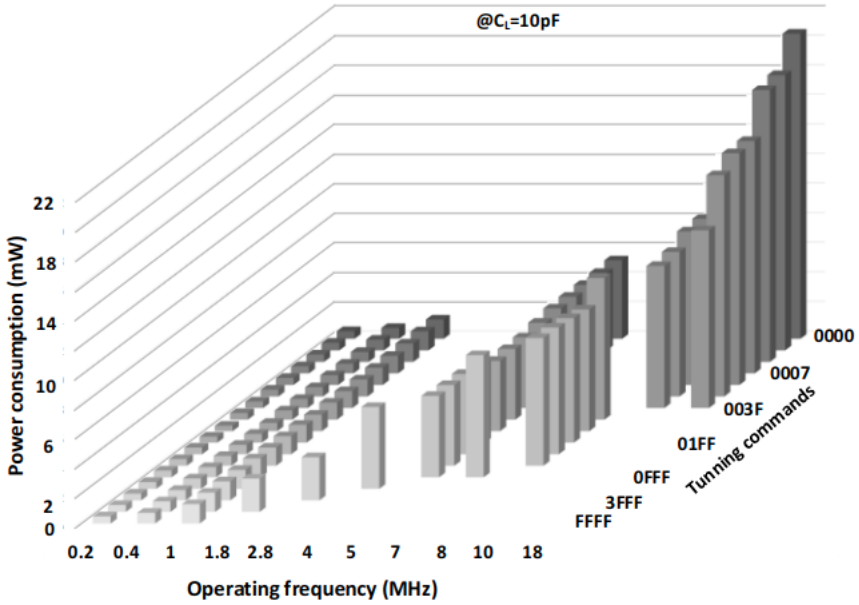


Figure 5.14: Measured power consumption versus operating frequency at different tuning commands.

to all ranges of deadtime produced by the proposed WRM-TDC in the different programed circuit configurations. The results are measured for five different values of capacitive loads. The largest power dissipation corresponds to the "0000" command (shortest delay) because all the tunable capacitive parts of A and B are added at the load in the circuit in this condition. The power dissipation results follow a descending curve (Figure 5.13.a) due to the removable of the tunable parts of A and B by the commands of "0001" to "00FF". The results follow an ascending curve due to inclusion of the integrated capacitors of part C at a longer deadtime. The circuit programed with command "FFFF" is tested with $C_L = 10nF$ at $V_{dd} = 3.3V$ and $f_s = 200kHz$ to see the performance of circuit in the case when driv-

ing big capacitive loads. The output waveforms of the chip are presented in Figure 5.13.b. Figure 5.13 shows that a long deadtime of $T_{DHL} = 960ns$ with the command of "FFFF" is achieved while the circuit is driving two large capacitive loads at its outputs. For TDLH, the value is set as short as possible, at the limit before shoot-through occurs. In Figure 5.13.b, the red waveform (i.e. the LSS activation signal) reaches zero then the blue one (i.e. the HSS activation signal) starts to increase. Given that the waveforms have no overlap between the transition, consequently, shoot-through does not occur). In this condition, the proposed deadtime circuit consumed $41mW$, while the measured output signal slew rate (SR) was $0.62V/ns$. The circuit has two outputs, namely, LS and HS, where the dynamic current is consumed to drive the capacitive loads. Therefore, to calculate the slew rate of the waveform at each output, half of the consumed dynamic current can be divided by the capacitive load ($SR = 0.5.i_{dynamic}/CL = 12.4mA/20nF = 0.62V/ns$), which is reasonable for typical applications. Figure 5.14 illustrates the measured power consumption versus operating frequency at different tuning commands, $C_L = 10pF$, and $V_{DD} = 3.3V$. According to the measured results, the power consumption increases with f_s. However, the maximum f_s is limited depending on the tuning commands. At $FFFF$, where the circuit can produce maximum T_{DLH} and T_{DHL}, the f_s is limited to $1MHz$. The circuit programed with command 0000 to generate the minimum T_{DLH} and T_{DHL} can work properly up to $18MHz$, and the measured power consumption is presented in Figure 5.14. The circuit programed with command 0000 consumed approximately 21 at $f_s = 18MHz$, whereas it dissipated $0.48mW$ for command FFFF at $f_s = 200MHz$.

5.5.2 WRM-TDC Circuit Validation with a Buck Converter

To validate the operation of the proposed WRM-TDC, a buck converter is mounted on a PCB, as shown in Figure 5.9. The fabricated chip is connected to the buck converter to measure the improvement of efficiency in the optimal T_{DHL} compared to a fixed T_{DHL}. Figure 5.15 shows the buck converter waveforms with optimal T_{DHL} and minimum T_{DLH} values. The converter specifications are $R_L = 80\Omega$, $V_{IN} = 12V$, $V_{out} = 2V$, duty cycle = 16.7%, $I_{Load} = 25mA$, $f_s = 0.4MHz$ $T_{DLH} = 12ns$, and $T_{DHL} = 80ns$. The conditions of $t_{Df} = 0$, $t_{Dr} = 0$, $t_{rL} = 0$, and $t_{fL} = 0$ in the V_{SW} waveform are achieved for optimal T_{DHL} and minimum T_{DLH}. In other words, the LSS Gate signal can increase exactly when the V_{SW} signal reaches zero (C_{eq} is fully discharged ($V_{Ceq}(T_{DHL} = 0)$)). Thus, compared with the use of a fixed random deadtime, the efficiency improves by 12%.

In order to set $I_{load} = 25 - 400mA$ (i.e. the inductor direct current resistance), the specifications of the buck converter are $V_{IN} = 12V, f_s = 0.4MHz, V_{OUT} = 2V, L = 100\mu H, C_O = 4.4\mu F, DCR = 200m\Omega, ESR = 100m\Omega$ (capacitor equivalent series resistance), and $R_L = 80\Omega - 5\Omega$. Thus, we can attain maximum efficiency of the buck converter at different loads ($25\check{}400mA$). Figure 5.16.a presents the measured results in three different conditions in-

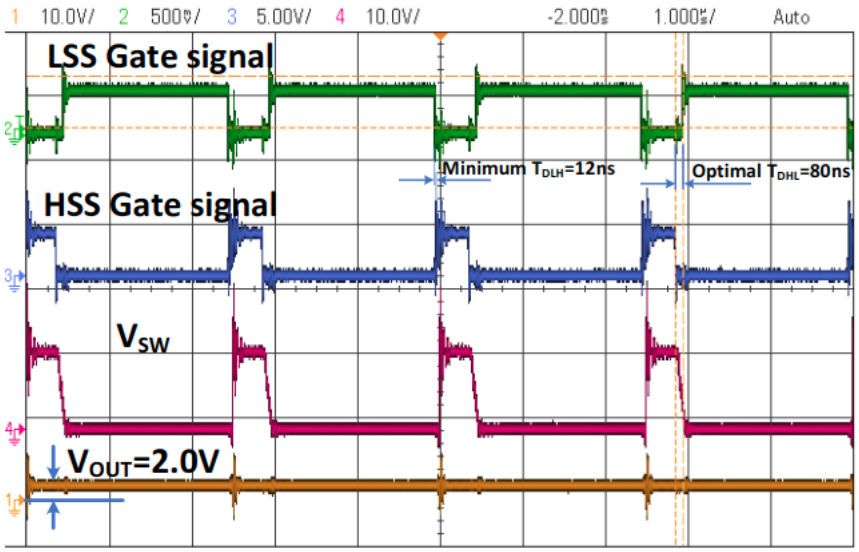


Figure 5.15: Buck converter waveforms with optimal T_{DHL} and minimum T_{DLH} under efficient design.

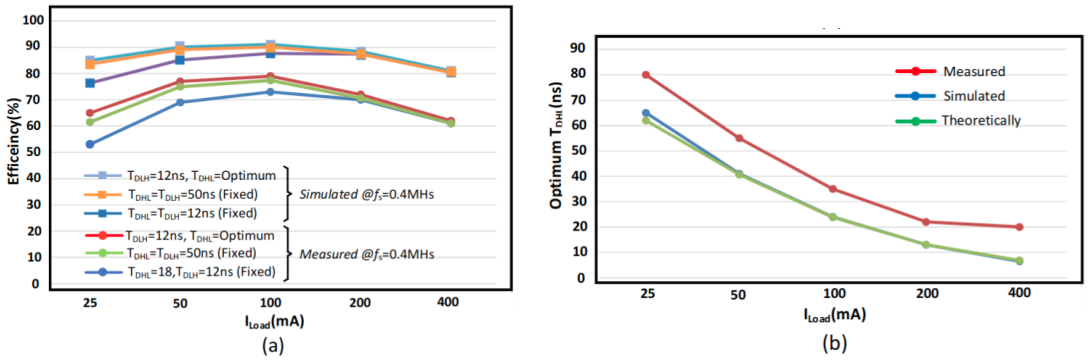


Figure 5.16: Measured results(a)achieved efficiency of the implemented buck converter for different T_{DHL} and T_{DLH} at $0.4MHz$ versus different I_{load}, (b) comparing the measured, simulated,and calculated optimal T_{DHL}.

cluding 1) $T_{DLH} = 12ns$, T_{DHL} = optimum at different I_{load}, 2) $T_{DLH} = T_{DHL} = 50ns$ (fixed deadtime determined by proposed circuit), and 3) $T_{DLH} = T_{DHL} = 12ns$ (fixed deadtime). At $f_s = 0.4MHz$, the measured efficiency is changed from 53% (at $I_{out} = 25mA$ and $T_{DHL} = T_{DLH} = 12ns$) to 80% (at $I_{out} = 100mA$ and $T_{DLH} = 12ns$, $T_{DHL} = optimum$). The curves in Figure 5.16.a are obtained using an array of resistive loads between 80 and 5.0Ω. The resistive loads are connected to the output of the described buck converter and manually switched between each measurement from 80Ω to 5.0Ω. The buck converter is connected to a $12.0V$ power supply and the duty cycle of the input PWM is set to 16.66% [duty cycle= $(V_O/V_{IN}) \times 100 = (2.0V/12.0V) \times 100 = 16.66\%$] by using a function generator. For each resistive load, the output and input power of the buck converter are measured,and the

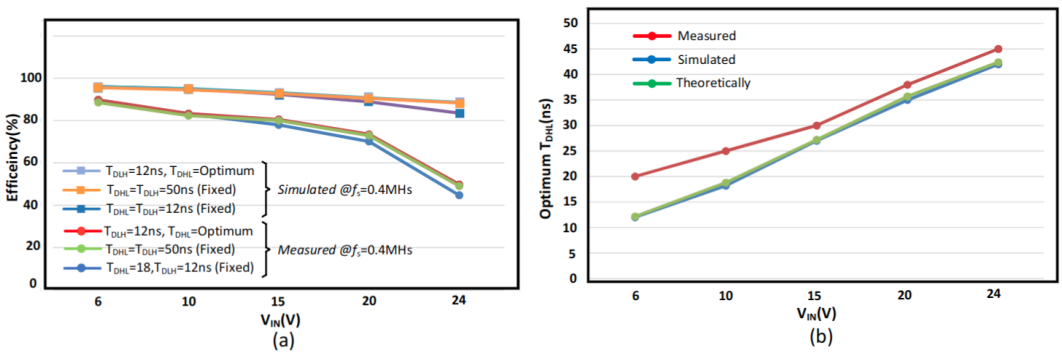


Figure 5.17: Measured results(a) achieved efficiency of the implemented buck converter for different T_{DHL} and T_{DLH} at $0.4MHz$ versus different V_{IN}, (b) comparing the measured, simulated, and calculated optimal T_{DHL}.

efficiency is then calculated. In addition, the three aforementioned deadtime scenarios are applied. Figure 5.16.a shows the measured efficiencies versus I_{load} for these three deadtime scenarios. In Figure 5.16.a, the red curve follows the maximum efficiency.

Figure 5.16.a shows that, although in the blue curve, the value of T_{DHL} is set to $12ns$ (shorter than the optimal value in Figure 5.16.b for different loads), the achieved efficiency is lower than the others. Indeed, the efficiency of the buck converter with minimum T_{DLH} and optimal T_{DHL} at $I_{Load} = 25mA$ is improved by 12% compared to converter with fixed deadtime of $T_{DLH} = T_{DHL} = 12ns$. In summary, a significant outcome of the analysis is that although the T_{DLH} must be as short as possible (before shoot through occurs) to attain maximum efficiency, it is different for T_{DHL}. In the buck converters at exact optimal T_{DHL} (no longer and no shorter than the optimal condition), the maximum efficiency would be achieved.

The efficiency of buck converter for $I_{load} = 100mA$ improved by 7% due to the optimal T_{DHL}. The optimal T_{DHL} that corresponds to different I_{out} for frequency of $0.4MHz$ are plotted in Figure 5.16.b. These optimal T_{DHL}, which are attained based on the measured maximum efficiency at different I_{out}, are compared with the calculated T_{DHL} on the basis of (10) and with the simulated optimal T_{DHL} as well. The results presented in Figure 5.16.b confirm the accuracy of (10). Figure 5.16.b shows that the maximum efficiency reached by the simulated converter at $f_s = 0.4MHz$ for $I_{load} = 25 - 400mA$ is achieved with the optimal deadtimes of $65 - 6.5ns$.

A buck converter with the following specifications is used to validate the anticipated dependency of T_{DHL} over V_{IN} in (10): $V_{OUT} = 3.3V, f_s = 0.4MHz, L = 100\mu H, C_O = 4.4\mu F, DCR = 200m\Omega$ (inductor direct current resistance), $ESR = 100m\Omega$ (capacitor equivalent series resistance), $R_L = 33\Omega$ ($I_{out} = V_{OUT}/R_L = 100mA$), and V_{IN} varied from $6.0V$ to $24.0V$. The maximum efficiency of the buck converter for different V_{IN} $(6.0 - 24.0V)$ is attained. Figure 5.17.a presents the measured results of the converter in three different con-

Table 5.2: Performance Comparison of the proposed WRM-TDCWITH similar works.

References	TPEL'21 [166]	ECCE'20 [66]	ISSC'16 [170]	ESSCIRC'11 [107]	JSSC'16 [4]	Ours
Technology (nm)	–	250	350	65	180	350
Results	Measured	Measured	Measured	Measured	Measured	Measured
Input Voltage (V)	Up to 40	12	$3-40$	Up to 5	$12-18$	$6-24$
Output Current (mA)	$240-8800$	$200-1000$	$10-1200$	≤ 120	$50-500$	$25-400$
Tunning range (ns)	Up to 50	$0.4-9.4$	$0.9-10.4$	$1-32$	$3-28$	$9.2-1000$
Power Switches	GaN	GaN	GaN	Si MOS	Si MOS	GaN
Bootstrap Capacitor	On-chip	On-chip	On-chip	External	External	External
Maximum efficiency (%)	$95.8\%@V_{IN}=30V$	87.9%	$90.7\%@V_{IN}=12V$	$76.4\%@V_{IN}=3V$	$81.2\%@V_{IN}=12V$	$90\%@V_{IN}=24V$
Efficiency improvement	$1.9\%@V_{IN}=40V$ $4.5\%@V_{IN}=30V$	$4\%@I_{OUT}=1A$	8.5%	3%	6%	$12\%@I_{OUT}=25mA$ $5.1\%@V_{IN}24V$

ditions, 1) $T_{DLH}=12ns$, $T_{DHL}=optimum$ at different V_{IN}, 2) $T_{DLH}=T_{DHL}=50ns$ (fixed deadtime), and 3) $T_{DLH}=T_{DHL}=12ns$ (fixed deadtime). The results are shown in Figure 5.17.a. The efficiency changes from 44.1% (at $V_{IN}=24V, T_{DLH}=12ns$, and $T_{DHL}=18ns$) to 90% (at $V_{IN}=6.0V, T_{DLH}=12ns, T_{DHL}=optimum$). The presented curves in Figure 5.17.a are obtained by setting the resistive load to 33Ω. The buck converter is connected to the power supply of 6.0V and the duty cycle of the input PWM isset to 33.33% [duty cycle=$(V_O/V_{IN})\times 100=(2.0V/6.0V)\times 100=33.33\%$]by using a function generator. This setup is implemented for different V_{IN} from $6.0V$ to $24.0V$ and the duty cycle is set manually in each step. For each V_{IN}, the output and input power of the buck converter are measured and the efficiency is then calculated. In addition, the three aforementioned deadtime scenarios are applied. Figure 5.17.a 17 shows the measured efficiencies versus V_{IN} for these three deadtime scenarios. The efficiency of the converter with optimal deadtime for $V_{IN}=24V$ is improved by 5.1% compared with the efficiency measured with a fixed deadtime (at $V_{IN}=6.0V$ and $T_{DLH}=T_{DHL}=12ns$). The improvement of efficiency for $V_{IN}=6.0V$ is of 0.4% due to the optimal T_{DHL} compared with the fixed T_{DHL}. In Figure 5.17.b, the optimal T_{DHL} that corresponds to different V_{IN} is presented. These optimal T_{DHL}, which are attained based on the measured maximum efficiency at different V_{IN}, are compared with the calculated T_{DHL} based on Equation 5.10 and with the simulated optimal T_{DHL} as well. The presented results in Figure 5.17.b confirm the accuracy of (10). The maximum efficiency achieved for the simulated converter at $f_s=0.4MHz$ for $V_{IN}=6.0-24V$ with the optimal deadtimes of $12-42ns$ is shown in Figure 5.17.a.

5.6 Discussion and Performance Comparison

Table 5.2 compares the performance of the presented WRM-TDC with other solutions. A deadtime optimization technique based on mathematical analysis is introduced in [166]. As shown in Table 5.2, the optimized deadtime circuit increases the efficiency by 4.5% compared to the fixed deadtime. One disadvantage of the approach described in [166] is that the values of both T_{DLH} and T_{DHL} must be changed based on the circuit parameters. However, we demonstrated that the value of T_{DLH} must be minimized while only the value of T_{DHL} should be determined using the derived equations. According to the measured results, the efficiency

can be improved by up to 12% when using the proposed circuit and deadtime optimization method. A bang-bang deadtime circuit that can generate a deadtime ranging from $0.4ns$ to $9.4ns$ is presented in [66]. The circuit proposed in [66] is suitable for applications with low V_{IN} and high I_{out} requiring a short deadtime. The work presented in [170] can improve efficiency by 8.5%. However, the range of generated deadtime is restricted between $0.9ns$ to $10.4ns$, which cannot support a wide range of power converter applications. The solutions presented in [107] and [4] lead to maximum efficiencies of 76.4% and 81.2%, respectively, while the efficiency improvement is between $3\% - 6\%$. In Table 5.2, the proposed circuit achieves the wider tuning deadtime range, producing delays between $9.2ns$ and $1000ns$. Additionally, the proposed optimization technique improves the efficiency by up to 12% compared to a fixed deadtime. Another advantage of the proposed circuit is to accommodate buck converters with a wide range of I_{out} and V_{IN}. In DC–DC converters, the three main types of losses are: 1-switching, 2-conduction, and 3-deadtime. Our method aims to minimize the deadtime loss. Switching and deadtime losses are dominant for light loads and high VINbut conduction loss is dominant for heavy loads. Accordingly, given that our proposed circuit improves deadtime and switching losses, Figures 5.16.a and 5.17.a show greater efficiency improvement in light loads and high V_{IN}.

5.7 Conclusion

We proposed a reconfigurable deadtime circuit to produce a vast range of delays between the high and low side waveforms activating a power converter. Three reconfigurable parts are allocated for the designed circuit to have a variable deadtime to accommodate different types of power converter loads and input voltage. In addition, the tunable procedure can help in finding an optimal deadtime for a given power converter to minimize deadtime loss, especially for GaN-based converters that suffer from the deadtime loss. The advantages of the proposed circuit include utilizing a digital approach to adjust the deadtime rely on three different adjustable topologies with different performance in the case of resolution. The circuit yields deadtimes ranging between $9.2ns$ and $1000ns$, which a wide variety of power converters driving different loads and operating at various input voltages. According to the measured results, the fabricated chip dissipated $41mW$ when configured to produce a long deadtime of $940ns$, while driving $C_L = 10nF$ with a slew rate of $0.62V/ns$. The circuit operates up to $18MHz$ when configured to generate the shortest deadtime of $9.2ns$. The fabricated chip was connected to a buck converter to validate the operation of the proposed circuit. The efficiency of the buck converter with minimum T_{DLH} and optimal T_{DHL} at $V_{IN} = 24V$ is improved by 5.1% compared to when the converter is using fixed deadtimes of $T_{DLH} = T_{DHL} = 12ns$.

Table 5.3: GAN Power Loss Formulas.

Loss	Equation
P_{SW}	$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times (t_r + t_f)$
P_{CON}	$P_{CON} = R_{ON} \times I_{RMS}^2$
P_{DT}	$P_{DT} = \frac{1}{2} \times f_s \times V_{SD} \times I_{OUT} \times (T_{DLH} + T_{DHL})$
P_{CAP}	$P_{CAP} = V_{IN} \times Q_{OSS} \times f_{SW}$
P_G	$P_G = (Q_{g-H} + Q_{g-L}) \times V_{gs} \times f_{SW}$
P_{DCR}	$P_{DCR} = (I_{OUT}^2 \times (\Delta I)^2/12) \times R_{DCR}$
P_{ESR}	$P_{ESR} = (\Delta I)^2/12 \times R_{ESR}$

5.8 Appendix

The power losses of a typical power converter shown in Figure 5.1.a using GaN power switches can be summarized in Table 5.3. The P_{SW}, P_{CON}, P_{DT}, P_{CAP}, P_G, P_{DCR}, and P_{ESR} are switching loss, conduction loss, dead-time loss, output capacitance loss, gate charge loss, DC resistance of the output inductance loss, and output capacitance ESR loss, respectively. These power converter losses can be categorized into two families. Time-dependent losses are those related to the converter's operating frequency (P_{SW}, P_{DT}, P_{CAP}, and P_G). Time-independent losses (T_{I_L}) are due to physical specifications of the power switches and packaging specifications (P_{CON}, P_{DCR}, and P_{ESR}). One of the considerable T_{I_L} is due to the layout routing and bonding wires, which can account for approximately 24% of the total loss in a typical power converter [149]. In the P_{CON} equation, the I_{RMS} is calculated by

$$I_{RMS} = \sqrt{(I_{OUT}^2 + (\Delta I)^2/12)D} \tag{5.11}$$

where D is the on-state percentage of either the HSS or the LSS in one cycle of power converter operation.

Conclusion and Future Work

The goal of the work presented in this dissertation was to develop a gate driver by focusing on the design of a reconfigurable type to provide an optimum and asymmetric deadtime for power converters to achieve maximum efficiency. We developed three CMOS chips using different circuit techniques, addressing different parts of the gate driver of power converters, including the level-up shifter, the level-down shifter, and the deadtime generator. The fabricated circuits were implemented in an AMS $0.35-\mu m$ CMOS process. The fabricated circuits were tested individually to evaluate their performance practically at different frequencies, voltages, and capacitive loads. Then, the fabricated chips were validated with the different power converters, such as half bridge and buck converters, and implemented with off-the-shelf electronics components. The total loss of the realized half bridge decreased by 40% when our proposed non-overlapping signal generator was used to provide appropriate signals for its low and high sides compared to when the half bridge worked alone. The efficiency of the implemented buck converter was improved by 12%, which can be attributed to our proposed reconfigurable asymmetric optimum deadtime generator that was connected to the buck converter. The performance of the fabricated chips is compared with that of state-of-the-art circuits in each work through performance comparison tables.

In Chapter 2, details of the proposed level-up shifter (LS) topology are presented, including the literature review of different efforts to improve the current mirror-based structure, the proposed idea, the circuit implementation, the mathematical analysis of the circuit operation, the derivation of the equation of propagation delay, and the validation of the idea with a custom designed CMOS chip. Finally, the proposed method is compared with similar recently published works. Monte-Carlo simulations over two essential parameters of the level shifter, namely power consumption and propagation delay, were performed. In the Monte-Carlo simulation of the power consumption, the mean value and standard deviation for 1000 occurrences were attained, namely, $7.92n$ and $839.6p$, respectively. In the Monte-Carlo simulation of the propagation delay, the mean value and standard deviation for 1000 occurrences were obtained, namely, $2.72n$ and $1.63n$, respectively. The fabricated chip was fully characterized by the Shmoo plot for operating frequency versus V_{DDL}, the power consumption evaluation versus the operating frequency and different supplies, the power consumption versus the capacitive load, the propagation delay versus VDDL, and the propagation delay versus V_{DDH}. The wave-

forms of LS were measured at 50-kHz input pulse with an amplitude of $80mV$ to $3.0V$, and an integrated inverter was used as the load. A fair Figure-of-Merit was defined based on the key parameter of LS, that is, the conversion range over the propagation delay. Our proposed LS circuit achieved the best value, exhibiting its superiority over the other solutions.

In Chapter 3, an active non-overlapping signal generator circuit with timing elements is proposed and validated with a 45-v input 1-mhz half-bridge converter. Using our proposed approach over the tested half bridge removed shoot-through and resulted in a loss reduction of 40%. Our circuit was implemented in AMS $0.35\mu m$ and occupied a silicon area of $70\mu m \times 180\mu m$. To implement the scheme, a two-sided wide swing current source, two switched-capacitor circuit, and two Schmitt trigger were used. The literature presents a strong discussion over the different causes of shoot-through in the half bridge configuration. The state machine representation and timing diagram of the proposed methodology are illustrated and well-clarified. The circuit implementation is elaborated, and Monte-Carlo simulation was performed to evaluate the operation of the proposed active circuit. The circuit specification was experimentally satisfied, including the consumed power versus the frequency, the calculation of different power losses, and the waveform of the different points of the circuit. In this work, the equations of the two required delays between the non-overlapping signals were derived.

In Chapter 4, we propose a new level-down shifter (LDS), which is required for the implementation of the R_x in data networks. In addition, the proposed circuit is required for the realization of the low side of gate drivers in power converter applications. In the introduction, the requirement of the level-down shifter in various applications is discussed. System-in-Package (SiP) and System-on-Chip (SoC) are two essential applications that require LDS. The presented LDS circuit is reconfigurable, using a diode connected topology, a current source, five transmission gates, and a combination of a diode and a supercapacitor to realize the main idea. This LDS provided a multiple-level down-shifter structure in the output while needing only a single-supply. The implemented circuit occupies an area of $80\mu m \times 100\mu m$. The circuit received a pulse shaped signal with an amplitude of $3.3V$ and provided three different signals with nominal amplitudes of $1.2, 1.8$, and $2.5V$ depending on the circuit configuration. The implementation and operation of the proposed circuit were explained through two general block diagrams and an actual transistor level realization. The resulting performance of the presented LDS at the three configurations at $V_{dd} = 3.3V$ and operating $frequency = 1MHz$, including static power consumption, dynamic power consumption, and rising and falling propagation delays, is discussed.

In Chapter 5, multi-tuned deadtime optimization for efficient GaN HEMT power converters is proposed. This circuit can provide a wide range of deadtime from 9.2-ns to 1-us to support power converters with variable V_{IN} and I_{load}. To implement the main idea, three tunable parts are proposed to provide an asymmetric deadtime with different resolutions for the low and high sides of the gate drivers of power converters. The optimal deadtime equation for a typical buck

converter was derived, and its dependency to the essential parameters of the buck converter, including the $V_{IN}, I_{load}, f_s, V_{OUT}, L$, and C_{eq} of power switches, is discussed. In this study, intensive investigation on all kinds of losses in power converters was conducted in addition to the clarification of the reasons for having a reconfigurable gate driver. Then, the flowchart of the operation of the proposed deadtime control circuit is presented. The transistor level realization of the idea is described in the circuit implementation section. To characterize the implemented asymmetric optimum deadtime generator, different experimental tests, including minimum and maximum achievable deadtime, the curve of achieved deadtime versus tuning commands at fixed and variable capacitive loads, power consumption versus tuning commands at fixed and various frequencies, were performed. Finally, the fabricated chip was connected to the buck converter implemented with off-the-shelf components to evaluate the efficiency of the buck converter implemented with the proposed circuit. The efficiency was calculated based on the measured parameters for three conditions, namely (1) setting the optimum deadtime for the buck converter, (2) a shorter deadtime than the optimum values, and (3) a longer deadtime than the optimum values. Then, the efficiency results for these three conditions were compared and experimentally prove that the asymmetric deadtime is required to achieve the maximum efficiency for buck converters. Furthermore, the curves of the optimum deadtime versus I_{load} and V_{IN} were extracted using the measured efficiency. These curves were compared with the simulation and theoretical analysis results. At the end, the performance comparison with state-of-the art methods is presented in a table.

In future work, the equation we derived for optimum deadtime would be implemented in a controller. The controller should have the $V_{IN}, I_{load}, f_s, V_{OUT}, L, C_{eq}$ parameters to calculate the optimum deadtimes for a given buck converter. These parameters could be attained through some embedded sensors in the converter and using the datasheet of power switch (for C_{eq}). Finally, using a self-adjusting configuration method, an autonomous system would be implemented. In addition, the integration of all our proposed circuits for the realization of the transmitter (T_X) and receiver (R_X) of a data bus network, could be recommended. Finally, the integrated data network chip would co-exist with the other integrated chips in the same package to have a single system-in-package as a sensor interface.

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