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FULL PAPER

Double Gate PbS Quantum Dot Field-Effect Transistors for Tuneable Electrical Characteristics

Artem G. Shulga, Laura Piveteau, Satria Z. Bisri, Maksym V. Kovalenko, and Maria A. Loi**

In this work colloidal quantum dots double gate transistors are introduced. A high-*k* ($k = 43$) relaxor ferroelectric polymer is used as a dielectric material for the top gate in a device where the other gate is fabricated from SiO_2. The device in double gate configuration is characterized by reduced hysteresis in the transfer curves measured by separately sweeping the voltage of the SiO_2 and of the polymer gate. Gating with the relaxor polymer leads to mobility values of $\mu_e = 1.1$ cm^2 V^{-1}s^{-1} and $\mu_h = 6 \times 10^{-3}$ cm^2 V^{-1}s^{-1} that exceed those extracted from the SiO_2 gating: $\mu_e = 0.5$ cm^2 V^{-1}s^{-1} and $\mu_h = 2 \times 10^{-3}$ cm^2 V^{-1}s^{-1}. Measurements under double gating conditions prove that the device works in a single channel mode that is delocalized over the whole film thickness. Double gating allows for shifting the threshold voltage into a desired position and also allows increasing the on-current of the devices.

1. Introduction

Colloidal quantum dots (CQDs) constitute a novel class of semiconducting materials that have enormous potential for electronics and optoelectronics.[1–3] Compared to conventional semiconductors, the main advantages of CQDs arise from their zero dimensionality and colloidal nature. Due to the nanoscale size of the particles which limits the spread of the electronic wavefunctions, dramatic effects on the optical, and charge transport properties appear.[4,5] When the particles' size becomes smaller than the de Broglie wavelength, the optical band-gap increases its energy with respect to the bulk semiconductor, with a consequent blue-shift of the absorption spectra. Such fascinating physical properties in combination with well-developed, controlled, and inexpensive synthesis methods have led to the investigation of quantum dots for potential applications in solar cells,[6–8] electrodes for photoelectrochemical hydrogen production,[9,10] light emitting diodes,[11] photodetectors,[12,13] and in field-effect transistors.[14] Among the many different semiconducting CQDs that have been synthetized in the last decade, one of the most studied families have been the Pb chalcogenides,[15] because of the highly reproducible synthesis, their overall quality, and the broad tuneability of their band-gap. The greatest success with CQDs solar cells has been obtained with PbS, which have recently reached power conversion efficiency higher than 8.5%.[7,16] Recent reports on multiple exciton generation have further increased the interest of the scientific community toward this class of material for solar energy conversion.[17–20]

Field-effect transistors (FETs) are commonly used device geometry to probe charge transport properties in CQD films. However, a number of difficulties have yet to be overcome in order to obtain high performing FETs. Because CQDs are capped with long ligands (oleic acid (OA) or similar) during synthesis, the charge transport in as-cast films is strongly suppressed. To facilitate the charge transport, a ligand exchange is performed. During ligand exchange, bulky insulating OA ligands are substituted by shorter entities, such as single atoms (Cl^-, I^-, Br^-),[21] molecular metal chalcogenides,[22,23] thiocyanates,[24] short organic molecules with one (n-butyl amine)[25] or two bonding sites (3-mercaptopropionic acid),[26] ethane dithiol (EDT),[27] or benzene dithiol[6] that can cross-link QDs to each other, forming a QD film. However, the substantial volume shrinking of the film during ligand exchange often leads to crack formation, thus breaking the connection between quantum dots and hindering the charge transport.[28] Transport properties are also affected by the presence of trap states, which can be intrinsic to the synthetic process but can also be caused by postsynthetic treatments,[29] such as imperfect ligand exchange and interaction with solvents used in the processing.[30] Moreover, in field effect transistors, the interface with the gate dielectric as well as the interaction with adsorbates (typically H_2O/O_2 redox couple[31,32]) is highly detrimental. Recently, several strategies to reduce the trap density were reported, including the close control of ambient conditions

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and thermal annealing,[26] as well as special treatments of the surface of the gate dielectric[33,34] and the use of OH-free dielectrics.[34]

Another strategy to overcome problems created by the trap density is the simultaneous biasing of the two gates, or double gating, which can allow shifting the off state of the device and the threshold voltage into the desired position, as well as to induce more charges in the channel increasing the drain current. Existing examples of double-gated devices reported for organic[35] and carbon nanotube transistors[36] have shown superior performance over single-gated ones because of controlled threshold voltage, increased charge induction, and improved stability. However, this strategy has never been attempted for CQDs field-effect transistors.

Here, we present the first double gate EDT-crosslinked PbS quantum dots FET, which uses the high-*k* relaxor ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene-1,1-chlorofluoroethylene) (P(VDF-TrFE-CFE)) as a top gate dielectric material and SiO_2 as a bottom gate. The electrical characteristics of the P(VDF-TrFE-CFE) gated devices exhibit significant variations with respect to the SiO_2 gated ones such as a reduction of the hysteresis and a smaller operational voltage. Moreover, using the P(VDF-TrFE-CFE) gate we improved the linear electron mobility by a factor of 2 (from the maximum value measured by silicon oxide gating of 0.5 up to 1.1 $cm^2 V^{-1} s^{-1}$ achieved by P(VDF-TrFE-CFE) gating with the same active layer. Furthermore, using the two gates simultaneously, we demonstrate superior control of the threshold shift and polarity of the PbS FET by effective channel tuning. Effective tuning of the threshold voltage and of the conduction types from p-type to n-type through ambipolar behavior was obtained with no substantial variation of the off-current.

2. Results and Discussion

The deposition of PbS QDs films crosslinked by short thiol ligands by spin-coating is often affected by poor film homogeneity and by formation of cracks.[37,38] Following procedures reported in the literature,[26,34] we spin-coated a layer of OA-capped PbS and subsequently exchanged OA ligands exposing the film to an EDT solution in acetonitrile. Due to differences in the surface properties of SiO_2 and EDT-capped PbS, the volume shrinking occurred anisotropically resulting in films with very rough surface with dips down to the silicon oxide substrate (see Figure S1a, Supporting Information). This film inhomogeneity has its origin at the nanometer scale and is highly detrimental to the charge transport.

In order to improve the film morphology and facilitate the charge transport process, we optimized the layer-by-layer spin-coating technique. As a first layer, we spin-coated a very thin layer of PbS with subsequent ligand exchange. The main purpose of this layer is to cover the substrate and thus create a scaffold that facilitates the further deposition of QD layers (see Figure S1b, Supporting Information). As a second step, we deposited a thicker “filler” layer. The final film (20 nm thick) displayed no dips or cracks and showed much smoother surface (see Figure S1c, Supporting Information) with respect to the film deposited without a scaffold layer.

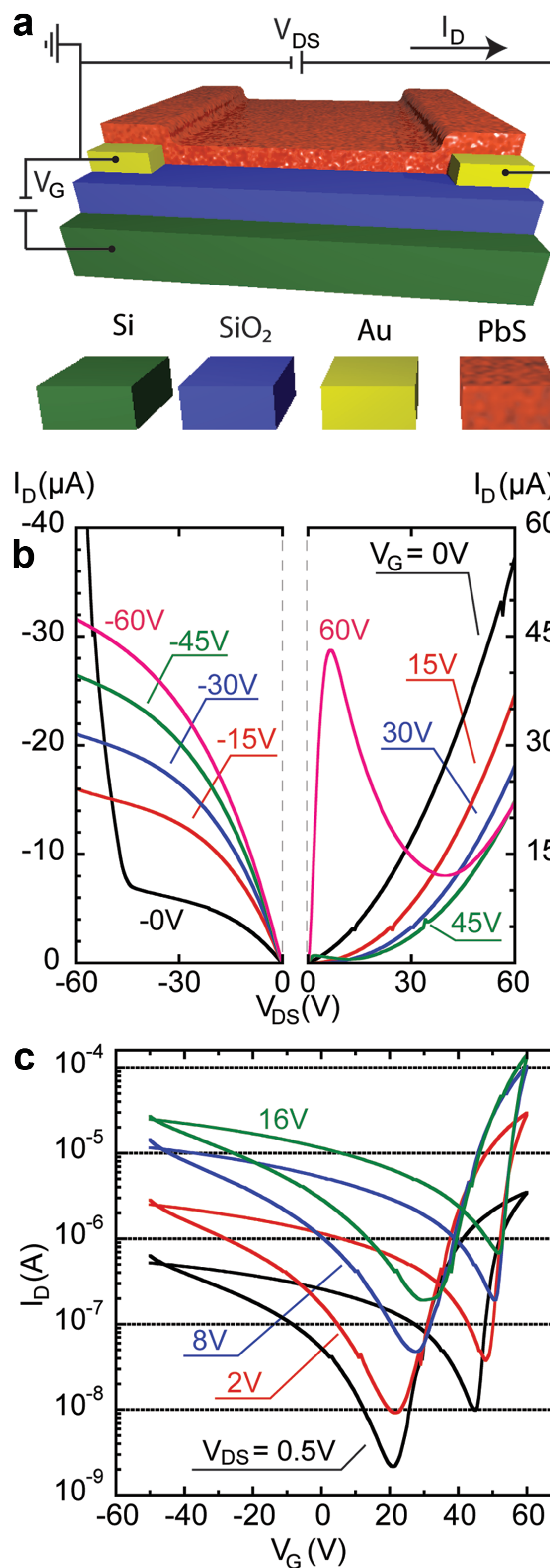

Figure 1. a) Schematics of the PbS QD FET structure on SiO_2/Si substrate. b) Output characteristics of the bottom-gate bottom-contact PbS FET. Only the forward hysteresis branch is depicted. c) Transfer characteristics of the bottom-gate, bottom-contact PbS transistor. V_{DS} from 0.5 V till 16 V are displayed.

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The schematic of the fabricated PbS field-effect transistors is reported in **Figure 1**a. The transistor has a bottom-gate bottom-contact configuration, and the gate is a highly n-doped Si substrate with 230-nm thick layer of oxide on top of which gold electrodes are patterned to create interdigitated structures with channel length of 20 µm and channel width of 10 mm. An example of the typical output characteristics, measured separately for the electron and the hole channel, are reported in Figure 1b. The transistor showed ambipolar behavior with signs of strong electron trapping that is reflected in a fast decay of electron saturation current and a large hysteresis (see Figure S4, Supporting Information) that is typical for the SiO_2/PbS interface. The transfer characteristics of the same transistor are reported in Figure 1c. Curves displayed the typical shape of ambipolar transistors with a more pronounced contribution of the electron current. As mentioned above, the charge trapping gives rise to ≈20 V hysteresis. Furthermore, the increase of the applied source-drain voltage resulted in a higher off-current, as is common for ambipolar FETs. This feature, typical of ambipolar transistors, limits the on-off ratio of the device at $V_{DS} = 2$ V to about 3×10^3, which is higher than that previously reported for EDT cross-linked PbS FETs.[14,27] The charge carrier mobilities extracted for different source-drain voltage values in the linear regime (see the Supporting Information) were 0.2 and 2.1×10^{-3} cm^2 V^{-1} s^{-1} for electrons and holes, respectively, which are the highest among any reported EDT-treated PbS films on SiO_2 substrate.

In order to check the influence of the morphology variations on the charge transfer properties of the film, we measured transistors based on single layer of the same thickness of the previously reported device deposited directly on the SiO_2 surface (see Figure S3, Supporting Information). The device exhibited mobilities $\mu_e = 4 \times 10^{-2}$ cm^2 V^{-1} s^{-1} and $\mu_h = 1.6 \times 10^{-3}$ cm^2 V^{-1} s^{-1} that were one order of magnitude lower for electrons and two times lower for holes than the performance obtained with the "scaffold" + "filler" layer devices. We infer from the mobilities that electrons are more sensitive to the film morphology than holes. As reported earlier, the limiting factor for hole mobility is the electronic structure of the PbS, which is influenced by the surface chemistry of the QDs.[39] It was also noted that by increasing the number of deposition steps, and therefore the thickness of the layer, the hysteresis could be reduced and the electron mobility be improved up to 0.7 cm^2 V^{-1} s^{-1} (see Figure S5, Supporting Information).

Despite the remarkable properties of fluorinated ferroelectric polymers as gate dielectrics, until now none have been implemented in the fabrication of colloidal quantum dot FETs. We selected P(VDF-TrFE-CFE), the monomers of which are depicted in **Figure 2**a. In the synthesis of this terpolymer, a small amount of CFE was introduced in the more typical ferroelectric copolymer P(VDF-TrFE). These CFE defects interrupt the ferroelectric domains of P(VDF-TrFE) reducing their size and thus turning its behavior from normal ferroelectric to relaxor ferroelectric (Figure 2b). Relaxor ferroelectrics, as in the case of P(VDF-TrFE-CFE), are characterized by an absence of ferroelectric hysteresis loop and by relatively high and constant dielectric permittivity, the value of which can be up to 50. Moreover, this terpolymer does not contain —OH or other chemical groups known to act as charge traps.[34] Recently, we have demonstrated that in the case of high quality QDs the effect of trapping at dielectric-CQD film becomes relevant,[6,26,34] in contrast to earlier reports which claimed that the traps in the QDs were dominating the FETs performances.[40,41]

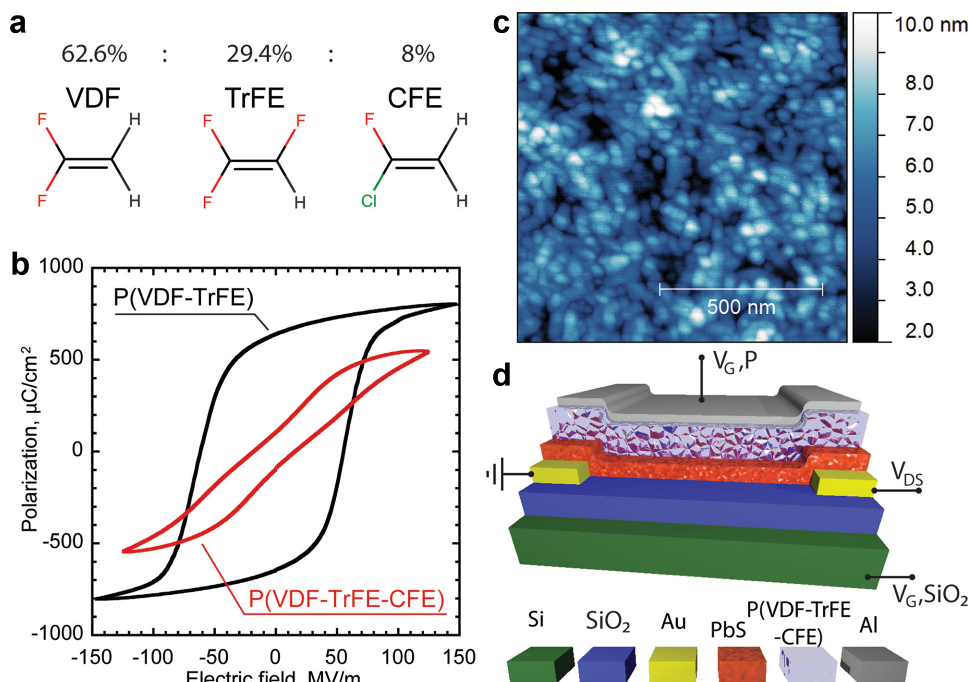

Figure 2. a) Chemical structure of monomers composing the terpolymer P(VDF-TrFE-CFE) with corresponding weight ratio. b) Electrical polarization of a plane capacitors using P(VDF-TrFE-CFE) and P(VDF-TrFE) as dielectric materials. c) AFM micrograph of the surface of a 200-nm thick film of P(VDF-TrFE-CFE) on top of PbS layer. d) Schematic structure of the device in the double gate configuration.

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In capacitor geometry, P(VDF-TrFE-CFE) films are characterized by high resistance per unit area depending on the area analyzed; for small area devices (9 mm^2) it reaches 10^{10} Ω cm^{-2} with capacitance in the order of 170–190 nF cm^{-2}, which is more than one order of magnitude higher than that of silicon dioxide. The measured thickness of the dielectric film was 200 nm, for an average dielectric constant value of about 43. It is important to underline that a variation of the dielectric constant can be obtained by varying the processing conditions.

The schematic of the double gate transistor is depicted in Figure 2d. The P(VDF-TrFE-CFE) polymer is added on top of a transistor with a silicon dioxide bottom gate. The thickness of the PbS film (20 nm) was optimized to be thick enough to ensure efficient charge transport through the film and thin enough to retain the single channel behavior of the double gate FET. The atomic force microscopy (AFM) image in Figure 2c shows that the P(VDF-TrFE-CFE) film deposited on top of the PbS film is composed of small domains with limited roughness (R_{RMS} = 1.5 nm).

Before utilizing the two gates simultaneously, the functionality of the P(VDF-TrFE-CFE) gate and the SiO_2 gate were tested individually. Single gate measurements were done separately for P(VDF-TrFE-CFE) and SiO_2 gates leaving the other gate disconnected/floating (connecting $V_{G,P}$ or $V_{G,SiO2}$ electrodes on Figure 2d). Double gate measurements were performed by simultaneously applying voltage sweeps to the two gates (connecting $V_{G,P}$ and $V_{G,SiO2}$ electrodes).

The single gate output characteristics for SiO_2 and the P(VDF-TrFE-CFE) gate are depicted in **Figure 3**a,c, respectively. Both transistors show ambipolar performances, proving that the fabrication of the P(VDF-TrFE-CFE) gate does not suppress any of the charges in the PbS film. However, in comparison with single gate devices, the properties of the transistor are changed significantly. The first and more noticeable difference is the reduced hysteresis and the appearance of a stable saturation current for both gates. This can be ascribed to the effect of the high capacitive top gate and to the screening provided by the top gate electrode able to further push the Fermi level of the active layer filling the trap states. The second difference is the shift of the off-state of the device to negative voltage (≈–20 V on SiO_2 gate) compared to the single gate device (≈20 V). The Fermi level in the PbS film shifts upward due to the screening caused by the presence of the top gate aluminium electrode leading to the shift of the threshold voltage. The third difference is that the output curves obtained sweeping the SiO_2 gate in the double-gated transistor reaches

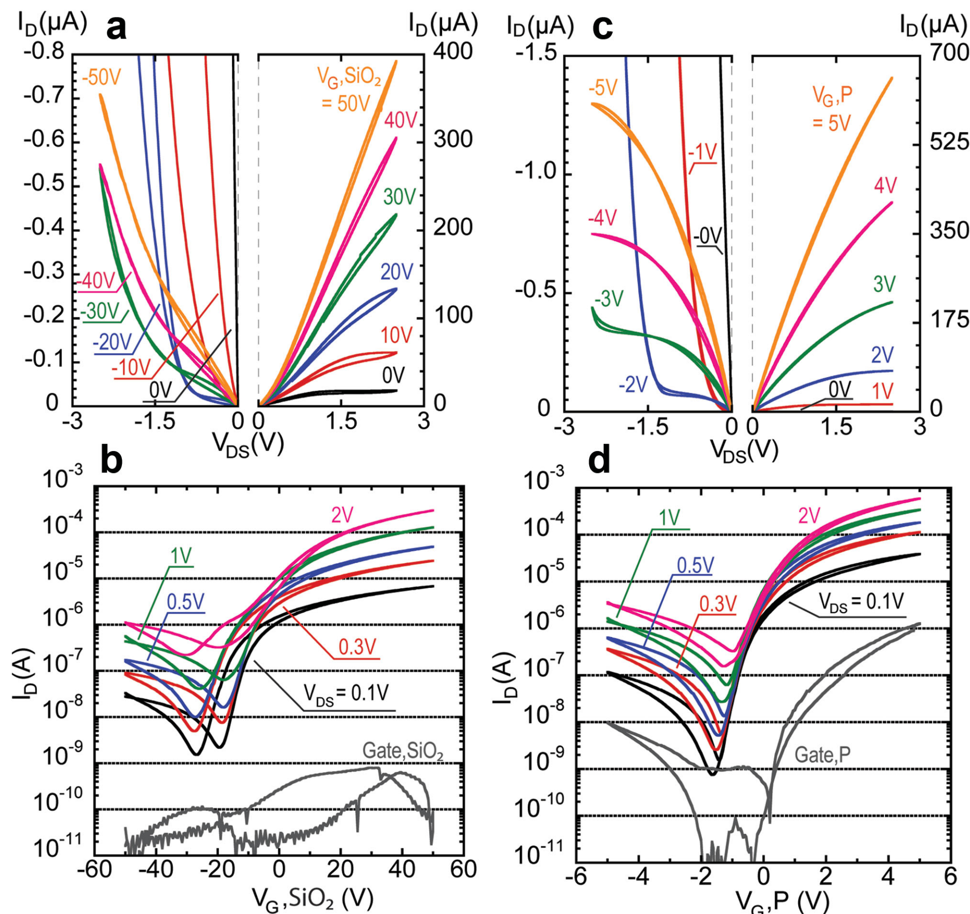

Figure 3. Output characteristics measured applying the voltage bias to the a) SiO_2 gate and to c) the P(VDF-TrFE-CFE) gate, leaving the other gate unconnected. Transfer characteristics measured doing the voltage sweep on b) the SiO_2 gate (Gate, SiO_2) and on d) the P(VDF-TrFE-CFE) gate (Gate, P). The grey-colored curves labeled Gate, P and Gate, SiO_2 are the measured gate leakage.

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the saturation regime at much lower source-drain voltage than in the single-gate device. The application of a source drain voltage of the order of several volts leads to a potential difference across the ungrounded gate electrode. Since the electrode is an equipotential surface, the P(VDF-TrFE-CFE) dielectric polarizes and induces a pinch-off of the channel more efficiently than the single SiO_2 gate. The electron injection process in the P(VDF-TrFE-CFE) gate operation (Figure 3c) is better than in the SiO_2 gate operation (Figure 3c) as indicated by the higher linearity of the electron current at low source-drain voltage.

The transfer characteristics upon single gate operation of SiO_2 and P(VDF-TrFE-CFE) gates are depicted on Figure 3b, d, respectively. In both figures, gate leakage current is plotted as a grey-colored curve. The gate leakage current during P(VDF-TrFE-CFE) gate operation is significantly higher than during SiO_2 gate operation. Most probably, this occurs because of the low mechanical resistance of the P(VDF-TrFE-CFE) gate to the contact tip, thus the contact tip easily penetrates the gate structure. However, this gate leakage current remains a few orders of magnitude lower than the drain current in the on-state and only about 1 nA during the off-state, indicating that the FET remains reliable and that the gate structure is not compromised. The hysteresis loop measured in the P(VDF-TrFE-CFE) gate operation case is narrower than the loop measured upon SiO_2 gate, which indicates diminished charge trapping at the P(VDF-TrFE-CFE)/PbS interface with respect to SiO_2/PbS.

Electron and hole mobility values extracted from the transfer curves are a fundamental figure-of-merit that can be used to compare the charge transport properties in the film with the two different interfaces – SiO_2/PbS and PbS/P(VDF-TrFE-CFE). The electron mobility is for SiO_2 gate $\mu_e = 0.5$ cm^2 V^{-1} s^{-1} and for the P(VDF-TrFE-CFE) gate $\mu_e = 1.1$ cm^2 V^{-1} s^{-1}. On the other hand, the hole mobility is $\mu_h = 2 \times 10^{-3}$ cm^2 V^{-1} s^{-1} and $\mu_h = 6 \times 10^{-3}$ cm^2 V^{-1} s^{-1} for SiO_2 gate and for the P(VDF-TrFE-CFE) gate, respectively. A limited dependence of the mobility values on the source-drain voltage for the P(VDF-TrFE-CFE) gate operation was observed (see Figure S6, Supporting Information). This limited dependency indicates the PbS/P(VDF-TrFE-CFE) interface favors the charge transport more than SiO_2/PbS interface because of reduced charge trapping, in addition to the much better charge carrier injection due to the staggered bottom-contact top-gate configuration that tends to give lower contact resistance than the coplanar bottom-contact bottom-gate configuration.

Multiple gate devices are considered to represent the future in the development of field-effect transistors because they can enhance the performance of the devices and extend the validity of Moore's law for another 20 years.[42] Multiple gate devices may eventually provide solutions to such fundamental problems as drain-induced barrier lowering and short channel effects. Additionally, they may help improving practical aspects such as lowering the operating power and the stand-by power, as well as enhancing possibilities for circuit design.[43]

Although it represents an opportunity to increase the tuneability of the functioning of the transistor, the simultaneous biasing of the two gates, or double gating, has not yet been reported for any colloidal quantum dot FET. Double gating can also allow shifting the off state of the device and the threshold voltage into the desired position and inducing more charges in the channel, thus increasing the drain current. As previously mentioned, we limited the thickness of the active material to 20 nm in order to induce a single channel that can be controlled simultaneously by the two gates; alternatively, in a thick film, two channels at the dielectric interface could be formed. In a single channel, delocalized over the whole thickness of the film, we expect the influence of the second gate bias should consist of a shift of the transfer characteristics without changing the off-current of the device.

The results of double gate FET measurements are reported in **Figure 4**. The transfer characteristics are obtained by sweeping the voltage of the SiO_2 gate (Figure 4a) and of the P(VDF-TrFE-CFE) gate (Figure 4b), and are shifted by applying a bias to the opposite gate. The behavior of the transfer characteristics with its rigid shift is a strong indication that the device is operating in single channel regime delocalized over the 20-nm thickness of the film. In most of the curves, the off-current remains lower than 1 nA; however, for negative voltage value higher than −0.5 V applied to P(VDF-TrFE-CFE) gate (Figure 4a), the off-current increases. This indicates a formation of parasitic hole inversion near the polymer gate, which screens the influence of the SiO_2 gate on the channel and prevents the device to be switched into a proper off-state.[44] The same parasitic hole inversion is observed in Figure 4b, also for voltage values on the SiO_2 gate lower than −30 V. The signs of parasitic electron inversion are more evident in the transfer curves measured sweeping the voltage of the polymer gate with positively biased SiO_2 gate ($V_{G,SiO2} > 0$ V).

Figure 4a shows that applying a voltage bias to the polymer gate shifts the threshold voltage for $\Delta V_{G,SiO2} = 7.0$ V for each $\Delta V_{G,P} = 0.5$ V applied. The double gate measurements for reversed gating in Figure 4b show that the voltage bias on the SiO_2 gate shift the threshold voltage of $\Delta V_{G,P} = 0.63$ V for each $\Delta V_{G,SiO2} = 10$ V. The ratio of the voltages $\Delta V_{G,SiO2}$: $\Delta V_{G,P}$ are 15.9 and 14.0 for the SiO_2 gate biasing and the polymer gate biasing, respectively. These ratios should be equal, since the shift of the Fermi level induced by either of the gates should be compensated by the other gate, or equivalently from: $\Delta V_{G,SiO2} \cdot C_{G,SiO2} = \Delta V_{G,P} \cdot C_{G,P}$, the ratio of the voltages should be equal to the inverted ratio of the respective capacitances of the gates. However, the ratio of the material capacitances of the polymer and the SiO_2 gate is 12, which implies that the polymer gate induces more charge carriers in the channel than it should, based on its calculated capacitance using the dimensions of the dielectric layer in the device. The origin of this mismatch is to be found in the asymmetrical position of the source and drain electrodes with respect to the top and bottom gates in the vertical plane (Figure 2d). The top (polymer) gate induces charges in the area of the active layer located above the electrodes in addition to the channel area that is also available for the carrier induction for the bottom (SiO_2) gate. Considering that the width of the electrodes in the interdigitated pattern is the same (20 µm) than the channel length, this makes the effective channel length for the polymer gating ≈15%–30% higher than for the SiO_2 gate. This underestimation of the channel length for the polymer gate should cause the same underestimation of the charge carrier mobility.

The transfer characteristics measured for gates tied together in comparison with single gate characteristics are reported in

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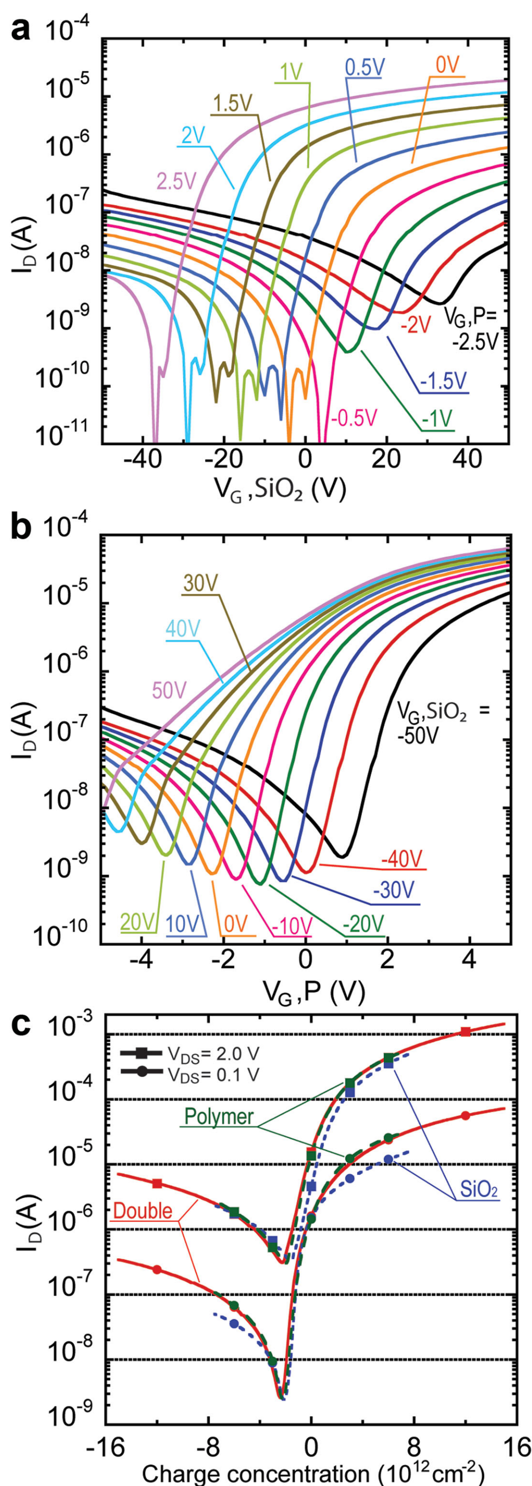

Figure 4. a) Double gate transfer characteristics measured with the indicated bias steps on the P(VDF-TrFE-CFE) gate and sweeping the voltage on the SiO_2 gate. b) Double gate transfer characteristics measured with the indicated bias steps on the SiO_2 gate and sweeping the voltage on the P(VDF-TrFE-CFE) gate. V_{DS} is kept constant at 0.1 V. Only the forward hysteresis branch is plotted. c) Transfer characteristics are plotted versus induced charge concentration measured for the P(VDF-TrFE-CFE) gate, the SiO_2 gate and the two gates working simultaneously. The reverse hysteresis branch is plotted.

Figure 4c. The characteristics are plotted versus the induced charge concentration; this is done for a better representation, since the gates have different capacitance and require different operating voltages. The reverse hysteresis branch is plotted in order to minimize the influence of charge trapping. The single gate characteristics were measured by sweeping the voltage on either of the two gates in a range chosen to induce the same charge carrier concentration at the boundaries. For the polymer gate, the interval is –5 to +5 V and –80 to +80 V for the SiO_2 gate. The values for the SiO_2 gate were obtained by multiplying the corresponding values taken for the polymer gate by the averaged ratio $\Delta V_{G,SiO2}$:$\Delta V_{G,P}$ previously extracted from the double gate measurements (16 for the particular device reported on Figure 4c). The double gate sweep characteristics were measured by sweeping the voltage simultaneously on the two gates: $V_{G,P}$ = –5 V to +5 V and $V_{G,SiO2} = V_{G,P} \cdot 16$. Under double gate sweep, the on-current in the device increases as a consequence of the increased total induced charge carrier concentration in the film. The twofold increase of the induced charge concentration achieved by double gating in comparison with single polymer gating (from 7.5×10^{12} cm^{-2} up to 15×10^{12} cm^{-2}) leads to slightly more than a twofold increase of the current in the device (from 32 µA to 72 µA for V_{DS} = 0.1 V and from 0.6 mA to 1.4 mA for V_{DS} = 2 V). For low source-drain bias, the current in the linear regime achieved by SiO_2 gating is different from double gate sweep and from polymer gating—as explained above—because of the asymmetrical location of the electrodes. The injection process for a channel induced by silicon dioxide gate is less efficient than for a channel induced by polymer gate, leading to a reduction of the current. For higher source-drain voltages, the injection problems are less noticeable and the transfer curves plotted versus charge concentration nearly coincide, regardless of which gate is used for the induction.

3. Conclusions

Our work introduces colloidal quantum dots double gate transistors. We utilized a high-k (k = 43) relaxor ferroelectric polymer as a dielectric material for the top gate in a device where the other gate is obtained with SiO_2. The device in double gate configuration is characterized by reduced hysteresis in the transfer curves measured by separately sweeping the voltage of the SiO_2 and of the polymer gate. Gating with the relaxor polymer led to mobility values of μ_e = 1.1 cm^2 V^{-1} s^{-1} and $\mu_h = 6 \times 10^{-3}$ cm^2 V^{-1} s^{-1} that exceed those extracted from the SiO_2 gating: μ_e = 0.5 cm^2 V^{-1} s^{-1} and $\mu_h = 2 \times 10^{-3}$ cm^2 V^{-1} s^{-1}. The source-drain voltage required to pinch off the channel was reduced in the double gate device in comparison with single gate because of the high capacitive top gate that pinches off the channel more effectively than the SiO_2 gate.

Measurements under double gating conditions proved that the device works in a single channel mode that is delocalized over the whole film thickness. Double gating allows for shifting the threshold voltage into a desired position and allows as well increasing the on-current of the devices. Therefore, CQDs can be ranked among materials compatible with all solution-processable multiple gate technology.

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4. Experimental Section

PbS QD Synthesis: PbS quantum dots were prepared according to synthetic method described by Hines et al.,[45] with slight modifications. Lead acetate [$Pb(OAc)_2 \times 3H_2O$, 1.5 g, 4 mmol], octadecene (50 mL), and oleic acid (4.5 mL, 14 mmol) were dried at 120 °C under vacuum conditions for 1 h. The heating mantle was removed and the flask was set under N_2 atmosphere before swiftly injecting bis(trimethylsilyl) sulfide [$(TMS)_2S$, 420 µL in 10 mL octadecene]. After 3 min, fast cooling to room temperature quenched the reaction. As a product, nanocrystals with the diameter of 3.15 nm were obtained displaying an absorption peak at 965 nm. The QDs were purified three times with hexane/ethanol and once with chloroform/methanol as solvent/nonsolvent systems.

Fabrication of PbS QD FET on Silicon Oxide Gate: PbS quantum dot field-effect transistors with SiO_2 gate (Figure 1a) were fabricated on top of a n-doped silicon substrate with 230 nm thermally deposited oxide layer and lithographically patterned interdigitated Au electrodes. A standard procedure to clean SiO_2 surface was followed, using acetone, isopropanol, and plasma treatment. After cleaning, the substrates were transferred into a N_2 filled glovebox, where the active layer was deposited. The "scaffold" layer was spin-coated at 4000 rpm from 2.5 mg mL^{-1} solution of OA-capped PbS quantum dots in chloroform. The ligand exchange was done from 1% EDT solution in acetonitrile with subsequent washing of the film with 5–8 droplets of acetonitrile dripped on the rotating substrate. After each spin-coating step and ligand exchange step, the substrate was dried for 20 s at 100 °C on a hotplate to dry the solvent. The next "filler" layer of PbS was spin-coated from 10 mg mL^{-1} solution at 1000 rpm. The total thickness of the film was 20 nm. After spin-coating, the devices were annealed for 25 min at 140 °C to remove solvents and improve the ligand-QDs binding.

Fabrication of P(VDF-TrFE-CFE) Gate: P(VDF-TrFE-CFE) terpolymer was dissolved in cyclohexanone at 50 mg mL^{-1} concentration and stirred at 60° for a few hours. Before spin-coating, the solution was filtered through 0.45 µm filter. A 200-nm thick film was deposited by spin-coating at 1200 rpm and then annealed at 100° for 60 min. The gate electrode was deposited by vacuum evaporation of 100 nm of aluminum through a shadow mask.

FET Measurements: Transistor measurements were done in a probe-station in a nitrogen glovebox. All electrical measurements were performed with a Keithley semiconductor characterization system 4200-SCS.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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