Application of a Test Structure for Minimising Seed Layer Thickness of Electroplated Ferromagnetic Films

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***Abstract*—This paper presents a previously documented full wafer test structure, designed to quantify the effect of seed layer thickness and conductivity on the plating uniformity of patterned electroplated structures. With magnetic films, non-magnetic seed layers need to be as thin as possible to minimise unwanted eddy currents. This paper uses the test structure to quantify the IR drop on the electroplated film and demonstrates how current distribution structures can be simply used to significantly improve wafer plating uniformity when using seed layer thicknesses of a few nanometers.**

I. Introduction

The electroplating method is perhaps the most widespread technique in microelectronics and microsystems fabrication for the production of thick (tens of μm) metallic films e.g. Cu and NiFe. This paper uses a previously reported test structure [1] to quantify the IR drop across a wafer when electroplating on seed layers with a thickness of a few nanometres. More importantly, it demonstrates how IR drops resulting from thin seed layers can be significantly reduced by using dummy structures as current shunts on the mask layout.

II. Background

The electroplating process typically involves the blanket deposition of a seed layer, upon which photoresist is coated and patterned to define a mould for the subsequent bottom-up plating process [2], as shown in Figure 1.

Once the electroplating has been completed, the photoresist is stripped, followed by the removal of the now exposed seed layer, which was electrically connecting all of the electroplated metal structures. This latter step is routinely performed using a wet-etch dip process. In many cases the seed and electroplated film are the same metal and care is needed with dimensional control. Clearly a more ideal situation is to use a seed layer with a good etch selectivity with respect to the electroplated film [1] to minimise any undercut and preserve the dimensions of the electroplated film. At the same time, for structures with

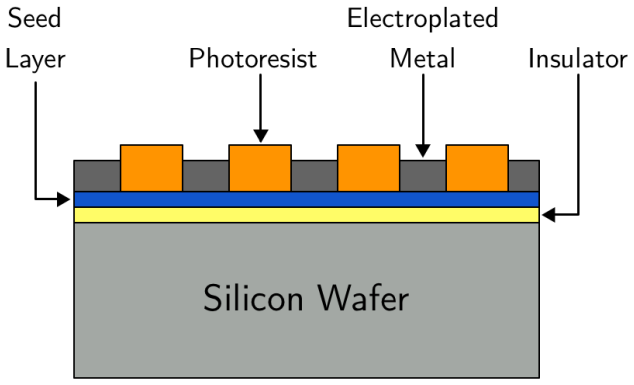

Fig. 1. Bottom up plating using a photoresist mask [1] (note. thicknesses not to scale).

dimensions approaching the seed thickness any undercut can result in the structure being released. Hence, in this situation there is a real need to minimise seed layer thickness while also minimising IR voltage drop.

For conducting films, e.g. Cu, the electrical characteristics of the seed layer under the electroplated film are not of key importance. For example, a thin Ti adhesion layer under Cu actually marginally reduces track resitivity. This is not the case for magnetic films. In this case there are conflicting requirements; the seed layer should have a high conductivity, to minimise IR drop during plating, but a very high resistivity, to minimise eddy current losses.

For magnetic films, the performance requirements dictate seed layer (e.g. Cu, Al) thickness to be as small as possible to minimise the conductivity of the seed layer during device operation. Clearly the increase in IR drop can be countered by using additional higher conductive tracks strategically placed to help distribute the plating current.

Typically, electroplating systems are set up to deliver uni-

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form blanket depositions, which minimises any non-uniformity related to current crowding resulting from the pattern. In this regime any IR drop across the wafer is rapidly reduced as the plating proceeds to increase the effective thickness of the seed layer, and will have a negligible effect on uniformity and final thickness of the deposited films. However, for bottom-up plating this is not the case as the seed layer between structures remains a high resistance path leading to high IR drops. With current flow being pattern dependent this presents a challenge when developing generic layouts for setting up plating systems.

Figure 2 shows the mask layout of the test structure, which has been designed with radial symmetry. It is also designed so that the resistance between any two adjacent electrodes will be the same for uniformly deposited films. The semi-automated design software is detailed in reference [1].

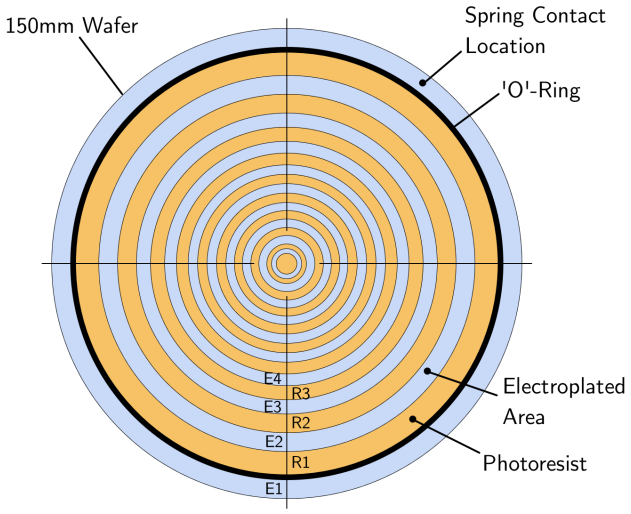


Fig. 2. Mask layout for the electroplating of the 150 mm wafer showing the position of the O-ring and jig contacts [1].

III. Assumptions

Extracting quantitative information from the proposed test structure makes the following assumptions

1) The seed layer is uniform.
2) The electrode connecting the outer electrode to the wafer jig is thick enough to ensure all the outer electrode ring is at the same potential.
3) There is good contact in the wafer jig.
4) Current flow is radial.
5) The resistance of each seed layer ring is identical.
6) The seed layer sheet resistance is $\gg$ than the electroplated layer.

Most of these conditions are met by the mask design and uniformity deposition issues will be discussed in the measurement section.

IV. Fabrication

Fabrication of the test structures used standard processes for depositing the adhesion and seed layers, and defining the area for electroplating. There are many options for improving the thickness/conductivity of the outer electrode. Ideally it would be good to use a conductor that is not attacked by the electrolyte so O-ring leakage on the wafer holder is less of an issue. In this paper e-beam evaporated Al was used in conjunction with a simple shadow mask. The same e-beam evaporation system was also used to deposit the adhesion and seed layers.

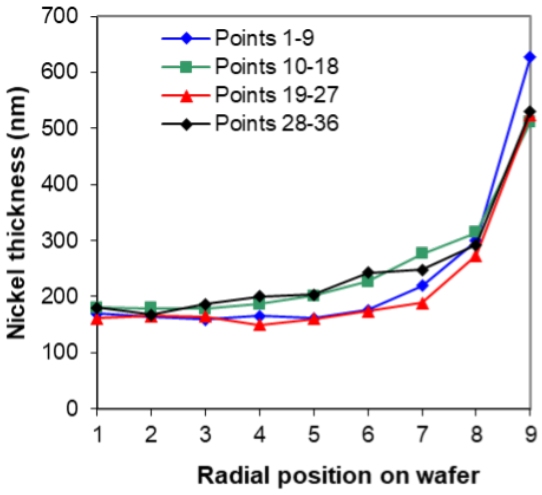
V. Measurements

Figure 3 shows results from [1] of the measured radial thickness of the Ni electroplated electrodes on three different thicknesses of Al/Ni seed layers with a total plating current of 0.65 mA (Note: a single power supply was used, with the wafer and thief currents [3] being individually recorded). Figure 4 shows this setup.

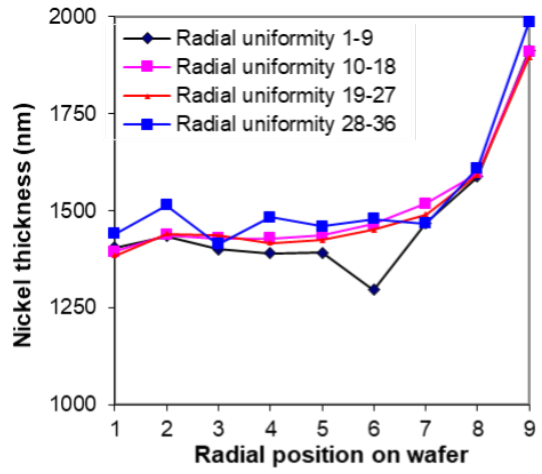
The thickness measurements were made on the nine electroplated rings starting from the centre of the wafer (1) out to the edge (9). These results indicated that it is feasible to electroplate on patterned moulds using very thin seed layers. However, it should be noted that the thickness (conductivity) of the seed layers significantly affects the plating rates and radial uniformity, especially for the 5/5 nm (Al/Ni) seed layer combination [1].

Assuming electroplating is 100% efficient, the test structure enables the IR drop of the seed layer rings to be calculated knowing the total electroplating current, and the thickness and area of each of the metal rings being plated. Figure 5 shows the calculated IR drops for the 5/5 nm wafer and it can be observed that the voltage drop reduces towards the centre of the wafer as the electroplating current reduces. Note that the numbering of the electrodes and resistors in this graph and in Fig. 2 is reversed compared to the numbering of the thickness measurements. This extraction of IR assumes the electrodes being plated are much more conductive than the seed layer and the resistance between any two electrodes is independent of position of the probes on the electrodes. For the measurements in Figure 3 it can be observed this is not the case and is only an approximation. This result was caused by uneven contact to the outer electrode, the O-ring leaking electrolyte which attacks the electrode, and known non-uniform deposition of the e-beam seed layer. Addressing seed layer non-uniformity requires access to a more modern sputter tool or an atomic layer deposition system.

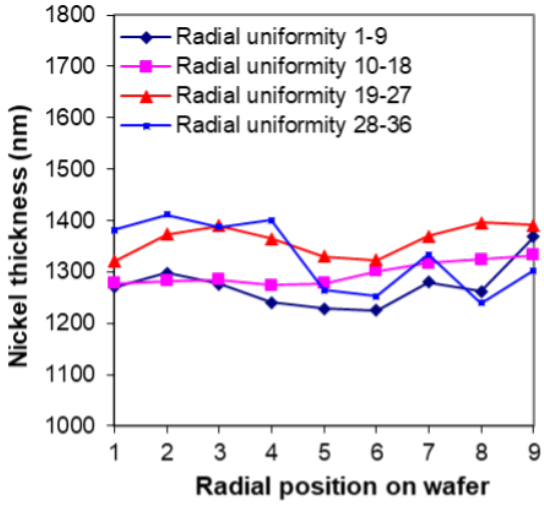
The test structure provides the opportunity to more quantitatively investigate the effect of adding current shunts to distribute current to reduce wafer IR voltage drops. Figure 6 shows a simple cross design with Figure 7 presenting the deposited thickness measurements along the horizontal and vertical radii. The improvement over the same measurement without the shunts is self-evident. Additional investigation is required to fully determine the reason for the variation in the trend of the thickness at different positions on the wafer.



(a)



(b)



(c)

Fig. 3. Radial uniformity measurements for different seed layers (1-9 centre-east, 10-18 centre-west, 19-17 centre-south, 28-36 centre-north). (a) 5 nm Al / 5 nm Ni, 0.068 A (b) for 10 nm Al / 10 nm Ni 0.212 A, (c) 50 nm Al / 50 nm Ni, 0.155 A.

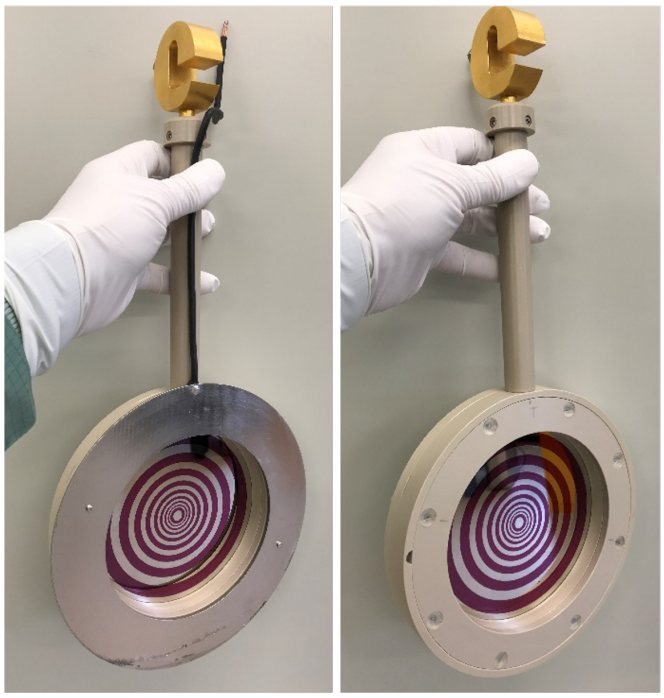


Fig. 4. Wafer plating jigs, with (left) and without (right) a current thief [1]

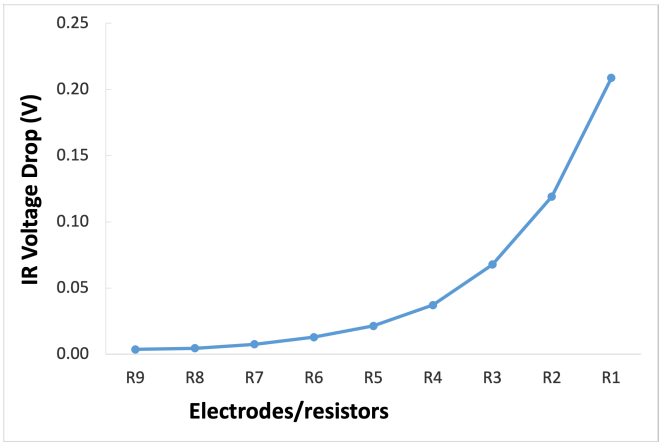


Fig. 5. IR drop on 150mm wafer (5nm Al / 5nm Ni seed)

VI. Discussion and Conclusions

A test structure has been presented, which has been specifically designed to quantify the IR drop across a wafer during electroplating in a more product independent manner.

It has been demonstrated how this test structure can be used to evaluate the concept of dummy structures or current shunts and their effectiveness in the distribution of currents for thin seed layers with sparse plating areas. The use of such dummy structures to enable uniform plating of such sparce patterns with thin seed layers is of particular importance with magnetic films and the need to minimise eddy currents. What is clear is that the deposited film in the reported results is non-uniform, in spite of which, this test structure still provides an excellent vehicle to investigate the effectiveness

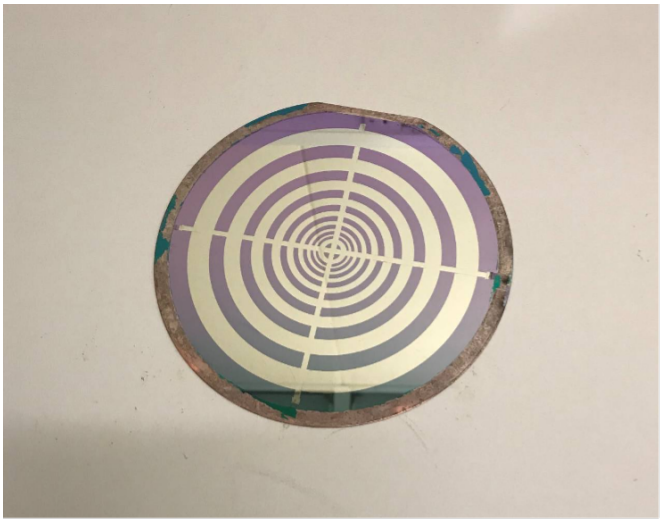


Fig. 6. 150 mm wafer with dummy current structures (5nm Al / 5nm Ni seed).

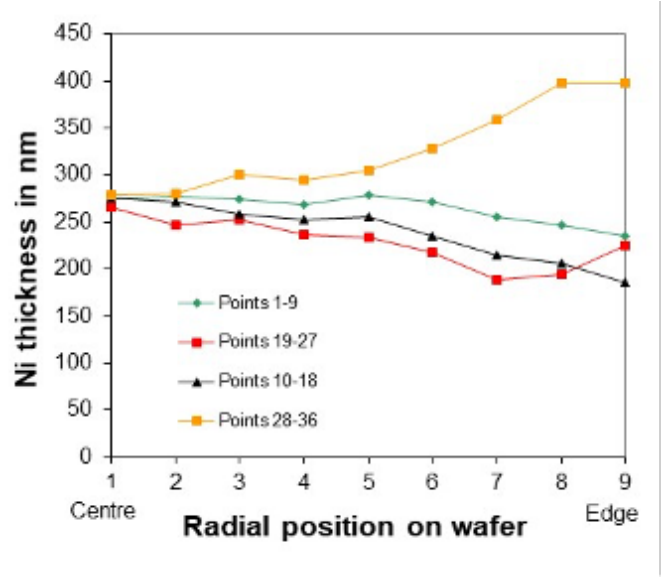


Fig. 7. Uniformity of deposition on 150 mm wafer with dummy current structures

of current shunts to reduce radial electroplating related non-uniformities. It confirms that 10 nm seed layers can be used for electroplating magnetic films with significantly lower eddy current losses.

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