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Resolution enhancement of VCO-based ADCs by passive interpolation and phase injection

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***Abstract*—This work describes a simple way to improve the resolution of low-pass voltage-controlled-oscillators based analog-to-digital converters (VCO-based ADCs) implemented with ring-oscillators. We propose to insert a passive resistive network into the differential delay cells of the oscillator to get additional interpolated phases. These interpolated phases are then injected to other similar oscillators. By increasing the number of phases coming from all the oscillators, the effective gain of the system is higher resulting in a resolution enhancement of the converter. To validate the idea, a prototype of an open-loop VCO-based ADC was built in VerilogA language with the ring-oscillators designed making use of a 65-nm CMOS process. The results of transient simulations were compared to the results of a behavioral ideal model of the system built in MATLAB to verify the correct performance. As expected, the SNR was improved in concordance with the expected increase in the number of phases. Finally, it was checked that the proposed circuit used to extract and inject the interpolated phases did not penalize the total power consumption. The proposed circuit structure is particularly suitable for high-bandwidth applications, where the oversampling ratio (OSR) is strongly restricted and the gain cannot be increased to the full-scale range due to non-linearity issues. Due to the highly digital nature of the VCO-based ADC structures, this solution may be of special interest to be implemented in new deep-submicron CMOS processes.**

I. Introduction

Nowadays, the development of deep-submicron CMOS processes has supposed the reduction of the voltage supply and the length of the transistors used to design circuits. This has lead to systems with lower power consumption, lower occupied area and higher speed. Whereas digital circuits specially benefit from the features of these new processes, the design of analog circuits may turn out to be challenging. Devices in narrow processes lack enough intrinsic gain and their performance is strongly affected by non-idealities, such as mismatch, leakage current, or channel-length modulation [1]. Consequently, the current trend is towards highly digital designs, more suitable for the new processes.

Within this trend, voltage-controlled-oscillators based analog-to-digital converters (VCO-based ADCs) have become of great interest for the designer community. On the one hand, VCO-based ADCs can be implemented with mostly digital circuits, specially if we talk about ring-oscillators based ADCs [2], [3]. On the other hand, the output digital signal is intrinsically first-order noise-shaped, making their performance similar to $\Delta\Sigma$ modulators but with more simple architectures [4].

If we focus on open-loop VCO-based ADC structures with ring-oscillators, the main impairment will be the non-linear voltage-to-frequency response of the oscillator. This relation strongly limits the resolution we may get from the whole converter [2]. Several ways of correcting the oscillator non-linearity have been proposed in the literature. Firstly, we may make use of digital calibration [3], [5], but higher power consumption and higher area are required for calibration circuits. Secondly, we may think of a VCO-based $\Delta\Sigma$ loop [6], where the non-linearity is corrected by the gain of the loop. Here the limitation is the requirement of analog circuits and the partial loss of the digital nature of the VCO-based solution. Recently some of the proposals are headed towards limiting the amplitude of the VCO input signal somehow [7], [8]. If our input signal is of low amplitude, we can approximate better the working region to a linear response, resulting in less harmonic components power. Nevertheless, if the input signal amplitude is limited, the oscillator gain will be limited as well. According to [4], the resolution of an open-loop VCO-based ADC depends on the oscillator gain. Consequently, the final resolution of the converter will be restricted, limiting this solution to low and medium oversampling ratio (OSR) applications.

In this manuscript, we propose a simple and passive way of overcoming the gain limitation by increasing the number of phases in a ring-oscillator. This way, the limitation due to restricted gain is compensated with a higher number of bits in the converter that boosts the resolution. The proposed solution allows us to get a time resolution even higher than the nominal time delay of an inverter in a narrow CMOS process, which makes our proposal especially suitable for high-bandwidth applications.

The outline of the manuscript is as follows. Section II describes the conventional architecture of an open-loop VCO-based configuration and the limitations introduced above. Section III proposes the new interpolated VCO-based architecture with no limitation in the number of phases. Section IV validates the approach through behavioral simulations with ring-oscillator designs in a 65-nm CMOS process. Finally, Section V concludes the manuscript.

II. Conventional open-loop VCO-based ADC architecture

The conventional open-loop configuration of a VCO-based ADC architecture is depicted in Fig.1. It is composed of a VCO (in this case a M-phase ring-oscillator) followed by two flip-flops in cascade and a XOR gate that make the sampling and the first difference in the discrete domain. The digital output $y[n]$ is first-order noise shaped. As can be observed this

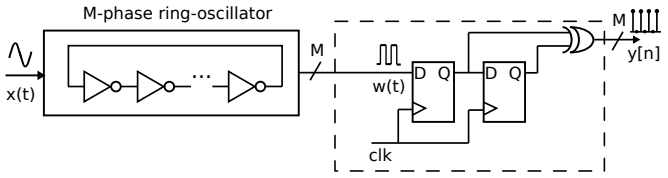

Fig. 1. Conventional open-loop VCO-based ADC architecture.

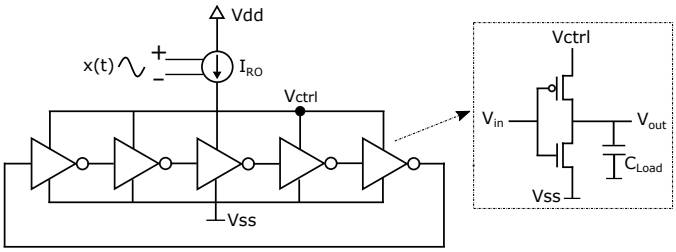

Fig. 2. Single-ended configuration of a ring-oscillator.

implementation takes advantage of the properties of narrow design processes due to its highly digital nature.

The oscillation frequency of the ring-oscillator ($f_{\text{osc}}(t)$) can be expressed as follows:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot x(t) \quad x(t) \in [-1, 1], \tag{1}$$

where f_{o} is the rest oscillation frequency and K_{VCO} is the gain of the oscillator. The input signal $x(t)$ is assumed to be dimensionless with values between -1 and 1. Ideally with linear oscillators the gain oscillator K_{VCO} establishes the final resolution of the converter [4].

The VCO implementation typically used to seize the advantages of narrow design processes is the ring-oscillator configuration, because of its digital implementation based on conventional CMOS inverters. Fig. 2 shows an example of a ring-oscillator circuit. The inverters are connected in a ring configuration and the input signal is connected to a voltage-controlled current source. The proportional current gets into the inverters modulating their time delay. The result is an oscillation frequency that ideally follows (1). Nevertheless, as stated in as stated in [9], this structure offers an intrinsic non-linear voltage-to-frequency relation due to the non-linear time dependent delay of the inverters. Consequently, distortion will be observed at the output spectrum and the final resolution will be restricted.

To compensate for this non-linearity effect, a low-amplitude input signal may be introduced into the ring-oscillator to make the oscillator work in a more linear range than when working in the whole range of oscillation [7]. Although this solution works nice for some applications, such as either audio or sensor applications [8], it strongly limits the oscillator gain and restricts the resolution we may get from the converter for high-bandwidth applications (tens of MHz). Looking at this last type of applications, there are two possible solutions to overcome the lack of gain. Firstly, we may think of increasing

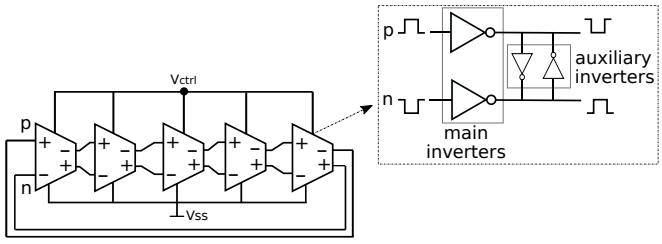

Fig. 3. Differential delay cell of a ring-oscillator.

the OSR. However, the highest sampling frequency we may achieve with proper jitter power is currently in the order of a few GHz. Therefore, we cannot increase the OSR indefinitely. Secondly, we may design a ring-oscillator with several phases to increase the number of bits at the output. Assuming that we make use of the fastest inverters available in the process, the higher the number of phases in the ring oscillator, the lower the oscillation frequency. Consequently, we will not improve the resolution.

To deal with this issue we propose a novel, simple and passive way of increasing the number of phases of a ring-oscillator at the same time that its oscillation parameters remain. The proposed solution does not depend on the time delayed by each tap in the ring-oscillator, so it applies even when we design a ring-oscillator with the fastest oscillation frequency possible. Additionally, we will see that the resulting system keeps working in the same linear range of frequency, but with more phases.

III. Proposed circuit to increase the number of phases in a VCO-based ADC

A differential circuit for a multi-phase ring-oscillator based VCO is shown in Fig. 3. Each delay element consists of two main inverters and two cross-coupled auxiliary inverters. This differential configuration composed of four inverters is widely used to design ring-oscillators with high common noise rejection ratio (CMRR) [8]. We will tap this circuit structure to interpolate phases from a master ring-oscillator and inject them into several slave ring-oscillators.

To interpolate two phases we can place a couple of resistors connected in series between consecutive opposite phases. Ideally the higher the number of resistors connected in cascade, the higher the interpolated phases we can get. However, the number of interpolated phases is limited in practice due to the thermal noise current of the resistors. In Fig. 4a the proposed circuit for the case of two resistors is depicted. As can be observed, the new interpolated phase is in-between the two original phases. Then, this additional phase could be injected into another identical oscillator (with the same number of taps and the same delay cell circuit) to double the number of phases but guaranteeing the same oscillation parameters in both the master and the slave ring-oscillators.

This interpolation technique allows us to theoretically double the number of phases and the amount of sampled edges

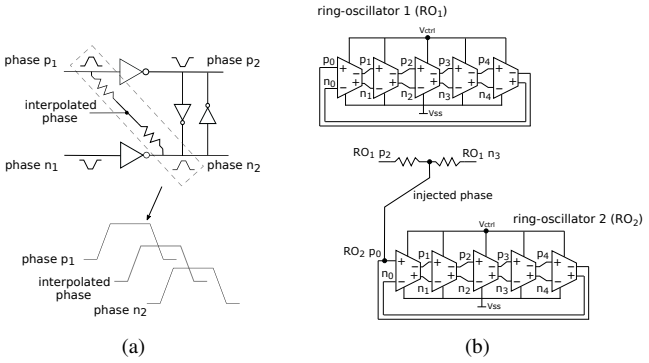

Fig. 4. (a) Resistive network and (b) phase injection connection.

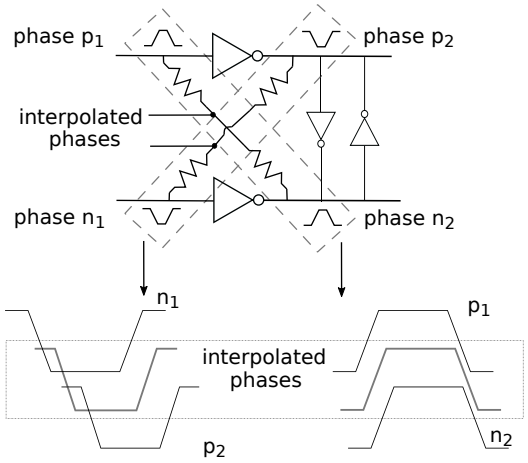

Fig. 5. Dual resistive network connection in a differential delay element.

in a certain period of time. According to [4] this is equivalent to increasing the efficient oscillation frequency by twice. In consequence, the signal-to-noise ratio will be improved in 6 dB. Notice that this statement is only true while we have no overlapping between the phases. By selecting a proper resistance value to obtain the edge of the interpolated phase exactly in the middle of the original phases, we ensure to get a proper improvement in the final resolution. Additionally, to subtract common noise from the phases we can benefit from the differential configuration shown in Fig. 3 making use of two resistive networks as shown in Fig. 5. This configuration also helps match the load in both branches of each tap and contribute to align the edges of both interpolated phases.

Keeping this configuration in mind, we can expand the proposal to more than two resistors as stated above. In Fig. 6 four resistors were placed in the resistive network to obtain three additional phases that can be used to inject three interpolated phases into three different slave ring-oscillators. In this case, as we have increased the number of phases by four, the expected improvement for the SNR equals 12 dB.

In [10] an alternative circuit to speed up the oscillation frequency of ring oscillators-based VCOs was published. The proposed solution consists of modifying the connections of the inverters that compose the oscillator. The circuit is based on a differential delay cell as Fig. 3 to design a ring oscillator, using the auxiliary inverters to make feed-forward connections and couple the different phases in the same oscillator. This way higher oscillation frequency is achieved because the state change of one single inverter does not only depend on the immediate previous inverter, but on several previous inverters. The advantage of our solution is a more simple layout design with the chance of just replicating the ring-oscillator design as many times as required. The disadvantage is a higher occupied area.

IV. Practical implementation

To validate the correct performance of the proposed circuit we designed a prototype in a pseudo-differential configuration with the architecture of Fig. 1. A 9-stage differential ring-oscillator was implemented in a 65-nm CMOS process, keeping the rest of the blocks modeled with VerilogA language. Transient simulations were performed for three systems: a system with a single 9-stage ring-oscillator, another system with two 9-stage ring-oscillators (one master oscillator and one slave oscillator), and the third one with four 9-stage ring-oscillators (one master oscillator and three slave oscillators).

To observe the behavior of this technique, we compared the simulation results from a behavioral ideal model in MATLAB and the corresponding designs at 65-nm. Fig. 7 depicts the output spectrum of the output digital signal $y[n]$ (Fig. 1) for each of the simulated cases (2^{12} samples were used to calculate the spectra). The oscillation parameters were $f_{\mathrm{o}} = 540$ MHz and $K_{\mathrm{VCO}} = 410$ MHz, for a sinusoidal input signal of 0 dBFS at a frequency of 10 MHz. The nominal supply voltage is 1 V. The sampling frequency equals 1 GHz and the band of interest equals 50 MHz.

The resulting SNR for the three systems were 57 dB, 63 dB and 67 dB respectively (the HD3 term was 41 dB). Regardless of VCO's non-linearity effect that strongly degrades the resolution, the SNR is enhanced in steps of 5 dB (average value) when going from Fig. 7a to Fig. 7b and going from Fig. 7b to Fig. 7c. The simulations made with the ideal model of MATLAB provided values of SNR equal to 59 dB, 64 dB, and 68 dB for cases a, b and c respectively. Due to the long time required for transient simulations at 65-nm, we were not able to average several input signal phases to get more accurate values that better match with the MATLAB results. Despite this, we get a proper resolution enhancement when making use of the proposed interpolation-injection circuit. Considering the difference of load of the inverters involved in the interpolation with respect to the others, we did not observed any impairment. The resistance chosen for the resistive network equals 10kΩ, which implies a very low current going through it.

Additionally, looking at the spectra of Fig. 7 it can be observed that the distortion power remains for the three cases as expected. This means that for any application we can firstly reduce the input amplitude signal until the distortion is not longer a restriction and secondly, increase the number of phases to get a proper level of quantization noise. This feature

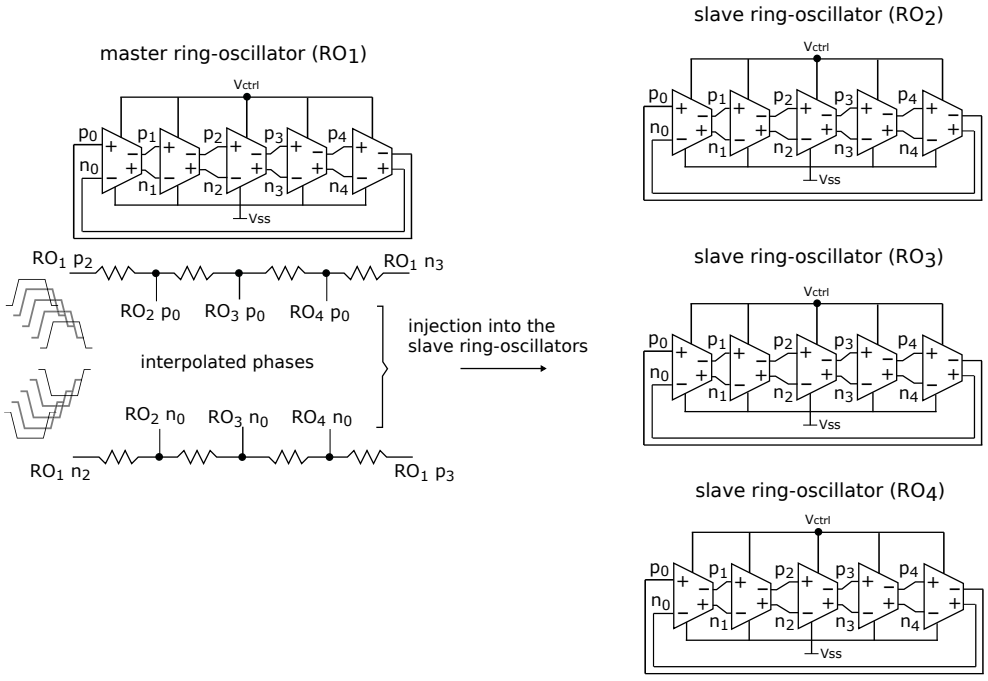

Fig. 6. Proposed system with one master ring-oscillator and three slave ring-oscillators.

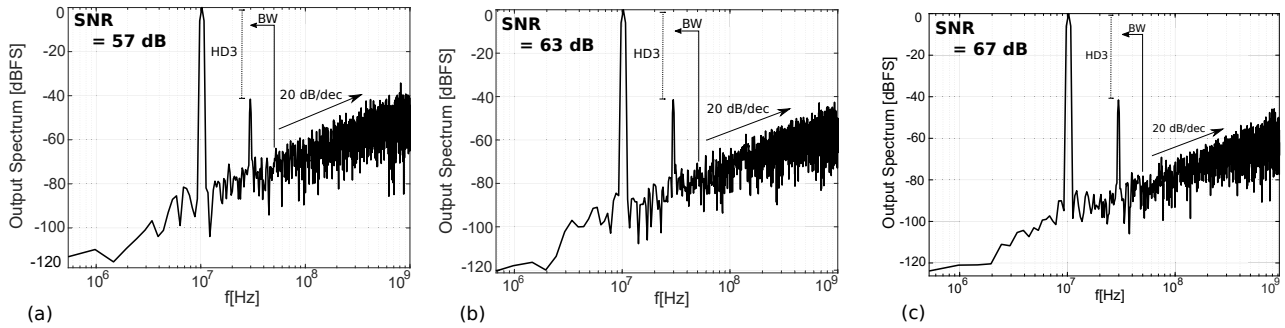

Fig. 7. Output spectrum of three cases: (a) one single ring-oscillator, (b) one master ring-oscillator and one slave ring-oscillator, and (c) one master ring-oscillator and three slave ring-oscillators.

makes this solution especially suitable for high-bandwidth applications, such as communication or IoT applications.

Finally, a case study of the power consumption was made for the ring-oscillators implemented in a 65-nm CMOS process. We estimated the power consumption of the oscillators for the three systems shown in Fig. 7, being the same for all the oscillators, 133 μW. This means that the resistive passive networks used for the phase interpolation and injection does not suppose a power consumption penalty. Therefore, the total power will only depend on the number of ring-oscillators added to the system.

V. Conclusion

We propose a simple passive circuit which allows us to increase the number of phases of a VCO-based ADC without modifying the oscillation parameters. Our circuit is based on inserting a resistive passive network between two consecutive phases of a differential ring-oscillator to get interpolated phases. These additional signals are injected into other similar ring-oscillators to rise up the equivalent K_{VCO} and increase the final resolution we may get from the converter. The proposed circuit is explained theoretically and validated through simulations of practical designs making use of a 65-nm CMOS process. The idea was tested with open-loop VCO-based configurations, but it could be expanded to closed-loop configurations as well. The results show the correct performance of the circuit, being very suitable specially for high-bandwidth applications, such as communication devices, implemented with new deep-submicron CMOS processes.

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