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Undergraduate Curriculum to Teach and Provide Research Skills on Hardware Design for SDR Applications in FPGA Technology

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ABSTRACT Software Defined Radio (SDR) technologies play today an important role in modern wireless networks due to their flexibility to implement re-configurable hardware designs. In light of the importance to operate and develop such technologies, academic programs in the communications engineering field demand an introduction to Digital Signal Processing (DSP) and SDR communication schemes accordingly. Typically, the teaching of this subject is afforded through projects and hands-on activities in classrooms. However, provided their relevance in the current state-of-the-art, this topic also provides a framework to teach soft skills concerning research abilities in students. This paper introduces an academic program to the development of SDR functionality as well as research skills based on exposure to state-of-the-art research. Through projects, hands-on activities are conducted to teach digital signal processing designs using Field Programmable Gate Array (FPGA) technology. The course aims to develop technical skills to implement communication system blocks. Besides, workshops and seminars are prepared to support the development of research and communication skills. The proposed course is flexible to incorporate on a given academic program as an elective subject to further support topics related to communication theory and discrete-time signals. Learning outcomes are designed to develop enhanced technical skills in SDR design and simultaneously a critical discussion of the devised solutions in light of the state-of-the-art. Also, skills related to identifying, formulating, and discussing engineering problems are further reinforced. Results from supported projects developed in the classroom exhibit completed assignments superior to 90% of participant students. Learning objectives concerning the technical skills were successfully covered (90%) in comparison to research and communicating skills (80%). Additionally, research skills and the ability to disseminate knowledge gradually improved in seminars. Finally, results of the current course exhibit improvements of 25% regarding the acquired skills in digital signal processing in comparison to previous courses.

INDEX TERMS Communication engineering education, communications technology, project-based learning, from research to practice, soft skills.

I. INTRODUCTION

Since its first definition provided by Mitola [1], nowadays Cognitive Radio (CR) has emerged on the current development of fifth generation of mobile communications (5G) networks [2] to deal with the increasing number of configuration parameters [3]. To handle their implementation, SDR devices are conceived to provide the reconfigurable capability of CR [4]. SDR systems are based on the current development of DSP functions such as filtering, parameter estimation, modulating and demodulating which are common features to dynamically implement on CR devices. Such features are

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reported to be conceived on a variety of digital devices such as microprocessors, System on Chip (SoC), FPGA [5], even on processing and system frameworks like GNU Radio [6] and others.

However, these highly specialized fields demand academic courses to provide the fundamentals of communications as well as hands-on abilities to implement such systems on digital technologies, then to respond to a rapidly evolving development in the industry sector [7]. A variety of teaching curriculum are reported for SDR components and systems by using digital hardware as well as software applications [7]–[15]. These courses are also provided not only into the undergraduate-level [10]–[15] but also for continuing studies in curriculums concerning advanced topics [7]–[11]. This is in accordance with the constant growing capabilities of digital technologies and higher development demands from communication industries.

Most of these courses achieve the implementation of real world communication systems by students [7]–[9], [11]–[13], [15], which in turn allows to recall theory from theory-driven lectures and reinforce learning by doing projects. The implementation of projects on SDR allows to experiment, then to demonstrate and support the better teaching of concepts in communication and signal processing with radio signals in real practices. These activities improve the learning of communication concepts from theoretical subjects and motivates student to get further insights into SDR topics.

Academic programs above are planned with a mixed distribution of tutorials and laboratories components. Tutorial components are used to teach the basics of SDR, the system environment to afford projects as well as the implementation of digital signal processing algorithms. Laboratory components offer the potentialities to implement modules by students guided by the assistant teachers.

Projects implemented in classroom cover a variety of topics ranging from analog to digital transceivers including specific blocks such as pulse shaping, timing synchronization and channel estimation. In this direction, hands-on activities are provided based on SDRs programming [7], [8], [10] by directly adjusting SDR device parameters to establish point to point communications [9], [11]–[13], or by implementing systems running on MatLab®[1] only [14], [15]. Applications are illustrated over real-time systems, the off-line processing of radio frequency (RF) signals and its simulations.

However, most of these curricular designs do not consider the development of research skills in the students during the course. In accordance to the 2020 engineering vision [16], to accomplish with research activities motivates the self-development of innovation and creativity as well as self-acquisition of new knowledge which for the long-life learning. Only the report in [11] introduces a DSP-based program to support research assignments based on three year bachelor and two years master degrees. However, this curriculum is based on a large time line curriculum, which makes it difficult to implement together to the already running curricular programs at universities. On the contrary, it is the intention of the current proposal to introduce an academic elective course, short and flexible, to address SDR applications through DSP projects. The development of practical DSP projects will stimulate student's activity to learn independently [17], [18]. Besides, the current proposal is not only intended to provide a background on technical issues but also on research methodologies to self-acquire and introduce novel reported solutions on the topic by the students.

In specifics, the current academic program is intended to cover the following Learning Outcomes (LO) concerning the technical topics:

- LO 1 Apply theoretical knowledge regarding telecommunication technologies to design SDR components for FPGAs,
- LO 2 Implement SDR components in FPGA to meet identified technical needs,

and concerning the research-methodologies and communication of ideas:

- LO 3 Ability to investigate, formulate, and solve engineering problems creatively, knowledge of contemporary issues, and ability to engage in life-long learning,
- LO 4 Ability to effectively communicate information in speech, presentation, and in writing.

By means of these declared learning outcomes, we expect for the students to complete a course not only related to the technical concerns but also to mature research skills.

The rest of the paper is organized as follows. Section II provides a detailed description of the course activities and their main guidelines. Section III summarizes the assignments and evaluation process. Section IV discusses main results and the effectiveness of the proposed course. Then, concluding remarks are provided in Section V.

II. ACTIVITIES AND THEIR IMPLEMENTATION

The academic program is provided to undergraduate students during the second semester. This within the third year as an elective course of five-years Engineering on Telecommunications and Electronics program from CUJAE University. These students have completed courses on fundamentals of communications for analog systems, digital and analog electronics as well as analog circuits. Thus, students have minimum prerequisites to start with the introduction and further development of SDR techniques. Additionally, in parallel to the course on SDR, students are receiving lectures on DSP methods. DSP course introduces basic concepts to implement processing blocks in FPGAs, which in turn allows to organize the current course to follow these topics.

The course is driven by design projects where students must implement SDR applications on Sysgen®[2] software. They are organized in working groups consisted of three

[1] MATLAB is a registered trademark of The MathWorks, Inc.

[2] System Generator (Sysgen) is a high-level tool developed by Xilinx and is fully integrated in MATLAB Simulink for designing high-performance DSP systems targeting FPGA.

members each to address the specifics in projects. Projects are developed to achieve the implementation of transmitters and receivers such as AM and FM modems. Besides, topics related to signal parameter estimation and spectrum sensing techniques are also covered by projects. The completion of projects is developed in Sysgen to interact with FPGAs capabilities from Xilinx vendor. Major advantage using Sysgen is focused on the time saving to teach and implement high complex systems provided the facilities of connections and block representation.

In addition to the technical concerns, the proposed course includes guiding steps and activities to develop research skills on student's work. Based on the state-of-the-art research, students must collect relevant papers, summarize trends, open problems and posed challenges, then to perform a comparison of reported solutions. These activities will broaden vision to interact not only with SDR, but to the most recent reported challenges for a contemporary knowledge of current problems.

The course is structured by the sequence of sessions as illustrated in Fig. 1, where the solid line describes the structure of the proposed course, and the dashed lines represent unit topics of the parallel course on DSP. A total sequence of 16 sessions, two hours each, is clustered by three Teaching Activities (TAs) as follows:

- TA 1 Introductory lecture and tutorial labs (1-4) to teach the implementation of core elements in 5 sessions, representing 31.25% of the course. This is in correspondence with the LOs 1 and 2.
- TA 2 Project development labs (5-11) to implement each specific task organized as workshops along 7 sessions, representing 43.75% of the course. This is in correspondence with the LO 2.
- TA 3 Workshop on research strategies and seminars (1-3) to address methodologies on state-of-the-art research and communicate summarized ideas in 4 sessions, which represent 25% of the course. This is in correspondence with the LOs 1-4.

The next subsections present detailed methodological guidelines for each TA.

A. TA 1: INTRODUCTORY LECTURE AND TUTORIAL LABS (1-4)

During this sequence of activities core concepts on SDR and their programming on FPGA is addressed. The fundamentals are introduced in the lecture followed by hands-on activities in labs. This will provide the basis for students to address the assigned projects. First lecture brings principles of SDR architecture, motivations, applications and the theoretical fundamentals to introduce a general view of SDR devices and functioning in accordance to LO 1. Tutorial labs introduce the basics on flow diagram design on Sysgen and the use of adder, delay and multiplier blocks to conform a linear time-invariant (LTI) system to cover the LO 2. These surveyed labs are divided to conform an Infinite Impulse Response (IIR) notch filter as shown in the diagram in Fig. 2. The notch filter is

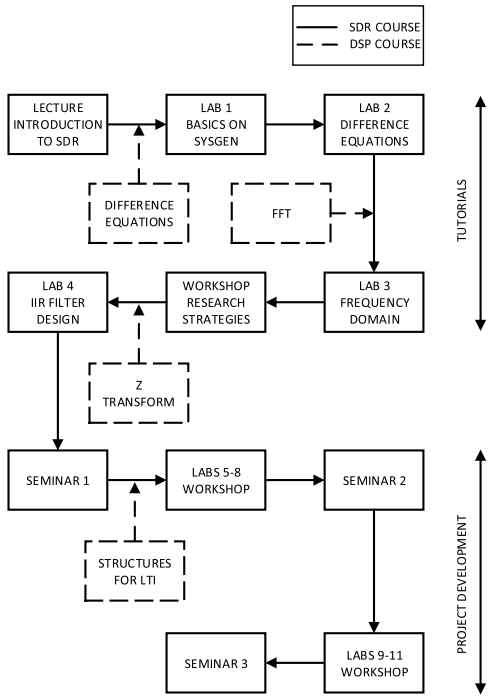

FIGURE 1. Sequence of topics for the FPGA-based SDR technology course.

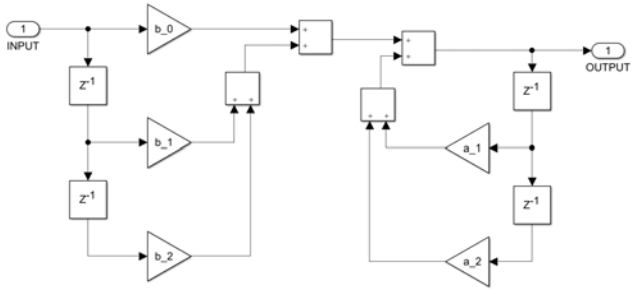

FIGURE 2. Direct Form I of second order IIR filter with coefficients from fdatool.

implemented to illustrate the filtering of a given tone from the superposition of cosine functions. Labs 1 and 2 introduce the implementation of Finite Impulse Response (FIR) and IIR difference equations, this based on the topic "Difference Equations" provided by the DSP course, as shown in Fig. 1. Additionally, these first two labs introduce the use of "Gateway in", "Gateway out", "Delay", "Adder", "Multiplier" and "Scope" blocks from Sysgen. The third lab introduces the obtaining of the notch's coefficients by using "fdatool" interface from MatLab and the obtaining of test results. Frequency description from "fdatool" is supported by the "FFT" unit block provided by the DSP course. Finally, the fourth lab conducts simulation tests based on the position of zeros and poles on the system function to analyze their effects in the output sequence. This is supported by the "Z-transform" unit block provided by the DSP course.

B. TA 2: PROJECT DEVELOPMENT LABS (5-11)

These labs are grouped in two blocks to implement the project solution in Sysgen software. The obtaining of the proper

diagrams must be devised by students with the support of assistant teachers covering the LO 2. Besides, students will discuss and present ideas following the dynamics of workshops. These two blocks' labs are supported by the main theoretical concerns and abilities provided on previous tutorial labs to the right use of Sysgen software and their components.

Both of these labs' blocks are preceded by a seminar to have a partial discussion on the solution to be implemented. Labs 5–8 are preceded by the first seminar where students discuss the system block diagram, then they have to identify the Sysgen components as well as their proper connections. The components to be developed here will be in accordance with each project topic, as detailed in the next Section. In this sequence of labs, further insights on hardware design are introduced to revisit Very High Speed Integrated Circuit Hardware Description Language (VHDL) and to introduce supported pre-built blocks from Xilinx. The use of Intellectual Property (IP) modules, their capabilities, and availability are discussed based on the supported FPGA families. The complexity of the given design and device utilization topics are also discussed. Additionally, time-restricted paths and the use of pipelines are introduced to have better designs. Further details are also addressed regarding the precision of arithmetic operations. Proper performance is validated by means of simulations to test the effect of quantization noise on filtered sequences.

Labs 9–11 are preceded by the second Seminar where students discuss details on the partial implementation of the system. Through the recommendations provided by the instructors during the sessions, the students will implement in this second labs' block their final solution and test their results. Labs 9–11 are conducted to refine and simulate implemented projects based on previous discussions from Seminar 2. Students must check again their designs to improve the settings, reduce critical paths by using pipelines, and reduction of design complexity mainly by lowering the total of bits for the fixed-point representation. Additionally, students must identify the proper FPGA family to implement their design, to obtain reports regarding details of device utilization, then to identify not used capacities such as DSP and memory blocks. Finally, students must evaluate the performance of their designs using scope blocks to depict input-output waveforms in time and frequency domains.

1) DEVELOPMENT OF APPLICATION PROJECTS

Projects emphasize the applications of SDR to communicate information based on the CR paradigm. Basic constitutive procedures of CR such as detection, estimation and demodulation are the groundwork of project assignments. Project's implementation has common blocks toward the obtaining of digital IIR filters. In this concern, students need to interact with DSP blocks and the floating point representation of signals. Additionally, on each project students need to obtain waveform sequences to be transmitted in order to test designs. These transmitted waveforms are demanded to be implemented on MatLab code without the use of Sysgen blocks, similar to example from Lab 3. Projects are addressed by the implementation of the following schemes: 1) Costas Loop, 2) Square Loop, 3) Radiometer, 4) AM demodulator, 5) FM demodulator by implementing a derivator followed by an envelope detector, 6) Energy Detector, and 7) Cyclostationary detector.

These projects cover topics regarding the implementation of modems, estimation of signal parameters, and spectrum sensing, which are the most common operations of SDR devices. These topics engage students in practical engineering problems to the future industry employment. The complexity of the technical aspects in projects is also in correspondence to prior knowledge acquired by students on previous completed courses and the available time frame.

Schemes in projects 1–6 are mainly theoretically described in [19], [20], which represents the used bibliography on the completed course of fundamentals of communications. Project in 7 demands further studies by the book in [21]. Additionally, to implement these systems on discrete-time processing basis, students have to review the main book of DSP course in [22].

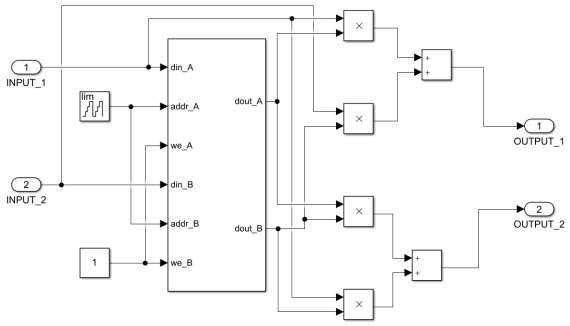

FIGURE 3. Correlator scheme implemented on Sysgen in a student project.

By means of this project the course motivates to follow five main objectives in unison: knowledge, science, research, innovation and engineering [23]. Knowledge and engineering are the basic objectives to accomplish after understanding and applying main technical issues to solve projects. However, science, research and innovation objectives are followed after results of revision of the state-of-the-art. Students are conducted to perform comparisons between reported solutions and current projects, then to devise some better ideas to consider novel solutions. To illustrate, Fig. 3 shows the diagram of the correlator, obtained by students, which is conceived for the cyclostationary detector project. This was derived after summarizing reported solutions from the state-of-the-art. By presenting this diagram on seminars, students will discuss the detailed functioning and performance description of their solution, as well as their fundamentals.

C. TA 3: WORKSHOP ON RESEARCH STRATEGIES

This workshop, placed between labs 3 and 4, introduces students in two basic strategies to follow specific subjects

on the current state-of-the-art and the use of bibliography management software covering the LO 3. After identifying the proper keywords, a first strategy is discussed regarding the search for related surveys, reviews and tutorials by using advanced search options on IEEE, Springer and similar databases. Keywords are defined relaying on the project they need to solve and these keywords are also updated from the searched results. Students must develop criterion regarding relevancy based on Then, homework assignments are oriented to summarize lines of research and open challenges based on these documented surveys. A second strategy is to search for the evolution of specific lines of research based on the cited articles. Homework assignments are presented to identify and summarize current development on one or more lines of research. Finally, students must identify the most important journals, conferences, institutions and authors on the field of research. This exercise represents the basics to conform the research profile. Students must summarize the state-of-the-art related to their project, then to be ready to identify and possibly solve a specific challenge. Besides, the identified research reports must be stored on reference management tools like Mendeley, Zotero, and EndNote.

This workshop also exposes the student to the most relevant academic journals and conferences related to each specific topic, where students receive a first overview regarding the mapping of main sections and organization of articles. Results of this exercise must be presented by two or three slides on Seminar 1 and last Seminar 3. This workshop is placed between labs 3 and 4, as illustrated on Fig. 1, to provide enough time to students to present a summary of reported solutions on next Seminar 1.

D. TA 3: SEMINARS (1-3)

Three seminars are conducted to present through oral presentations the project implementation, their performance (LOs 1 and 2), and the results of research-methodologies (LO 3) by means of oral presentations (LO 4). First seminar attends three main concerns: a summary of the state-of-the-art on reported solutions based on assignments from first workshop, fundamentals on main topics of projects, and discussion regarding the block diagram to implement the project solution. Team members must present main ideas by slides and open discussion between students is motivated by posing general and specific questions. This seminar is not only useful to discuss on technical details but to teach main procedures to present ideas and concepts with the use of slides. State-of-the-art must reflect a summary of reported applications, lines of research as well as open problems and challenges on the subject. Finally, the team must present a general block diagram to implement the solution. This final discussion pave the way to later search for proper blocks on Sysgen and implement their project for FPGA technology on next laboratories 5 to 8.

Second seminar is addressed to discuss technical details regarding project implementation. Students must justify the use of each block, connections and settings. Special discussions must be conducted toward the correct fixed point representation of numbers as well options on the use of available blocks from Sysgen.

Finally, Seminar 3 is focused on having a final evaluation of projects. This final evaluation must comprise a most complete discussion considering partial expositions in seminars 1 and 2 along to their final results from labs 9 to 11. Students must illustrate the proper functioning of solutions from their projects and concurrently present the state-of-the-art reports concerning the given topic.

On each seminar, feedback criteria are provided to each team to improve not only their designs but also their exposition. In addition, these seminars are also used to disseminate ideas in classroom and share best practices to implement solutions and to conduct projects. Most valuable experiences between students are interchanged in the specific details and in the general procedures to develop the project.

III. ASSIGNMENTS AND EVALUATION PROCESS

A. ASSIGNMENTS

Throughout this course we implement a variety of assignments to fulfill the declared LOs. These assignments are conducted in tutorial labs (TA 1), during the project discussion (TA 2), and in seminars (TA 3), as follows:

1) ASSIGNMENTS IN TUTORIAL LABS

Here we address problems directly related to the content provided in labs 2 to 4. Students must provide solutions to problems concerning the implementation of difference equations and filtering in Sysgen software, while the frequency domain analysis is covered through the development of the MatLab codes. We state problems to implement a given difference equation by using registers, adders and multipliers blocks. Students must obtain plots to account for the frequency response of the given difference equation. Furthermore, students filter mixed tones by implementing bandpass IIR and FIR designs, and concepts like impulse response and frequency analysis are re-visited from a modeling environment. To address these assignments, students work on a workstation comprised by a desktop PC and Xilinx board (Spartan 6) as shown in the picture from Fig. 4. In general, these problems are of reduced difficulty but broaden enough to support the ability to design (LO 1) and implement components through hands-on activities (LO 2).

2) ASSIGNMENTS TO IMPLEMENT THE PROJECT'S SOLUTIONS

Assignments are focused in the design of the specifics solutions to the given project subject to support LO 1. Then, projects are implemented during the labs 5 to 11 and the own work of students at home. Students must devise a block diagram in accordance to the project needs, then to implement it with the corresponding blocks for FPGA. They should also implement the proper testbed to verify the functioning of the proposed solutions. These assignments will support the LO 2.

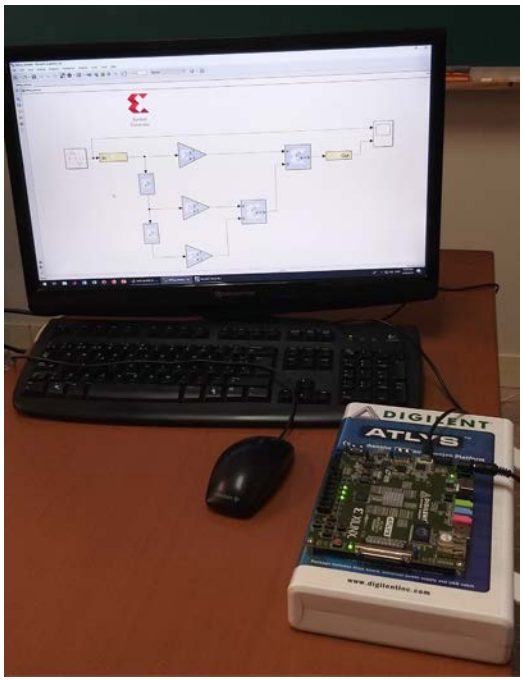

FIGURE 4. Workstation to develop projects.

Additionally, each team have to deliver a technical report at the last seminar concerning their derived work on the project.

3) ASSIGNMENTS IN SEMINARS

During the three seminars, students must conduct through oral presentations the development of their specific projects and their analysis of the state-of-the-art reported solutions. Each team presents a total of three oral presentations, one per seminar (LO 4). First seminar is dedicated to introduce the current state-of-the-art, directly related to project development, where students must summarize the fundamentals and illustrate their proposed block design (LO 1). Besides, the students must prepare a comparative summary of their own and reported solutions in the state-of-the-art (LO 3). During the second seminar, students will provide the technical details to implement their projects in Sysgen (LO 2). This is where students will exhibit main achievements and get focus on main implementation issues. In the third seminar students will illustrate their findings and the overall description of the project.

B. EVALUATION PROCESS

Evaluations are basically performed through the solution of problems during the tutorial labs, expositions of ongoing projects in seminars, and the delivered project report. Evaluation on labs pursues to assess the development of main technical concepts. Evaluation on seminars integrates technical, research, and communication skills development as well as the conducted research on each specific project topic. Evaluation of reports accounts for the completeness of the technical solutions and the quality of the written report.

1) EVALUATION ON TUTORIAL LABS

It is applied on short quizzes, with 20 minutes duration each, to cover contents from labs 2 to 4. Labs 2, 3 and 4 are evaluated on labs 3, 4 and 5, respectively. These three short quizzes consist of assigning to students some specific exercises related to the implementation of difference equations and filtering in Sysgen software, while the frequency domain analysis is evaluated through the devised MatLab code. These evaluations via short quiz are graded as follows: 50% to represent arithmetic relations by diagram blocks in Sysgen, 20% to obtain the frequency response of the system in MatLab code, and 30% to obtain proper results. Then, the grade for these three labs represents 30% of the total final grade in the course corresponding 10% to each lab. These evaluations will account for the LOs 1 and 2.

2) EVALUATION ON SEMINARS

According to defined schedules to achieve project solutions, seminars evaluate the following: design completion (40%, LOs 1 and 2), performance of the proposed solution (35%, LO 2), creativity (15%, LO 3), as well as quality and completeness of the oral presentation (10%, LOs 3 and 4). Seminars do not only evaluate performance and development of projects, but evaluate creativity based on own solutions and discussion of the related state-of-the-art (from workshop assignments) as well as quality of slides and the explicitness of expositions. This is why these two concerns represent 25% of the total grade. On each seminar, open discussions between students are motivated by suggesting new formulations and concerns regarding technical details.

3) EVALUATION OF THE PROJECT REPORT

The project report will be graded by the completeness of technical concerns (40%, LOs 1 and 2), the addressing of research strategies (30%, LO 3), comprehensibility of the content (15%, LO 4), and quality of graphs (15%, LO 4). Finally, total grade of the course is provided by combining results from evaluations quiz evaluations on labs (30%), evaluations on seminars (40%), and the delivered project report (30%).

IV. RESULTS AND EFFECTIVENESS

The results and effectiveness of the course is summarized considering the marks obtained in evaluations and the feedbacks obtained from students in an anonymous survey. The next sections summarize these two issues, and the last section discusses about the effectiveness of the course.

A. RESULTS IN ASSESSMENT OF STUDENTS

The assessment of students is fulfilled by short quiz evaluations, the expositions in seminars, and the delivered project's report. Fig. 5 summarizes the obtained results illustrating the total of students per mark and evaluation. Marks are given by four categories: *Excellent* (5/5) to describe the outstanding achievement of results, *Good* (4/5) when assignments completion is without major concerns, *Regular* (3/5) when the

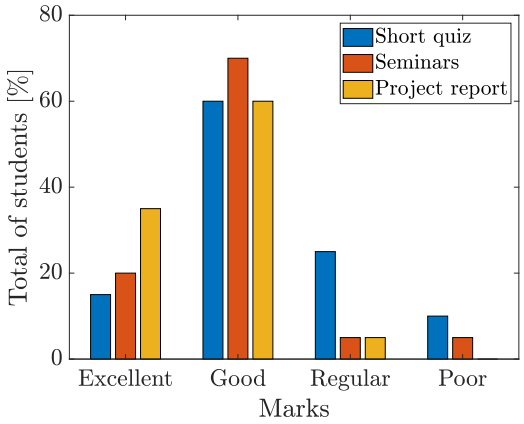

FIGURE 5. Summary of student's marks concerning the short quizzes, evaluations in seminars, and project report.

student at least achieves the completion of the intended goal, and *Poor* (2/5) when the student is not able to fulfill the goal addressed on the evaluation. Note that 2 is the minimum grade allowed and it is considered that the students pass when they obtain 3 or above.

Regarding the results of the assessment of students, the short quiz evaluations on tutorial labs exhibited an increased acquired maturity on students to implement solutions from the analytic formulation. On these short quiz evaluations, 15%, 60%, 25% and 10% of total students got excellent, well, regular and poor completion of their assignments, respectively. In total, 90% of the students passed the labs part.

Evaluation on seminars gave a better quality of completed assignments in comparison to labs evaluations. A 20%, 70%, 5% and 5% of the total students get excellent, well, regular and poor completion of assignments, respectively. Thus, 95% of the students passed the seminars part. Regarding the delivered written projects, the 35%, 60%, and 5% obtained excellent, well, and regular results, respectively.

Based on the tutorial labs, seminars, and report evaluations, the final result exhibited completed assignments superior to 90% of participant students. Considering the bar plot in Fig. 5, the short quiz evaluations resulted in worse students' performance according to the regular and poor marks. This is presumably caused by their early evaluation in the course during sessions 4 to 6 (labs 3, 4, and 5, c.f. Fig. 1). In the next edition, we will consider applying these short quizzes after students get a better maturity and practice in Sysgen during labs 6 to 8.

B. STUDENTS' ATTITUDE SURVEY

An attitude survey was also conducted with students by answering anonymously to the following questions:

- Q1 In this course, I was able to apply the theory from DSP subjects to conceive SDR applications in FPGA technology.
- Q2 The course provided me a better understanding of DSP topics.
- Q3 The level of the technical complexity of projects was in correspondence with my background knowledge on DSP topics.
- Q4 The topics I developed in projects were challenging and motivating.
- Q5 Addressing the project's solutions demanded from my side a creative attitude.
- Q6 In this course, I got research skills to search, summarize, and identify technical problems on the current state of the art reports.
- Q7 In this course, I got abilities regarding communication skills to present ideas in oral expositions.

The first three questions are directly addressing the technical concerns of the course and its connection to the parallel course in DSP. The last four questions handle the motivation and the intended soft skills concerning the research abilities and the communication of ideas. The survey asks to provide a grade in the range 1–10 for each question, where 10 corresponds to the greatest expectation.

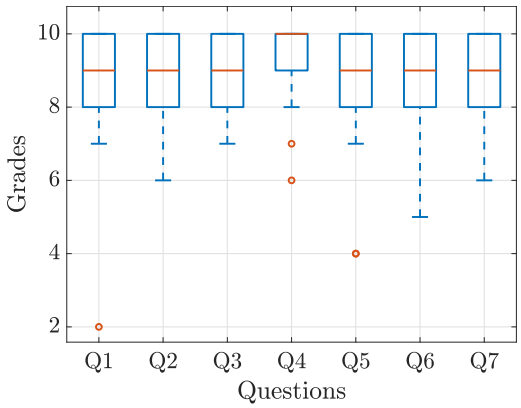

FIGURE 6. Results from the student's attitude survey to seven questions (Q1-Q7) graded in the range 1–10, where 10 is the greatest expectation.

Fig. 6 summarizes in a box plot the obtained results for each different question. On average, the evaluations per question present a high score given by 9, with a higher value in the case of question Q4 concerning the motivation and challenges of the project topics. Concerning the minimum for each box plot, the question in Q6 obtained the less score. This question addressed the skills regarding the research abilities. We suppose that the reason behind is that the workshop on research strategies TA3 was reinforced, with an additional training, to those students in charge of gathering more relevant research papers in their respective teams (2 students per team project). It seems that their content was not later appropriately shared with their team mates. Future editions will conceive this additional teaching activity with all the students in the course.

C. EFFECTIVENESS OF THE PROPOSED COURSE

This course has been proven to have positive outcomes for the students from two viewpoints. Technical skills on DSP design (LOs 1 and 2) and the research of novel solutions' ability

(LO 3) were improved on the student work. The supporting evidence from the evaluation on labs, derived reports, and the expositions on seminars exhibited a successful completion of assignments. Besides, considering the evaluation results, it is also remarked that a better quality in the written reports was obtained in comparison to the oral presentation.

Evaluation on seminars gave additional evidence to assess outcomes considering the exposure of students to the state of the art (LO 3), as well as the ability for oral presentations and discussion of their own ideas (LO 4). Seminar 1 brought first assessments regarding the ordering of ideas and quality of slides. Here students acquired some tips for a better exposition of the addressed topics. Students were aware of developing research skills in finding and comparing current reported results with respect to the received theory from courses. In Seminar 2, students showed abilities on the specifics to configure and properly connect a variety of blocks to achieve a large design. Finally, in Seminar 3 they exhibited a better maturity of concepts along to the projects' development. Students showed results of their functioning systems and further elaborated ideas concerning the fundamentals and implementation of subsystems. In addition, students discussed additional comparison metrics, fields of application, and the relevancy of their projects based on published papers' revision.

Considering the fulfillment of LOs, 90% of the students well accomplished with the technical ones (LOs 1 and 2), while the 80% with the research methodologies and communication concerns (LOs 3 and 4). Besides, this group of students exhibited better results on the parallel DSP course than the students from the previous course (improved by 25%), when this SDR course was not offered.

Finally, the assessment of the course from the student opinions, gathered in informal interviews, provided qualitative feedback on three main acquired skills: design and implementation of SDR modules on FPGA technology (LOs 1 and 2), research abilities to gather relevant information (LO 3), and best practices to present ideas (LO 4). The resulting feedback was very positive to judge a good correspondence between the course topics and the need to grasp theory from practice. Learned skills to search for novel reported solutions and present results were positively considered as well. Moreover, this feedback from the personal interviews was consistent with the results of the student's attitude survey presented in Fig. 6.

V. CONCLUSION

Our course proposal is based on the development of specific projects to improve engineering skills and knowledge. The proposed curriculum introduces to students how to develop and validate their own DSP blocks' design for communication systems. Although the current curriculum is based on offline processing, a second course based on this program may be offered to consider real-time signal processing scenarios. In this direction, the block design implemented in this course can be considered to test and conform dynamic real-time processing systems through low-cost transceivers, which may even be accessed remotely. The proposed curriculum also focusses on the students' abilities regarding research and innovation. By means of specific activities in workshops and seminars, students are motivated to study the state-of-the-art and perform comparisons of their current project with reported solutions. In future work, we will address the design of a curriculum where students are encouraged to publish their own ideas in the form of research papers. Additionally, guidelines to manage collaborative projects will be addressed to boost teamwork skills.

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