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Spiking neural networks based on two-dimensional materials

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The development of artificial neural networks using memristors is gaining a lot of interest among technological companies because it can reduce the computing time and energy consumption. There is still no memristor, made of any material, capable to provide the ideal figures-of-merit required for the implementation of artificial neural networks, meaning that more research is required. Here we present the use of multilayer hexagonal boron nitride based memristors to implement spiking neural networks for image classification. Our study indicates that the recognition accuracy of the network is high, and that can be resilient to device variability if the number of neurons employed is large enough. There are very few studies that present the use of a two-dimensional material for the implementation of synapses of different features; in our case, in addition to a study of the synaptic characteristics of our memristive devices, we deal with complete spiking neural network training and inference processes.

npj 2D Materials and Applications (2022)6:63 ; https://doi.org/10.1038/s41699-022-00341-5

INTRODUCTION

The Artificial Intelligence (AI) revolution, boosted by the internet-of-things, terahertz communications and social media, requires a new hardware infrastructure that can overcome important hurdles of conventional computers, such as the von Neumann's bottleneck (i.e., the effects related to the physical separation of data processing and memory units) and the memory wall (i.e., the steadily growing performance gap between the different types of memory and the microprocessors)[1]. Hardware implementation of neural networks (NNs) has attracted a lot of interest due to its ability to compute and store information at the same location, i.e., at the electronic neurons (nodes that process signals and generate a corresponding output) and the electronic synapses (nodes that memorise information by means of an electrical parameter and influence the signals that pass through them), as this computing architecture spares time and energy related to data transfer. However, the use of traditional circuits based on metal-oxide-semiconductor (MOS) transistors to construct electronic neurons and synapses is not power- and area-efficient because many transistors are needed to build them up. The use of crossbar arrays of memristors, i.e., a resistor with memory effect[2], to construct NNs has shown promising performance (i.e., low power consumption, high accuracy) when employed for different fundamental AI applications, such as face and speech recognition[3–8]. Such crossbar circuits[2,9] also allow in-memory computing (IMC), i.e., an approach where certain computation functions are performed in-place in the memory itself[10,11].

The NNs running most AI applications can be divided in two big groups: artificial neural networks (ANNs) and spiking neural networks (SNNs). In an ANN the information is represented with values that are continuous in time and can achieve high data recognition accuracy by using at least two layers of nonlinear neurons interconnected by adjustable synaptic weights[10]. This feature led to large networks with thousands of synapses[11]. Conversely, in a SNN the information is coded with time-dependent spikes, which remarkably reduces the power consumption compared to ANNs[12]. The main differences between ANNs and SNNs stand on: (i) the way the information is encoded (ANNs use real-value activations to convey information whereas SNNs modulate information on spikes), (ii) ANN neurons do not have memory while SNNs typically do have, and (iii) the output generated by most ANNs (e.g. feedforward ones) is not time dependant while most SNNs are time-varying[12]. This latter feature allows the creation of algorithms that can adapt and evolve with time; in addition, SNNs have an asynchronous nature with respect to ANN, this latter characteristic permit a greater system scalability and general efficiency since no synchronisation mechanisms are needed[13].

Moreover, the SNNs operation is more similar to the actual functioning of biological neural networks, and it can help to understand complex mammal's neural systems. In this work, we are going to study the development of memristors for the implementation of SNNs.

The main figure-of-merit of a memristor enabling its use as electronic synapse in a SNN is the spike-timing dependent plasticity (STDP) plot, a temporally asymmetric form of Hebbian learning that is induced by tight temporal correlations between the spikes of pre- and postsynaptic neurons[13]. A few implementations of SNN with memristors have been reported although a strong software perspective is employed in the studies in most of the cases[14,15]. Thereby both the synapses and neuron realisations have to be investigated deeply in the future.

Two-dimensional (2D) layered materials have shown excellent performance for the emulation of ANNs; devices based on these materials showed remarkable artificial synaptic behaviour (STDP, excitatory/inhibitory postsynaptic potential current (EPSC/IPSC), paired-pulse facilitation/depression (PPF/PPD) as well as short-/long-term plasticity (STP/LTP))[16]; optic-neural networks formed by these 2D material-based devices have been successfully reported where the coloured and colour-mixed pattern recognition capability of the human visual system is emulated[17]. Memristors made of 2D layered hexagonal boron nitride (h-BN) have exhibited

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the lowest energy consumption per state transition ever reported for any type of memristor (≈8.8 zJ)[18], which may be an important advantage for low-power computation. There are studies with memristors (not based on 2D materials) where synaptic features needed for SNN implementations have been addressed at the device level[19], others use 2D material devices to analyse the synaptic behaviour, also at the device level[20,21]. SNNs have been studied making use of memristive devices (without 2D materials)[22,23]. Nevertheless, the use of 2D materials for the development of complete SNNs, including training and inference with hundreds of neurons and a conventional dataset remains poorly explored. Here we fabricate Au/Ti/h-BN/Au memristors, characterise the presence and quality of the resistive switching (RS) phenomenon, and investigate their potential for the implementation of SNNs. Our study reveals that SNNs based on Au/Ti/h-BN/Au memristors perform reasonably well for the recognition of images form the Modified National Institute of Standards and Technology (MNIST) database. In addition, if we model the experimental variability measured along with STDP data, the influence on the recognition accuracy of the SNN considered is negligible if a number of neurons above 400 is employed. Our study opens up new horizons for the use of 2D materials based memristors to implement SNNs for advanced computation.

RESULTS AND DISCUSSION

Device fabrication and physical characterisation

We fabricated several arrays of 5 μm × 5 μm cross-point memristors with a top-to-down Au/Ti/h-BN/Au structure on 300 nm SiO_2/Si wafers, by patterning the metallic electrodes via photolithography and electron beam evaporation and transferring 6-nm-thick (i.e., ≈18 layers) h-BN sheets previously grown by chemical vapour deposition (CVD) on an independent Cu foil. Figure 1a shows a schematic of all the steps followed for the fabrication of the samples; this process employs low temperatures (<85 °C), it is compatible with CMOS technologies, and has already been employed to fabricate hybrid 2D/CMOS circuits[24]. The main concerns when trying to introduce CVD-grown 2D materials on silicon chips are the formation of cracks and the introduction of polymer residues during the transfer process. However, in our samples these two issues are not a problem because: (i) we are employing a 6-nm-thick h-BN stack, which can withstand well the mechanical stresses, and (ii) below a certain dose, the presence of contaminants does not change the properties of the devices because the out-of-plane currents driven by the memristors always flow across the weakest point/s in the sample (i.e., regions with polymer contaminants are not affecting because they are highly insulating)[25]. Optical microscope images demonstrate the absence of cracks (Fig. 1b), and scanning electron microscope images show the presence of continuous wrinkles on both the SiO_2 substrate and on the bottom and top electrodes (Fig. 1c), confirming the continuous nature of the multilayer h-BN sheet. Cross-sectional transmission electron microscope (TEM) images reveal correct layered structure with some native defects embedded, i.e., lattice distortions (Fig. 1d, e). It is worth noting that, in the TEM images, the atoms (of any type) appear with dark colour, and the space between them with bright colour — because electrons pass across the thin lamella and hit the detector. Figure 1e shows that the bright lines (spaces between layers) are interrupted with dark colours, indicating the presence of interstitial atoms between the layers. These can be manifested as individual locations (yellow arrows) or as few-atoms-wide amorphous regions (dashed ovals). Moreover, it can be observed that the interfaces contain a large amount of defective bonding, while the bulk of the h-BN stack exhibits a better 2D layered structure. These native defects in the h-BN stack produce leakage currents and premature dielectric breakdown that hinders applications as dielectric in transistors; however, such low energy-to-breakdown allows partially recovering the initial electrical resistance of the devices and observing the memristive effect[26].

Electrical characterisation and variability analysis

The devices exhibit clear bipolar RS when they are exposed to sequences of electrical stimuli of different polarities; however, the nature of the switching can be controlled depending on the type of stress applied. When the devices are exposed to sequences of current-limited (100 μA) ramped voltage stresses (RVS), sharp switching between a high resistive state (HRS, ≈ 10 nS) and the low resistive state (LRS, ≈ 8 mS) can be observed (Fig. 2a) — after a forming process at voltages between ≈4 V and ≈8 V). In our previous study[27] we demonstrated that bipolar RS in Au/Ti/h-BN/Au devices is related to the formation and disruption of a Ti-based conductive nanofilament across the h-BN stack, probably at the native defects embedded within the crystalline 2D layered lattice due to the lower energy for metal penetration at such sites[28]. For positive voltages Ti^{X+} go into the dielectric defects and under negative voltages these ions go back; in this manner, the conductive nanofilament is formed and disrupted to facilitate resistive switching operation.

The variability of the switching voltages and the state currents (shown in Fig. 2b–c) is not the best ever reported[29], but similar to that observed in many other metal-oxide-based memristive devices reported in the literature[9]. Also, after forming, if the devices are subjected to sequences of pulsed voltage stresses (PVS) the resistive switching can be provoked in an analog manner, i.e., by inducing many stable resistive states (Fig. 2d, left plot). This behaviour should be related to the injection of small amounts of Ti^+ ions into the h-BN stack, similar to what happened during the HRS-to-LRS transition in bipolar RS (Fig. 2a) but in a smaller quantity and in a more controllable manner. It is remarkable that resistance variation over time (commonly referred to as retention) is extremely low (Fig. 2d, right plot); this is an important feature when trying to use these devices to implement an ANN because it allows their use as electronic synapses during the inference process, as demonstrated in our previous publication[26].

Next, we characterised the presence of STDP in our devices by applying a pair of electrical spikes (i.e., a type of pulsed voltage stress, see Fig. 3a) that are delayed a specific time from each other to the top and bottom electrodes of the 5 μm × 5 μm Au/Ti/h-BN/Au memristors. Figure 3a shows the shape of the pulses applied; the time at which the spike at the top and bottom electrodes is applied are named t_{PRE} and t_{POST}, and the delay between them is calculated as $\Delta t = t_{POST} - t_{PRE}$. By subtracting the post-spike and pre-spike voltage signals, we can leave the bottom electrode grounded and use the composed signal at the top electrode in an equivalent manner (Fig. 3b). As Fig. 3c–e shows, the device conductance variation (ΔG) was measured with respect to the initial conductance ($G_{INITIAL}$). The devices show good STDP response, and we are able to control the slope of the exponential trend by adjusting the duration of the electrical spikes applied (S_w). This result is remarkable because previous attempts to measure STDP in similar 5 μm × 5 μm Au/Ti/h-BN/Au memristors only were able to see a linear trend[26], which indicates a rather poor STDP behaviour. The improvement achieved in this study may be related to the use of a thicker h-BN stack (≈6-nm-thick in this study versus ≈2-nm-thick in ref. [26]). The asymmetric shape of the STDP plot should be related to the different composition of the metallic electrodes (i.e., top Ti and bottom Au), which for the same spike duration ($\pm\Delta t$) produce different speed for Ti^+ ion migration.

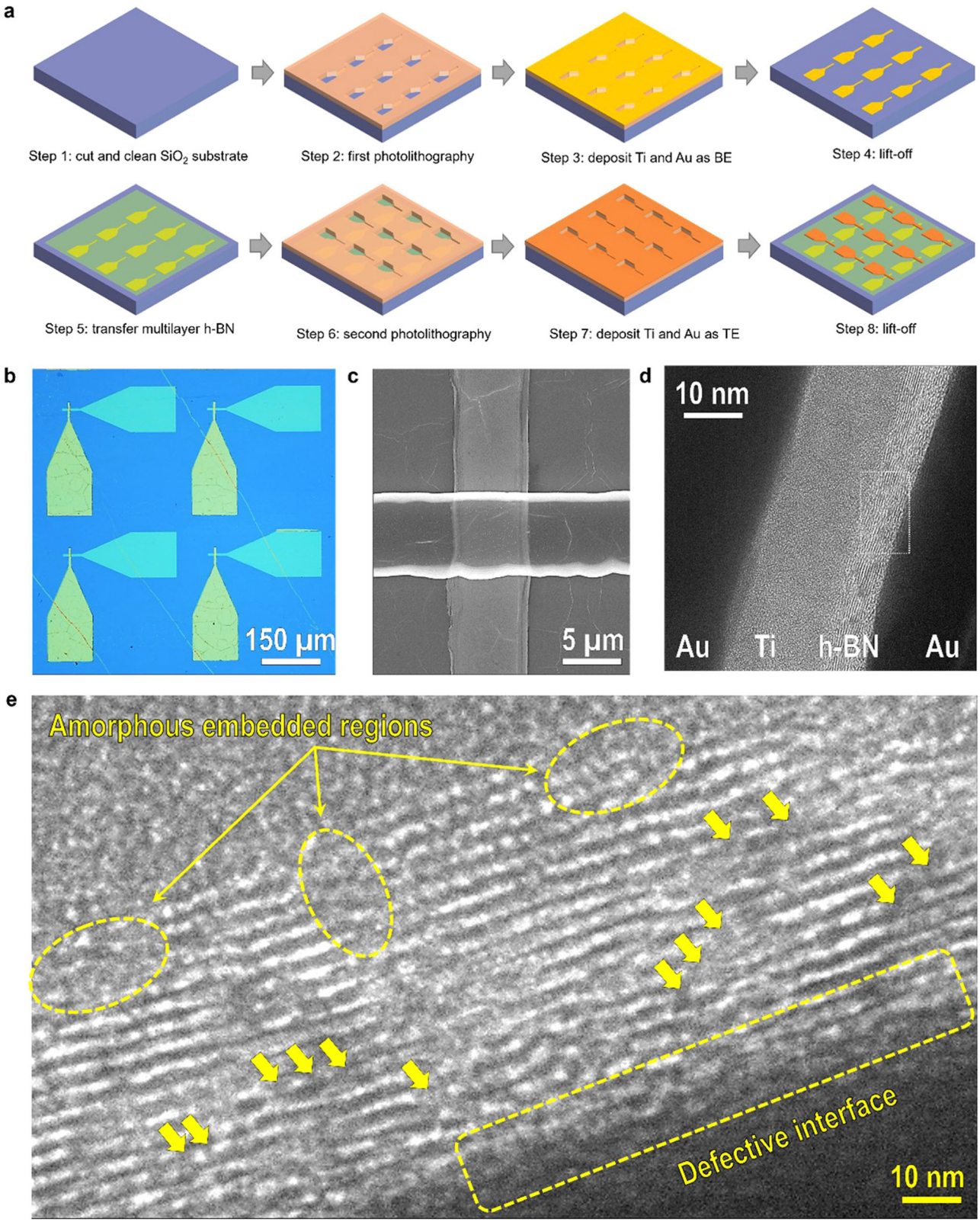

Fig. 1 Fabrication of synapses based on Au/Ti/h-BN/Au/Ti memristors. a Experimental process followed for the fabrication of the devices, which can be divided in eight steps. **b** Large-area optical microscope image of the samples proving that there are no cracks in the h-BN. **c** Detailed SEM image of one device, in which h-BN wrinkles on the SiO_2 substrate and on the top/bottom electrodes can be observed, proving he continuity of the h-BN film. **d**, **e** Cross-sectional transmission electron microscope image of the h-BN stack, showing a good layered structure with some native defects (lattice distortions). **e** corresponds to the area highlighted with a white dashed square in panel **d** (rotated 90 degrees), in which we indicate the most common type of defects: defective bonding at the top interface with the Au electrode, local interstitial atoms between the h-BN layers (small arrows), and few-atoms-wide amorphous regions embedded in crystalline 2D layered h-BN stack (dashed ovals).

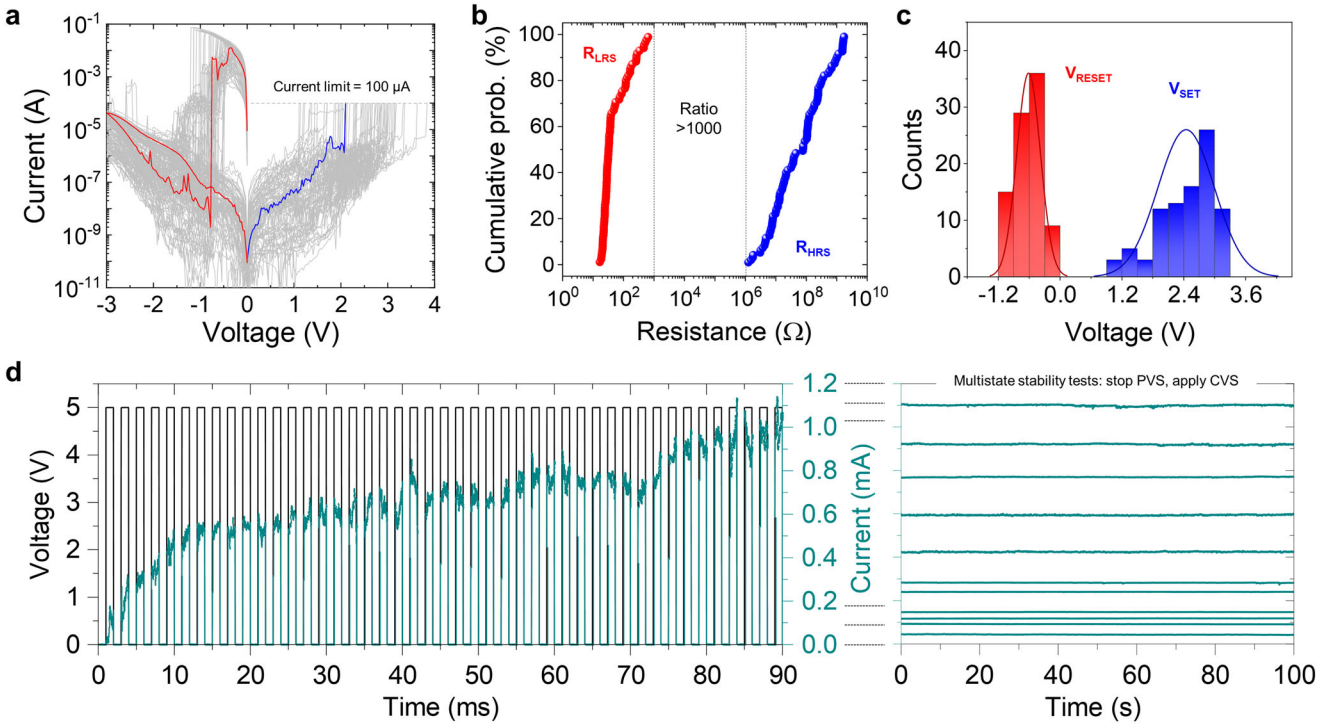

Fig. 2 Resistive switching in Au/Ti/h-BN/Au/Ti memristors. a Experimental current versus applied voltage for different RS cycles in a long series for our devices (the compliance current used was $I_{CC} = 0.1$ mA). We have plotted 88 set (blue curve) and reset (red curve) processes. **b** Variability analysis accounting for the resistances for the low and high resistance states (R_{LRS}, R_{HRS}) measured at low voltages. **c** Variability analysis accounting for the switching voltages for the HRS-to-LRS and LRS-to-HRS transitions (V_{SET}, V_{RESET}). **d** Voltage and current versus time plot showing the progressive potentiation of a memristor when applying sequences of PVS. The right panel, which has the same vertical (current) axis, shows the current versus time plot collected after stopping the PVS at a specific current level.

Spiking neural network study

The shape of the STDP plot can be used in the framework of SNNs to implement the network learning rule. To do so, the most common methodology is to calculate the fitting parameters A and τ both for potentiation and depression, using Eq. (1)[30]:

$$\begin{cases} \frac{\Delta G}{G_{INITIAL}} = A_+ e^{-\frac{\Delta t}{\tau_+}} \text{ for } \Delta t > 0 \\ \frac{\Delta G}{G_{INITIAL}} = -A_- e^{+\frac{\Delta t}{\tau_-}} \text{ for } \Delta t < 0 \end{cases} \quad (1)$$

These parameters will allow the calculation of the synaptic weight variations as shown in the Supplementary Note 1. Hence, we fit the experimental data obtained during STDP characterisation to Eq. (1), as shown in Fig. 3c–e. An average fitting for the distribution can be obtained (solid lines) and two other fittings that enclose the experimental data distributions (dashed lines) are also shown. All the fitting parameters are displayed in Table 1; the values assigned are meaningful from a mathematical point of view. The time constants both for the potentiation and depression modelling are the same for a determined spike duration. Therefore, variability in the STDP, and consequently in the SNN learning rule, can be concentrated on the study of the variation of the A_+ and A_- constants.

We use these fitting parameters to implement the learning rule in the SNN with an unsupervised learning scheme and evaluate its main figures of merit. The input layer consists of 784 neurons, which is designed for the dataset we utilise: the MNIST database of handwritten digits. A schematic representation of the SNN is displayed in Fig. 4a. The MNIST dataset is formed by 28×28 grayscale pixel images that consist of 70,000 handwritten digits labelled in the interval [0, 9], divided into a training set (60,000 images) and a test set (10,000 images)[31]. The excitatory layer (for data processing) contains the same number of neurons than the layer with the inhibitory neurons. The neurons of the input layer are connected in an all-to-all fashion to the excitatory neurons (see arrows). The excitatory neurons of the processing layer connect one-to-one to inhibitory neurons; therefore, a spike in the excitatory neuron will trigger a spike in its corresponding inhibitory neuron. However, each inhibitory neuron connects to all excitatory neurons excepts to the one from which it receives connection. This architecture allows lateral inhibition that leads the excitatory neurons to compete (see Fig. 4a)[32]. The inhibitory and excitatory synaptic conductance ratio needs to be balanced to modulate lateral inhibition in order to avoid this to have no influence or, on the contrary, let a winner prevent other neurons from firing. Class labels are not presented to the network, so the learning is unsupervised.

We have implemented the synapses of our SNN using STDP as the learning rule, and used the mathematical expressions obtained from the modelling of the electrical characteristics of our Au/Ti/h-BN/Au devices (Fig. 3c–e and Table 1). This learning rule applies exclusively at synapses between the input layer and excitatory neurons. The synapses between excitatory and inhibitory neurons are kept fixed to ensure that lateral inhibition is neither too strong, preventing other neurons from firing at all, nor too weak, causing it to have no effect. The learning process is explained in depth in Supplementary Note 1 — see that the time constants for potentiation and depression are included in Supplementary Eqs. 4 and 5 (respectively), and that the A_+ and A_- constants are included in Supplementary Eqs. 6 and 7 (respectively). The preexponential constants (A_+ and A_-) corresponding to the average distribution of STDP experimental data (solid lines in Fig. 3c–e) were used as reference parameter. The variability was taken into account by calculating the change in the A_+ and A_- parameters ($\Delta A_+ = |A_+(\text{solid line}) - A_+(\text{dashed line})|$). Variability was incorporated in the Supplementary Eq. 7; with this

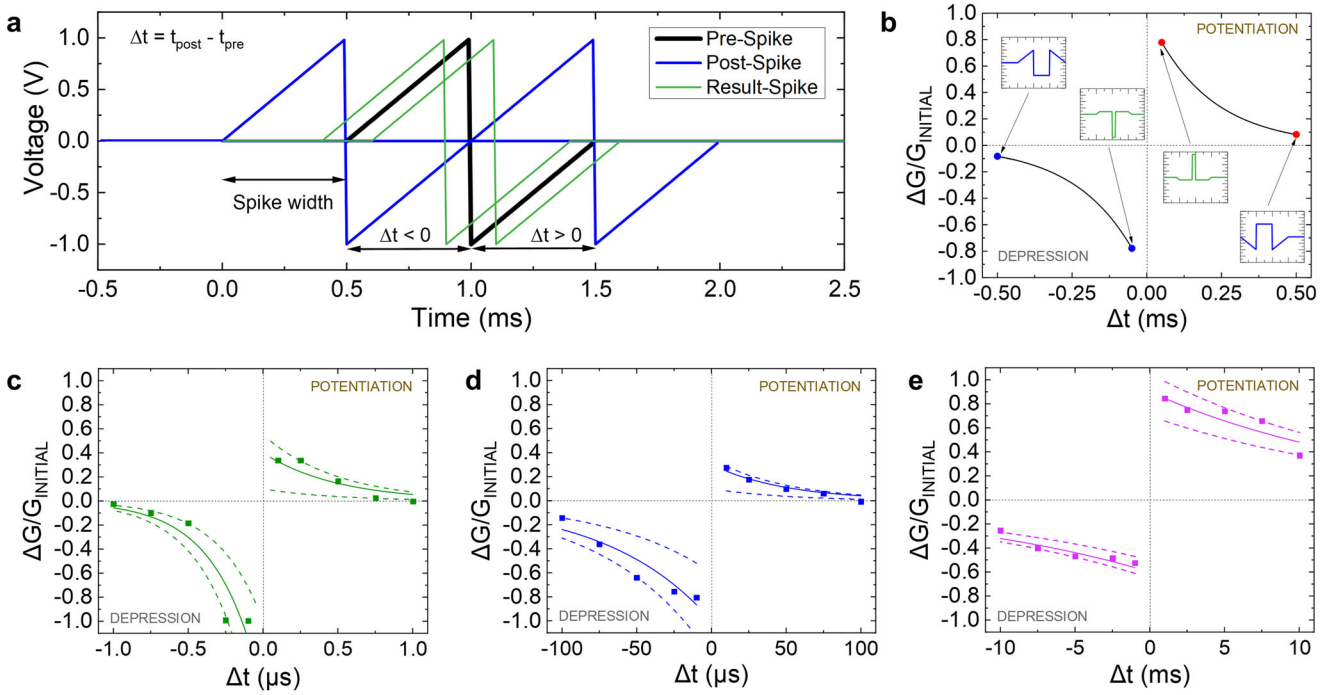

Fig. 3 STDP function in Au/Ti/h-BN/Au/Ti memristors. a Spiking protocol applied to the memristors to measure STDP. Different spike widths (S_w) can be employed. In our case, we made use of the following values for the spike widths, $S_w = 1$ µs, $S_w = 100$ µs, $S_w = 10$ ms. The post-spike and pre-spike are subtracted to ease the measurement process, the resulting signal generated (shown in the insets of the next figure, **b**) is applied to the top electrode while the bottom one was grounded. **b** Theoretical memristor STDP behaviour; the signals employed for the measurements are shown as insets, they are generated as a subtraction of spikes (post-spike – pre-spike) with different delays ($\Delta t = t_{post} - t_{pre}$). **c**–**e** STDP function measured in the devices. The input signals were made of sequences of pre-spike and post-spike pairs with different delays to characterise the depression and potentiation regimes. The spike width was **c** 1 µs, **d** 100 µs and **e** 10 ms. The $G_{INITIAL}$ values for each curve were the same for coherence; i.e., the initial conductance prior to the application of the spikes was the same in every point of the same plot, to make the $\Delta G/G_{INITIAL}$ comparable along the curves shown. The solid lines show the best fitting in each case for the experimental data. The dashed lines are calculated to enclose the experimental data distributions, maintaining the same time constant parameters (τ_+, τ_-) for the three curves corresponding to depression or potentiation (the fitting constants, according to Eq. 1, to reproduce de experimental data (symbols) of the STPD learning window are given in Table 1).

Table 1. Fitting parameters for the mathematical representation of the STDP measured.

Line fitted	Fitting variable	Potentiation			Depression		
		1 µs	100 µs	10 ms	1 µs	100 µs	10 ms
Top (dashed line)	A_+/A_-	0.55	0.35	1.05	1	0.6	0.5
	τ_+/τ_-	0.5 µs	50 µs	16 ms	0.3 µs	70 µs	16 ms
Average (solid line)	A_+/A_-	0.4	0.3	0.9	1.6	1	0.6
	τ_+/τ_-	0.5 µs	50 µs	16 ms	0.3 µs	70 µs	16 ms
Bottom (dashed line)	A_+/A_-	0.1	0.1	0.7	2.2	1.3	0.65
	τ_+/τ_-	0.5 µs	50 µs	16 ms	0.3 µs	70 µs	16 ms

Equation 1 is employed along with the data in columns 3–5 for memristor conductance potentiation modelling in the STDP measurements shown in Fig. 3c–e, for different temporal spike widths. Equation 1 is employed along with the data in columns 6–8 for memristor conductance depression modelling in the STDP measurements shown in Fig. 3c–e, for different temporal spike widths.

new equation we obtained the change in the synaptic weights and repeated the SNN training process. Then we performed a study considering a different number of neurons for our network (Fig. 4b, c) as well as a different number of training epochs (Fig. 4d, e) and achieve better recognition accuracy for the MNIST dataset as we increase the number of neurons. We observe a saturation behaviour in terms of accuracy for a number of epochs higher than 3. Variability affects the results for a low number of neurons; however, for 400 neurons, and specially for 800 neurons, its influence is much lower due to the inherent stochasticity behaviour of the SNN. In fact, slightly higher accuracy values are obtained if variability is considered (Fig. 4c and e).

In summary, we have evaluated the potential of Au/Ti/h-BN/Au memristors to implement spiking neural networks for image recognition. We have fabricated and characterised the devices to study the different features needed to implement synapses in the context of neuromorphic computing. The memristive behaviour in terms of resistive switching and variability was good both under ramped and pulsed input signals. The spike timing dependant plasticity and its corresponding variability were measured and modelled. These data, used as the learning rule in SNNs, were employed to train the network, considering different number of neurons and epochs. The role of STDP variability was analysed and it was shown that, for the architecture employed, 400 or more neurons are needed to ensure that the variability of our devices did not penalise the network recognition accuracy.

METHODS

Device fabrication

The structure of the memristors from top to bottom was 40 nm Au/10 nm Ti/6-nm h-BN/40 nm Au, which were fabricated on a Si wafer with 300 nm SiO_2 on top. First, we deposit the bottom electrodes, which consisted of a squared pad of 100 µm × 100 µm

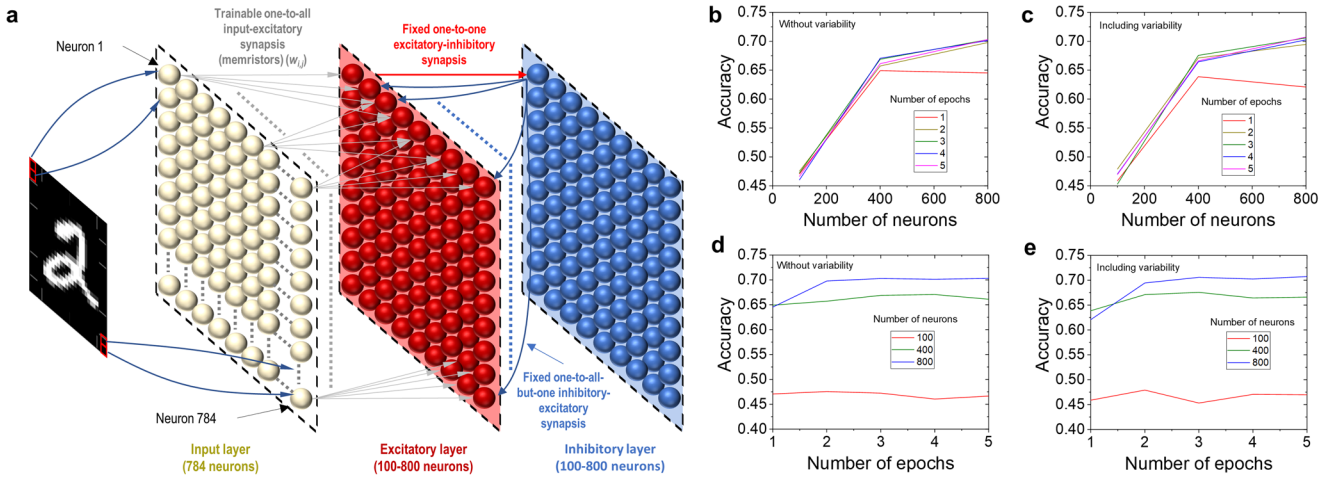

Fig. 4 SNN architecture and recognition accuracy. a The input neurons (pre-neurons) are connected to every neuron in the excitatory layer (post-neurons). Each excitatory neuron has a corresponding one-to-one connection to an inhibitory neuron, which in turn inhibits all the neurons in the excitatory layer except the one from which it received a forward connection (lateral inhibition). **b** Recognition accuracy for the NMIST dataset versus the number of neurons for an SNN without variability and **c** including variability. In both scenarios different numbers of epochs were employed in the study; **d**, **e** accuracy versus number of epochs for an SNN without and with variability, a different number of neurons were employed in the study.

and a metallic wire with a width of 5 µm; the transition between them was done by reducing the width from 100 µm to 5 µm. The electrodes were deposited by photolithography, electron beam evaporation and lift-off, using a mask aligner MJB4 from SUSS MicroTech and an electron beam evaporator PVD 75 from Kurt Lesker. Below the 40 nm Au bottom electrode we used a 10 nm Ti adhesion layer, but we did not mention it throughout the text because the current does not flow along or across it. After the deposition of the bottom electrode, a sheet of commercially-available ≈18-layers-thick h-BN (grown independently on a Cu substrate by CVD method) was transferred on the bottom electrodes.

Device characterisation

The devices were characterised by using a Keysight B1500A semiconductor parameter analyser connected to a probe station (Karl Suss PSM6). We employed two different measuring units: i) the B1511B medium power source measurement unit (MPSMU) module for quasi-static ramped voltage stress, and ii) the B1530 module, which is a waveform generator and fast measurement unit (WGFMU) that is ideal to apply the pulsed voltage stresses.

SNN simulation

The SNN architecture is described in Fig. 4a in the main manuscript. This network has been developed using BindsNet[33], a Python library built on top of PyTorch[34], so its network models can easily be executed on CPU or GPU. It implements a wide variety of neurons, input encoding methods and several learning methods such as STDP. The details regarding the learning rule and the mathematical models employed in the implementation are described in the supplementary information. Both during training and testing each input image is presented to the network for 350 ms in the form of Poisson-distributed spike trains, with firing rates proportional to the intensity of the pixels of the MNIST images, with firing rates between 0 (black pixel) and 128 Hz (white pixel). After training is done, we disable the postsynaptic spike (to prevent further potentiation/depression), fix each neuron's spiking threshold, and assign a class to each neuron, based on its highest response to the ten classes of digits over one presentation of the training set. This is the only step where labels are used, i.e., for the training of the synaptic weights we do not use labels. The response of the class-assigned neurons is then used to measure the classification accuracy of the network on the MNIST test set. The predicted digit is determined by averaging the responses of each neuron per class and then choosing the class with the highest average firing rate. We employed a 2 nodes Intel Xeon E5-2634, 128 GB DDR4 2400 MHz, using one GPU at a time. For 800 neurons (including variability in the learning rule), the training time was around 120,000 s, for 400 neurons the training time was around 80,000 s.

DATA AVAILABILITY

The datasets generated and/or analysed during the current study are available from the corresponding author on reasonable request.

CODE AVAILABILITY

The code employed during the current study is available from the corresponding author on reasonable request.

Received: 8 May 2022; Accepted: 24 August 2022;
Published online: 09 September 2022

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ACKNOWLEDGEMENTS

This work has been supported by the Ministry of Science and Technology of China (2018YFE0100800), the National Natural Science Foundation of China (grant no. 61874075), the Collaborative Innovation Centre of Suzhou Nano Science & Technology, the Priority Academic Program Development of Jiangsu Higher Education Institutions, and the 111 Project from the State Administration of Foreign Experts Affairs of China. We also acknowledge the Consejería de Conocimiento, Investigación y Universidad, Junta de Andalucía (Spain) and European Regional Development Fund (ERDF) under projects A-TIC-117-UGR18, B-TIC-624-UGR20 and IE2017-5414, as well as the Spanish Ministry of Science, Innovation and Universities and ERDF fund under project RTI2018-098983-B-I00. M.L. acknowledges generous support from the King Abdullah University of Science and Technology.

AUTHOR CONTRIBUTIONS

Conceptualisation by J.B.R. and M.L.; software and neural network analysis by R.R.-Z., A.M.G.-V. and F.A.; electrical measurements and data curation by D.M., C.A.-P., E.M. and Y.S.; Y.S. fabricated the h-BN memristors. Y. S. realized the physical characterization of the devices. Original draft preparation, review and editing by J.B.R., M.L., D.M., F.A., R.R.-Z. and A.M.G.-B. All coauthors have checked and validated the final version of the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-022-00341-5.

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