


Article

Design of a Gate-Driving Cell for Enabling Extended SiC MOSFET Voltage Blocking

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Abstract: A series connection of SiC MOSFETs for kV blocking capability can enable more design flexibility in modular multi-level converters as well as other topologies. In this paper, a novel gate driver circuit capable of driving series-connected SiC MOSFETs for high voltage applications is proposed. The primary advantage of the proposed design is that a single gate driver was used to switch all the series devices. The circuit used switching capacitors to sequentially charge and discharge device gate capacitances during switching and enable a negative turn-off voltage to avoid device coupling from Miller-capacitive feedback effects. With the proposed gate driver design and appropriate component values selection, avalanche breakdown due to voltage divergence during switching transients could be avoided with only a minor imbalance in the top device. Simulations and experimental measurements showed that the zero-current turn-off transition of all switches was achieved, and this approved the validity of the design.

Keywords: series SiC MOSFET; driving circuit; high voltage



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1. Introduction

In the recent years, wide-bandgap semiconductor devices have enabled more improvements in applications in the power electronics field [1]. At the time when silicon (Si) devices are coming close to the limitations of the material, the high switching speed offered by silicon carbide (SiC) materials, alongside their high breakdown voltage and high thermal conductivity make them superior to Silicon (Si). SiC MOSFET is a promising alternative in medium- and high-voltage power electronics applications [2].

Existing commercial SiC MOSFETs are still commonly 1.2 and 1.7 kV. Some higher voltage SiC switches are in the development stage and, if available commercially, they would be costly [3,4]. According to the work in [5], series-connected SiC MOSFETs brings a lower on-resistance which allows for higher current density than using a single high-voltage device. Therefore, investigating the series connection of multiple SiC MOSFETs does worth.

For series connection of MOSFET switches, the common driving method uses fully separated drivers for each device equipped with its own isolated power supply [6]. Although this method provides more control flexibility, it brings some challenges in terms of compact designs for high power density applications [7]. An auxiliary voltage source was required in [8] to provide enough power to drive the upper devices.

One way to drive the upper-side MOSFETs without an auxiliary power supply [8] is by using capacitive coupling [9], where the lowest MOSFET acts as a master and the upper ones as slaves. The concept uses the charge variation in the capacitor to produce the driving signals for the upper MOSFETs. A floating self-driving circuit was developed in [10,11] utilizing DC capacitors to support switching the high side of two series switches. Another concern while driving series MOSFET devices is the off-state voltage balancing during both the steady state and dynamic transition [12]. Uneven leakage current between

series MOSFETs is the main reason behind the unbalanced voltage distribution. Equal parallel resistors across series MOSFETs will not always guarantee a balanced voltage if the leakage current is significant. An active control technique was proposed in [13] to achieve dynamic sharing for series IGBTs. Ruchira et al. in [14] proposed a voltage-clamping circuit to balance the voltages. In [15], a snubber circuit was presented to achieve adequate voltage sharing during the transient across series-connected SiC MOSFETs. To mitigate the false turn-on events and provide more gate immunity, a negative voltage, i.e., -5 V is recommended to switch-off the MOSFET [7].

Active gate driving for IGBTs was proposed in [16] for both switching loss reduction and voltage balancing of the series-connected IGBTs. A quasi-active gate control uses a simple RC network to balance the voltage in [17]. A single-gate driver for series SiC MOSFETs was designed for solid-state circuit breaker (SSCB) applications in [7,18] and the design is simple and compact. Particularly for SiC MOSFETs, other designs of single-gate drivers are reviewed in [19,20], where some of them depended on adding a more peripheral circuit to shape the driving signal or to determine the slope to mitigate electromagnetic interference (EMI) issues. A gate driver dedicated to SiC MOSFET modules is presented in [21]. Usually, voltage gate driving is used for gate driving, however, in [22] a current-source gate driver for SiC MOSFETs was developed, which contributed to less switching losses, but the development was just for an individual switch. It is a competitive solution for SiC MOSFETs where its gate capacitance is much less than for Si MOSFETs, for example.

In all previous studies, the component selection for voltage balance circuits has depended on the test conditions and no generalized design has been developed. In addition, most of the designs are not modular for duplication and use a different numbers of series MOSFETs.

The contribution of this paper is in presenting a new modular design of a single-gate driving cell able to drive a stack of series MOSFETs with a systematic design rule. The cell design was able to bias the MOSFETs gates at a negative voltage level. The design criteria of all the components are stated with LTspice simulation validation. The driven MOSFETs were able to switch voltages in the KV range with a switching transition less than 100 ns, in addition to balancing the voltage among all MOSFETs at the off-state. Zero-current switching (ZCS) was achieved during turn-off transition. The focus here was on SiC but the design can be used for other MOSFETs technologies with some value amendments. The experimental results of the designed prototype achieved coherent switching under double-pulse testing with a clamped inductive load.

2. The Proposed Driving Cell

Figure 1 shows the proposed basic driving cell for a SiC MOSFET that can be cascaded with other cells to drive series SiC MOSFETs. As shown in the figure, the circuit consists of basic passive components (2 resistors, 1 diode, 2 Zener diodes, and 1 capacitor) that provide reliability to the design against variations in temperature, frequency, and voltages spikes and do not include magnetic components that might produce EMI issues and add complexity. The footprint and selection of these components could be optimized to achieve a compact design. Figure 2 shows how three SiC MOSFETs can be driven by the cell. Each cell can provide bipolar driving, gate protection, and on- and off- state voltage balancing. The operation principle is described as follows:

2.1. Off-Steady-State Operation

Threshold voltages are lower in SiC MOSFETs compared to silicon MOSFETs and IGBTs due to their incomplete p-type dopant post-anneal activation. For dopants to become active, they must ionize and either donate their valence electrons (for n-type doping) or accept electrons (for p-type doping). The wide bandgap characteristics of SiCs make this difficult for p-type dopants. Since p-body doping is proportional to the threshold voltage, this causes a lower threshold voltage. A negative gate-drive voltage is recommended to achieve a stable and reliable off-state in SiC MOSFETs and prevent a false turn-on. In the

proposed design, the supply voltage V_s was used to bias the Zener diodes, which resulted in a negative voltage, which was, in our case, -5 V. Figure 3 shows the driving cell for two SiC MOSFETs during the off-state where N is the order of the MOSFET.

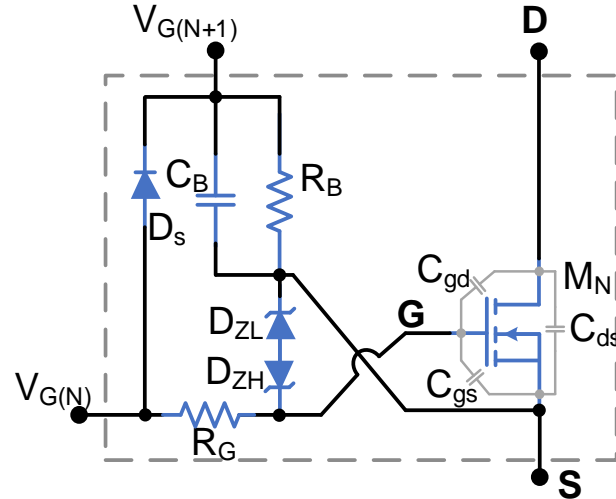


Figure 1. Proposed driving cell.

To bias the Zener diodes, a minimum current $I_{z(min)}$ should pass through the network. Each cell has two resistors (R_B, R_G) and two Zener diodes (D_{ZL}, D_{ZH}). In a proper steady state, one will be forward biased while the other is reversed, resulting in a gate–source voltage as follows:

$$V_{GS} = -(V_{D_{ZL}} + V_{D_{ZH}}) \quad (1)$$

For n number of series MOSFETs, $I_{z(min)}$ should follow:

$$I_{z(min)} = \frac{V_s - n \times (V_{D_{ZL}} + V_{D_{ZH}}) - V_{off-drive}}{n \times (R_B + R_G)} \quad (2)$$

MOSFETs have different values of leakage currents, $I_{leakage}$, even when they are forced to have a similar balanced V_{DS} . To make the design robust against the uncertainty of leakage current, the $I_{z(min)}$ was set as,

$$I_{z(min)} > 10 I_{leakage} \quad (3)$$

In case of dissimilarities of $I_{leakage}$ of MOSFETs [7], and by considering the worst case of one having $I_{leakage} = 0$ and the other having $I_{leakage}$ as a maximum from the datasheet, then the $I_{z(min)}$ will be between $9 I_{leakage} < I_{z(min)} < 11 I_{leakage}$. For our experimental tested SiC MOSFET in this paper, SCT20N120, the maximum leakage drain current was $100 \mu\text{A}$. So, the design oriented $I_{z(min)}$ to be 1 mA , which is enough to bias the Vishay Zener diodes BZX55 series [23]. The maximum number of series MOSFETs can be obtained from (4), as a function of other components values and $I_{z(min)}$ as

$$n = \frac{V_s - V_{off-drive}}{I_{z(min)} \times (R_B + R_G) + (V_{D_{ZL}} + V_{D_{ZH}})} \quad (4)$$

From MOSFET 1 to $(n - 1)$, the voltage across each MOSFET, V_{DS} will equal

$$V_{DS} = I_{z(min)} \times (R_B + R_G) + (V_{D_{ZL}} + V_{D_{ZH}}) \quad (5)$$

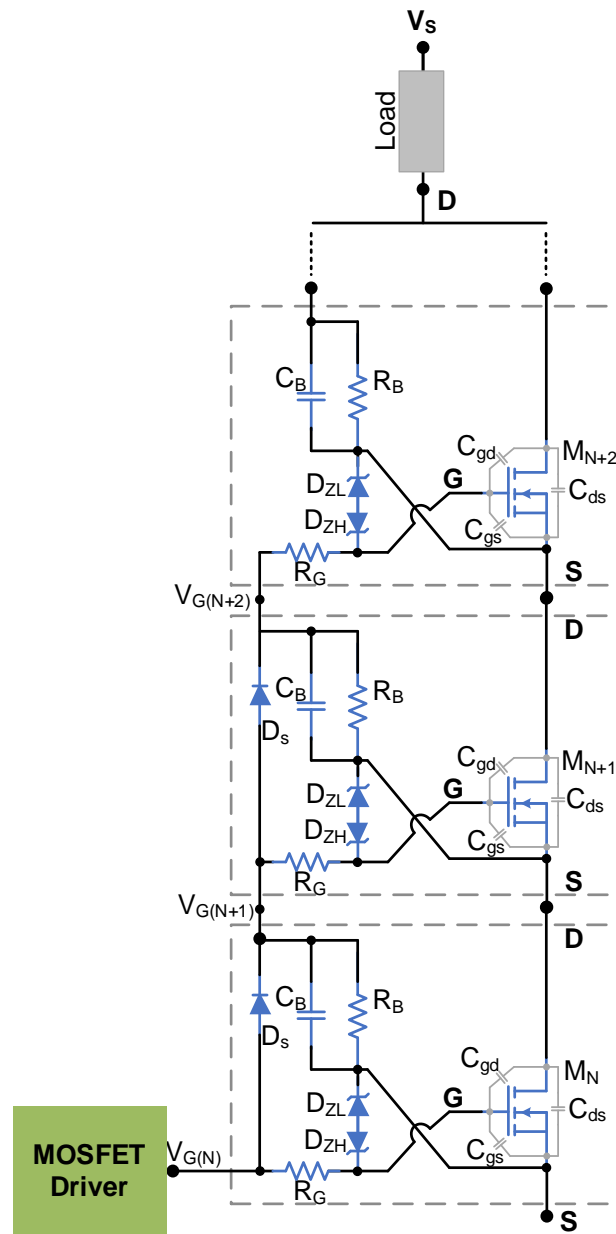


Figure 2. Cascaded driving cells.

However, for the MOSFET n ,

$$V_{DS} = I_{z(min)} \times R_B \tag{6}$$

So, the maximum steady state imbalance between MOSFET n and the other MOSFETs is

$$\Delta V_{DS(max)} = I_{z(min)} \times R_G + (V_{D_{ZL}} + V_{D_{ZH}}) \tag{7}$$

Because the design targets high-voltage applications using hundreds to thousands of volts, ΔV_{DS} is considered to be negligible. Therefore, the maximum R_B can be designed as

$$R_B = \frac{V_s - V_{off-drive} - n \times (V_{D_{ZL}} + V_{D_{ZH}}) - (n - 1) \times I_{z(min)} \times R_G}{n \times I_{z(min)}} \tag{8}$$

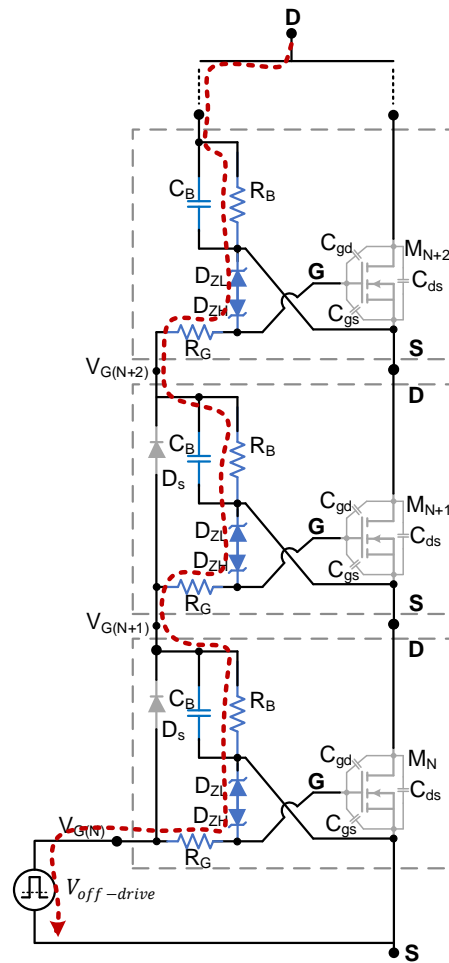


Figure 3. Off-steady-state. The arrow illustrates the current flow while all MOSFETs are off.

2.2. Turn-On Transition

The analysis explained in this section for the voltage and current waveforms and switching transitions was based on a clamped inductive load in the commonly used double-pulse testing. Three SiC MOSFETs were assumed in this analysis to emphasize its modular operation if more MOSFETs are stacked. The turn-on transition is divided into three main stages. Figure 4 shows the current paths during the turn-on transition stages for the three MOSFETs. Figure 5 illustrates the gate-to-source voltage (V_{GS}), the drain-to-source voltage (V_{DS}), the drain currents (I_D), and the gate resistance current (I_{RG}) during the transition.

Stage 1 (S1): It was assumed that before this stage starts, all switches are off and the shared supply voltage is $\frac{V_s}{n}$ across each MOSFET and the V_{GS} is at a negative value. A turn-on signal is given by the gate driver to the first MOSFET, $M(N)$. The gate voltage starts rising, passing the threshold voltage while the MOSFETs are still in the off-state. The voltage across MOSFET $M(N)$, $V_{DS M(N)}$, is at a high voltage and the current $I_{D M(N)}$ is zero. The gate current is dominated by the current through the resistor $R_{G M(N)}$ and Figure 5 shows the current $I_{RG M(N)}$, which follows Equation (9).

$$V_{on-drive} - I_{RG M(N)} \times R_{G M(N)} - V_{GS M(N)} = 0 \tag{9}$$

The diode $D_{M(N)}$ is in the off-state as the voltage across the $C_{B M(N)}$ is still higher than the drive voltage. The Zener diodes also will not operate as the drive voltage is lower than the protection threshold (+22 V).

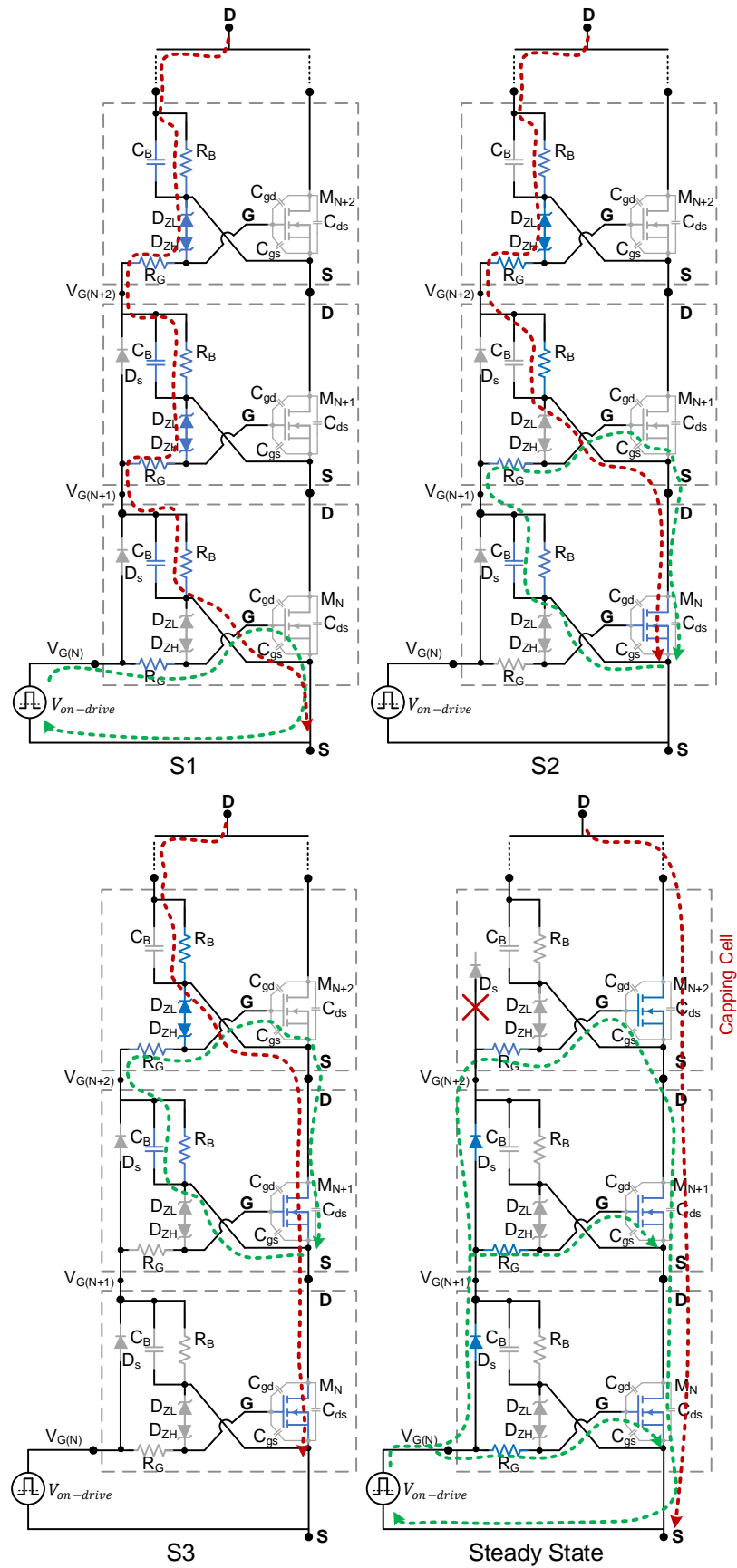


Figure 4. Main current paths during turn-on while the circuit transitions from stage 1 (S1) to steady state. Red path denotes the drain current and green path denotes the gate–source current.

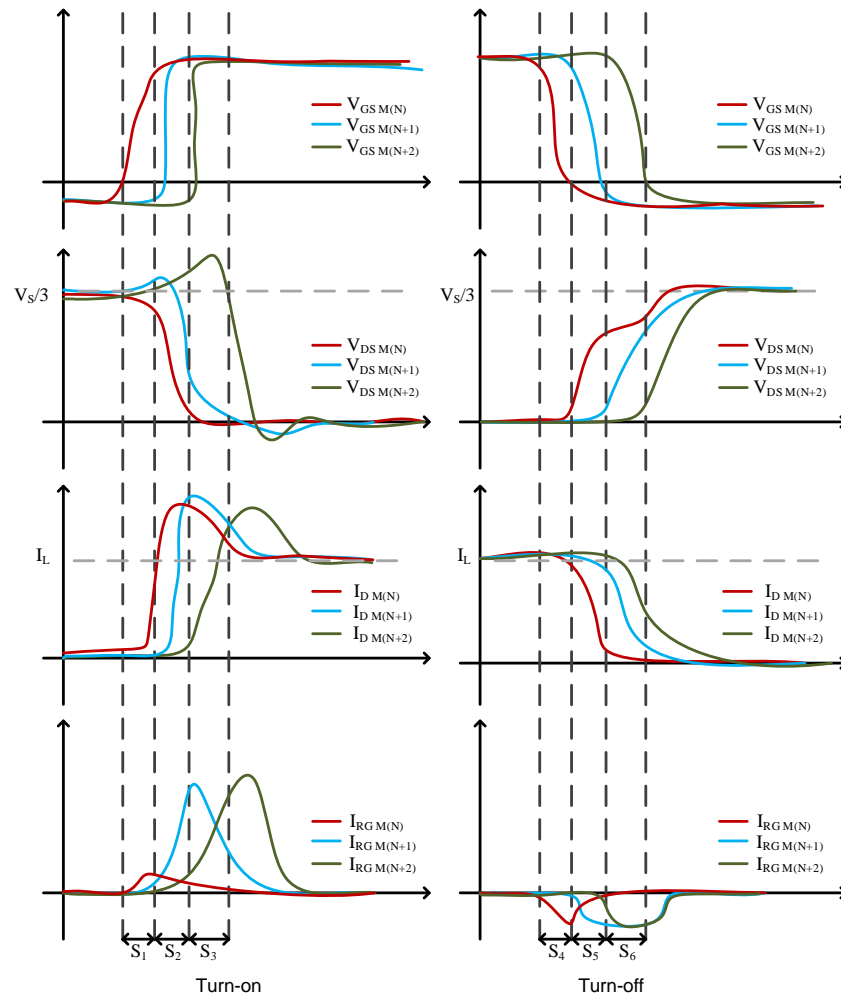


Figure 5. Analytical waveforms during turn-on and turn-off transitions.

Stage 2 (S2): At the beginning of stage 2, the current $I_{D M(N)}$ starts to rise while the voltage $V_{DS M(N)}$ of MOSFET $M(N)$ starts to fall, bringing the source node of MOSFET $M(N + 1)$ to a lower voltage than the drain node, which is illustrated by an overshoot of its voltage $V_{DS M(N+1)}$. The maximum voltage can be estimated as

$$V_{DS M(N+1),max} = R_{B M(N+1)} \times I_{D M(N)} \tag{10}$$

where

$$I_{D M(N)} = g_m \times (V_{GS M(N)} - V_{GS(th) M(N)}) \tag{11}$$

At the same time, the capacitor $C_{B M(N)}$ will have a new current path to discharge through the gate-to-source capacitance of $M(N + 1)$, allowing $V_{GS M(N+1)}$ to rise followed by a rise in its current $I_{D M(N+1)}$ and a fall in its voltage $V_{DS M(N+1)}$. The discharging current of capacitor $C_{B M(N)}$ is determined by the change in voltage at the source node of $M(N + 1)$ caused by the $R_{ds(on) M(N)}$ and the gate capacitance charge of $M(N + 1)$, in addition to the value of $R_{G M(N+1)}$. A basic illustration of the discharging circuit is shown in Figure 6. The peak current through $R_{G M(N+1)}$ can be calculated by Equation (12) with the assumption of the worst case of a complete change in $V_{DS M(N)}$ from V_s/n to zero.

$$I_{G M(N+1),max} = (C_{B M(N)} // C_{GS M(N+1)}) \times \frac{V_s/n}{t_{on M(N)}} \tag{12}$$

where t_{on} is the turn-on switching time and n is the number of MOSFETs. Obviously, a larger C_B produces a higher peak current, which is required for charging C_{GS} in a fast manner. However, large capacitance leads to a longer time to balance the voltages at the off-state and reach a steady state. Furthermore, it increases the switching loss when its cell MOSFET is on through its $R_{ds(on)}$.

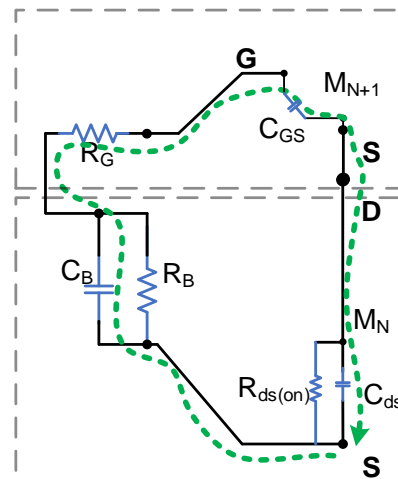


Figure 6. Discharging circuit to turn on MOSFET $M(N+1)$.

Stage 3 (S3): Similar to stage 2, when MOSFET $M(N+1)$ is turned on, the voltage at the source node of $M(N+2)$ drops. Consequently, the capacitor $C_{B M(N+1)}$ discharges and the time constant is determined by the value of the path capacitances, $R_{G M(N+2)}$ and $R_{B M(N+1)}$. Larger values of R_G and R_B increase the time of discharge, keep V_{GS} steadier and dissipate less power, but this will disturb the turn-off operation dynamics.

At steady state and when all MOSFETs are on, diode $D_{s M(N)}$ is used to prevent $V_{GS M(N+1)}$ from dropping because its gate capacitances will discharge through $R_{G M(N+1)}$ and $R_{B M(N)}$. Therefore, $D_{s M(N)}$ keeps supplying a minimal steady state current. A similar case is for $D_{s M(N+1)}$ in keeping $V_{GS M(N+2)}$ at sufficient gate voltage level. The current through the diode in each cell (N) is calculated based on Equation (13)

$$I_{D_s M(N)} = \frac{V_{on-drive} - V_{D_s} \times (n-1)}{R_{B M(x)}} \quad (13)$$

where V_{D_s} is the forward voltage drop across the diode D_s . Larger $C_{B M(N)}$ capacitance provides a steadier $V_{GS M(N+1)}$, but it will deteriorate the turn-off time.

As is shown in Figure 4, the last driving cell for $M(N+2)$ has no supply diode D_s because it will create a current path from the driver through $D_{s M(N, N+1, \dots)}$ to the top drain node, which has a low voltage due to the MOSFETs being on. This will draw a significant current and decrease the capability of the driver to keep all MOSFETs at the on-state properly. For this reason, a “Capping Cell” was proposed, which has the same structure but with no supply diode.

2.3. Turn-Off Transition

Figure 5 shows the transition during the turn-off, and it is divided into three stages. Similarly, the current paths during each stage are shown in Figure 7.

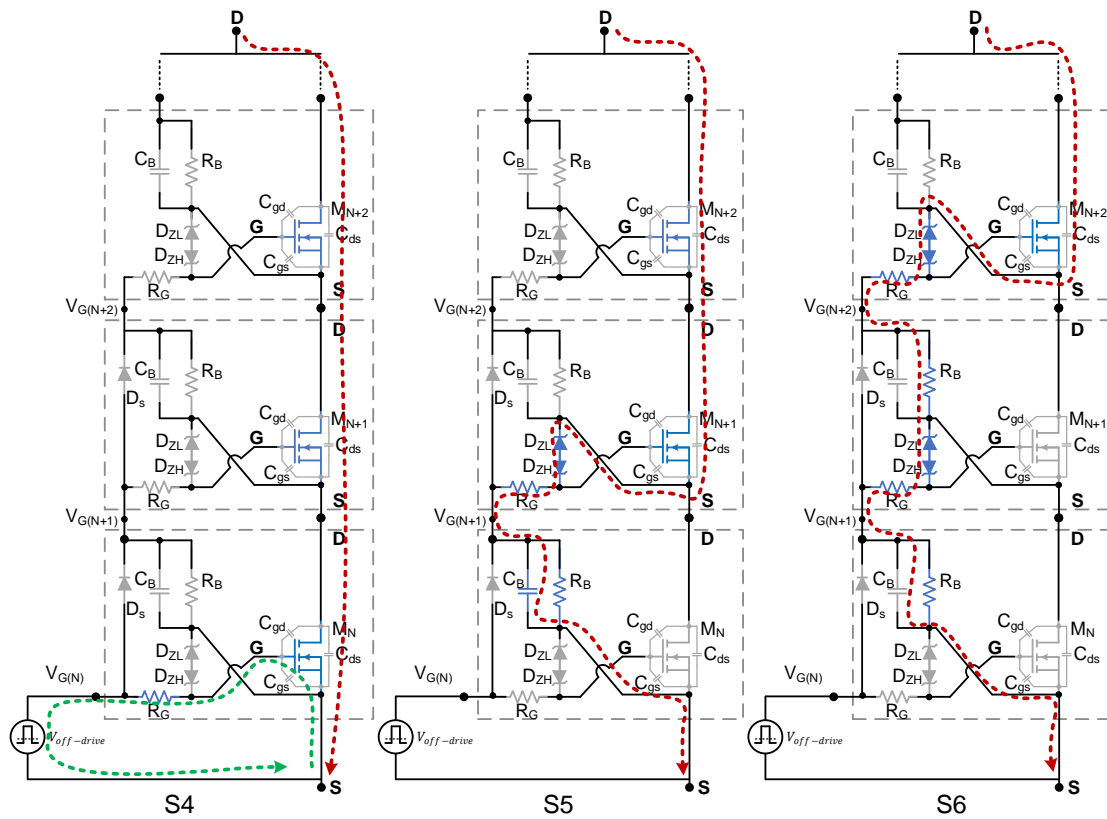


Figure 7. Main current paths during turn-off.

Stage 4 (S4): Before this stage, it was assumed that all MOSFETs are in an on steady state and they are conducting the current from the top drain node to the bottom source node through their on-state resistances. At this stage, a negative driving voltage is generated by the driver, $V_{off-drive}$ and is discharging the gate capacitance $C_{GS M(N)}$ through $R_{G M(N)}$. The current through the resistance is as follows.

$$I_{R_{G M(N)}} = \frac{V_{off-drive} - V_{GS M(N)}(0)}{R_{G M(N)}} \quad (14)$$

where $V_{GS M(N)}(0)$ is the initial voltage across the gate–source of MOSFET $M(N)$. While the current $I_{R_{G M(N)}}$ rises, as shown in Figure 5, the gate voltage drops.

Stage 5 (S5): The gate voltage $V_{GS M(N)}$ drops to a level below the threshold voltage and the voltage $V_{DS M(N)}$ starts rising while the current $I_{D M(N)}$ starts dropping, turning off MOSFET $M(N)$ completely. The I_D through MOSFETs $M(N + 1)$ and $M(N + 2)$ is commutated through the Zener diodes $D_{Z M(N+1)}$, the gate resistor $R_{G M(N+1)}$, and the balance resistance $R_{B M(N)}$ to the source terminal, as shown in Figure 7. This current will charge $C_{B M(N)}$, making the voltage across the MOSFET $M(N)$ increase slowly to realize ZCS. This current will also bias the Zener diode to produce a negative voltage equal to $V_{D_{ZL M(N+1)}}$ across the $C_{GS M(N+1)}$. The applied voltage will start turning off the $M(N + 1)$ MOSFET. It is worth mentioning here that $R_{B M(N+1)}$ should be selected to pass the minimum Zener current, $I_{z(min)}$. It is important to keep the switching time as short as possible to avoid higher dissipation when I_D flows through the Zener diodes.

Stage 6 (S6): Similar to S5, after turning off $M(N + 1)$ MOSFET, the current I_D passes through a series of Zener diodes, R_G 's and R_B 's, to the source node as shown in Figure 7. This will bias the Zener diode $D_{ZL M(N+2)}$ to turn off the $(N + 2)$ MOSFET. Here, the combination of R_B 's should be able to pass the $I_{z(min)}$ through all Zener diodes. The balance capacitors achieve turn-off soft switching, which is crucial for applications such as SSCBs.

3. Parameter Calculations

3.1. Parameter Calculation of R_B

As shown in Equation (8), R_B is responsible for proper Zener diode biasing during the turn-off transition. A large value of R_B limits the number of stacked SiC MOSFETs in series due to inability to bias the Zener diodes for a particular source voltage. A small value of R_B limits the number of stacked SiC MOSFETs in series due to the significant power dissipation at the off steady state if a high voltage is present across C_B . Figure 8 shows combined plots for the limitations brought by the Zener diode currents $I_{z(min)}$ and $I_{z(max)}$ on the number of stacked MOSFETs when $10\text{ k}\Omega \leq R_B \leq 100\text{ k}\Omega$. In addition, it shows the power dissipation brought by a resistor value for different numbers of stacked MOSFETs when $n = [2 : 10]$. The selected source voltage for these calculations was $V_s = 2500\text{ V}$. Obviously, at least four stages, $n = 4$, are required to fulfil the Zener diodes biasing requirements. It is important to assume that four MOSFETs have a total rating more than the operating $V_s = 2500\text{ V}$. Otherwise, more cells are required. In our example, each MOSFET had a maximum voltage of 1200 V and in total, this was $4 \times 1200\text{ V} > 2500\text{ V}$. If 5 W is selected as an example of a maximum resistor power in the design due to size considerations, the red line in Figure 8 depicts the resistor values limits and shows that the best resistor value, denoted by the red circle, for the least number of stages, was $R_b \geq 80\text{ k}\Omega$ with $n = 4$.

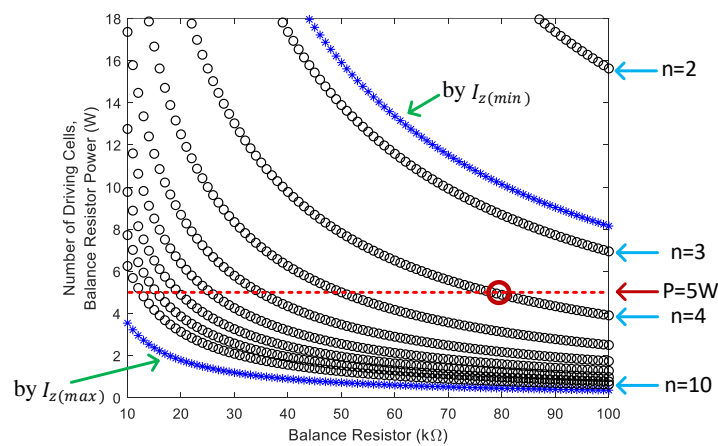


Figure 8. Balance resistor R_B in relation with n and P_{R_B} .

A simulation was conducted for $n = 4$ and R_B being set to three different values (50, 80, and 100 kΩ) and the turn-on and turn-off times for each MOSFET were measured and are listed in Table 1. For the tested case, the impact of R_B on the t_{on} and t_{off} was negligible. However, it significantly increased the steady state off-time when R_B increased. Figure 9 shows the instantaneous power and voltage waveforms during the turn-off transition when $R_B = 100\text{ k}\Omega$ and $200\text{ k}\Omega$. The total turn-off time was slightly affected but the power peak increased from 3.85 kW to 4.7 kW , which increased the total energy loss.

Table 1. Impact of changing R_B .

Test Conditions: $C_B = 100\text{ pF}$, $V_s = 2500\text{ V}$, $n = 4$										
R_B	$t_{on M(N)}$	$t_{on M(N+1)}$	$t_{on M(N+2)}$	$t_{on M(N+3)}$	$t_{off M(N)}$	$t_{off M(N+1)}$	$t_{off M(N+2)}$	$t_{off M(N+3)}$	t_{ss-off}	
50 kΩ	38 ns	32 ns	29 ns	33 ns	23 ns	23 ns	24 ns	24 ns	23 μs	
80 kΩ	37 ns	32 ns	29 ns	33 ns	23 ns	23 ns	23 ns	24 ns	36.5 μs	
100 kΩ	36 ns	31 ns	28 ns	33 ns	20 ns	21 ns	22 ns	23 ns	46 μs	

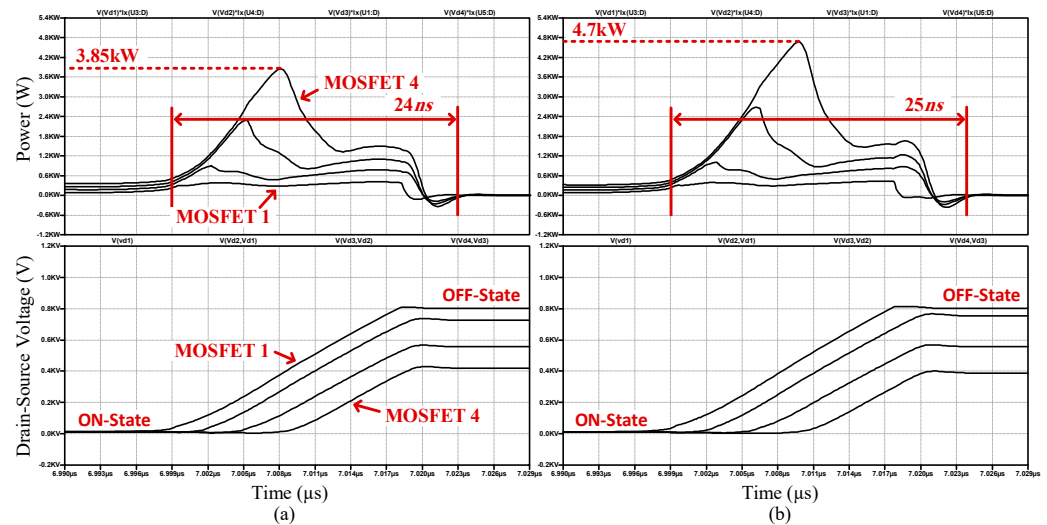


Figure 9. The simulated instantaneous power and voltage waveforms during turn-off transition when (a) $R_B = 100 \text{ k}\Omega$ and (b) $R_B = 200 \text{ k}\Omega$.

3.2. Parameter Calculation of C_B

As discussed previously, C_B is responsible for charging the next stage MOSFET gate, and the dynamics of charging the gate of MOSFET $M(N + 1)$ is dominated by the turn-on transition of MOSFET $M(N)$ and how the voltage at the drain node drops to the source node. Large values will delay the MOSFETs in balancing the supply voltage when they are turned off. In addition, this increases the switching time and losses.

Table 2 shows how higher C_B values increased the steady state time at the off-state. It increased the turn-on time by 45% and the turn-off time by 100%. The value of $C_B = 20 \text{ pF}$ provided the shortest time. However, even with a shorter on-transition, the instantaneous power and V_{DS} waveforms had high peaks during the on-transition, as shown in Figure 10, which might exceed the MOSFET rating and incur a high value of $\frac{dV_{DS}}{dt}$. The top device needs to be avalanche-rugged to withstand this voltage and additional losses from repetitive avalanches might break it down. During turn-off, the $E_{off-loss \text{ Total}}$ was the highest because it had a high instantaneous power peak, as shown in Figure 11. The figure also shows the non-uniform voltage dynamics compared with the case of $C_B = 100 \text{ pF}$, where less power peaks, uniform dynamics among all MOSFETs and soft switching were achieved. Therefore, the selection of C_B is a trade-off between the turn-on voltage overshoot, steady state and the switching loss.

It is worth mentioning that the peak voltage of MOSFET 4, in Figure 10, could be reduced significantly by selecting a higher value of C_B compared with the other cells. This allowed a smoother turn-on for MOSFET 4 as the capacitor absorbed the load current while the voltage increased. Figure 12a shows the turn-on transition when $C_B = 500 \text{ pF}$ for the $M(N + 3)$ cell while keeping the others with a value of $C_B = 20 \text{ pF}$. The peak voltage was then within 1.1 kV. However, this sacrificed the settling time during the off-time as shown in Figure 12b and consequently the switching frequency. The designer might tailor this value according to the application.

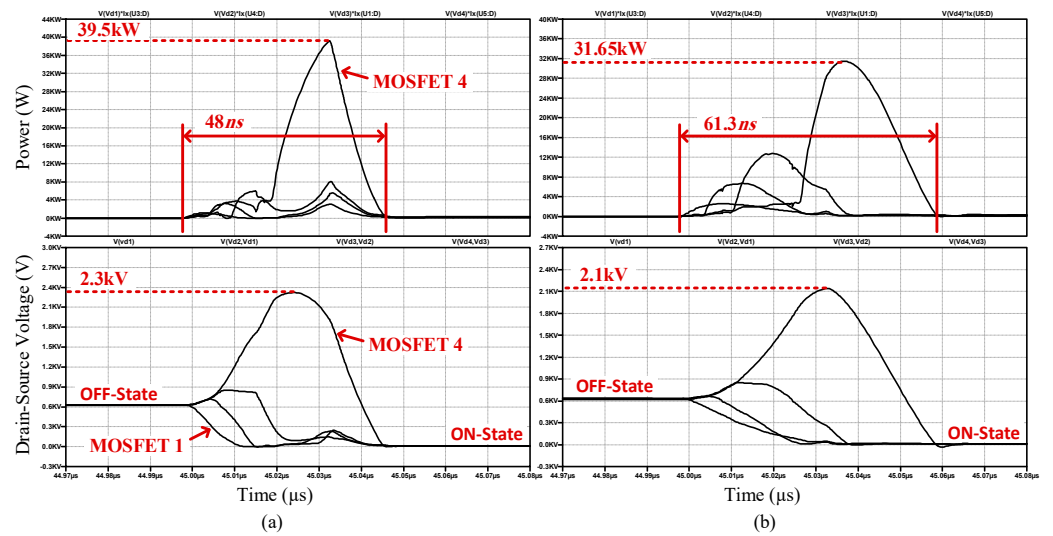


Figure 10. Simulated instantaneous power and voltage waveforms during turn-on transition when $R_B = 80 \text{ k}\Omega$ and (a) $C_B = 20 \text{ pF}$, (b) $C_B = 100 \text{ pF}$.

Table 2. Impact of changing C_B .

C_B	t_{ss-off}	$t_{on\ Total}$	$t_{off\ Total}$	$E_{on-loss\ Total}$	$E_{off-loss\ Total}$
20 pF	13 μs	48 ns	17.8 ns	878.42 μJ	131.85 μJ
50 pF	20 μs	55 ns	20.4 ns	908.87 μJ	102.46 μJ
100 pF	26 μs	61.3 ns	23.6 ns	1077.84 μJ	78.09 μJ
150 pF	37 μs	67.5 ns	31.23 ns	1247.21 μJ	71.97 μJ
200 pF	53 μs	70.4 ns	35 ns	1362.59 μJ	65.65 μJ

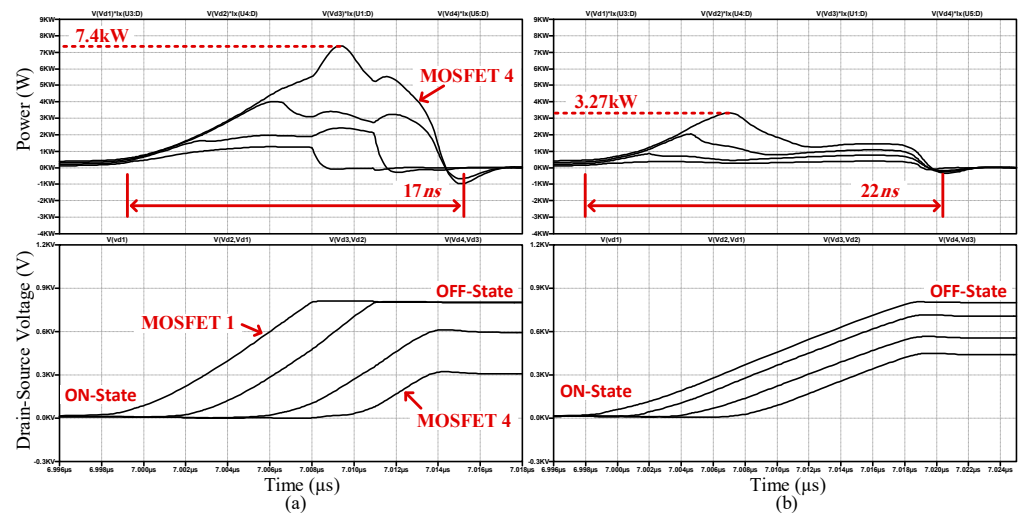


Figure 11. Simulated instantaneous power and voltage waveforms during turn-off transition when $R_B = 80 \text{ k}\Omega$ and (a) $C_B = 20 \text{ pF}$, (b) $C_B = 100 \text{ pF}$.

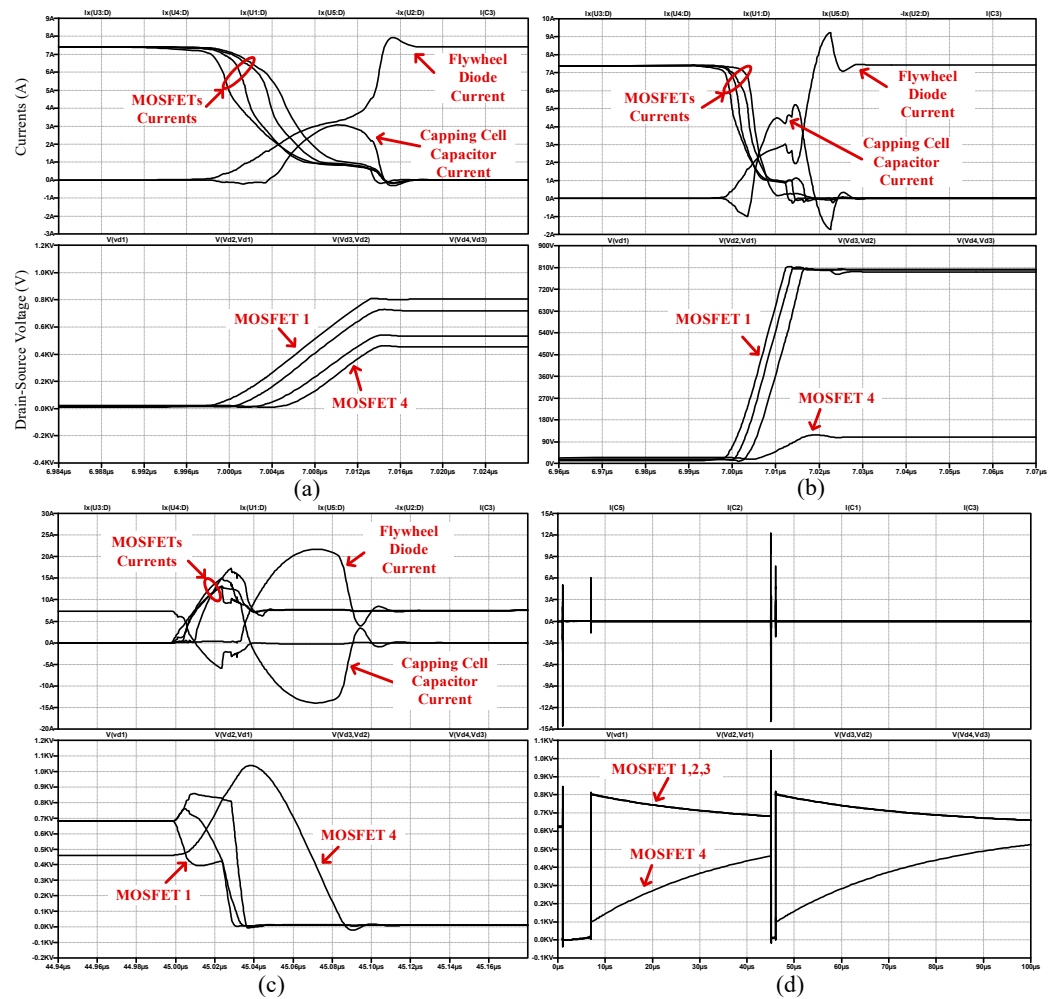


Figure 12. Simulated MOSFETs voltages and capping capacitor current when (a) $R_B = 80 \text{ k}\Omega$ and $C_B = 20 \text{ pF}$ for the capping cell, (b–d) $C_B = 500 \text{ pF}$ for the capping cell.

3.3. Parameter Calculation of R_G

Figure 13 shows the inclusion of stray inductances within the driving circuit. L_{gs} represents the gate inductance induced by the printed circuit board tracks and terminal lengths. L_{ss} represents the lamped source and drain inductance of adjacent MOSFETs. The path capacitances and inductances will resonate if R_G does not provide enough damping. By neglecting R_B , due to its large value and R_{ds-on} because it is not a design parameter that can be fixed, and it is also very small, the damping factor of the circuit is:

$$\zeta = \frac{R_G}{2} \times \sqrt{\frac{C_{gs}}{L_{gs} + L_{ss}}} \tag{15}$$

To prevent oscillation, ζ should be greater than 1, therefore, R_G is selected to satisfy.

$$R_G > 2 \times \sqrt{\frac{L_{gs} + L_{ss}}{C_{gs}}} \tag{16}$$

Furthermore, it is worth mentioning here that the R_G value should not be selected to be large because it will increase the switching loss and slow down the MOSFET switching in addition to disturbing the Zener diode biasing at turn-off. Usually, resistors can withstand high peak currents for short times, i.e., during turn-off transitions.

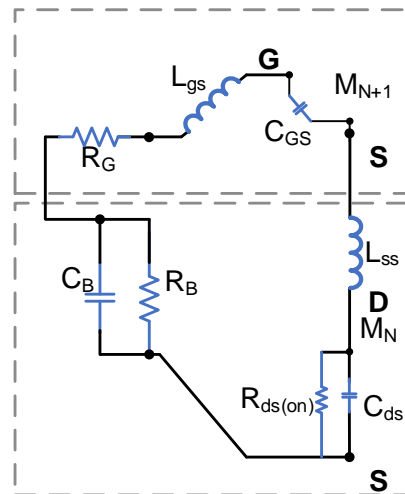


Figure 13. The stray inductances in the driving circuit.

3.4. Parameter Calculation of D_s

The supply diodes provide a continuous charge for the balance capacitors C_B during the turn-on steady state for all MOSFETs. In the proposed topology, the diodes are connected in series. Therefore, the final voltage at each cell drops with the increase in cell number. If we assume that each MOSFET needs at least $2 \times V_{GS(th)}$ to keep it in a proper conduction with minimal $R_{DS(on)}$, then the maximum number of cascaded cells will follow:

$$n < \frac{V_{on-drive} - 2 \times V_{GS(th)}}{V_{D_s(max)}} \quad (17)$$

where V_{D_s} is the forward voltage drop across the supply diode. For the used diode in the experimental setup, i.e., the US1M diode, the voltage drop was 1.7 V at a current of 1 A and the $V_{GS(th)}$ for the MOSFET was 3.5 V and $V_{on-drive} = 20$ V. Therefore, $n \leq 7$. By replacing the diode with a low voltage drop, the number of possible cascaded cells will increase.

4. Simulation Verification

LTspice was used to simulate three stacked MOSFETs in series. The modelled SiC MOSFET was C2M1000170D. Wolfspice provided the spice model. A double-pulse test (DPT) with a clamped inductor load was simulated. The circuit is shown in Figure 14 and the simulation values are shown in Table 3. The source voltage was chosen to be $V_s = 350$ V to mimic the experimental setup, which had a maximum voltage of 350 V due to the available sources.

Table 3. Parameters for the tested setup.

Component	Value	Component	Value
V_s	1200 V	D_{ZL}	6.8 V
L_{Load}	1800 μ H	D_{ZH}	22 V
D_{FW}	STPSC1206	D_s	US1M ULTRA-FAST 700 V, 1 A
C_B	300 pF	R_G	1.5 Ω
R_B	10 k Ω	MOSFETs	SCT20N120 SiC

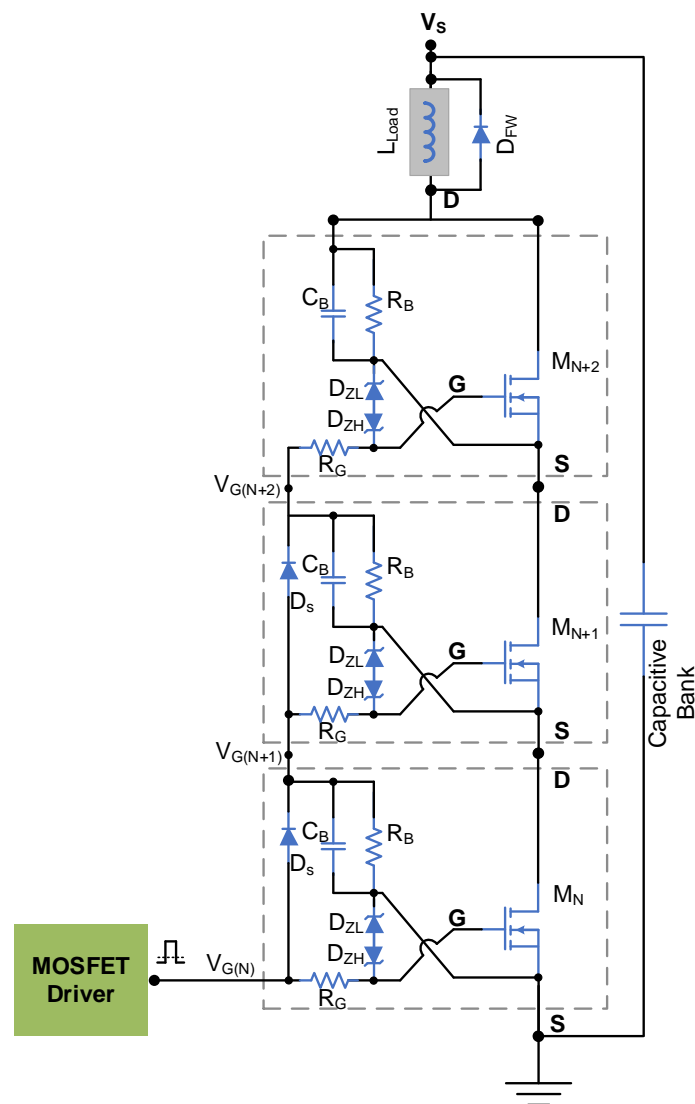


Figure 14. The proposed topology for simulation and experimental testing.

The DPT waveforms are shown in Figure 15 including the gate–source voltages, the drain–source voltages, drain currents, and instantaneous power. The results depicted a balanced voltage sharing at the off steady state. In addition, it showed consistent dynamics of voltage and current among all the MOSFETs. The maximum voltage during the turn-on transition was 320 V.

Figure 16 shows how the supply diodes D_s shaped the gate voltages. Figure 16a is the normal proposed topology with populated supply diodes for each driving cell except the capping cell. The results in Figure 16b are shown for the design without any supply diodes. The balance capacitors kept discharging and this might have driven the MOSFETs to a linear region. Figure 16c is when the capping cell supply diode was populated, and it shows how the voltages were clipped differently with a difference between each cell equal to the Zener diode (6.8 V).

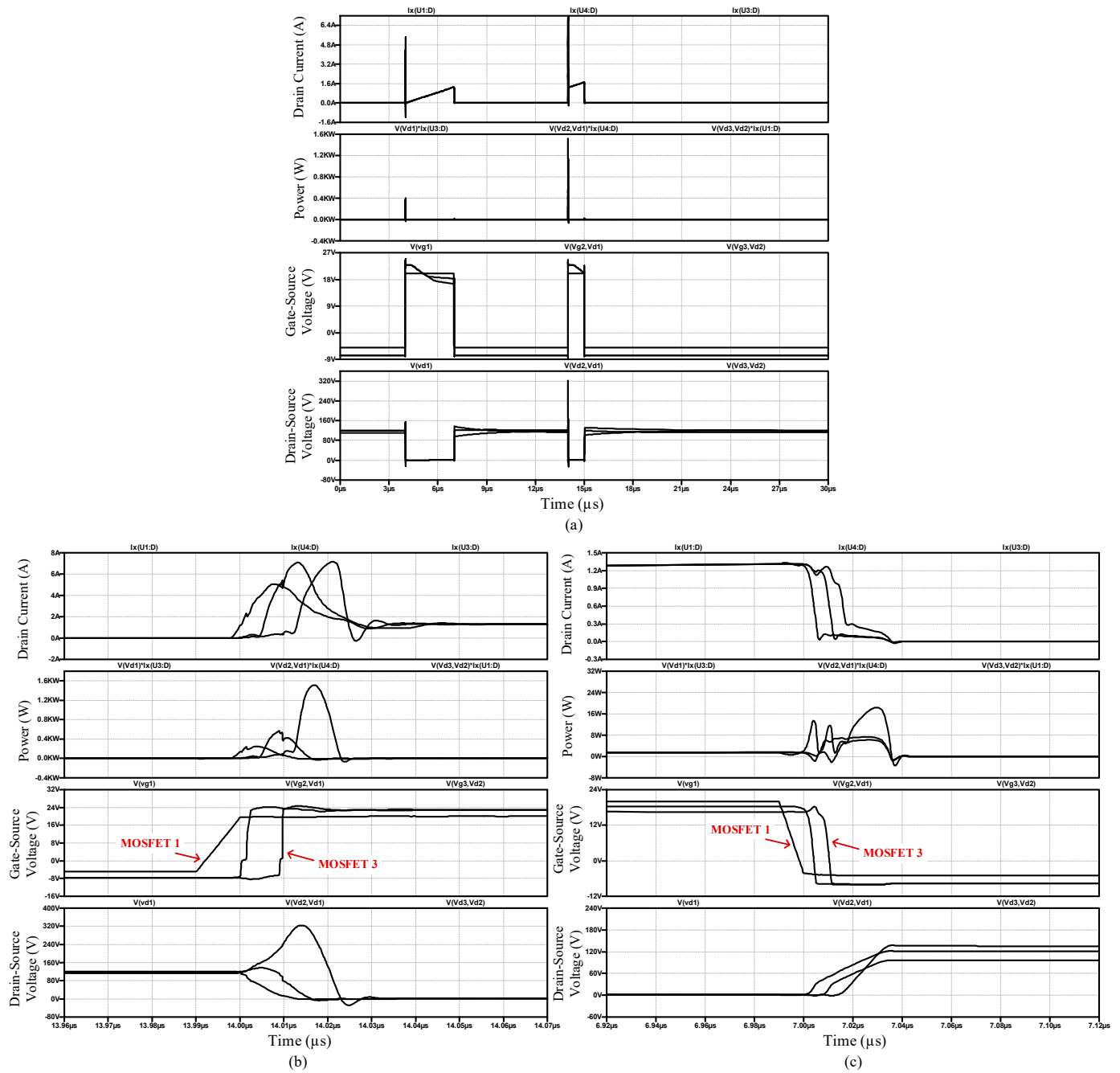


Figure 15. Simulation results: (a) DPT simulation, (b) turn-on zoom, and (c) turn-off zoom.

As shown and discussed, the single gate-drive approach proposed switches the series-connected SiC-MOSFETs in a sequential manner. To compensate for the transient switching speed differences among the individual SiC-MOSFETs, some adjustments to the values of auxiliary capacitors could be made.

Figure 17 shows how the capping cell-balance capacitor, C_B , affected the transient time and the voltage peak. Figure 17a shows a similar balance capacitor for all cells (300 pF), while in Figure 17b, the capping cell capacitor is reduced alone to 100 pF. A faster response was achieved but with a higher turn-on voltage peak for the MOSFET $M(N + 2)$. The selection of C_B also impacted the maximum switching frequency. Therefore, a trade-off should be considered here.

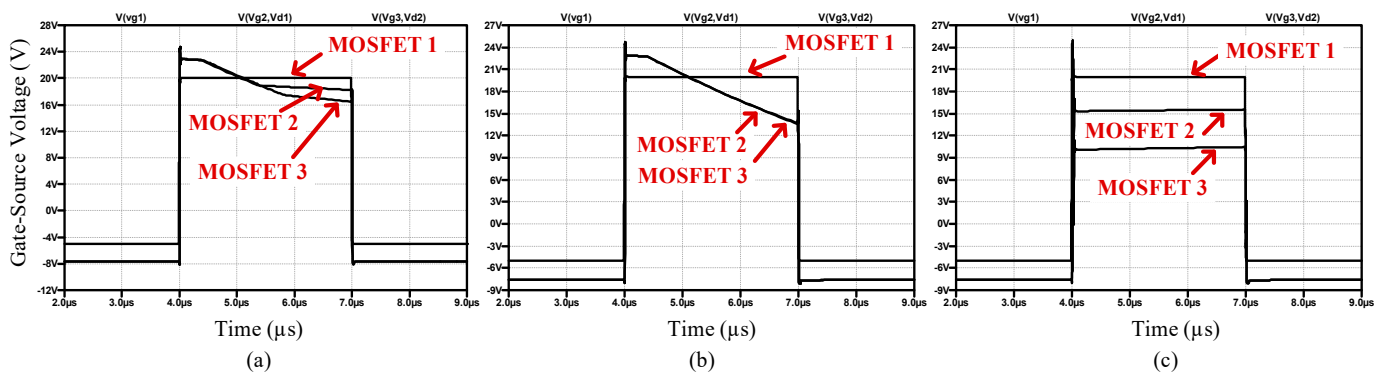


Figure 16. Gate–source voltage when supply diodes: (a) are populated except the last cell, (b) are not populated, and (c) are populated for all cells.

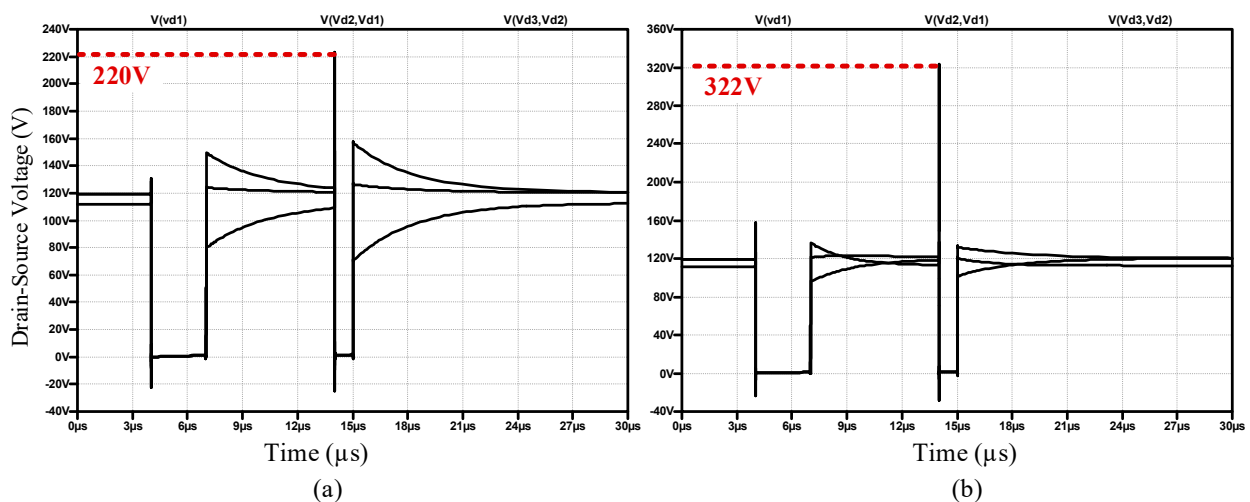


Figure 17. Drain-to-source voltage during the DPT when (a) $C_B = 300$ pF and (b) $C_B = 100$ pF.

5. Experimental Results

The proposed topology was built and tested experimentally to validate the design. The circuit was as shown in Figure 14, and the experimental setup is shown in Figure 18. The setup was composed of three series SCT20N120, 1200 V, 20 A MOSFETs. The conducted test was a DPT with a load inductance of 1800 μ H and the freewheeling diode was a STPSC1206 Schottky silicon carbide diode. The PCB boards were designed in a modular manner and could be soldered together to stack different numbers of MOSFETs. The power supply was a 350 V DC source with a bulk capacitor array. The detailed experimental setup components are listed in Table 3. Micsig differential voltage and current probes were used with a 100 MHz bandwidth. The DPT signals were produced by a microcontroller.

Figure 19a shows the experimental results for the DPT. Obviously, the proposed circuit was able to turn on and off the three series MOSFETs successfully. Each MOSFET shared an almost equal voltage during the turn-off steady state. The differences were due to the voltage drop across the Zener diodes. The gate voltages were supplied by a negative voltage when they were off.

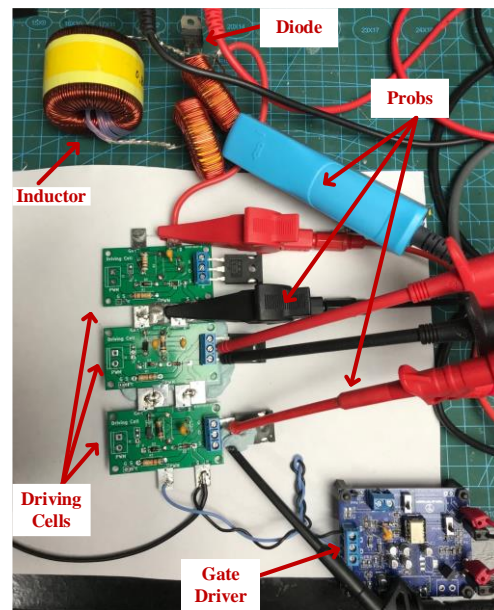


Figure 18. Experimental setup.

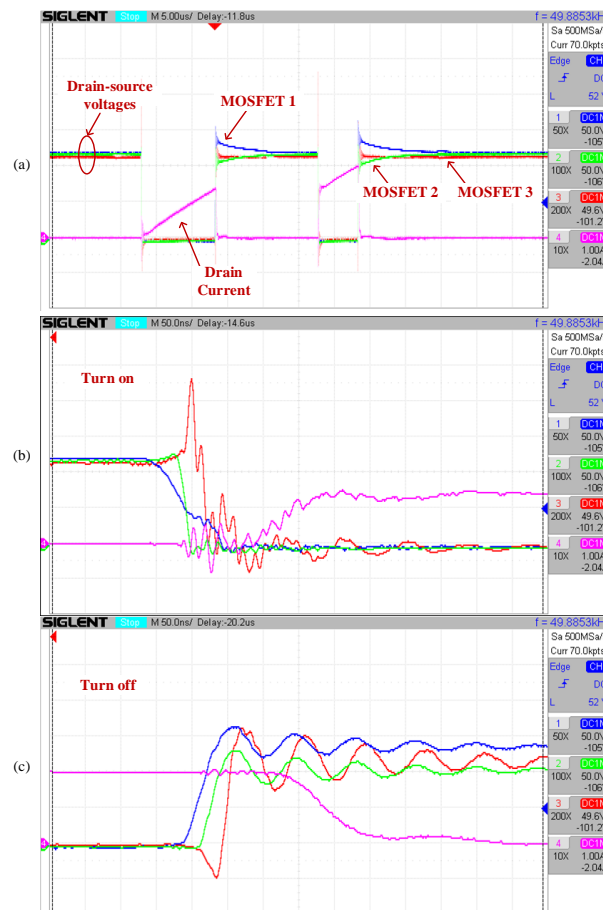


Figure 19. Experimental results: (a) DPT test, (b) turn-on zoom, and (c) turn-off zoom.

Figure 19b shows a zoomed-in view of the turn-on transition. The maximum voltage of MOSFET $M(N + 2)$ was 227 V, which was similar to the simulation results. The total turn-on transition was 96 ns, while the turn-off transition was 87 ns, as shown in Figure 19c.

The oscillation was caused by the stray inductance. The results confirmed the analysis and design.

The main advantage of this gate-drive strategy is that a single gate driver is required to switch more than one device since the energy stored in the balance capacitors are used to charge and discharge the gate capacitances in subsequent devices. This is unlike other designs that require each device in a series configuration to be driven by a dedicated gate driver. The design also provides flexibility in mitigating higher voltage stresses on MOSFETs by the proper selection of the switching capacitors.

The voltage blocked for each device will be, as a maximum, the ratio of the DC link voltage and the number of devices (V_{DC}/n). The ratio of this voltage to the intrinsic breakdown voltage of the device (V_{DC}/V_{BRn}) will determine the headroom for each device and, hence, the additional voltage each device can block under voltage imbalance conditions. If a small capacitor is used for the capping cell, more MOSFETs can be considered to further distribute the switched voltage while switching.

6. Conclusions

In this paper, a modular switching capacitor-based driving cell was proposed to drive series SiC MOSFETs. The proposed circuit did not require any active components and could be driven by a single gate driver. The proposed driving cells were able to provide negative voltages during the off-states and sufficient charge during the on-transition. The analysis of the proposed topology validated its modular aspects and highlighted its limitations and criteria of component selection. The balance capacitor was key for the settling time and voltage overshoot adjustments. LTspice simulations for three and four MOSFETs were conducted. The experimental prototype for three MOSFETs in series approved the validity of the design with a less than 100 ns transition and coherent switching. The potential of this topology can be applicable for high-voltage circuit breakers and high-stressed MOSFETs in power supplies.

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