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Controller Platform Design and Demonstration for an Electric Aircraft Propulsion Driv

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Controller Platform Design and Demonstration for an Electric Aircraft Propulsion Drive

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ABSTRACT

With the growth in the aerospace industry there has been a trend to optimize the performance of an aircraft by reducing fuel consumption and operational cost. Recent advancements in the field of power electronics have pushed towards the concepts of hybrid electric aircraft also known as more electrical aircrafts. In this work, a custom controller board for an electric aircraft propulsion drive was designed to drive a permanent magnet synchronous motor. Design of the controller board required knowledge of the topology selection and power module selections. Simulations of the system were performed using MATLAB/Simulink to analyze the overall performance of the selected topology. Implementation of the control algorithm was tested on the hardware prototype of a three-phase, two-level voltage source inverter. Complete testing of the system at high power was accomplished; thus, demonstrating the inverter's ability to operate at the desired power level.

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DEDICATION

I dedicate this thesis to my family, thank you for your endless support and encouragement.

TABLE OF CONTENTS

CHAPTER 1 1
INTRODUCTION 1
1.1 Introduction 1
1.2 Research Background 1
1.3 Challenge and Research Objective 2
1.4 Requirements from Ampaire 3
1.5 Thesis Outline 4
1.6 References 5
CHAPTER 2 6
SYSTEM MODELING OF PERMANENT MAGNET SYNCHRONOUS MOTOR 6
2.1 Introduction 6
2.2 Mathematical Model of Permanent Magnet Synchronous Motor 7
2.3 Equivalent Circuit of a PMSM 8
2.4 PMSM Control Strategies 8
2.4.1 Scalar Control 9
2.4.2 Direct Torque Control 9
2.4.3 Field Oriented Control 10
2.5 Coordinate Transformation 11
2.6 Clarke Transformation 12
2.7 Park Transformation 13
2.8 Voltage Source Inverter 14
2.9 Modulation Techniques 15
2.10 Sinusoidal Pulse Width Modulation 16
2.11 Space Vector Modulation 18
2.12 Determining V_{ref} and θ 19
2.13 Determining Switch Duration T_a, T_b, T_0 20
2.14 References 22
CHAPTER 3 23
SIMULINK MODEL OF THE CONTROL ALGORITHM 23
3.1 Introduction 23

3.2 Permanent Magnet Synchronous Motor Model 23
3.3 Clarke Transformation 24
3.4 Park Transformation 24
3.6 Space Vector PWM 26
3.7 Voltage Source Inverter 27
3.8 Simulation Results 28
3.9 References 31
CHAPTER 4 32
REAL TIME HARDWARE IN THE LOOP SIMULATIONS 32
4.1 Introduction 32
4.2 Typhoon HIL schematic editor 34
4.3 Program Implementation 37
4.4 PWM Configuration 38
4.5 ADC Configuration 41
4.6 Clarke Transformation code 42
4.7 Park Transformation code 43
4.8 Inverse Park code 44
4.9 Space Vector Pulse Width Modulation 44
4.10 Simulation Results 46
4.11 Reference 49
CHAPTER 5 50
CONTROLLER HARDWARE DESCRIPTION PROCESS 50
5.1 Introduction 50
5.2 Controller Selection 50
5.3 Gate Driver Interface 52
5.4 Resolver to Digital Converter 54
5.5 Power Supplies 56
5.6 CAN Interface 56
5.7 Current measurement 58
5.8 DC link Voltage Sensing 59
5.9 Throttle Signal 59

5.10 References 60
CHAPTER 6 61
CONTROLLER BOARD PCB LAYOUT 61
6.1 Introduction 61
6.2 Schematic 61
6.3 Component Placement Controller Board V.1 63
6.4 Testing the Prototype with the Controller board V1 66
6.5 References 69
CHAPTER 7 70
EXPERIMENTAL STUDIES AND PERFORMANCE VERIFICATION 70
7.1 Introduction 70
7.2 Vibration Testing 70
7.3 Operational Shock Testing 72
7.4 Thermal Testing 73
7.6 Experiment and Evaluation 76
7.7 Torque-Speed Test 77
7.8 Warning and Fault testing 79
7.9 References 82
CHAPTER 8 83
8.1 Conclusion 83
Best practices for PCB design 83
8.2 References 84
Appendices 85
Output Voltage Waveforms with different gate resistance 88

LIST OF FIGURES

Figure 1. Three phase, 2 level VSI 2
Figure 2. Internal Structure of a Permanent Magnet Synchronous Motor[11] 6
Figure 3. Equivalent circuit of PMSM without damper windings [9] 8
Figure 4. Scalar control scheme block diagram 9
Figure 5. Direct torque control block diagram 10
Figure 6. Field Oriented Control block diagram 11
Figure 7. Transformation overview[11] 11
Figure 8. $\alpha\beta 0$ stationary reference frame 13
Figure 9. dq rotating reference frame 14
Figure 10. 2-Level, 3-Phase voltage source inverter 15
Figure 11. Sinusoidal Reference Waveforms 16
Figure 12. Gating signals for high side switches 17
Figure 13. Line-Line voltages 18
Figure 14. Space vector diagram for a two-level inverter. 20
Figure 15. PMSM Simulink model 24
Figure 16. Clarke transformation block diagram 24
Figure 17. Park transformation block diagram 25
Figure 18. Inverse Park transformation block diagram 26
Figure 19. Reference voltage calculation 27
Figure 20. Sector detection 27
Figure 21. Three phase 2-Level voltage source inverter 28
Figure 22. Simulink model of the system 28
Figure 23. Three phase output current waveforms 29
Figure 24. Speed changes from 30 to 300 rpm 30
Figure 25. Typhoon Hardware in the Loop 602 system [1] 32
Figure 26. Typhoon HIL DSP Interface board [2] 33
Figure 27. Pin relationships between TI's DSP and Typhoon HIL 602[3] 33
Figure 28. Electrical schematic of the overall system 34
Figure 29. Three phase inverter settings 35
Figure 30. PMSM settings in Typhoon HIL schematic editor 36

Figure 31. Analog output settings 37
Figure 32. ePWM configuration parameters 39
Figure 33. Up-Down-Count configuration [4] 39
Figure 34. Dead-Band configuration of ePWM1a/b. [4] 40
Figure 35. PWM signals simulated with fs =10 kHz 40
Figure 36. ADC trigger command 41
Figure 37. Motor phase currents 41
Figure 38. DC link voltage 42
Figure 39. Throttle command 42
Figure 40. Block diagram of Clarke module [5] 42
Figure 41. Clarke transformation 43
Figure 42. Block diagram of Park module [5] 43
Figure 43. Park transformation 43
Figure 44. Block diagram of Inverse Park module [5] 44
Figure 45. Inverse Park transformation 44
Figure 46. Block diagram of SVPWM Module [6] 45
Figure 47. Space vector modulation 45
Figure 48. SCADA user interface 46
Figure 49. a) Alpha, Beta waveforms b) Three phase output currents c) Electrical angle (Theta) 47
Figure 50 SCADA user interface 48
Figure 51. a) Three phase output currents b) Alpha, Beta waveforms c) dq currents 48
Figure 52. Texas Instrument TMS320F28335 51
Figure 53. Wolfspeed CGD12HBXMP Gate Driver Module 54
Figure 54. BRX resolver schematic [5] 55
Figure 55. Resolver to Digital Converter Functional Block Diagram [11] 56
Figure 56. CAN Interface 57
Figure 57 Isolated CAN Transceiver 62
Figure 58. Inverter E-stop Run Command 62
Figure 59. DC Bus Monitoring circuit 63
Figure 60. Controller Board V.1 64

Figure 61. 3D model of the inverter 66
Figure 62. Test setup for the 250-kW inverter 67
Figure 63. Three phase test setup 68
Figure 64. (a) Load testing schematic (b) Load testing waveforms 68
Figure 65. Vibration and Shock Chamber 71
Figure 66. Mounting of the inverter in the Vibrational Chamber 71
Figure 67. Shock pulse profile 73
Figure 68. Interior of Environmental Chamber 74
Figure 69. Mission profile of the aircraft 75
Figure 70. Inverter verification setup 76
Figure 71. Continuous test waveforms at 410 V 77
Figure 72. Torque Step commands at 1020 rpm 78
Figure 73. Torque Step commands at 2040 rpm 79
Figure 74. CAN communication interface 80
Figure 75. Layer 1 - Top Layer 85
Figure 76. Layer 2 – Ground Plane 85
Figure 77. Layer 3 – Signal Layer 86
Figure 78. Layer 4 – Signal Layer 86
Figure 79. Layer 5 – Signal Layer 87
Figure 80. Layer 6- Ground Plane 87
Figure 81. 650 Vdc Terminal Voltages 2040RPM Gate resistance 1.0 Ω 88
Figure 82. 650 Vdc Terminal Voltages 1020RPM Gate resistance 1.8 Ω 89
Figure 83. 650 Vdc Terminal Voltages 2040RPM Gate resistance 1.8 Ω 89
Figure 84. CLC Filter [1] 90

LIST OF TABLES

Table 1. Cesena 337 system parameters 3
Table 2. EMRAX 348 Motor parameters[4] 4
Table 3 Space Vector, Switching States 19
Table 4. Space Vector Switch Duration Times 21
Table 5. TMS320F28335 Specifications [1] 51
Table 6 CGD12HBXMP Gate Drive Signals [3] 53
Table 7. CAN Communication Inverter Signals 58
Table 8 Speed, Torque Values for UUT 78
Table 9. Inverter warnings threshold values 80
Table 10. Inverter fault threshold values 81

CHAPTER 1

INTRODUCTION

1.1 Introduction

The University of Arkansas Power Electronics Research group was presented with a challenging task, to design an inverter for a Cessna 337 Skymaster aircraft. This inverter will replace the engine that is located in the nose of the aircraft, converting the Cessna 337 Skymaster to a hybrid electric aircraft. The proposed inverter presented in this thesis will undergo numerous Federal Aviation Administration (FAA)/DO-160G test procedures such as an Operational Shock and Crash Safety test, Robust Vibrational testing, and Temperature Variations testing. The purpose of the DO-160G test procedures is to determine the performance characteristics of the inverter in flight.

1.2 Research Background

With the continuous growth of the aerospace industry, there has been a trend to optimize the performance of an aircraft by reducing fuel consumption and operational cost. Recent advancements in the field of power electronics have pushed towards the concepts of hybrid electric aircraft also known as more electrical aircrafts. Traditionally aircraft were driven by a combination of hydraulic, pneumatic, mechanical, and electrical systems. Numerous aircraft companies in [1] have replaced their traditional systems with power electronics, which improved the overall efficiency of the aircraft. National Aeronautics and Space Administration (NASA) has set a goal to have a fully scaled electrified propulsion system on aircraft by 2035 [2].

Transitions from internal combustion engines to hybrid or fully electric drive systems decreases the emission of greenhouse gases, which leads to better quality of air in dense urban areas. Today, probably the biggest factors hindering electrification of transportation are its cost,

range, and space. These shortcomings can be addressed these downfalls by increasing the power density (kW/l) and specific power (kW/kg) of the power electronics systems.

This thesis focuses on the design, implementation, and optimization of a custom PMSM controller that will be used for a hybrid electric aircraft. A 3-phase, 2-level inverter utilizing three SiC half bridge modules allows for faster switching and very low losses. Figure 1 shows the basic configuration of this topology. This thesis also describes common PMSM motor control techniques and their effects on efficiency or speed. The primary goal of this project is to design a prototype motor drive that can be used for a hybrid electric aircraft. Custom features like data collection and built in current and voltage limitations will also be added to the inverter. The complete inverter was tested to demonstrate the functionality of the design.

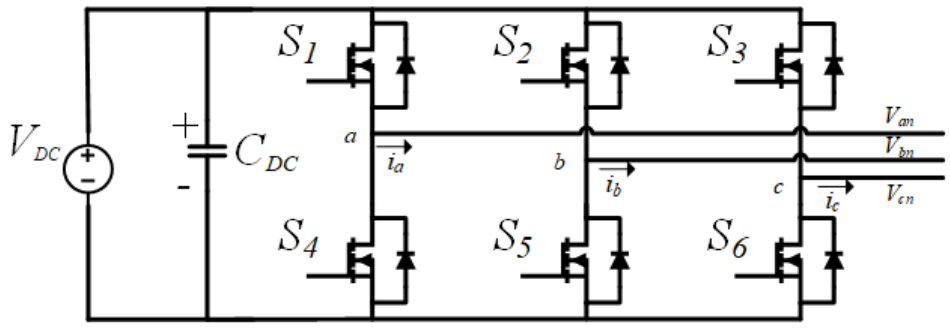

Figure 1. Three phase, 2 level VSI

1.3 Challenge and Research Objective

There are numerous challenges still present when it comes to designing, prototyping, and evaluating motor drives for hybrid electric aircraft. Several of these are as follows:

1. As the aircraft increases in altitude, the converter is working under low air pressure. Paschen's law states that partial discharge could occur inside the converter, which can potentially cause insulation breakdown and reduce system reliability.

2. All motor drives designed for hybrid electric aircraft are required to meet Federal Aviation Administration (FAA) qualifications. This certification ensures that the aircraft meets the highest safety standards from the initial design to retirement.

3. Increase the overall performance of inverters such as power density and efficiency.

1.4 Requirements from Ampaire

The requirements of the project are presented below:

- The continuous power of the EMRAX 348 is 55 kW and 160 kW peak power.
- Voltage and current limits should be monitored by the controller. Overvoltage limit must not exceed 850 Vdc, Overcurrent limit must not exceed 325 A.
- The inverter should be able to receive throttle commands from the pilot via an analog input.
- Controller should send data (motor and modules temperature, etc.) and error messages to the control until of the aircraft via CAN Communication.

Table 1. Cessna 337 System Parameters

Parameter	Value
Battery Voltage	650-800 Vdc
Motor Type	EMRAX 348
Peak Power	160 kW
Nominal Power	55 kW
Cooling system	On board
Cooling water maximum input temperature	25ºC
Cooling flow rate	8L/min

Table 2. EMRAX 348 Motor Parameters [4]

Parameter	Value
Peak motor power	290 kW
Maximal rotation speed	4000 rpm
Continuous motor torque	500 Nm
Continuous motor current	210 A(*rms*)
L_d	180μH
L_q	195μH
Internal phase wire resistance at 25 C	14mΩ
Number of pole pairs	10
Magnetic flux-axial	N/A
Temperature sensor in the motor	Kty 81/210

1.5 Thesis Outline

This thesis is comprised of several chapters and sections within. Chapter 1 introduces the goal and purpose of this thesis. Chapter 2 describes the theoretical background of a PMSM and control algorithms that are used in electric drives. Relevant equations are presented to clarify the design process. Chapter 3, examples how to design the selected control algorithm (Field Oriented Control) in Simulink. Chapter 4 presents the overall design process of building and testing the system in Typhoon HIL. Chapter 5 presents the overall controller architecture for the electric motor drive. The hardware components of the prototype are explained as well. The PCB layout and testing of the PCB is be presented in Chapter 6. Chapter 7 presents the overall results for the test of the 250-kW PMSM inverter.

1.6 References

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CHAPTER 2

SYSTEM MODELING OF PERMANENT MAGNET SYNCHRONOUS MOTOR

2.1 Introduction

Permanent magnet synchronous motors (PMSMs) are AC synchronous motors that use magnets imbedded into or attached to the surface of the rotor to generate a constant motor flux. Depending on the construction of the stator and rotor it can provide high-power efficiency and high-power density. PMSMs can be classified into two categories: non-salient pole PMSM, and salient pole PMSM. Non-salient pole PMSM also known as surface mounted PMSMs (SPMSM) has permanent magnets mounted on the surface of the rotor, which makes them a good choice in low-speed applications. Salient pole PMSM also known as interior PMSMs (IPMSM) has permanent magnets embedded within the rotor. These particular PMSMs are used for high-speed application. Figure 2 shows the internal structure of an IPMSM. In the chapter, a mathematical model of a PMSM will be derived. Different control strategies for a PMSM will be discussed in this chapter. Then different modulation strategies for a 2-level inverter will be analyzed.

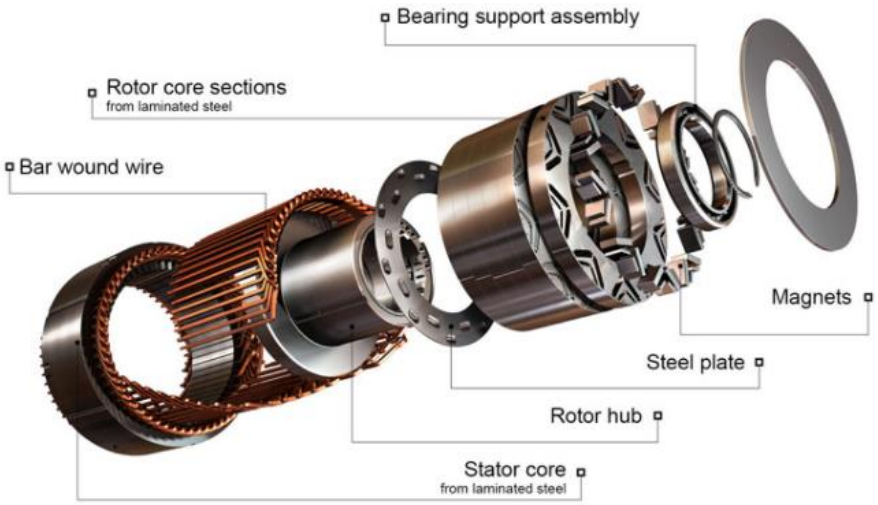

Figure 2. Internal Structure of a Permanent Magnet Synchronous Motor [11]

2.2 Mathematical Model of Permanent Magnet Synchronous Motor

Comparing a PMSM stator to that of the wound rotor synchronous motor, they are similar except that the excitation of a PMSM is provided by permanent magnets instead of field windings. The mathematical model of the PMSM can be derived from that of the wound rotor synchronous motor. When deriving the stator equations there are numerous factors that need to be considered [1] [2]:

- Eddy current and hysteresis losses are negligible
- The stator windings are balanced with sinusoidally distributed magneto-motive force (mmf)
- The induced emf is sinusoidal

With these factors taken into consideration, the stator dq equations in the rotor reference frame [1] are expressed as shown below:

The voltage equations are given by :

$$v_d = R_s i_d + p\lambda_d - P\omega_r \lambda_q \tag{2.1}$$

$$v_q = R_s i_q + p\lambda_d + P\omega_r \lambda_q \tag{2.2}$$

The flux linkages equations are given by :

$$\lambda_q = L_q i_q \tag{2.3}$$

$$\lambda_d = L_d i_d + \lambda_{af} \tag{2.4}$$

The torque equation is :

$$T_e = 3P\left[\lambda_{af} i_q + \left(L_d - L_q\right) i_d d i_q\right]/2 \tag{2.5}$$

where λ_{af} is the magnet mutual flux linkage,

L_d and L_q are the d-q axis synchronous inductances,

Rs is the stator resistance and

i_d, i_q are the stator currents in the d-q coordinates

For constant flux operation, i_d is equal to zero and the electrical torque equation can be further simplified as :

$$T_e = 3P\lambda_{af} i_q/2 = K_t i_q \quad (2.6)$$

2.3 Equivalent Circuit of a PMSM

An equivalent circuit for a PMSM without damping is shown in Figure 3.The equivalent circuit is derived from the d-q modeling of the motor using the voltage equations of the motor.

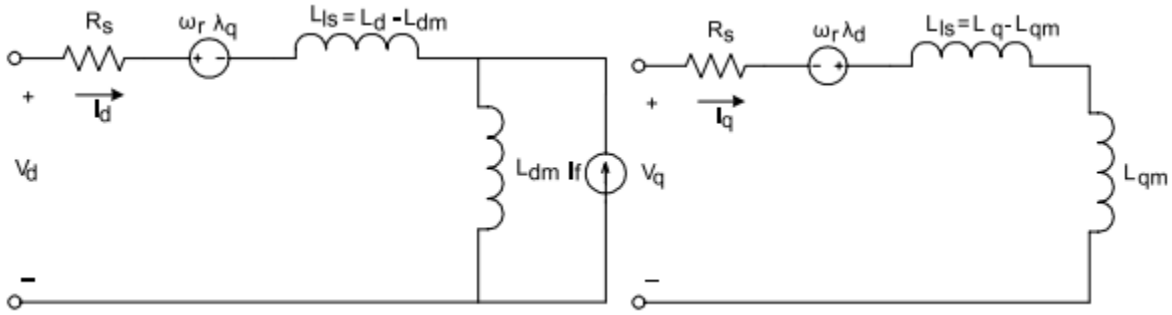

Figure 3. Equivalent circuit of PMSM without damper windings [9]

2.4 PMSM Control Strategies

There are many different ways to drive a PMSM. The main difference between them are the motor's performance and the cost of implementation. Variable frequency drives allow synchronous motors to run at different speeds. PMSM control methods can be divided into three categories, scalar control, field-oriented control (FOC) and direct torque control (DTC).

2.4.1 Scalar Control

Scalar control is a control technique that keeps the voltage/frequency ratio constant throughout the full operating speed range of an induction motor. Scalar control was first developed for induction motors but was later implemented for PMSM. This control is considered to be an open loop method because there is no feedback present. This control method does not achieve good accuracy in both speed and torque response due to the fact that the torque and stator flux are not directly controlled. Figure 4 shows the block diagram of the Scalar control scheme for a PMSM.

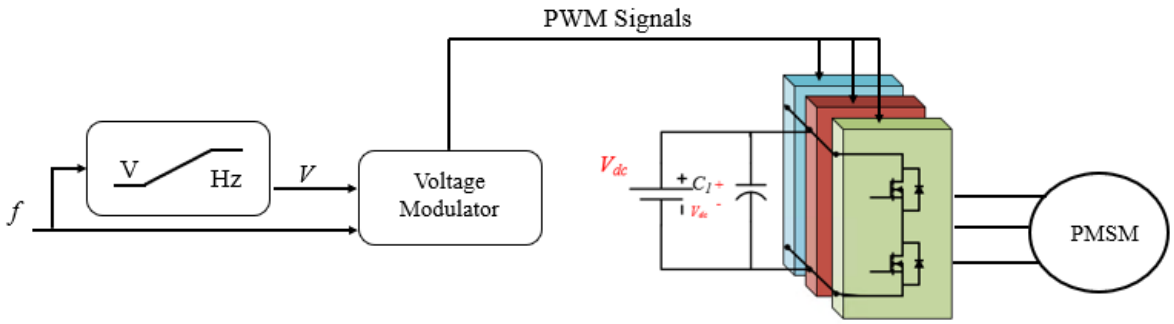

Figure 4. Scalar control scheme block diagram

2.4.2 Direct Torque Control

Direct Torque Control was proposed by Takahashi and Noguchi in 1986 for induction motors to be used for low power applications [10]. Direct Torque Control directly controls the torque and stator flux linkage [10] which then reduces the need for a current control loop. Direct Torque Control is very different than that of Field Oriented Control since it doesn't require complicated transformation such as the Park and Clarke transformation and it also eliminates the need for a position sensor. There are some disadvantages with Direct Torque Control such as it

suffers from higher torque ripple and also higher total harmonic distortion (THD) in the motor stator current. The control block diagram for Direct Torque control is shown in figure 5.

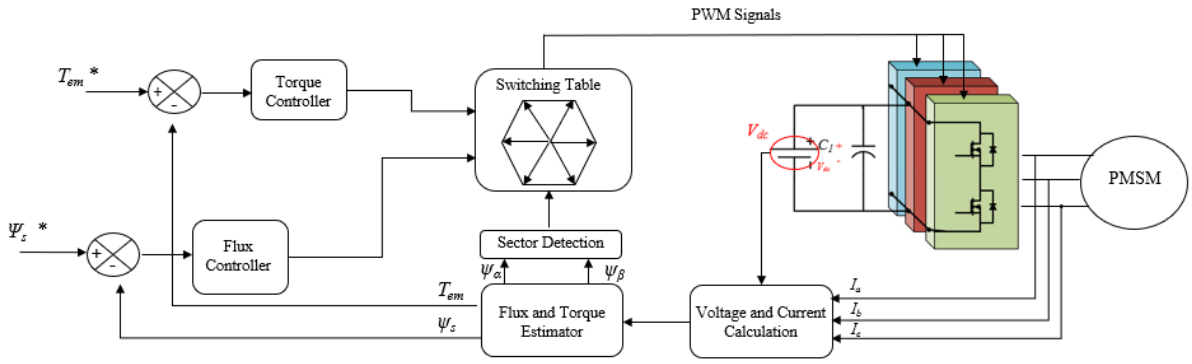

Figure 5. Direct torque control block diagram

2.4.3 Field Oriented Control

Field Oriented Control is a technique used in variable frequency drives to effectively control the speed or torque of a three-phase motor. The basic principle of the field-oriented control is to separate the flux and torque components of the stator current. This allows the PMSM to operate as a separately excited DC machine. Using the Clarke and Park transformation the torque and flux currents can be decoupled. The results of the transformations are the flux i_d component and the torque i_q component. By setting the current reference for i_d to zero maximum torque can be obtained. It should be noted that negative values for i_d results in flux weakening. Negative values for i_d reduce the air gap flux which lowers the back EMF, this enables the motor to achieve higher rated speeds. In this thesis, there is no need to increase the maximum rated speed so i_d will be set to zero.

Figure 6 shows the overall block diagram of the field-oriented control for a PMSM. From [8] it states that knowledge of the rotor position and electric angle is essential to perform the Park

and Inverse Park transformations. This can be accomplished by using a resolver or incremental encoder. In this thesis, the Field Oriented Control algorithm was selected.

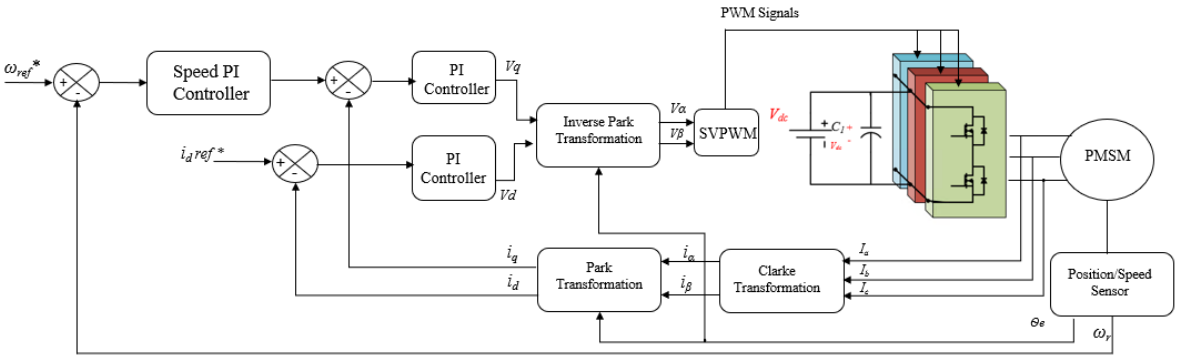

Figure 6. Field Oriented Control block diagram

2.5 Coordinate Transformation

There are two stages that are required for establishing the Field Oriented Control algorithm. The first step is the transformation between the three-phase system to the two-phase system. The second step is the transformation from the two-phase stationary frame to the rotating reference frame. After the transformations the control strategy can be implemented. Figure 7 shows the transformation chain.

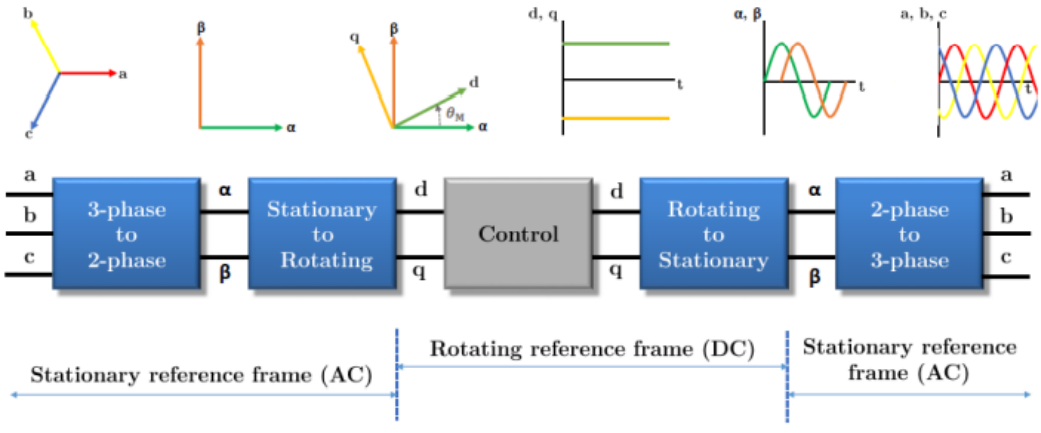

Figure 7. Transformation overview[11]

2.6 Clarke Transformation

The Clarke transform is a space vector transformation of the voltage or current in a three-phase system into a two-phase reference frame. It projects the three phase variables onto the stationary frame which is shown in Figure 8. The matrix equation describing the Clarke transformation for the currents is presented below:

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.7}$$

In the Clarke transform matrix i_0 represents the zero-sequence component of the three-phase current, it is zero for balanced three phase systems [3]. The $\frac{2}{3}$ scaling factor in the Clarke matrix is added to maintain the amplitude across the transformation. The inverse Clarke transformation can be used to obtain the phase variables from the stationary frame. The inverse matrix is shown below:

$$\begin{bmatrix} ia \\ ib \\ ic \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} & 1 \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} & 1 \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{2.8}$$

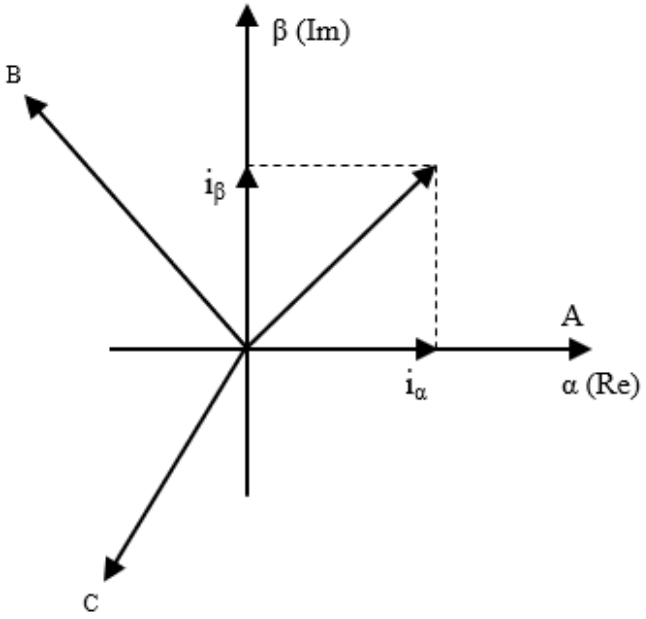

Figure 8. *αβ0* stationary reference frame

Using the Clarke transformation, a space vector can be represented by its α and β components. These two components still change sinusoidally with a phase difference of 90º.

2.7 Park Transformation

The Park transformation converts the stationary reference frame *αβ0* to a rotating reference frame *dq*. The transformation from the stationary reference frame *αβ0* to the rotating reference frame *dq* is shown in Figure 9. The Park transform depends on the current *αβ* vectors and the rotor flux position Θ_e. The matrix equation describing the Park transformation is presented below:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos\Theta_e & sin\Theta_e \\ -sin\Theta_e & cos\Theta_e \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.9}$$

The inverse Park transform is expressed in equation 2.10.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} cos\Theta_e & -sin\Theta_e \\ sin\Theta_e & cos\Theta_e \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{2.10}$$

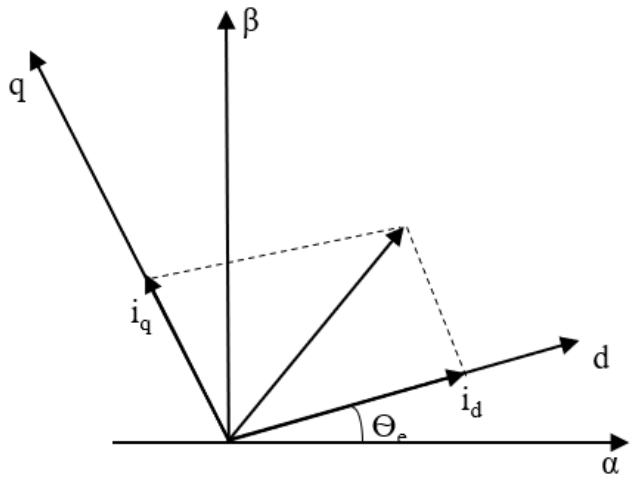

Figure 9. *dq* rotating reference frame

The d-axis is aligned with the rotating flux vector produced by the permanent magnets of the motor and the q-axis leads the d-axis by 90 electrical degrees. At this point the torque i_q, current and flux linkage i_d can easily be controlled in the rotating reference frame. The rotating reference can be directly obtained by combining the Clarke and Park equations. The matrix for the rotating reference frame is shown below:

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos\Theta_e & \cos(\Theta_e - \frac{2\pi}{3}) & \cos(\Theta_e - \frac{4\pi}{3}) \\ -sin\Theta_e & -\sin(\Theta_e - \frac{2\pi}{3}) & -\sin(\Theta_e - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.11}$$

2.8 Voltage Source Inverter

Voltage source inverters (VSI) have been widely used in different power rating applications such as electrical vehicles, variable speed drives and grid connections. A voltage source inverter converts a DC supply to an AC output. A VSI consist of a DC supply, MOSFETs or IGBTs, output filters, three phase load and a digital controller. There are three basic requirements for a three-phase voltage source inverter sinusoidal output voltage with low distortion, controlled output power and controlled power factor [4]. A 2-level, 3-phase voltage

source inverter is depicted in Figure 10. It consists of a voltage source (DC supply), 6 active devices and their gate drivers. The active devices are usually controlled by pulse width modulation (PWM) techniques which either turns the switches on or off based on the duty ratio of the pulse width modulation signal generated. Based on these pwm techniques this can lead to different rms voltages being obtained for different applications.

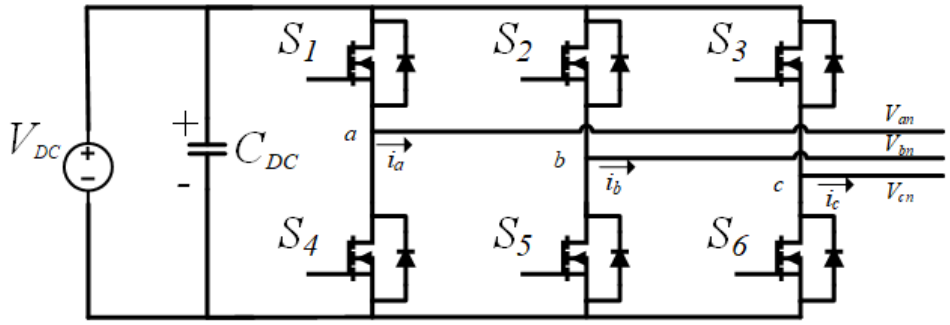

Figure 10. 2-Level, 3-Phase voltage source inverter

In Figure 10, the active devices are three half bridge modules, one for each phase of the motor. The switches S_1-S_6 are silicon carbide MOFESTs. The reason for using SiC Mosfets instead of IGBTs is because SiC Mosfets support higher switching frequencies and reduce switching losses which provide higher efficiency and higher current density.

2.9 Modulation Techniques

To control the output voltage of an inverter for specific loads, different modulation techniques can be used. Modulation techniques are used in power electronics systems to generate an analog voltage level to control semiconductor devices. By manipulating the on and off time of a device within a switching period, the desired output rms voltage can be achieved. Pulse width modulation is an industry standard for electric motor drives.

There are numerous different modulation techniques that are used in inverters/motor drives, such as sinusoidal, third harmonic injection and space vector PWM. With Sinusoidal PWM the utilization of the DC bus voltage is around 78% which is considerably low compared to the other PWM techniques. Third harmonic injection PWM improves the utilization of the DC bus from 78% to above 90% and also reduces the harmonic distortion. Space Vector PWM (SVPWM) improves the utilization of the bus even further (1.15) and reduces the harmonic distortion.

2.10 Sinusoidal Pulse Width Modulation

Sinusoidal Pulse Width Modulation is a modulation technique that changes the output voltage in magnitude and in frequency with a constant input voltage $V_{d.}$ The PWM scheme is illustrated in Figure 11, in which v_c is the peak value of the triangular carrier wave and v_r is that of the reference signal. For a three-phase inverter, sinusoidal pulse width modulation uses three reference waveforms that are displaced 120° from each other. Each waveform is used as a reference for a single phase of the inverter. When the reference waveform has a magnitude higher than the triangular carrier wave the gating pulse is high, otherwise it is low, this is shown in Figure 12.

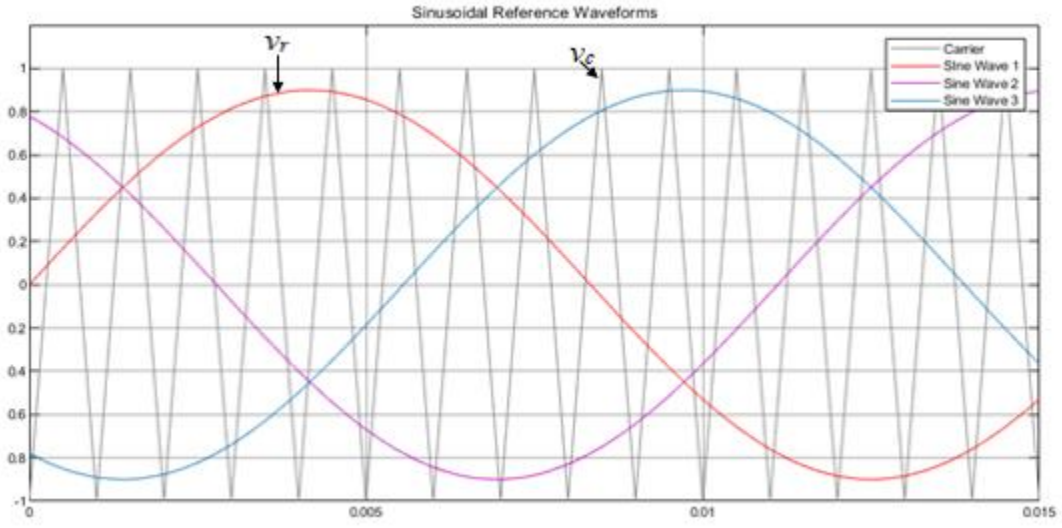

Figure 11. Sinusoidal Reference Waveforms

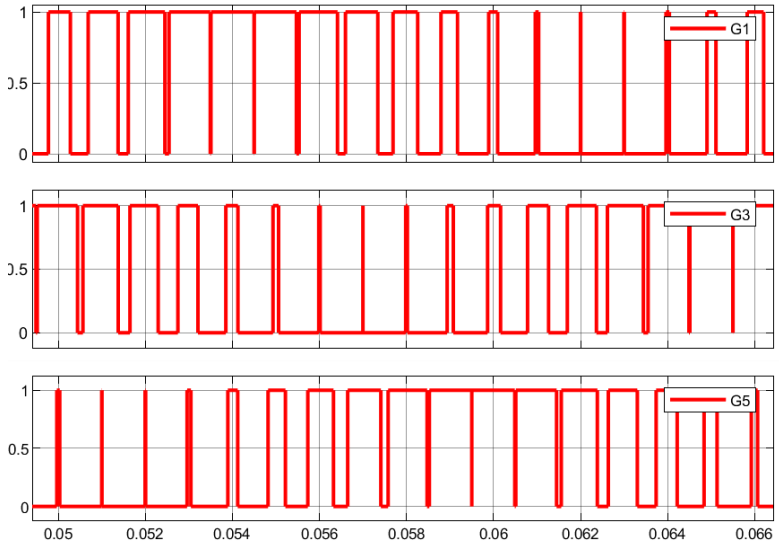

Figure 12. Gating signals for high side switches

Figure 13 shows the Line-to-Line voltages of a three-phase inverter using sinusoidal pulse width modulation. The RMS phase output voltage can be obtained from the equation below:

$$V_{L-N} = \frac{V_d}{2\sqrt{2}} * \text{M.I} \tag{2.12}$$

M.I is the Modulation index and

V_d is the DC-link voltage.

The RMS line-to-line output voltage can be obtained from the equation below:

$$V_{L-L} = \frac{V_d * \sqrt{3}}{2\sqrt{2}} * \text{M.I} \tag{2.13}$$

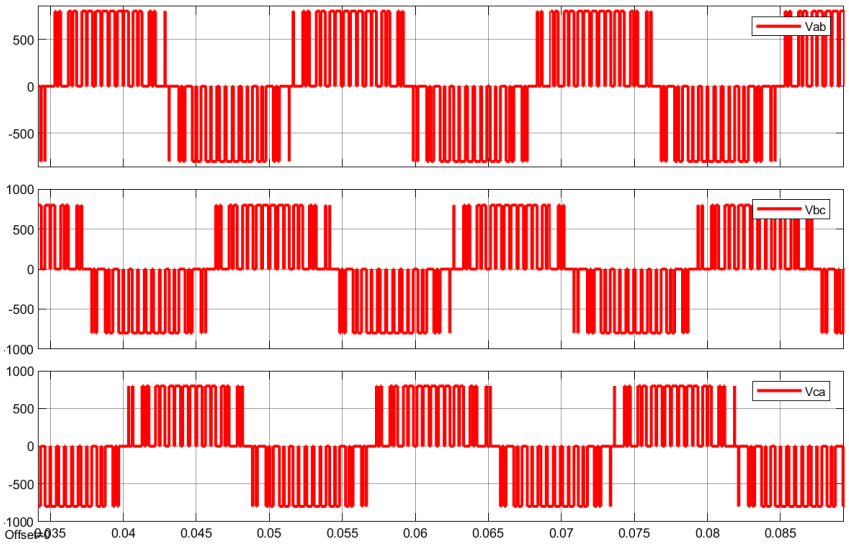

Figure 13. Line-Line voltages

2.11 Space Vector Modulation

Space vector modulation has become a popular modulation technique for three phase voltage source inverters in applications to control AC induction and permanent magnet synchronous motors. Space Vector Modulation determines the switching sequences of the upper three power devices of a three-phase voltage source inverter. This technique has been shown to generate less harmonic distortion in the output voltages or current in the windings of the motor [5] and provide more efficient use of the supply voltage compared to sinusoidal pulse width modulation.

To implement Space Vector Modulation, the three-phase output voltage must be transformed into the stationary αβ frame. Table 3 shows the eight possible switching states in the two-level inverter. There are eight space vectors in total Six are non-zero vectors that form diagonals of a hexagon and two zero vectors which are positioned at the origin of the hexagon and supply zero voltage to a three-phase load. The angle between any two non-zero vectors is 60º.

Table 3 Space Vector, Switching States

Space Vector		Switching State	On-State Switch	Vector Definition
Zero Vector	V_0	111	S_1,S_2,S_3	$V_0 = 0$
		000	S_4,S_5,S_6	
Active Vector	V_1	100	S_1,S_5,S_6	$V_1 = \frac{2}{3}V_d e^{j0}$
	V_2	110	S_1,S_2,S_6	$V_2 = \frac{2}{3}V_d e^{j\pi/3}$
	V_3	010	S_4,S_2,S_6	$V_3 = \frac{2}{3}V_d e^{j2\pi/3}$
	V_4	011	S_4,S_2,S_3	$V_4 = \frac{2}{3}V_d e^{j3\pi/3}$
	V_5	001	S_4,S_5,S_3	$V_5 = \frac{2}{3}V_d e^{j4\pi/3}$
	V_6	101	S_1,S_5,S_3	$V_6 = \frac{2}{3}V_d e^{j5\pi/3}$

There are two main steps when implementing SVPWM as outlined in Sections 2.10 and 2.11.

2.12 Determining V_{ref} and θ

To determine V_{ref} , the output from the *d* and *q* PI controllers are converted to the alpha beta reference frame by using the inverse Park matrix (2.10). V_{ref} is then found by taking the square root of the alpha and beta vectors. It can be seen in Figure 14 that as V_{ref} passes through the individual sections different sets of switches are turned on or off. The aim here is to rotate the voltage reference vector in the $\alpha\beta$ reference frame at a given angular velocity ($\omega = 2\pi f$), where *f* is the fundamental frequency of the inverter's output voltage.

$$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2} \tag{2.14}$$

$$\theta = \tan^{-1}\left(\frac{V_\alpha}{V_\beta}\right) \tag{2.15}$$

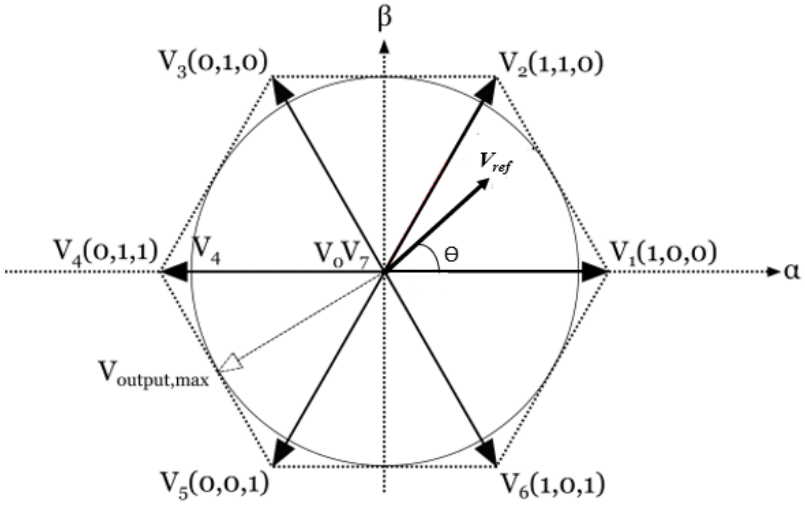

Figure 14. Space vector diagram for a two-level inverter.

2.13 Determining Switch Duration T_a, T_b, T_0

If the voltage reference vector is constant while the sampling time is sufficiently small, the switching durations can be calculated using the equations below. V_a and V_b are the active vectors and $V_{0,7}$ are the null vectors. The switching time for all switches are presented in Table 4.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_a}T_a + \overrightarrow{V_b}T_b + \overrightarrow{V_{0,7}}T_0 \tag{2.16}$$

$$T_s = T_a + T_b + T_0 \tag{2.17}$$

$$T_{sample} = 2T_s \tag{2.18}$$

The equations given below show a generalized formula to obtain the switching duration T_a, T_b and T_0.

$$T_a = \frac{\sqrt{3}T_s V_{ref}}{V_{dc}}\left(\sin\left(\frac{\pi}{3} - \theta\right)\right) \tag{2.19}$$

$$T_b = \frac{\sqrt{3}T_s V_{ref}}{V_{dc}}(\sin\theta) \tag{2.20}$$

$$T_0 = T_s - T_a - T_b \tag{2.21}$$

Table 4. Space Vector Switch Duration Times

Sector	Upper Switches (S_1,S_2,S_3)	Lower Switches (S_4,S_5,S_6)
1	$S_1 = T_1 + T_2 + \frac{T_0}{2}$	$S_4 = \frac{T_0}{2}$
	$S2 = T_2 + \frac{T_0}{2}$	$S_5 = T_1 + \frac{T_0}{2}$
	$S_3 = \frac{T_0}{2}$	$S_6 = T_1 + T_2 + \frac{T_0}{2}$
2	$S_1 = T_1 + \frac{T_0}{2}$	$S_4 = T_2 + \frac{T_0}{2}$
	$S_2 = T_1 + T_2 + \frac{T_0}{2}$	$S_5 = \frac{T_0}{2}$
	$S_3 = \frac{T_0}{2}$	$S_6 = T_1 + T_2 + \frac{T_0}{2}$
3	$S_1 = \frac{T_0}{2}$	$S_4 = T_1 + T_2 + \frac{T_0}{2}$
	$S_2 = T_1 + T_2 + \frac{T_0}{2}$	$S_5 = \frac{T_0}{2}$
	$S_3 = T_2 + \frac{T_0}{2}$	$S_6 = T_1 + \frac{T_0}{2}$
4	$S_1 = \frac{T_0}{2}$	$S_4 = T_1 + T_2 + \frac{T_0}{2}$
	$S_2 = T_1 + \frac{T_0}{2}$	$S_5 = T_2 + \frac{T_0}{2}$
	$S_3 = T_1 + T_2 + \frac{T_0}{2}$	$S_6 = \frac{T_0}{2}$
5	$S_1 = T_2 + \frac{T_0}{2}$	$S_4 = T_1 + \frac{T_0}{2}$
	$S_2 = \frac{T_0}{2}$	$S_5 = T_1 + T_2 + \frac{T_0}{2}$
	$S_3 = T_1 + T_2 + \frac{T_0}{2}$	$S_6 = \frac{T_0}{2}$
6	$S_1 = T_1 + T_2 + \frac{T_0}{2}$	$S_4 = \frac{T_0}{2}$
	$S_2 = \frac{T_0}{2}$	$S_5 = T_1 + T_2 + \frac{T_0}{2}$
	$S_3 = T_1 + \frac{T_0}{2}$	$S_6 = T_2 + \frac{T_0}{2}$

2.14 References

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CHAPTER 3

SIMULINK MODEL OF THE CONTROL ALGORITHM

3.1 Introduction

Simulation of complex control systems are beneficial before attempting to start the design process. Control systems can be tested and easily changed by this method. Results of the chosen algorithms could be observed before experimental tests. Matlab/Simulink is used to build models of the overall system and to gather preliminary results on the performance of the control algorithm. Throughout the simulation, the EMRAX 348 motor parameters which was summarized in Table 2 will be used.

3.2 Permanent Magnet Synchronous Motor Model

Figure 15 shows the symbol for a three-phase permanent magnet synchronous motor model. Behavior of the model is described in equations 2.1 - 2.5. The EMRAX 348 permanent magnet synchronous motor has sinusoidal back EMF and is defined as a salient pole machine since there is a small difference between the direct and quadrature axis inductance according to the datasheet. Figure 15 is the Simulink model of a PMSM. It belongs to the Simulink Simscape Electrical library. The parameters of the motor can be specified by using the “Compute from standard manufacturer specifications” option.

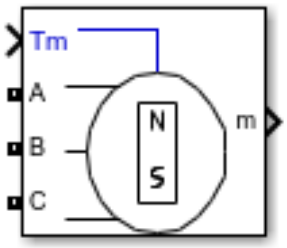

Figure 15. PMSM Simulink model

3.3 Clarke Transformation

As mentioned in the Chapter 2, the motor phase current of a three-phase system is transformed into a two-phase reference frame by means of Equation 2.7. Figure 16 shows the Simulink block diagram of the Clarke transformation.

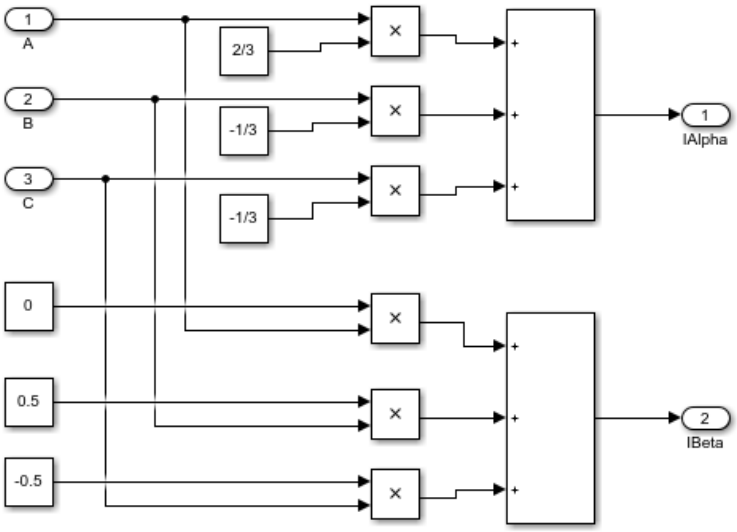

Figure 16. Clarke transformation block diagram

3.4 Park Transformation

Figure 17 shows the Simulink block diagram of the Park transformation. It converts the stationary reference frame $\alpha\beta 0$ obtained from the Clarke transformation to a rotating reference

frame *dq*. The transformation from the stationary reference frame *αβ0* to the rotating reference frame is shown below. To implement the Park Transformation, the Trigonometric Function is used for axis rotation. The range of the Trigonometric Sine and Cosine function is from 0 to 2π in radian.

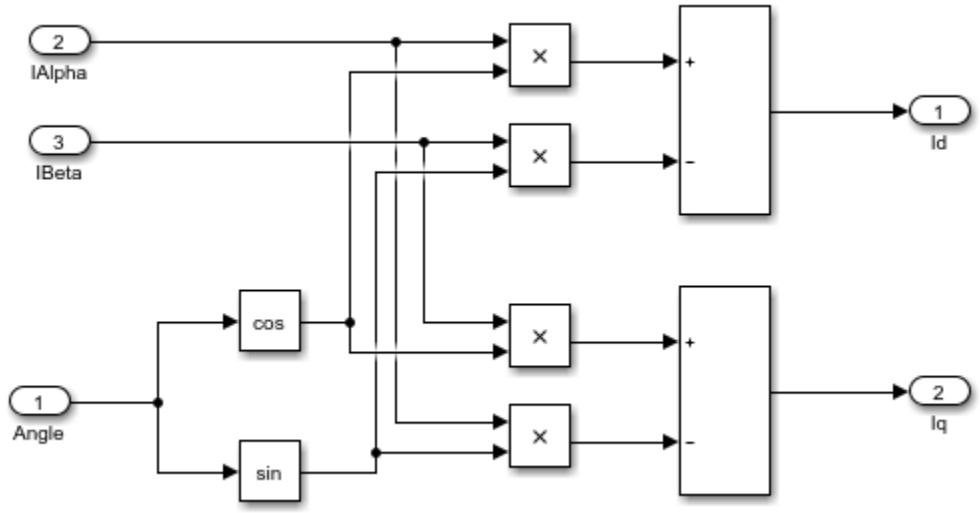

Figure 17. Park transformation block diagram

3.5 Inverse Park Transformation

The inverse Park transformation is used to convert the *dq* outputs from the current controllers to *αβ* stationary reference frame. The transformation matrix is shown in 2.10. As seen from Figure 17, the rotor electrical position is needed for both the Park and Inverse Park transformation. The Simulink model for the Inverse Park transformation is shown in Figure 18.

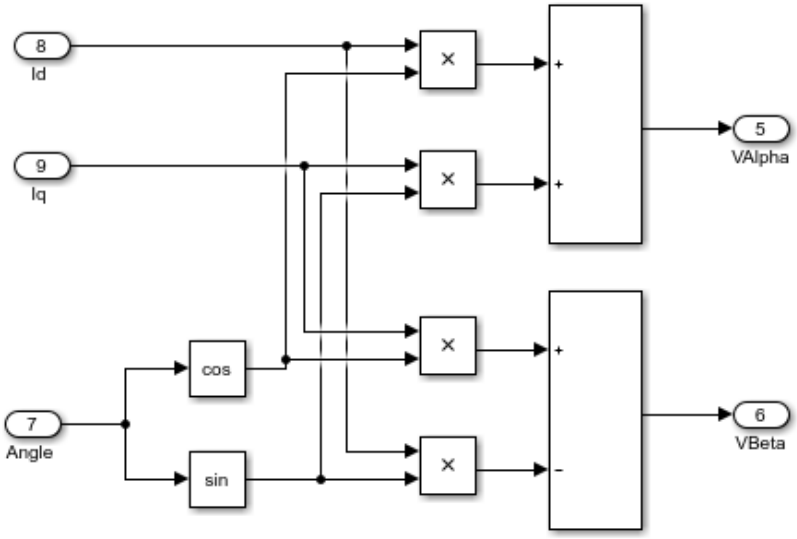

Figure 18. Inverse Park transformation block diagram

3.6 Space Vector PWM

Space Vector Modulation has become a popular modulation technique for three phase voltage source inverters in applications to control AC induction and permanent magnet synchronous motors. Space Vector Modulation determines the switching sequences of the upper three power devices of a three-phase voltage source inverter. Figure 19 shows the reference vector block used to calculate the reference vector used. Outputs of the Inverse Park transformation are fed into the Reference Vector calculation block. As a result of the calculations, the magnitude and phase angles are obtained. Figure 20 shows the block diagram for the switching schemes for Space Vector Modulation. The theta value that is obtained from the reference voltage calculation is first converted from radians to degrees. Using this value as well as a look-up table the appropriate sector is calculated. In every 60º sector changes, switching durations are calculated based on equations 2.19 – 2.21. Based on the calculated durations, PWM signals should be applied to the switches based on [1].

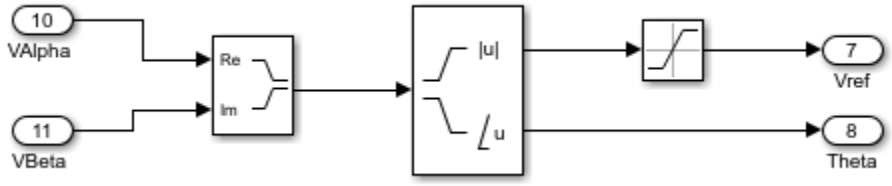

Figure 19. Reference voltage calculation

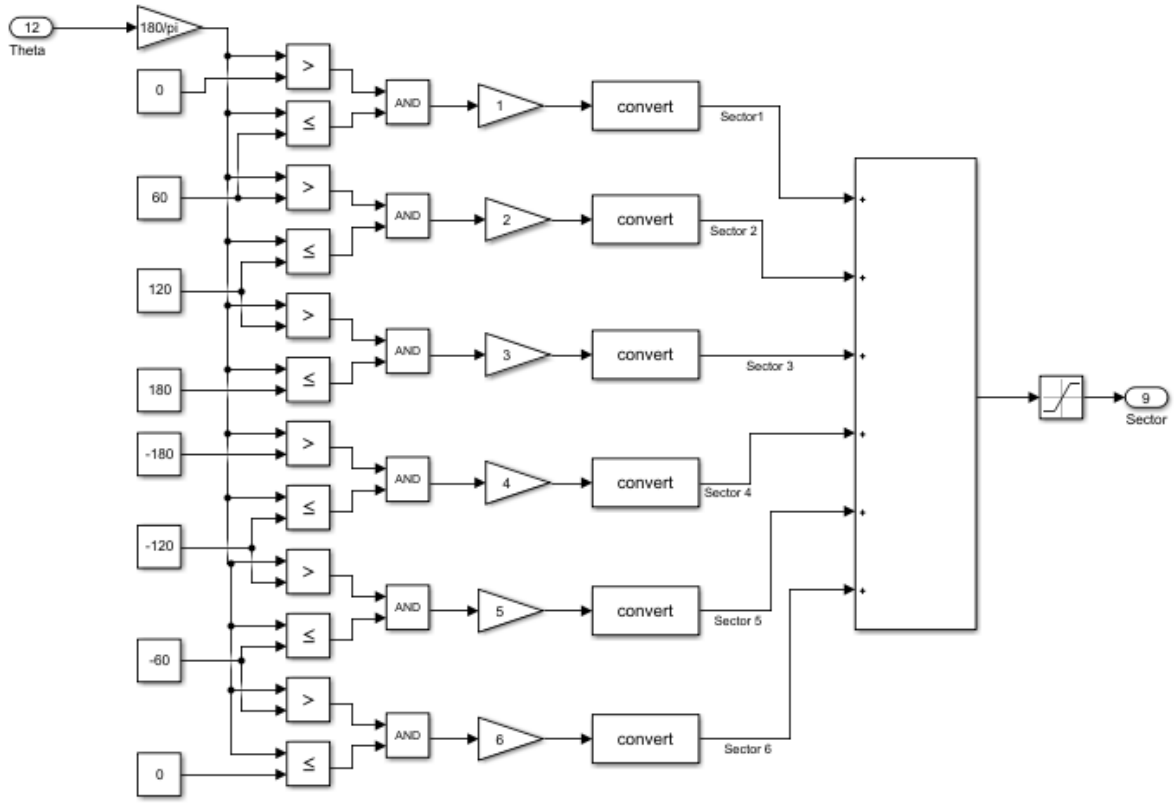

Figure 20. Sector detection

3.7 Voltage Source Inverter

Figure 21 shows a diagram of a Voltage Source Inverter. It consists of a DC voltage source, MOSFETs and logical NOT operators. The internal resistance of the MOSFET which is the Drain-to-Source On-Resistance is set to 2.6 mΩ based on [2].

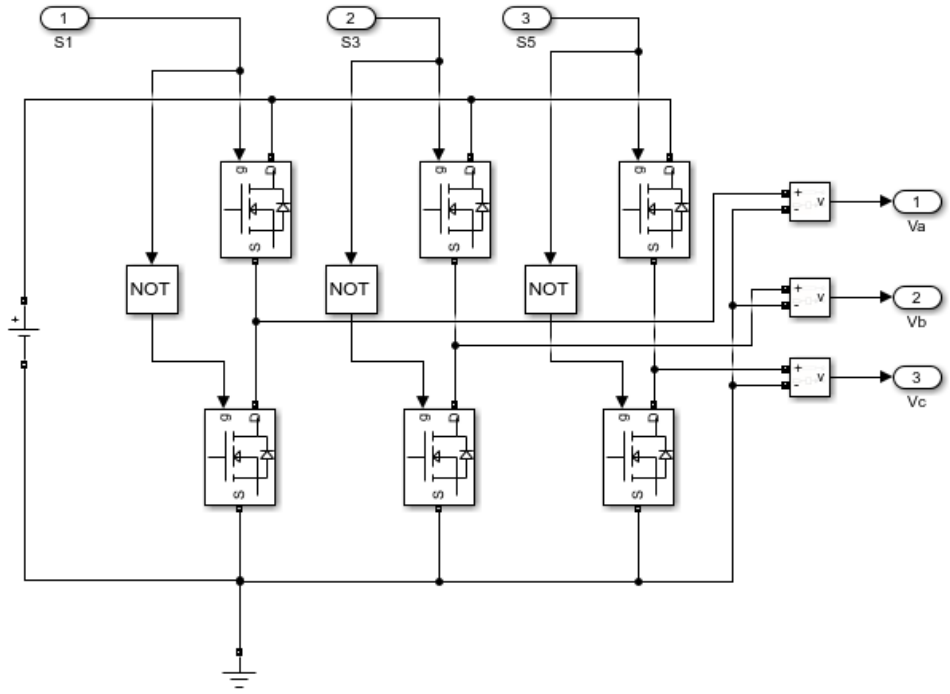

Figure 21. Three phase 2-Level voltage source inverter

3.8 Simulation Results

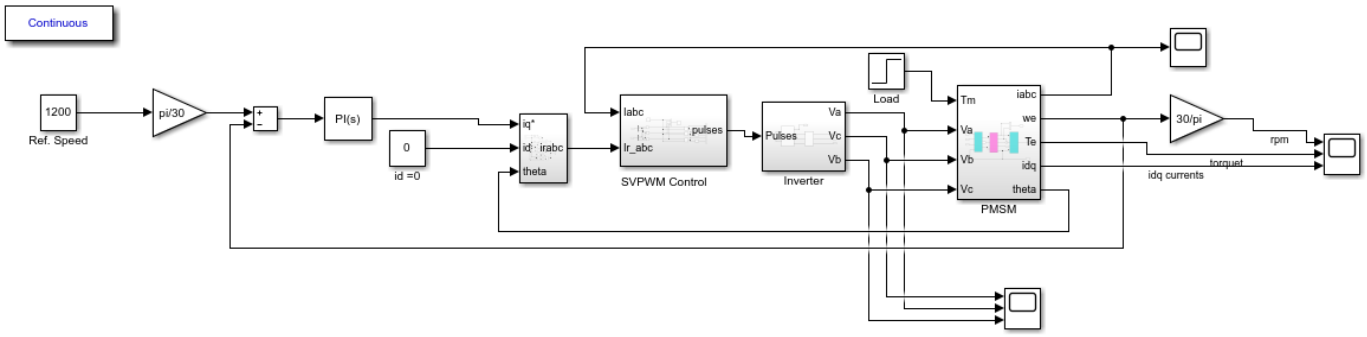

Figure 22. Simulink model of the system

In order to understand the proposed control scheme, a simulation model was developed in MATLAB/Simulink. Figure 19 shows the Simulink model that will be used for the simulation. The simulations presented in this section are used to investigation how the controller will respond to different load changes. Simulation results for the Field Oriented Control were obtained by using the parameters from table 2.

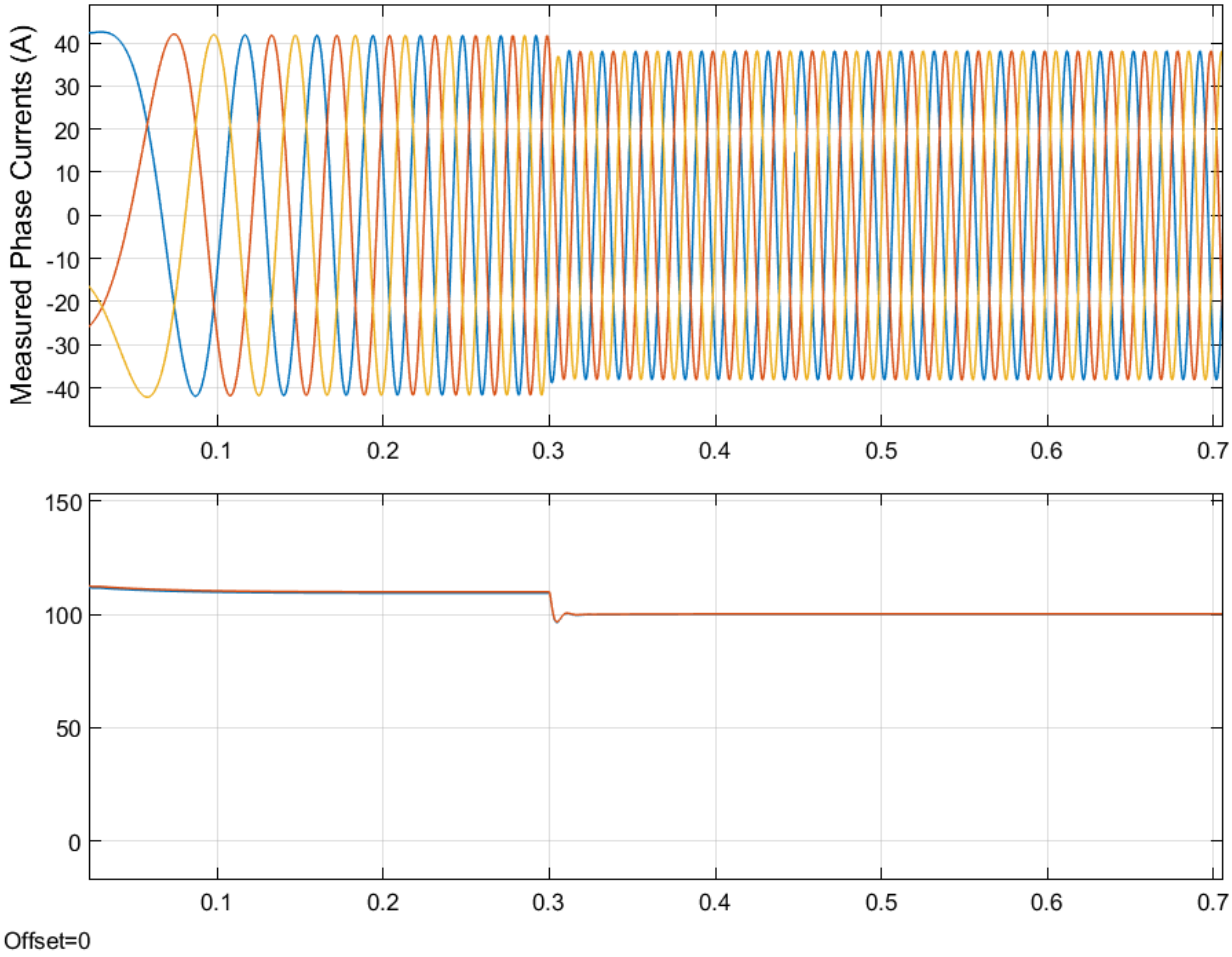

Figure 23. Three phase output current waveforms

Figure 20 shows the output phase currents when there is a step change in the load torque., the command speed is set to 600 rpm and the load torque is 100 Nm. Then at 0.3s the load torque is decreased to

80 Nm. The simulation stop time is 0.2s The blue curve represents the command speed, and the yellow represents the real speed response.

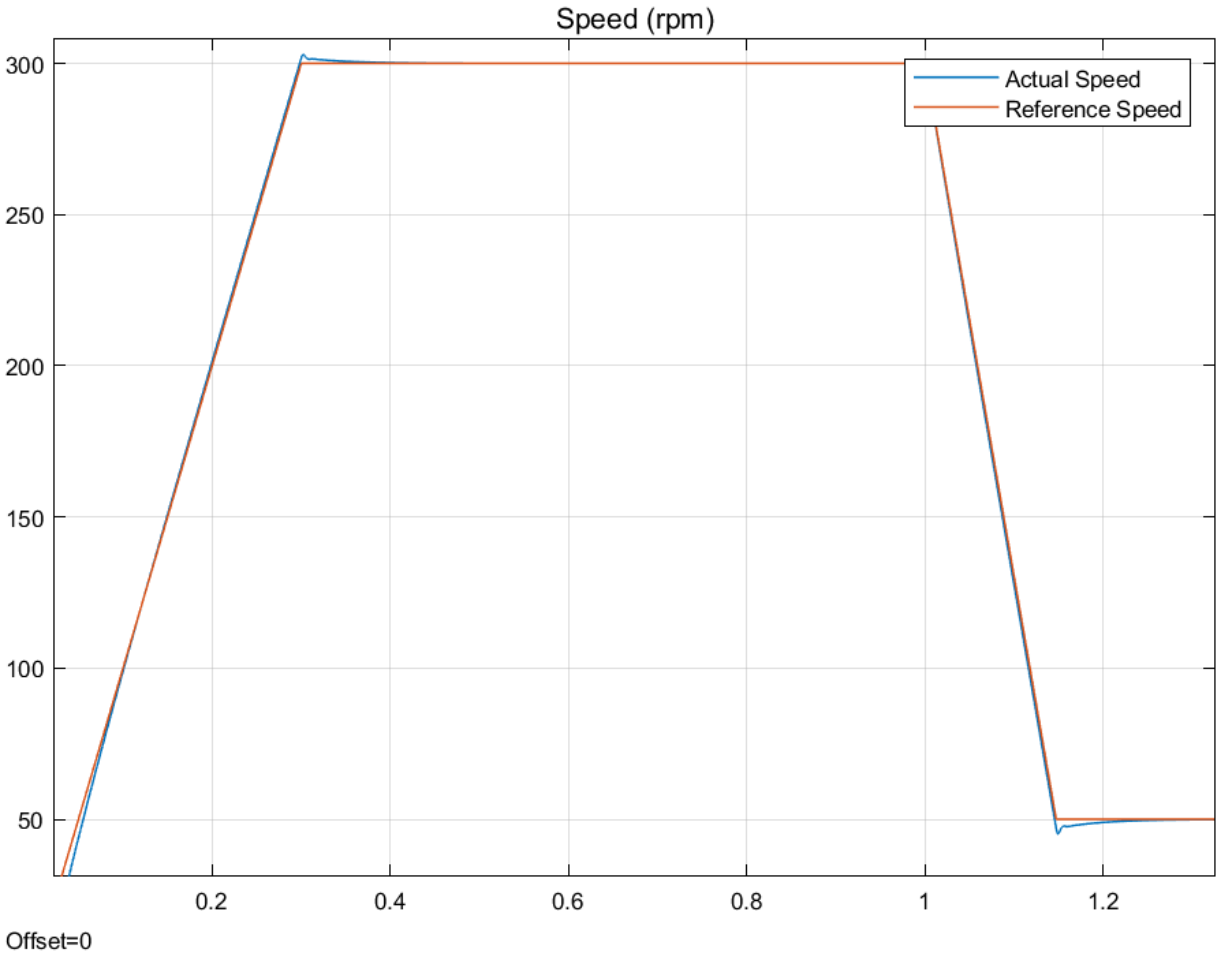

Figure 24. Speed changes from 30 to 300 rpm

Figure 21 shows a step change speed from 30 rpm to 300rpm at 0.25s. At first, the command speed is set to 30 rpm and the load torque is 15 Nm. Next the speed is increased to 300 rpm, this is done to evaluate the speed controller. The blue curve represents the command speed, and the red represents the real speed response.

3.9 References

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CHAPTER 4

REAL TIME HARDWARE IN THE LOOP SIMULATIONS

4.1 Introduction

Hardware In the Loop (HIL) testing is a technique where real control signals are connected to a test system that simulate real-life scenarios. Testing and design iterations take place as though real-world systems are being used. Using HIL extreme testing can be conducted without the danger of any damages.

With 20 ns PWM sampling time, 500 ns simulation time step and an ultra-low latency[1], Typhoon HIL has set the industry standard for real-time emulation of power electronics systems. Testing of the control algorithm and generation of the automated C-code a Typhoon HIL 602 (Figure 25) system is used. An interface board shown in Figure 26 is used for connecting the DSP the Typhoon 602 hardware.

Figure 25. Typhoon Hardware in the Loop 602 system [1]

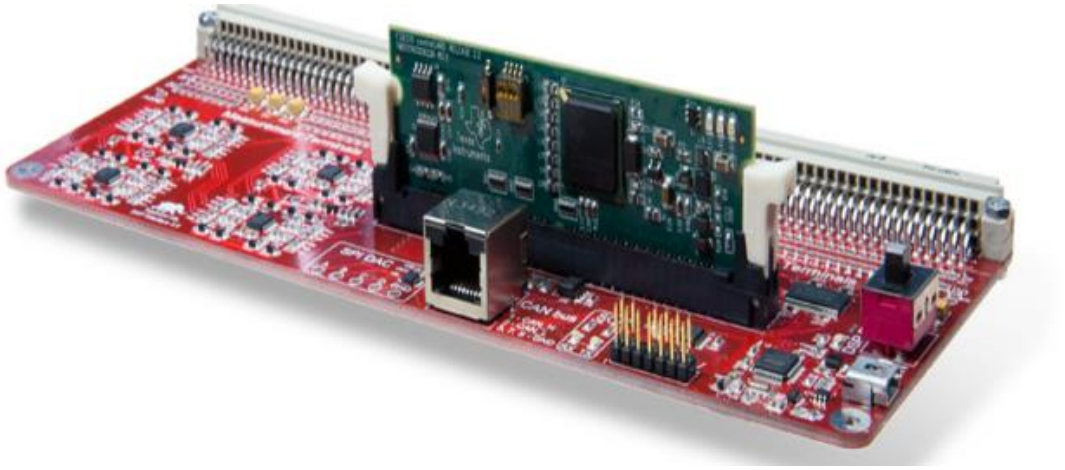

Figure 26. Typhoon HIL DSP Interface board [2]

Typhoon HIL Digital Output	DSP Digital Input	Typhoon HIL Digital Input	DSP Digital Output
DO1	GPIO-24 / EQEPA-2	DI1	GPIO-00/EPWM-1A
DO2	GPIO-25 / EQEPB-2	DI2	GPIO-02/EPWM-2A
DO3	GPIO-26 / EQEPI-2	DI3	GPIO-04/EPWM-3A
DO4	GPIO-20	DI4	GPIO-06/EPWM-4A
DO5	GPIO-21	DI5	GPIO-08/EPWM-5A
DO6	GPIO-22	DI6	GPIO-10/EPWM-6A
DO7	GPIO-23	DI7	GPIO-01/EPWM-1B
DO8	GPIO-27	DI8	GPIO-03/EPWM-2B
DO9	GPIO-32	DI9	GPIO-05/EPWM-3B
DO10	GPIO-33	DI10	GPIO-07/EPWM-4B
DO11	GPIO-48/40**	DI11	GPIO-09/EPWM-5B
DO12	GPIO-49/41**	DI12	GPIO-11/EPWM-6B
DO13	GPIO-60/44**	DI13	GPIO-14/EPWM-8A*
DO14	GPIO-61/45**	DI14	GPIO-12/EPWM-7A*
DO15	GPIO-62/46**	DI15	GPIO-15/EPWM-8B*
DO16	GPIO-63/47**	DI16	GPIO-13/EPWM-7B*

Typhoon HIL Analog Output	DSP Analog Input
AO1	ADCIN – A0
AO2	ADCIN – A1
AO3	ADCIN – A2
AO4	ADCIN – A3
AO5	ADCIN – A4
AO6	ADCIN – A5
AO7	ADCIN – A6
AO8	ADCIN – A7
AO9	ADCIN – B0
AO10	ADCIN – B1
AO11	ADCIN – B2
AO12	ADCIN – B3
AO13	ADCIN – B4
AO14	ADCIN – B5
AO15	ADCIN – B6
AO16	ADCIN – B7

Figure 27. Pin relationships between TI's DSP and Typhoon HIL 602[3]

One of the advantages of using Typhoon HIL is that all the connections are realized through the Typhoon HIL DSP Interface board. Figure 27 shows a full description of all analog and digital

inputs/output pins. The goal of using Typhoon HIL is to be able to use the code in the simulated system and the implemented algorithm in the hardware.

4.2 Typhoon HIL schematic editor

Figure 28 shows the overall electrical system that will be used for testing. It is important that the design be as close as possible to the hardware set-up that is going to be tested. Shown in Figure 28 the circuit is composed of a 2-level voltage source inverter, a Permanent Magnet Synchronous Motor, and all the associated current and voltage measurement probes. The Core coupling seen in the figure is used by the software in Typhoon HIL to separate the circuit into two dependent circuits which makes the compilation of the design easier.

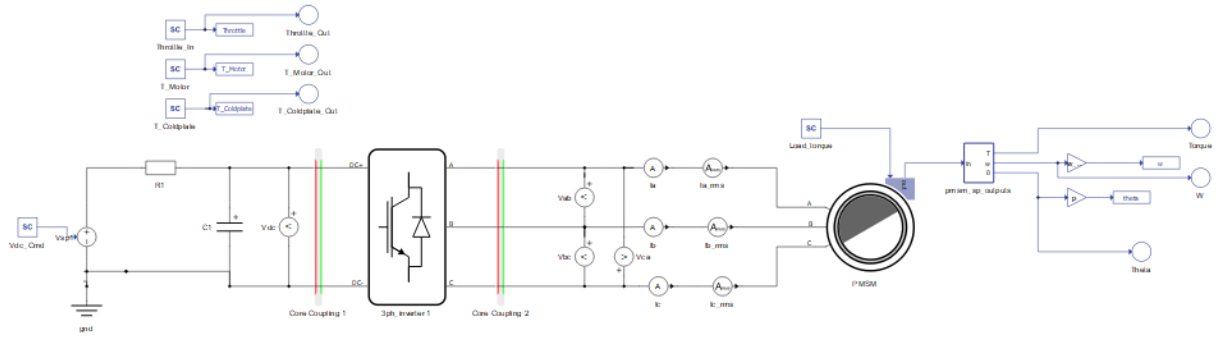

Figure 28. Electrical schematic of the overall system

The next step after designing the schematic in Typhoon HIL is to set the digital inputs for the three phase inverter. Figure 29 shows the three phase inverter with their associated digital inputs. Sa_top 1 and Sa_bot 7 correspond to the DSP digital output GPIO-00/EPWM-1A and GPIO-01/EPWM-1B. Sb_top 2 and Sb_bot 8 correspond to the DSP digital output GPIO-02/EPWM-2A and GPIO-03/EPWM-2B. Sc_top 3 and Sb_bot 9 correspond to the DSP digital output GPIO-04/EPWM-3A and GPIO-05/EPWM-3B.

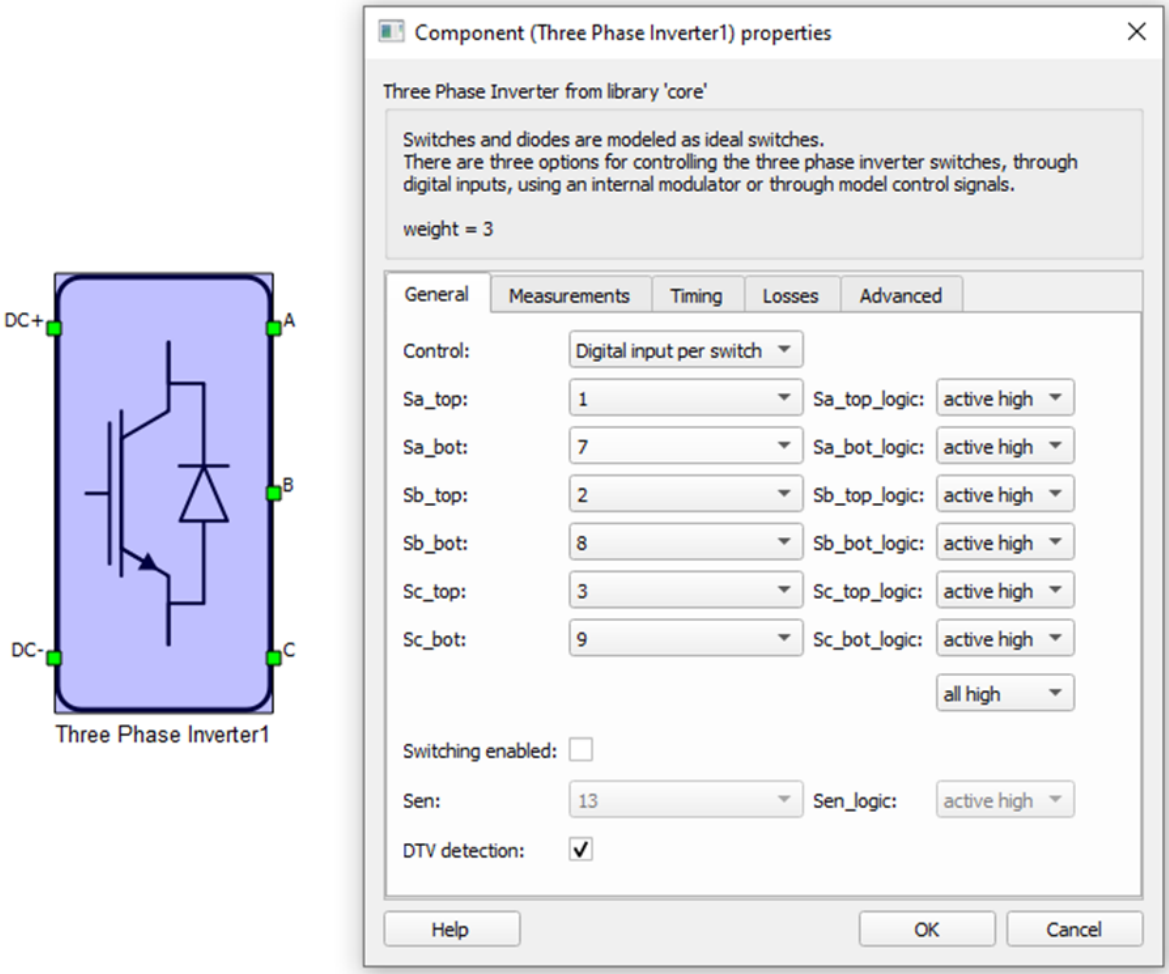

Figure 29. Three phase inverter settings

Figure 30 shows the PMSM component properties setting where different output measurements can be selected. For this application the Electrical torque, Mechanical speed and Mechanical angle was selected to be used in the control algorithm. Figure 31 shows the analog output settings menu, this is where you can assign any analog signals that are present in the schematic to any of analog output channel.

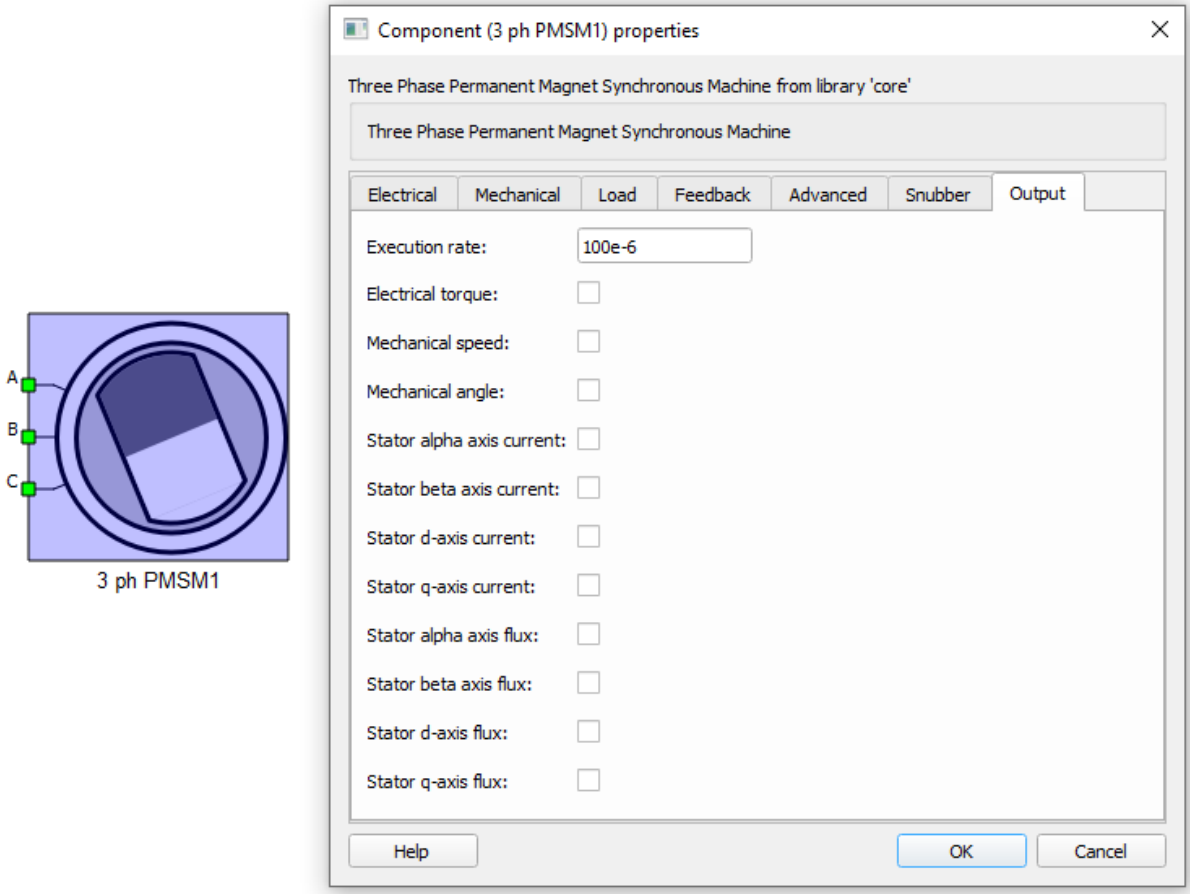

Figure 30. PMSM settings in Typhoon HIL schematic editor

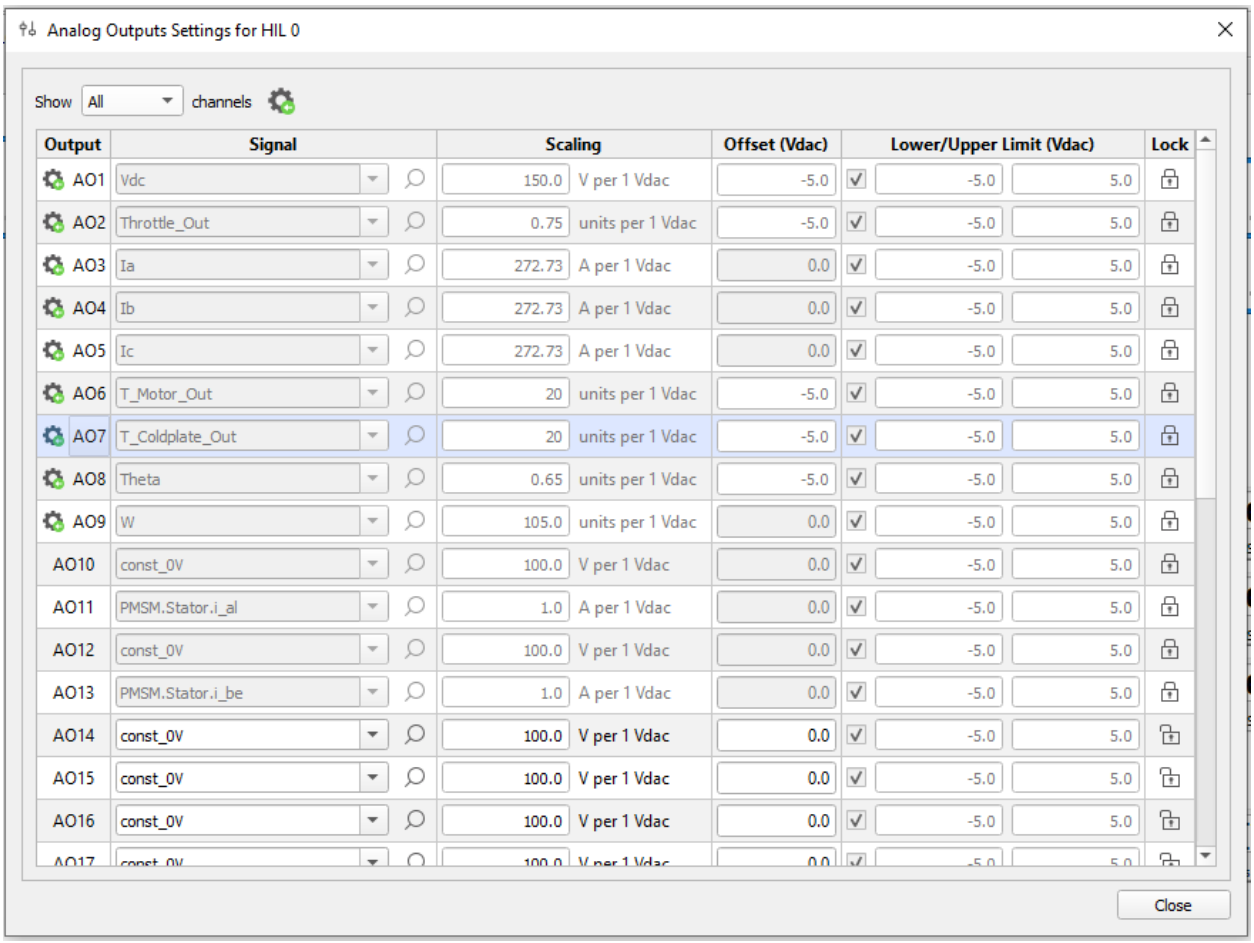

Figure 31. Analog output settings

4.3 Program Implementation

Once the system is built in Typhoon HIL, the system will be complied and ran in real time on the FPGA inside the HIL 602. Presented in this section is an overview of the C-Code implemented in Code Compose Studios and ran on the Typhoon HIL interface board. The first step will be to configure the PWM and ADC registers, once this is done the control loops will be coded. This will be presented in the following sections.

4.4 PWM Configuration

For the Voltage Source Inverter presented in Figure 29 there are 6 Enahanced Pulse Width Modulator (ePWM) modules that can be used. For the application presented in this section ePWM1, ePWM2 and ePWM3 are going to be configured as shown below.

- ePWM1a (GPIO0) and ePWM1b (GPIO1) corresponds to switched T1 and T2.
- ePWM2a (GPIO2) and ePWM2b (GPIO3) corresponds to switched T3 and T4.
- ePWM3a (GPIO4) and ePWM3b (GPIO5) corresponds to switched T5 and T6.

The pins that are used to configure the ePWM modules are shown in Figure 32. First the pins must be configure as outputs, enable the internal pullup resistors and then each GPIO should be configured as part of the ePWM module.

```
GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;          // Enable GPIO0 as an output
GpioCtrlRegs.GPADIR.bit.GPIO1 = 1;          // Enable GPIO1 as an output
GpioCtrlRegs.GPADIR.bit.GPIO2 = 1;          // Enable GPIO2 as an output
GpioCtrlRegs.GPADIR.bit.GPIO3 = 1;          // Enable GPIO3 as an output
GpioCtrlRegs.GPADIR.bit.GPIO4 = 1;          // Enable GPIO4 as an output
GpioCtrlRegs.GPADIR.bit.GPIO5 = 1;          // Enable GPIO5 as an output
```

```
GpioCtrlRegs.GPAPUD.bit.GPIO0 = 0;    // Enable pull-up on GPIO0 (EPWM1A)
GpioCtrlRegs.GPAPUD.bit.GPIO1 = 0;    // Enable pull-up on GPIO1 (EPWM1B)
GpioCtrlRegs.GPAPUD.bit.GPIO2 = 0;    // Enable pull-up on GPIO2 (EPWM2A)
GpioCtrlRegs.GPAPUD.bit.GPIO3 = 0;    // Enable pull-up on GPIO3 (EPWM3B)
GpioCtrlRegs.GPAPUD.bit.GPIO4 = 0;    // Enable pull-up on GPIO4 (EPWM3A)
GpioCtrlRegs.GPAPUD.bit.GPIO5 = 0;    // Enable pull-up on GPIO5 (EPWM3B)
```

```
GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;    // Configure GPIO0 as EPWM1A
GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;    // Configure GPIO1 as EPWM1B
GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;    // Configure GPIO2 as EPWM2A
GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;    // Configure GPIO3 as EPWM2B
GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;    // Configure GPIO4 as EPWM3A
GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1;    // Configure GPIO5 as EPWM3B
```

Figure 32. ePWM configuration parameters

Figure 33 shows the Up-Down Count mode that will be configured for the switches.

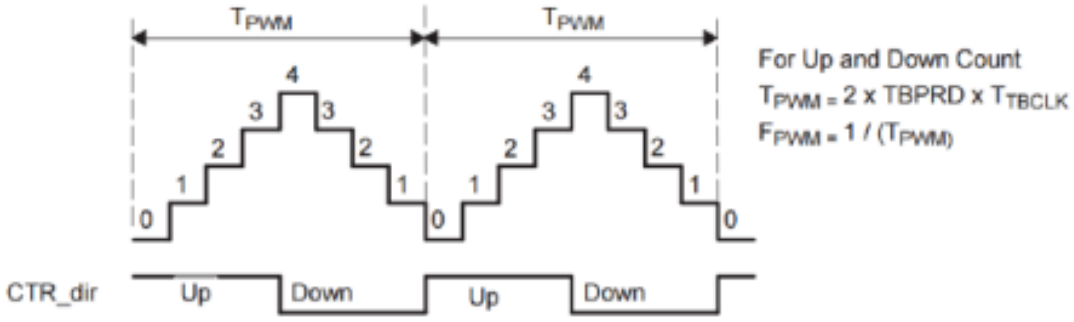

Figure 33. Up-Down-Count configuration [4]

Once the count mode is chosen, the next step is to determine the Time Base Period. Knowing the frequency of the DSP is 150 MHz and the desired switching frequency is set to 10kHz the value for the Time Base Period register (TBPRD) is given by 4.1.

$$TBPRD = \frac{f_{CLK}}{2 * f_{sw}} = \frac{150000[MHz]}{2 * 10[kHz]} = 7500 \tag{4.1}$$

To avoid a short-circuit a dead-band will be configured. Figure 34 shows the deadband range for the ePWM module, it consist of two dead-bands, RED and FED. The counter is set to 300 which is equal to the value given in Eqaution 4.2.

$$TDB = \frac{DB_{Counter}}{f_{CLK}} = \frac{300}{150000[kHz]} = 2\mu s \tag{4.2}$$

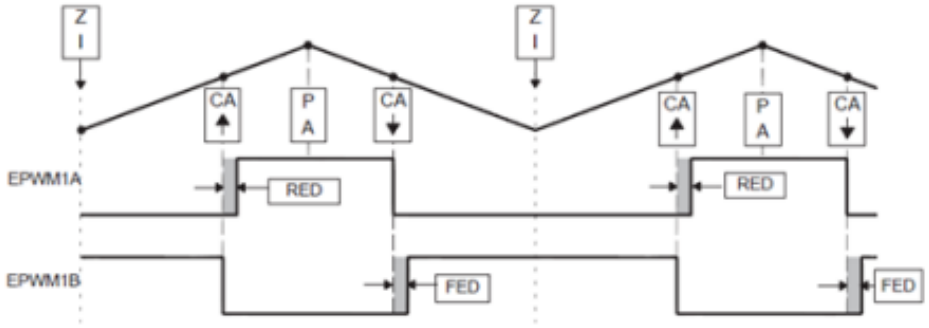

Figure 34. Dead-Band configuration of ePWM1a/b. [4]

Figure 35 shows the PWM siganls at 10 kHz with a plot of 100µs per division. In Figure 35 it shows the six PWM signals where ePWM11/b corresponds to leg “A”, ePWM2a/b corresponds to leg “B” and ePWM3a/b corresponds to leg “C”.

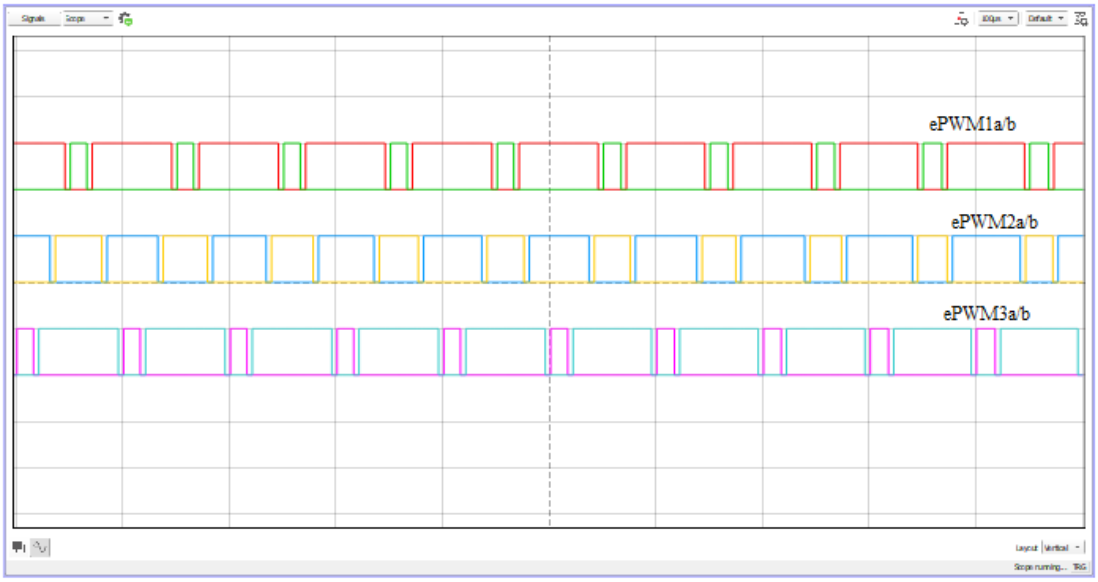

Figure 35. PWM signals simulated with fs =10 kHz

4.5 ADC Configuration

In order to trigger the ADC module, ePWM1 will be used to trigger the start of conversion. The ADC is going to work at 10 kHz. Figure 36 shows the following commands used to trigger the ADC.

```
EPwm1Regs.ETSEL.bit.SOCAEN = 1;        // Enable SOC on A group
EPwm1Regs.ETSEL.bit.SOCASEL = 0x2;     // Select SOC from CPMA on Period
EPwm1Regs.ETPS.bit.SOCAPRD = 1;        // Generate pulse every event
```

Figure 36. ADC trigger command

For the test in Typhoon HIL the motor currents, DC link voltage and speed (throttle) values will be converted by the ADC module. The next step is to obtain the scaling factor, this is the value read by the ADC module which is given by 4.3

$$Digital\ Value = 4095 * \frac{Analog\ Value(Input)}{3} \tag{4.3}$$

Motor Current: The conversion for the motor current is obtained from the LEM HAH3DR 900-S0D current sensor. Equation 4.4 is used to obtain the scaling factor.

$$Scaling\ factor = \frac{3}{4095} * 450.4505 * (5/3) \tag{4.4}$$

Figure 28 shows the code used to obtain the motor current.

```
I_PhA = (ADC_DSP[1] * Scaling_Factor_Iphase);      // Phase A motor current
I_PhB = (ADC_DSP[2] * Scaling_Factor_Iphase);      // Phase B motor current
I_PhC = (ADC_DSP[3] * Scaling_Factor_Iphase);      // Phase C motor current
```

Figure 37. Motor phase currents

DC link voltage : The scaling factor for the DC link voltage is shown in Equation 4.5.

$$Scaling\ factor = \frac{3}{4095} * 500 \tag{4.5}$$

```
DC_Bus = ADC_DSP[0] * VBus_Scale_Factor; //  DC link voltage
```

Figure 38. DC link voltage

Throttle Command : The range of the throttle value is [0, 5V]. The scaling factor is shown in Equation 4.6.

$$Scaling\ factor = \frac{3}{4095} * 2.5 \tag{4.6}$$

```
Throttle = ADC_DSP[1] * VThrottle_Scale_Factor;  // Throttle command
```

Figure 39. Throttle command

4.6 Clarke Transformation code

As already mentioned in chapter 2, using the Clarke transformation the motor phase currents are transformed into the two-phase reference frame. The Clarke transformation code is shown below. Figure 40 shows the Clarke transformation macro that is used to convert the three phase currents to a two-phase reference frame. Macros presented in the following sections are located in *C:ti\controlSUITE\libs\app_libs* folder.

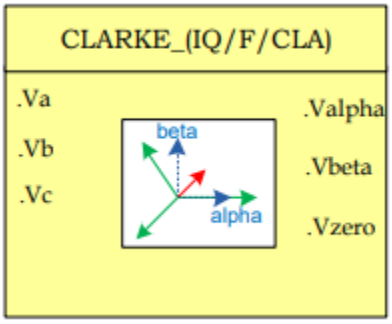

Figure 40. Block diagram of Clarke module [5]

```
clarke1.As=_IQ((ADC_DSP[2]*0.00024414-offsetA_pu)*2*0.909); // Phase A current.
clarke1.Bs=_IQ((ADC_DSP[3]*0.00024414-offsetB_pu)*2*0.909); // Phase B current.
clarke1.Cs=_IQ((ADC_DSP[4]*0.00024414-offsetC_pu)*2*0.909); // Phase A current.
CLARKE_MACRO(clarke1)  // Clarke Macro
```

Figure 41. Clarke transformation

4.7 Park Transformation code

The Park module shown in Figure 42 is used to transform from the stationary reference frame to the rotating reference frame. This module can be found in the control SUITE library from Texas instrument. The Park transformation code is shown below in Figure 43.

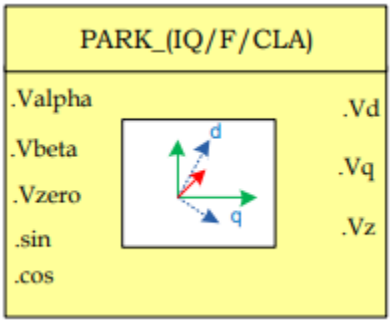

Figure 42. Block diagram of Park module [5]

```
park1.Alpha = clarke1.Alpha;        //     park transformation
park1.Beta = clarke1.Beta;          //     park transformation
park1.Sine = _IQsinPU(park1.Angle);     // angle used for park transformation
park1.Cosine = _IQcosPU(park1.Angle);   // angle used for park transformation
PARK_MACRO(park1)               //      park macro
```

Figure 43. Park transformation

4.8 Inverse Park code

The Inverse Park module shown in Figure 44 is used to transform from the rotating reference frame to the stationary reference frame. The Inverse Park transformation code is shown below in Figure 45.

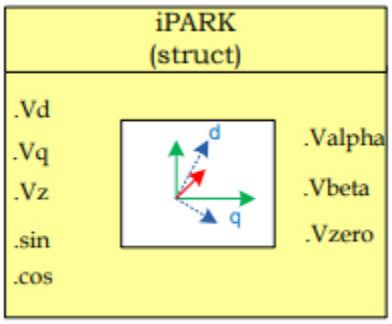

Figure 44. Block diagram of Inverse Park module [5]

```
ipark1.Ds = pi_id.Out;          //    Input of Inverse Park d
ipark1.Qs = pi_iq.Out;          //    Input of Inverse Park q
ipark1.Sine=park1.Sine;
ipark1.Cosine=park1.Cosine;
IPARK_MACRO(ipark1)             //      Inverse Park macro
```

Figure 45. Inverse Park transformation

4.9 Space Vector Pulse Width Modulation

To generate the require SVPWM the SVGEN module will be used. This module calculated the duty ratios needed to generate the stator reference voltage. The module's inputs are the inverter αβ voltages obtained from the Inverse Park transformation. The code to implement SVPWM is shown below.

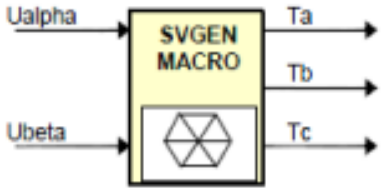

Figure 46. Block diagram of SVPWM Module [6]

```
svgen1.Ualpha = ipark1.Alpha;    //      Output from Inverse Park transformation
svgen1.Ubeta = ipark1.Beta;      //      Output from Inverse Park transformation
SVGENDQ_MACRO(svgen1)            //      SVM macro
//scale the time multipliers
da = (svgen1.Ta + 1)/2;
db = (svgen1.Tb + 1)/2;
dc = (svgen1.Tc + 1)/2;
EPwm1Regs.CMPA.half.CMPA = da * PWM_TBPRD;
EPwm2Regs.CMPA.half.CMPA = db * PWM_TBPRD;
EPwm3Regs.CMPA.half.CMPA = dc * PWM_TBPRD;
```

Figure 47. Space vector modulation

4.10 Simulation Results

In this section the results of the HIL simulations are presented. Based on the system schematic present in Figure 48, shows the Typhoon HIL SCADA interface while the motor is running when a constant load torque is applied. The interface also shows the motor temperature, cold plate temperature and the throttle value, all of which are used in the C-Code. Figure 49 shows the Alpha and Beta waveforms that are obtained from the Clarke transformation as well as the waveform for the electrical angle used for both the Park and Inverse Park transformation. Figure 50 shows the SCADA interface when the model is running, it also all three phase currents Ia, Ib and Ic, the results from the Clarke transformation (*iα, iβ*) and the *dq* currents. Figure 51 shows a view of all the signals presented in Figure 50.

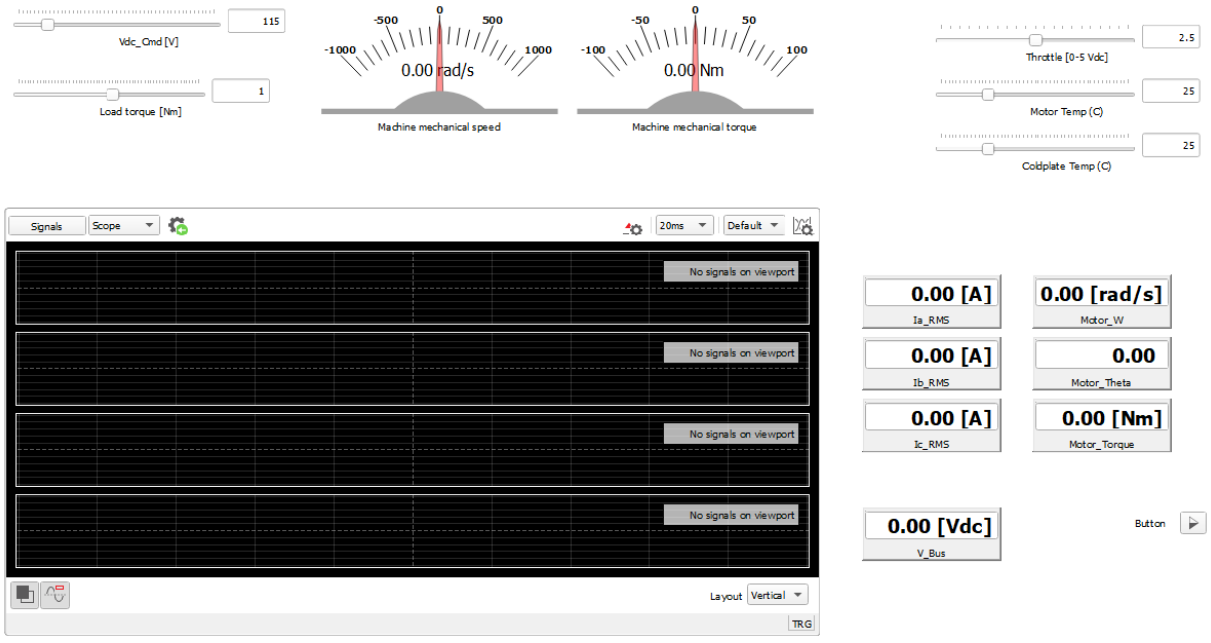

Figure 48. SCADA user interface

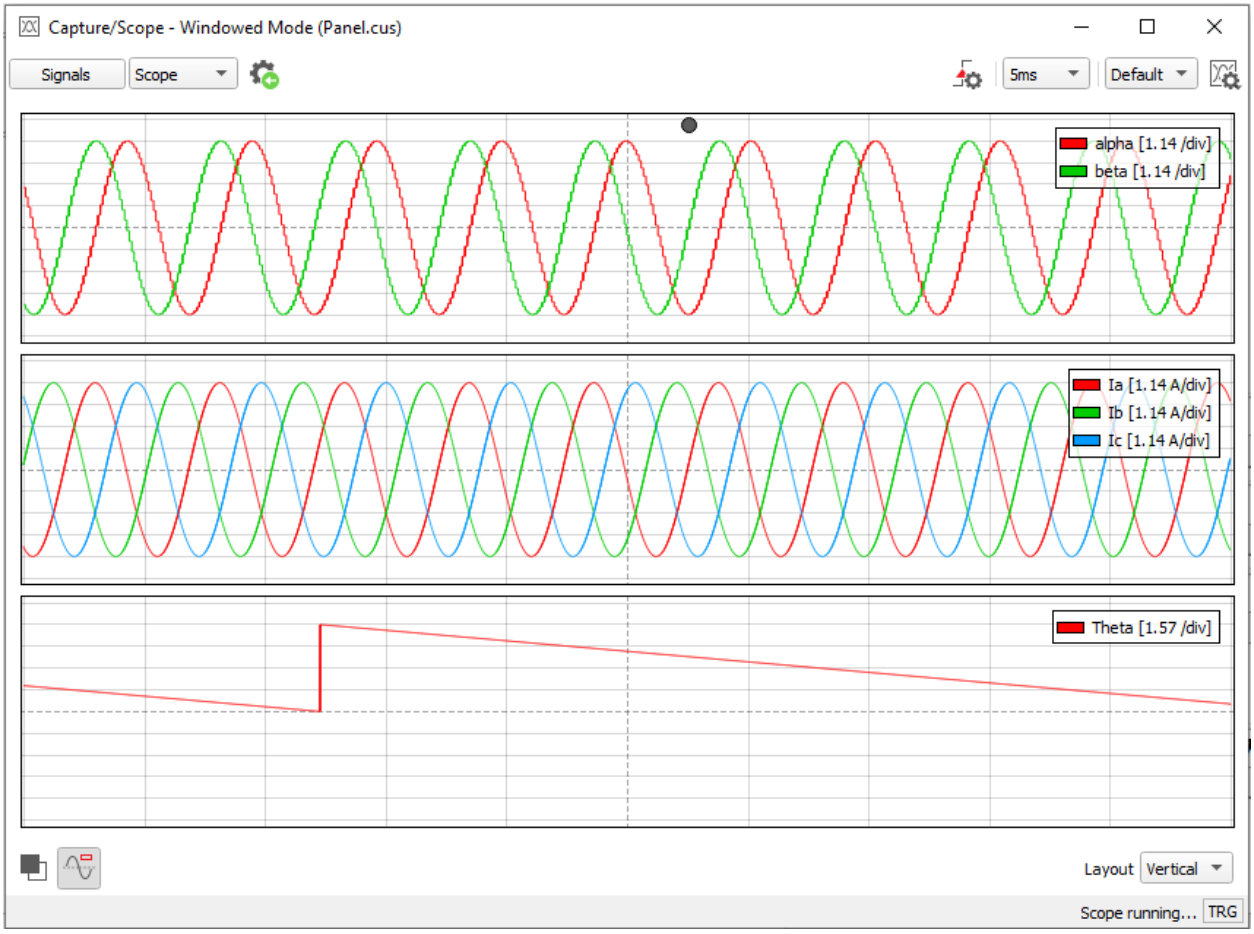

Figure 49. a) Alpha, Beta waveforms b) Three phase output currents c) Electrical angle (Theta)

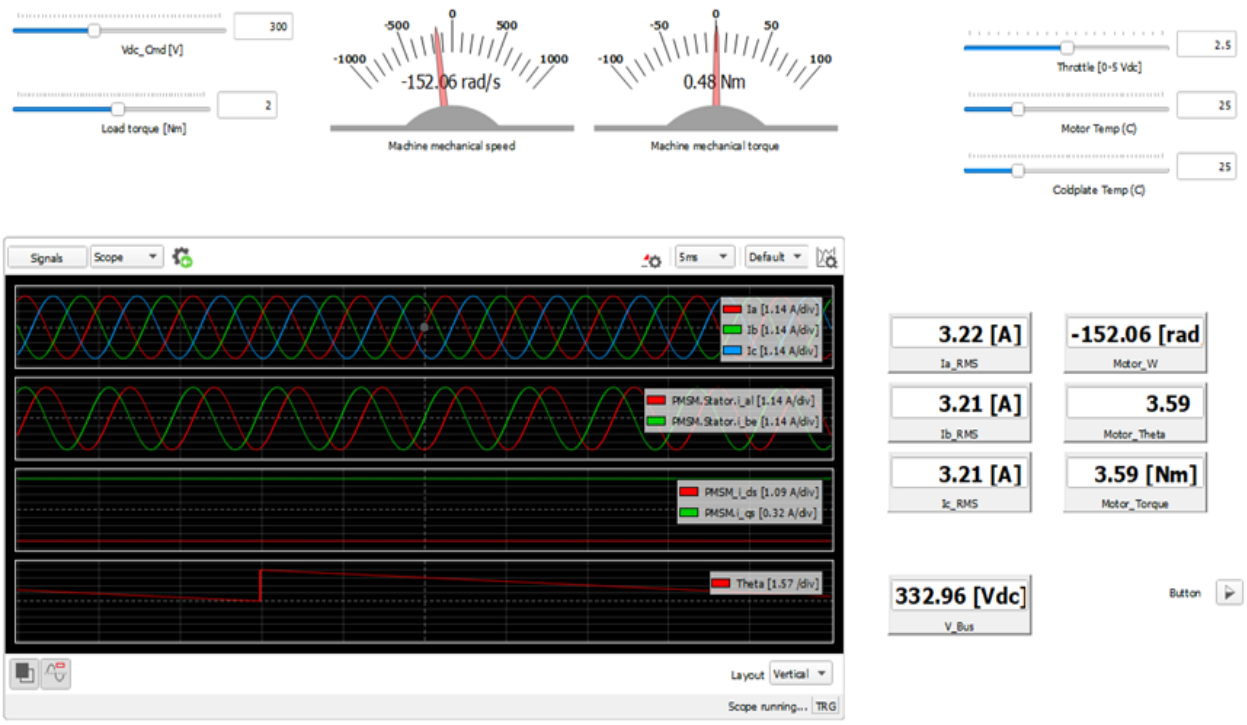

Figure 50 SCADA user interface

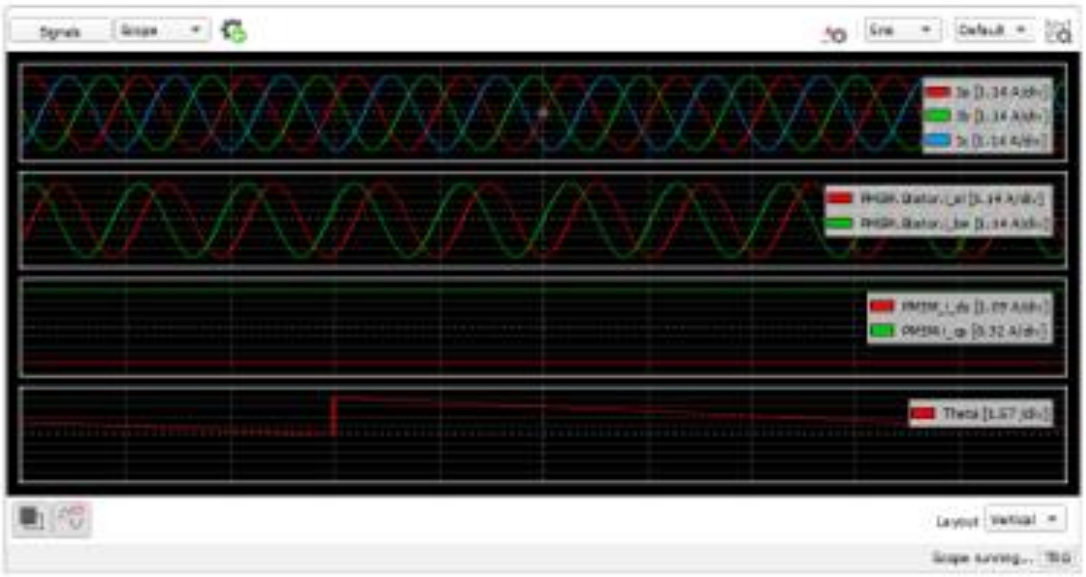

Figure 51. a) Three phase output currents b) Alpha, Beta waveforms c) dq currents d) Electrical angle (Theta)

4.11 Reference

[1] *HIL602*. Typhoon HIL. (2019, September 19). Retrieved September 19, 2021, from https://www.typhoonhil.com/products/hil602/?__hssc=85443206.1.1480032000000&__hstc=85443206.e6e3fe43a844f9b0aec92bf5cd3c2a17.1480032000000.1480032000000.1480032000000.1&hsCtaTracking=7c235e3b-e5c3-4bbc-95c3-714b91664928%7C29878d5d-79be-4b09-baa5-08efbfb85ce4.

[2] *HIL DSP 180 interface*. Typhoon HIL. (2021, February 26). Retrieved November 19, 2021, from https://www.typhoon-hil.com/products/hil-dsp-interface/.

[3] *Typhoon Hil DSP interface - quarbz.com*. (n.d.). Retrieved November 19, 2021, from https://www.quarbz.com/wp-content/uploads/2020/01/Typhoon-HIL-DSP-Interface-Brochure.pdf.

[4] *TMS320X2833X, TMS320X2823X technical reference manual - ti.com*. (n.d.). Retrieved October 5, 2021, from https://www.ti.com/lit/ug/sprui07/sprui07.pdf.

[5] *CONTROLSUITE*. CONTROLSUITE Driver or library | TI.com. (n.d.). Retrieved October 19, 2021, from https://www.ti.com/tool/CONTROLSUITE.

[6] *TMS320X2833X, TMS320X2823X technical reference manual - ti.com*. (n.d.). Retrieved October 1, 2021, from https://www.ti.com/lit/ug/sprui07/sprui07.pdf.

CHAPTER 5

CONTROLLER HARDWARE DESCRIPTION PROCESS

5.1 Introduction

In this chapter, a detailed description of the overall design will be given including all the hardware components. This overview will mainly focus on the controller board, the design architecture, component selection, the sensing hardware such as the current sensors, the resolver as well as all the other electronic circuitry for the controller board.

5.2 Controller Selection

Every embedded system design has a controller that reads inputs, runs complex calculations, and communicates with other devices. The most used controllers that can complete these tasks are microcontroller, FPGAs, and digital signal processors. When selecting a controller there are numerous parameters that should be considered such as processing power, memory, system architecture, hardware architecture and hardware interface. Even though microcontrollers are easy to program it lacks the computational power needed for this project. FPGAs are fast, powerful and offer considerable number of I/O pins which enable multiple control singles to be connected to or controlled but can produce numerous programing challenges. The core of the controller board design is centered around the digital signal processor (TI TMS320F28335) which will be required to accomplish numerous task such as complex calculations and motor controls. The LATTICE MachXO2 FPGA will also be used for version 1 of this project. Figure 52 shows the DSP that will be used for the project

Figure 52. Texas Instrument TMS320F28335

Table 5. TMS320F28335 Specifications [1]

Parameters	TMS320F28335
CPU	C28x
Total Processing Power	150 MIPS
Operating Frequency	150 MHz
Flash	512 KB
RAM	68 KB
ADC	16 Channels 2 Sample and hold Circuits 12-bit resolution
SPI	1 Module
PWM	12 Channels
SCI	3 Modules
GPIO	88
CAN	2 Modules
QEP	2 Modules
Features	32-bit CPU Timer Watchdog Time 2-pin Oscillator External Interface

Texas Instrument provides numerous solutions for implementation digital motor control. They provide DSPs with high computational power and provide all the necessary peripherals need for motor controls. It contains modules for CAN and SPI communication, 12 PWM channels, 12-bit ADC module with 16 channels for voltage, temperature, and current measurements, 88 GPIOs pins and it contains a floating-point unit to accelerate mathematical calculations. Table 5 shows

the available resources associated with the TMS320F28335 DSP. Texas Instrument also provides the motor control libraries with all the necessary headers, maps, and configuration files.

5.3 Gate Driver Interface

The TI TMS320F28335 DSP operates at 3.3 V logic, while the CGD12HBXMP gate drivers require differential input. To convert the single ended signal from the DSP to a differential signal a AM26LV31E Low-Voltage High-Speed Quadruple Differential Line Driver was placed between the gate drivers and the DSP. A low pass filter circuit is constructed for each single ended signal before entering the differential transceiver. The reason for the low pass filter is to minimize noise that could create false signals. Converting from single ended signal to differential signal significantly reduces the impact of the radiated noise significantly when power modules switch states. The gate driver status signals are converted to a single ended signal before being sent to the DSP. The CGD12HBXMP gate driver module has numerous features such as undervoltage lockout, over current protection, reverse polarity, and fault indicators. Table 6 shows the gate driver signals for a single module. The differential signals presented in Table 6 will be converted to a single ended signal before being sent to the DSP. For the proposed system each of the gate driver modules require two PWM channels, one I/O for the fault signal, one I/O for the power supply disable, one I/O for the PWM enable, one I/O for the RTD, and one I/O for the reset signal.

Table 6. CGD12HBXMP Gate Drive Signals [3]

Pin Number	Name	Description
1	VDC	Power supply input pin
2	Common	Common
3	HS-P(*)	Positive line of 5 V differential high-side PWM signal pair. Terminated into 120Ω.
4	HS-N(*)	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120Ω.
5	LS-P(*)	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120Ω.
6	LS-N(*)	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120Ω.
7	$\overline{\text{FAULT}} - \text{P}(*)$	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA.
8	$\overline{\text{FAULT}} - \text{N}(*)$	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	RTD-P(*)	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA.
10	RTD-N(*)	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA.
11	$\overline{PS - Dis}$	Pull down to disable power supply. Pull up or leave floating to enable. Gate and source are connected with 10kΩ when disabled.
12	Common	Common
13	PWM-EN	Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common
15	Reset	When a fault exists, bring this pin high to clear the fault.
16	Common	Common

Figure 53. Wolfspeed CGD12HBXMP Gate Driver Module

5.4 Resolver to Digital Converter

In sensor Field Oriented Control, there are several options to measure position and speed of the motor which include resolvers, encoders, hall sensors etc. Resolvers are used in harsh environments and for extreme applications such as oil and gas production, control systems in military vehicles and in steel and paper mills. Resolvers also are resistant to the shock and vibration often encountered in aerospace applications, so based on these facts a resolver will be used for this application. Ampaire provided NCREPT with the EMRAX PMSM motor which has a BRX-TS2620N21E11 resolver attached. The operation principles of the resolver are similar to a transformer. A resolver consists of a primary winding and a pair of secondary windings which are the sine and cosine windings that are positioned with a 90º offset from one another. Figure 54 shows a schematic for a variable reluctance resolver used for this application.

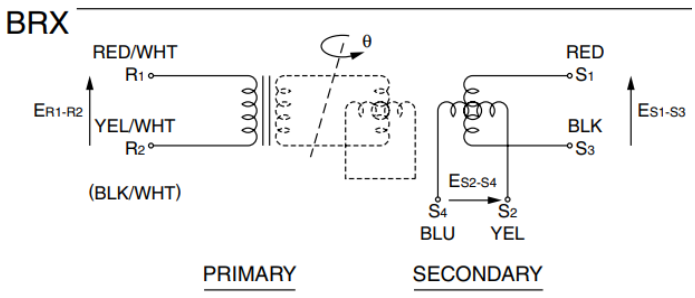

Figure 54. BRX resolver schematic [5]

The resolver output voltage :

$$\text{S3-S1} = E_0 sin\omega t * sin\theta \tag{5.1}$$

$$\text{S2-S4} = E_0 sin\omega t * cos\theta \tag{5.2}$$

where Θ is the shaft angle,

Sinωt is the rotor excitation frequency,

E_0 is the rotor excitation amplitude,

When the resolver turns with the load it induces sinusoidal voltages on the secondary windings. The ratio of the output voltages can then be used to calculate the angular position of the load. A resolver to digital chip is needed to converter the output signals of the resolver to a value that the DSP can use. The AD2S1210 RDC chip is used in the design. The functional block diagram of the AD2S1210 is shown in Figure 55. An on board programmable sinusoidal oscillator provides the excitation signal to the resolver; additional circuitry is used to increase the gain and current to drive the resolver. This is the excitation signal that drives the primary windings of the resolver. The resolver then generates the sine and cosine signals which are transformed to digital signals by the ADC of the AD2S1210. The digital signals are the angular position or velocity of

the motor. Serial Peripheral Interface (SPI) communication is used to transfer the data from the position/velocity registers of the AD2S1210 to the spi registers of the DSP.

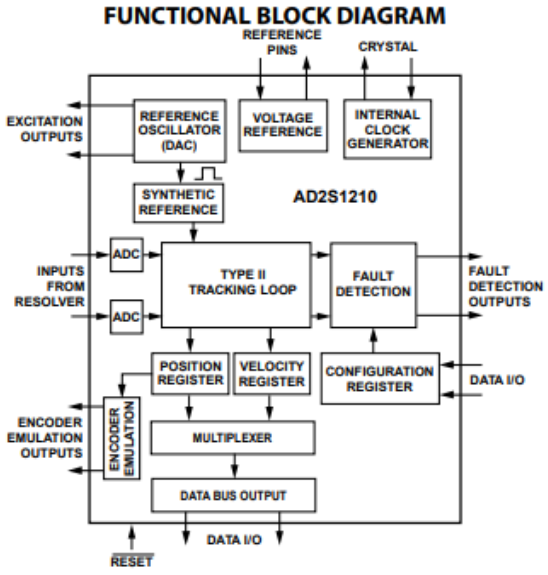

Figure 55. Resolver to Digital Converter Functional Block Diagram [11]

5.5 Power Supplies

The main power input for the controller board is 24 Vdc supplied via a terminal block. This input voltage is then supplied to three DC/DC converters which are used to generated three power rails, +5V, 3.3 V, and +12V. The +12V is the dedicated supply for the gate drivers, the +5 V and +3.3 V are used for the numerous IC located on the controller board. There is an isolated +5V to +5V power rail to supply the CAN transceiver. Finally, there is a triple buck converter that supplies the +1.8V and +3.3 V from both the microcontroller and the FPGA. LEDs are present on the board to indicate the +12 V, +3.3V +5V power rails.

5.6 CAN Interface

Failures in a CAN network results from high-voltage noise and spikes on the power distribution bus, ground potential differences between subsystems and from radiated energy. For

a robust CAN network, isolation from the power bus and isolation of the communication buses should be implemented.

The TMS320F28335 supports two Control Area Network modules that can be programmed to be used independently. The CAN modules of the TMS320F28335 can be mapped to serval GPIO pins for the CAN TX and CAN RX pins. The CAN TX and CAN RX signals must be connected to a CAN transceiver to interface with the differential High and Low signals which are present on the CAN bus. The ISO1050 Isolated CAN transceiver IC was used for this application. It provides an isolation barrier of 2.5 kV and supports CAN FD with speeds of 5 Mbps. The ISO1050 also provides bus fault-protection voltage and stronger EMC performance. The CAN interface circuit is shown in Figure 49. Table 7 shows all the data that will be sent to the aircraft from the inverter via CAN Communication.

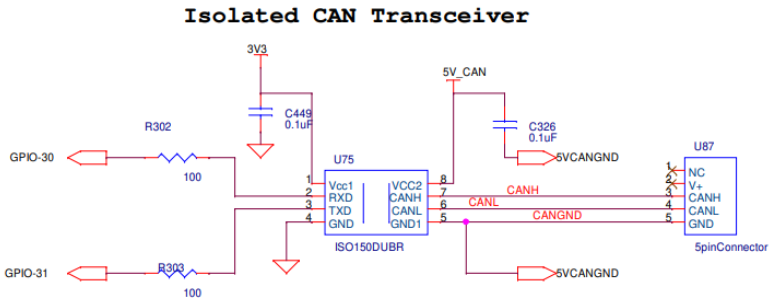

Figure 56. CAN Interface

Table 7. CAN Communication Inverter Signals

Message Name	Signal	Description
System Status	Fault	Fault
	PWM Fault	PWM Fault
	Status	Inverter System Status
	Speed Measurement	Mechanical Shaft RPM
Commands	Command Word	Run State
	Speed Reference	Speed Reference
Calculated Values	Vbus	Vbus dc input
	Ia_RMS	Phase A RMS Current
	Ib_RMS	Phase B RMS Current
	Ic_RMS	Phase C RMS Current
Temperatures	T_Module1	Module 1 temperature
	T_Module2	Module 2 temperature
	T_Module3	Module 3 temperature
	T_Motor	Motor temperature
Warning Status	Warning	Warning
	PWM Warning	PWM warning
	Resolver Warning	Resolver warning
Resolver Values	Resolver Position	Resolver position
	Resolver Velocity	Resolver velocity

5.7 Current measurement

For many motor control schemes, phase currents are required as input values. There are different methods presented in literature used to measure the phase currents of a motor. The LEM HAH3DR 900-S0D current sensor was implemented in this application. The HAH3DR 900-S0D is a tri-phase, open loop transducer which provides galvanic isolation between the primary and secondary circuits. The sensor also provides low thermal offset and sensitivity drift and high frequency bandwidth. Each phase of the current sensor has an integrated Hall effect circuit which converts the measured flux into a voltage based on the current flowing through the conductor. The HAH3DR sensor is capable of measuring currents between ± 900 A_{peak} [2] which corresponds to a 0-5 V signal. The voltage signal is filtered and scaled before being sent to the analog-to-digital converter (ADC).

5.8 DC link Voltage Sensing

Sensing the DC link bus voltage is an important parameter for motor control algorithms. The DC link voltage sensing circuit consist of a high impedance voltage divider circuit, an isolated op-amp (ACPL-C87B) and a differential to single ended op-amp. The high impedance voltage diver circuit scales the DC-link voltage to a range that is suitable for the isolated op-amp. A differential output voltage that is proportional to the input voltage is created on the output side of the isolated op-amp [4]. The differential voltage is then filtered and converted to a single ended signal before reaching the ADC input. A 0 – max DC link voltage signal is scaled to a 0-2 voltage.

5.9 Throttle Signal

The pilot of the Cesena 337 provides the throttle signal from the throttle lever of the aircraft, which produces a 0-5 V signal. To correctly read the throttle value the analog signal should be scaled and filtered prior to reaching the ADC of the DSP. The circuit consist of a resistive divider network which scales the signal to 0-3 V, a low pass filter and AD8615 Op amp.

5.10 References

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CHAPTER 6

CONTROLLER BOARD PCB LAYOUT

6.1 Introduction

In this chapter, a detailed description of the how the controller board for the 250 kW SiC three phase inverter was designed and evaluated. The process starts with the specification of the system and results with the finished hardware that fulfills these requirements. This process mentioned above can be split into several steps such as the initial design, fabrication of the controller board and testing of the overall system.

6.2 Schematic

The schematics for the initial design were created using Allegro PCB Designer (Cadence) software. A schematic should include the following, pin numbers, component names, values, and rating. The schematic was a preliminary draft of the initial design, but many revisions were expected based on scope of the project. When designing a schematic: 1) Design your schematic so that it can be easily printable. 2) Use the same symbols for the same device, this will allow for you schematic to be organized and consistent. 3) Separate your schematic into logical blocks, this makes it easier to review and troubleshoot.

A custom library was created for each of the core components for the controller board. The footprints for the components located on the controller board were designed using Cadence PCB Editor software. There are a few practices that should be followed when designing footprints for components: [3] 1) Ensure that the copper for each pin for the component is slightly larger and is properly located. 2) Ensure that at least 2.5 to 3 mils of soldering mask is applied between every pin on the board.

Figure 57 shows the schematic for the CAN Communication circuitry, which has a CAN transceiver that requires an isolated 5-volt supply and a 5-pin header to connect to the CAN bus. Figure 58 shows the schematics for the Run/Enable and the Estop. Both the Run/Enable and Estop require an optocoupler to be place between the input control voltage and GPIO of the DSP. Optocoupler provides isolation between the control circuitry and the input control voltage. Figure 59 shows the schematic for sensing the DC link bus voltage.

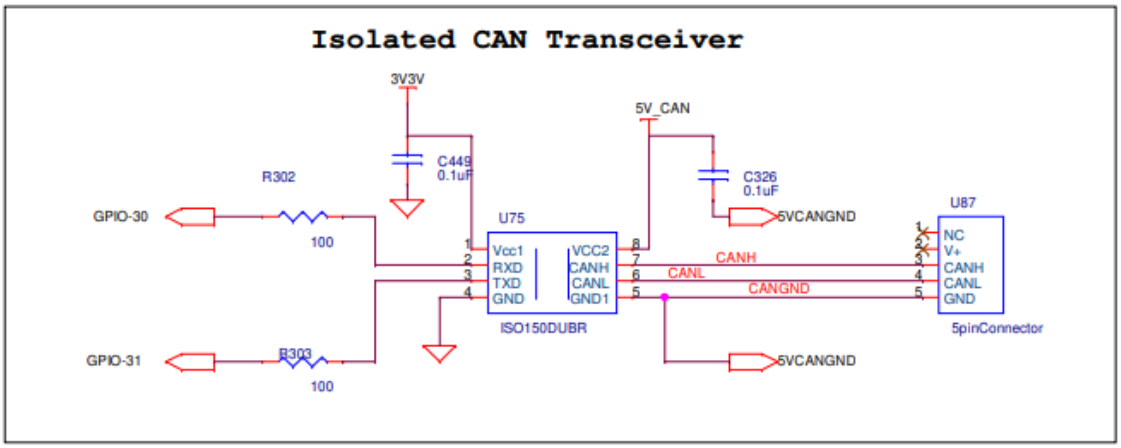

Figure 57 Isolated CAN Transceiver

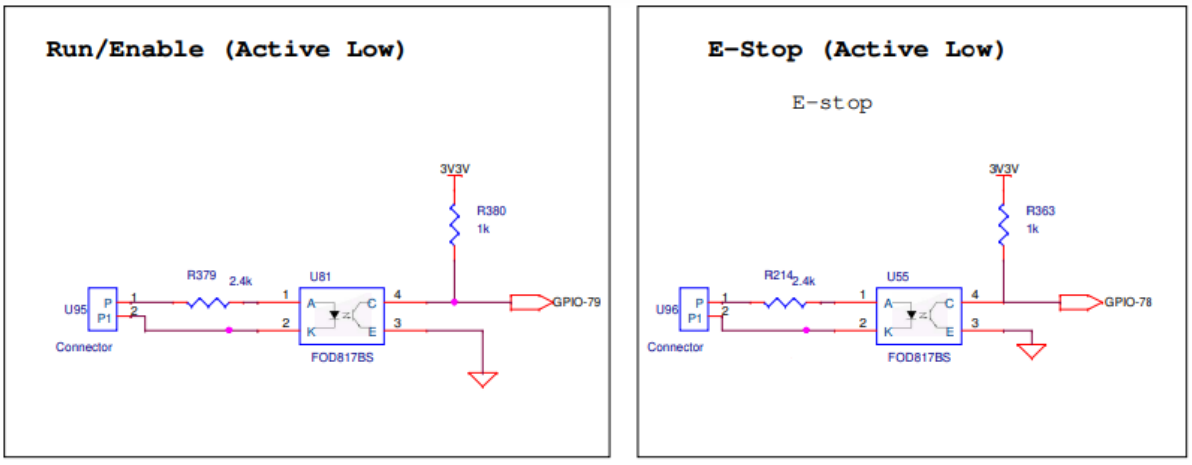

Figure 58. Inverter E-stop Run Command

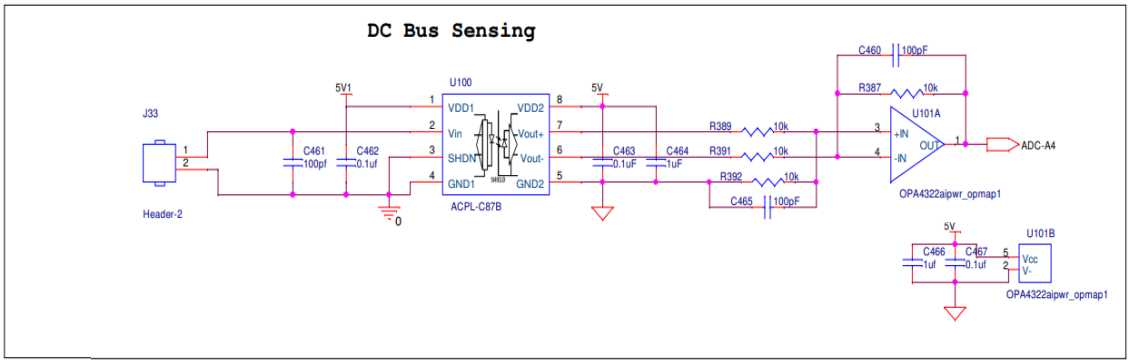

Figure 59. DC Bus Monitoring circuit

6.3 Component Placement Controller Board V.1

Component placement can be considered one of the most important aspects when designing the layout of a PCB. The optimal placement maximizes the circuit performance while also adhering to spacing guidelines for thermal, electrical noise, mechanical and manufacturing requirements[1]. Components must be separated based on their functions i.e., power, digital and analog components should be grouped separately to minimize intersecting connection paths. In [2] there are certain requirements that should be followed when placing components such as 1) placing must-have components first i.e., components that must be placed in specific locations, 2) placing large processors and IC chips in the center of the PCB. Locating these components in the center of the board makes trace routing easier. 3) Surface Mount Devices (SMD) PCB design rule – it is recommended to place all SMD components on the same side of the board.

The controller board can be divided into four main sections: Power filtering, gate drive circuity, resolver circuitry and the FPGA/digital signal processor/peripheral connections. The layout of the control board, seen in Figure 60 contains several important features. Power is supplied through a screw terminal located on the top left of the board next to an electrolytic capacitor. The input power is then distributed to the DC/DC converters that are used to set down in the input supply to the voltage values that were mentioned in Chapter 5, Section *5.5* section.

Figure 60. Controller Board V.1

The drive circuitry for the gate driver is located on the bottom of the controller board. It consists of the AM26LV31E Low-Voltage High-Speed Quadruple Differential Line Driver, the supported passive components, and the external connectors for the gate driver modules. The main object of the driver circuitry is to convert the single ended signal from the DSP to a differential signal for the high/low gate of the MOSFET.

The TI TMS320F28335 DSP and the Lattice FPGA are placed in the center of the controller board. Within this section, there are a few subsections including the FT2232HL FTDI chip which is the JTAG interface for the Lattice FPGA chip. This component is located on the top right of the

controller board with its associated circuitry. A JTAG interface is used to program the TMS320F28335 DSP, a 14-pin header is used for this task it is located on the top of the controller board.

The Resolver to Digital chip is located next to the FPGA with its associated circuitry. Test points were added to measure the differential excitation voltages applied to the resolver as well as the differential input Sin and Cosine voltages produced by the resolver. The resolver connector is a 6-pin lock connector which is located on the bottom right of the controller board.

The traces for each of the sections mentioned previously were designed based on how much current was expected to be running through them. The traces on the board can be divided into two groups: signal level traces and power level traces. There are a total of 6 layers for the controller board.

- Layer 1 – Power Plane
- Layer 2 – Ground Plane
- Layer 3;4;5;6 – Signal Planes

The complete layer by layer stack up is included in Appendix A.

Figure 61 shows a 3D rendering of the controller board inside the 250-kW inverter.

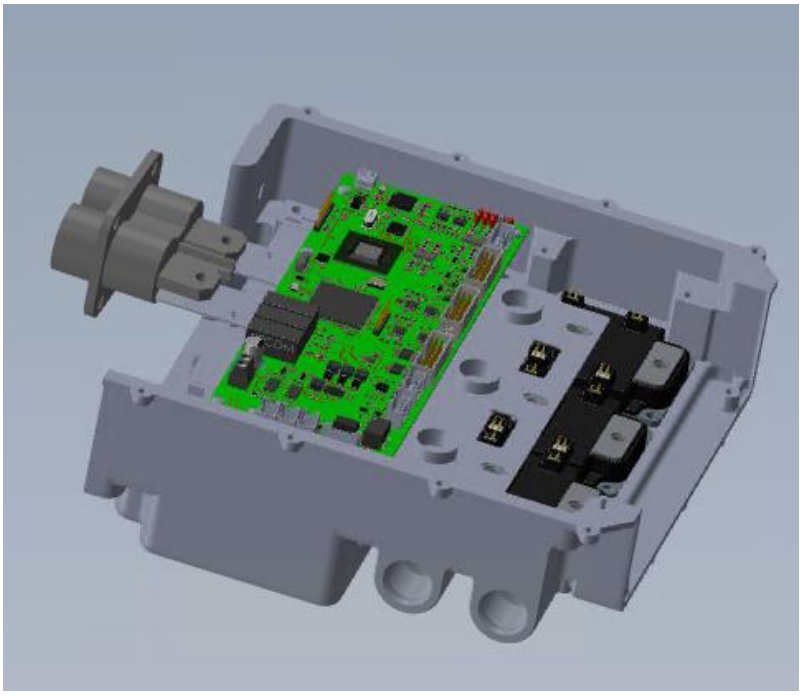

Figure 61. 3D model of the inverter

6.4 Testing the Prototype with the Controller board V1

After fabrication of the controller board completed, the next step was testing the prototype. The protoype is a 2-Level three-phase inverter that consist of three half bridge SiC MOSFETs.There also are three gate driver boards located on the top of the SiC MOSFETs. Figure 62 shows a completed picture of the inverter.

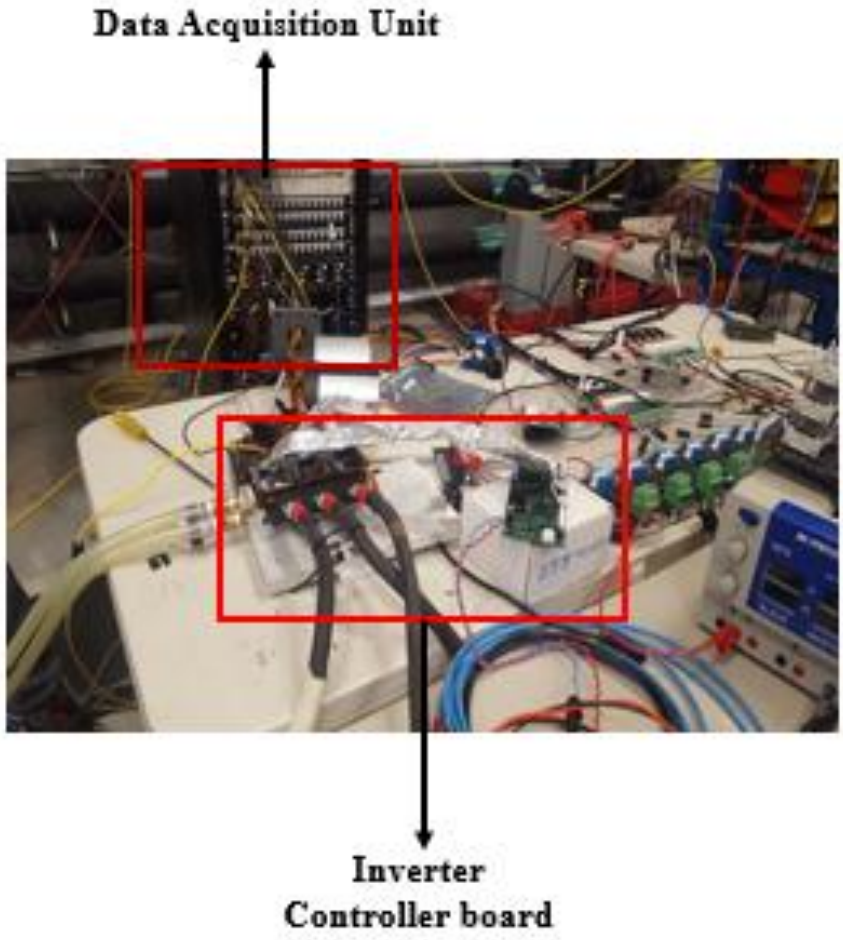

Figure 62. Test setup for the 250-kW inverter

The test setup shown in Figures 63 and 64 consisted of the 250-kW inverter, a Sorensen dc power supply, coolant loop and the simplex load. This test allowed the inverter to reach a maximum peak power of 160 kW. The schematic of the test setup is shown in Figure 64a with the test results.

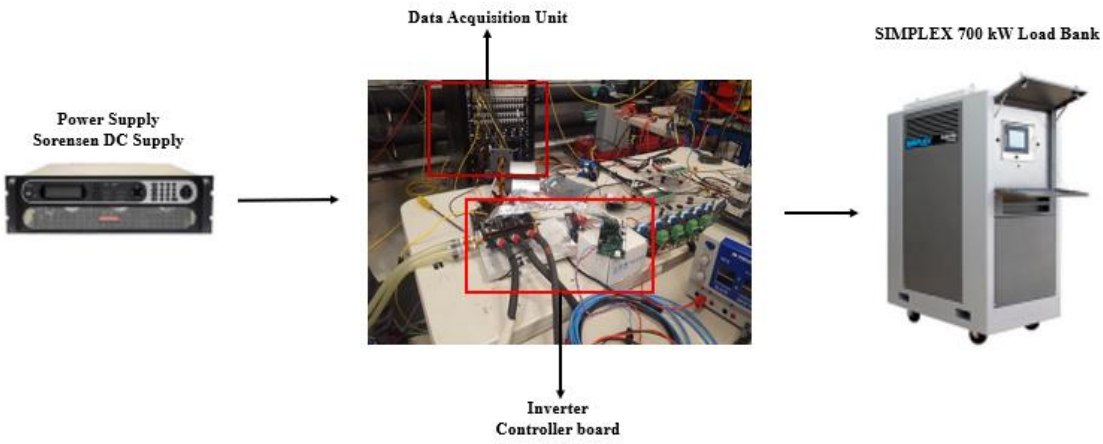

Figure 63. Three phase test setup

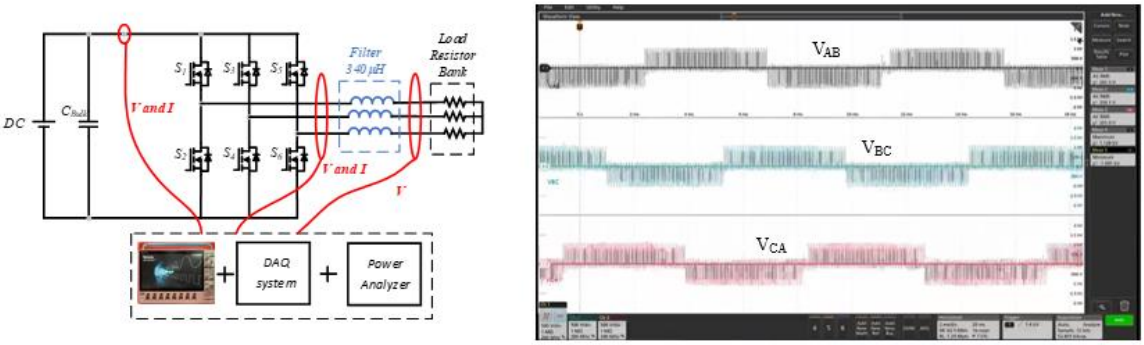

Figure 64. (a) Load testing schematic (b) Load testing waveforms

The efficiency of the inverter was also obtained from the test. The input and output power were obtained from the Yokogawa WT1600 Power Analyzer. At rated power the efficiency of the inverter is around 99.1%.

6.5 References

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CHAPTER 7

EXPERIMENTAL STUDIES AND PERFORMANCE VERIFICATION

7.1 Introduction

Different test procedures were conducted to verify the design. (Version 2 of the controller board was used with the inverter for testing, designed by Dr. Farnell). The reason to perform these different test procedures is to ensure the equipment is safe to fly. In this chapter, information about these tests will be presented. These tests have been derived from DO-160G. The test procedures that were conducted were:

- High-Temperature Operation
- Operational Shocks/ Vibration

7.2 Vibration Testing

In this section information about the vibration test will be presented. The test setup consisted of the 250-kW inverter, a Sorensen dc power supply, coolant loop and a resistive load. The purpose of this test is to verify that the equipment can function when experiencing vibration that is normally in aircraft operation within margin. Vibrational testing was done by The University of Arkansas Mechanical team. This vibration test is derived from DO-160G, Section 8.0, Aircraft Type 4, Category S, Curve M/Curve L, Zone 1[1].

Figure 65. Vibration and Shock Chamber

Figure 65 shows the vibrational chamber used throughout the testing procedure.

The test procedure is as followed:

1. The inverter was secured to the shaker mounting plate oriented along the z-axis by means of intermediate mounting plate.

2. The equipment was then turned on to become operational and coolant was turned on. A waiting period of a few minutes was implemented to ensure thermal equilibrium.

3. With the equipment operating and coolant flowing through the loop, frequency sweeps were conducted from 14 Hz to 150 Hz at 1 octave per minute at 3.0 g-PK.

4. In total, 8 frequency sweeps were completed.

Figure 66. Mounting of the inverter in the Vibrational Chamber

5. Functionality of the equipment was verified in real time throughout the testing period, and at the end inspection for evidence of structural failure was carried out.

6. The steps were then repeated for the x-axis and the y-axis.

7.3 Operational Shock Testing

In this section information about the shock test will be discussed. The test setup consisted of the 250-kW inverter, a Sorensen dc power supply, which will be used to provide the 800 V dc bus for the inverter, the coolant loop which is at 25ºC and a resistive load. The purpose of this test is to verify that the equipment can function when experiencing shocks that are normal in aircraft operation with margin, for example, taxiing, landing, and gusts in flight. The following test is derived from DO160G, Section 7.0, Category A [2]. The University of Arkansas Mechanical team performed the Operational Shock testing.

The test procedure is as followed:

1. Inverter was secured to the shaker mounting plate by means of intermediate mounting plate and frame, oriented along the z-axis.

2. The equipment was then turned on to become operational and coolant was turned on. A waiting period of a few minutes was implemented to ensure thermal equilibrium.

3. Three shocks with T-sawtooth waveform with a peak acceleration value of **6g** in the z-direction (positive and negative). The shock pulse duration was 11 ms.

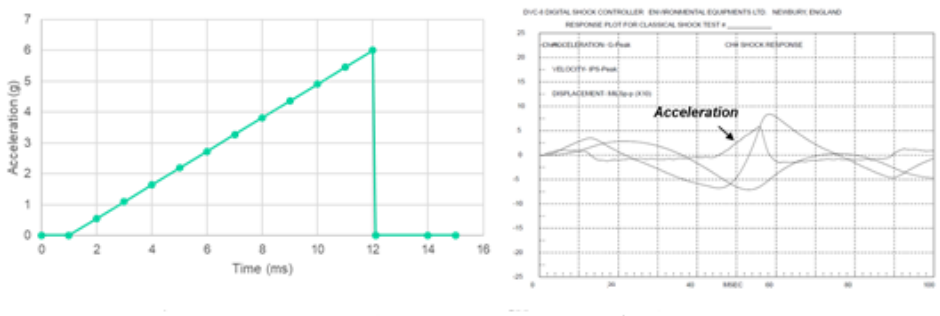

Figure 67. Shock pulse profile

4. At the end of this test, verify the functionality of the controller board and inspect for evidence of structural failure.

5. The above procedure was repeated for y and z directions as well.

7.4 Thermal Testing

In this section information about the thermal test of the inverter will be discussed. The test setup can be seen in Figure 68. It consisted of an Environmental chamber, the 250-kW inverter, a Sorensen dc power supply, coolant loop and a 700 kW Simplex Load Bank. The purpose of this test is to verify functionality at high operating temperatures that could be experienced in an aerospace environment with margin. High temperatures could also be exacerbated by being within a protective enclosure. The following test is derived from DO-160G, Section 4.5.4, Category A1[3] [4].

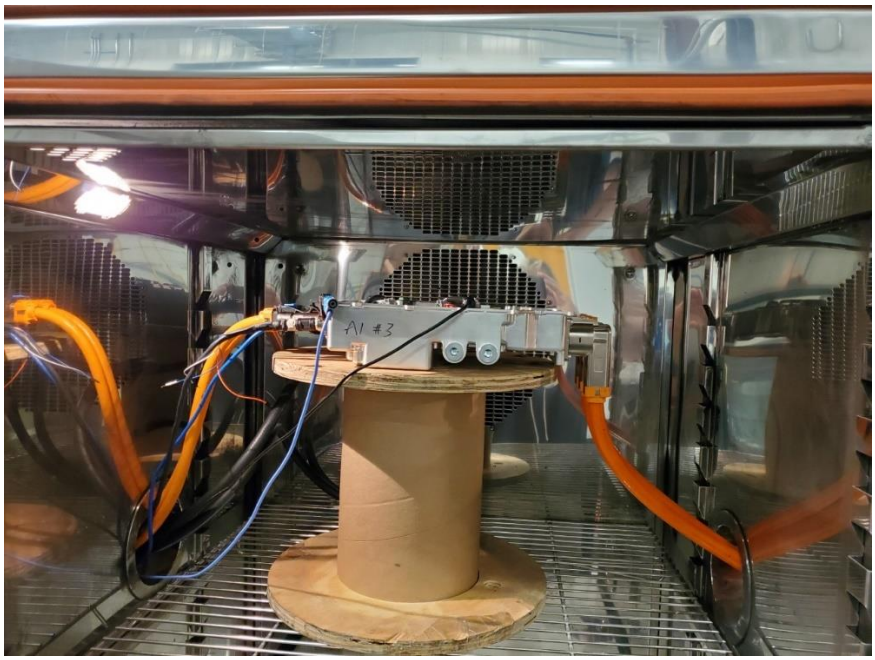

Figure 68. Interior of Environmental Chamber

The test procedure is as followed:

1. With the equipment operating, set the temperature chamber to 55°C at ambient pressure. This should be a measurement of the chamber air, not the wall of the chamber. The chamber air should be circulated to keep the chamber temperature approximately uniform, but the flow should not be directed over the equipment.

2. Allow the equipment's internal temperature to stabilize with the chamber. The internal temperature is considered stabilized when the part of the equipment with the longest thermal lag changing at less than 2°C/hour or 2 hours has elapsed whichever is shorter.

3. Operate the equipment at its highest steady-state thermal dissipation condition for two hours while maintaining the chamber at 55°C.

4. Following this period, verify the functionality of the equipment (to Performance Spec).

5. Figure 69 shows the mission profile used for the thermal testing.

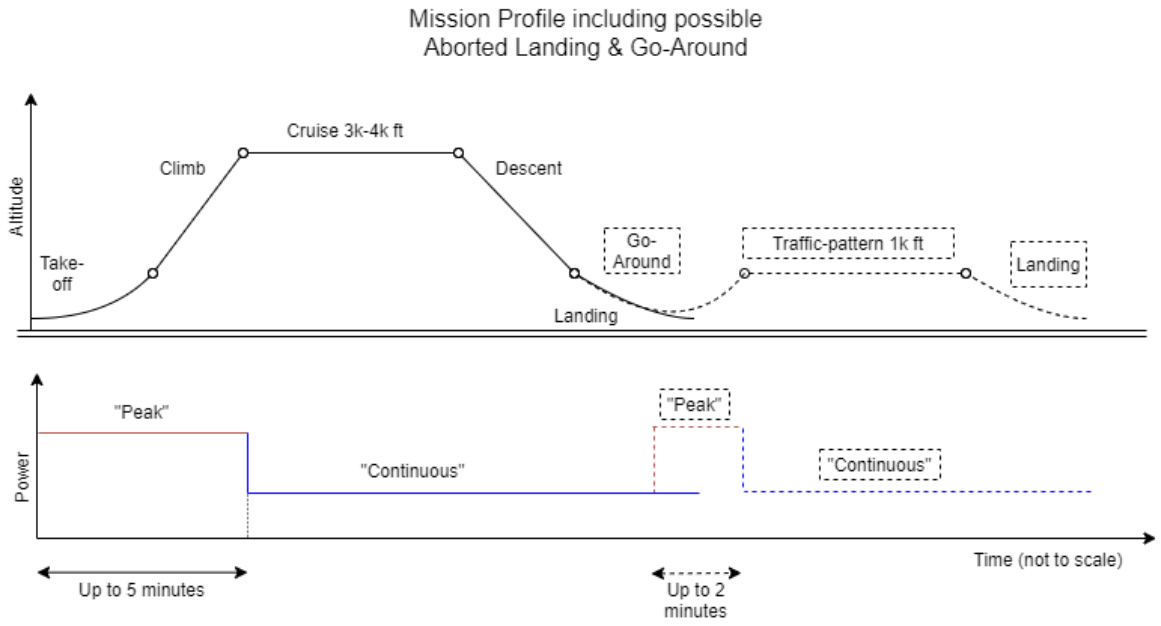

Figure 69. Mission profile of the aircraft

7.5 Test Setup for Controller Performance Validation

In this section information regarding the electrical testing will be presented. The test setup consists of the inverter, EMRAX 348 permanent magnet synchronous motor, dynamometer, two Sorensen dc power supplies, power cables, CAN communication cables, oscilloscope, differential probes, current sensors, resolver, and PC. Additionally, a LabVIEW interface was designed to monitor the controller data via CAN communication. Electrical testing was led by Dr Chris Farnell Managing Director at National Center for Reliable Electric Power Transmission (NCREPT).

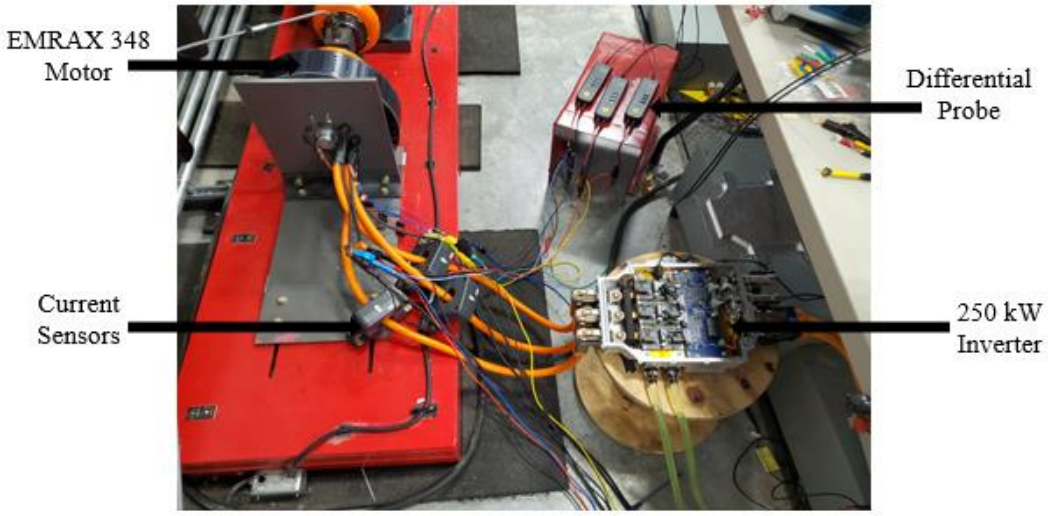

Figure 70. Inverter verification setup

7.6 Experiment and Evaluation

The test setup of the inverter is shown in Figure 70. The phase-to-phase output voltages of the motor are measured by with Tektronix high-voltage probes. The probes enable up to 1.5kV measurement range and 200 MHz bandwidth. The motor currents are measured by high frequency Rogowski coils.

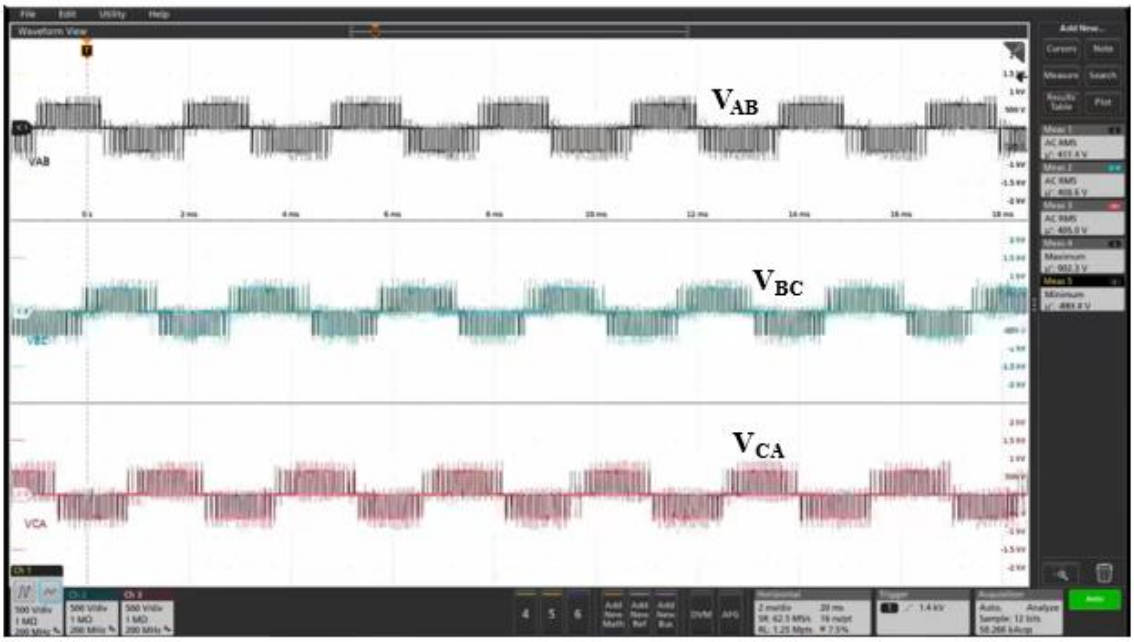

Figure 71. Continuous test waveforms at 410 V

The waveform for the continuous tests were captured in Figure 71. A HIOKI power analyzer was used to obtain the efficiency of the inverter. The overall efficiency of the inverter under test is estimated at 99.5%.

7.7 Torque-Speed Test

Figure 63 shows the setup for the torque speed test. In the test the EMRAX 348 permanent magnet synchronous motor is connected to the dynamometer which will be applying the desired torque value. An ABB drive is used to control the amount of torque that the dynamometer can applied to the load motor. The test procedure is as follows:

1. The equipment was then turned on to become operational and coolant was turned on. A waiting period of a few minutes was implemented to ensure thermal equilibrium.

2. Constant speed command was applied to the EMRAX 348 permanent magnet synchronous motor.

3. The desired torque is then applied to the load motor (dynamometer). Table 8 shows the varies torque speed test points used for this test.

Table 8. Speed, Torque Values for UUT

kW/rpm	680	1020	1700	2040	2380	2550
5	70.21525	46.81017	28.0861	23.40508	20.0615	18.72407
10	140.4305	93.62034	56.1722	46.81017	40.123	37.44813
20	280.861	187.2407	112.3444	93.62034	80.246	74.89627
30	421.2915	280.861	168.5166	140.4305	120.369	112.3444
40	561.722	374.4813	224.6888	187.2407	160.492	149.7925
50	702.1525	468.1017	280.861	234.0508	200.615	187.2407
55	772.3678	514.9118	308.9471	257.4559	220.6765	205.9647

The torque and speed graphs are shown in Figure 72-73.

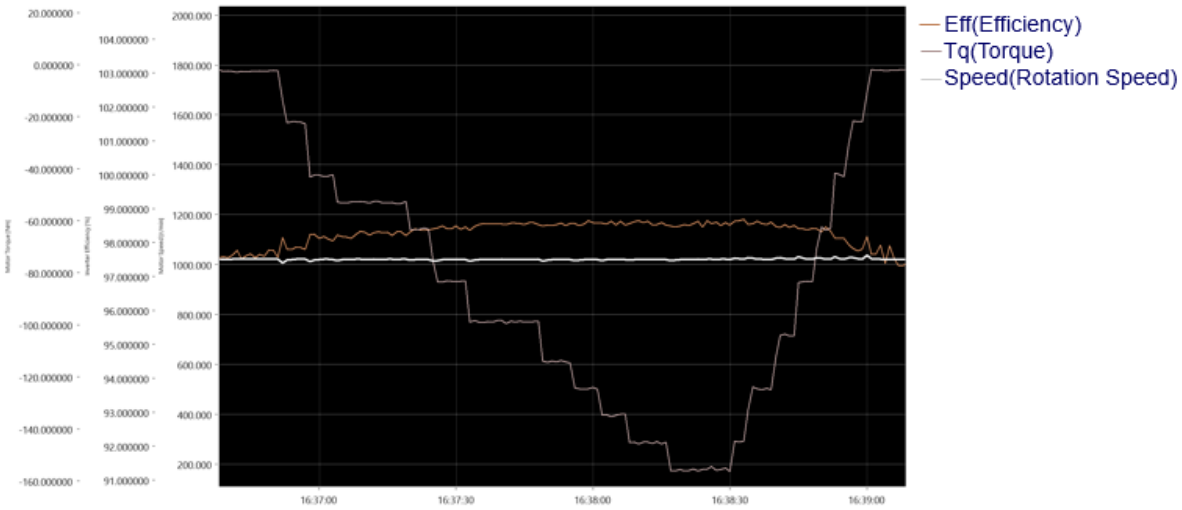

Figure 72. Torque Step commands at 1020 rpm

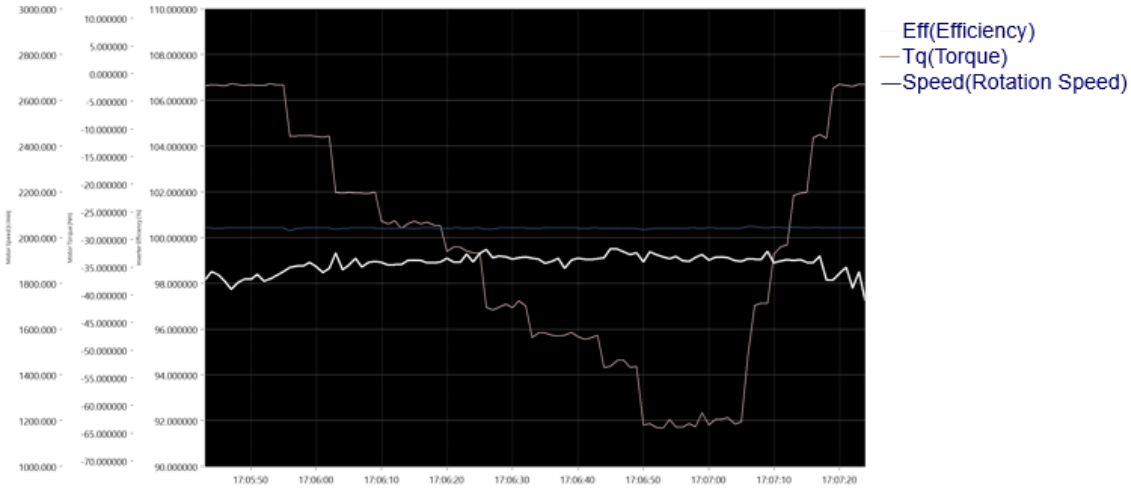

Figure 73. Torque Step commands at 2040 rpm

7.8 Warning and Fault testing

The specific goals of the warning and fault testing are to:

- Verify all warnings and faults thresholds are operating correctly.
- Demonstrate how the inverter and motor react when there is either a warning or fault.

The warning and fault testing gives you an important starting point to ensure a safe and successful operation. Figure 74 shows the CAN communication interface used for the testing. All values for the faults and warning are shown in at the end of this section. The faults/warning that will be tested are:

- E-stop
- XM3 temperature warnings/faults
- Motor overtemperature warning/faults
- Overcurrent warnings/faults
- Overvoltage warning/faults

Table 9 shows the inverter warnings threshold values and Table 10 shows the inverter fault threshold values.

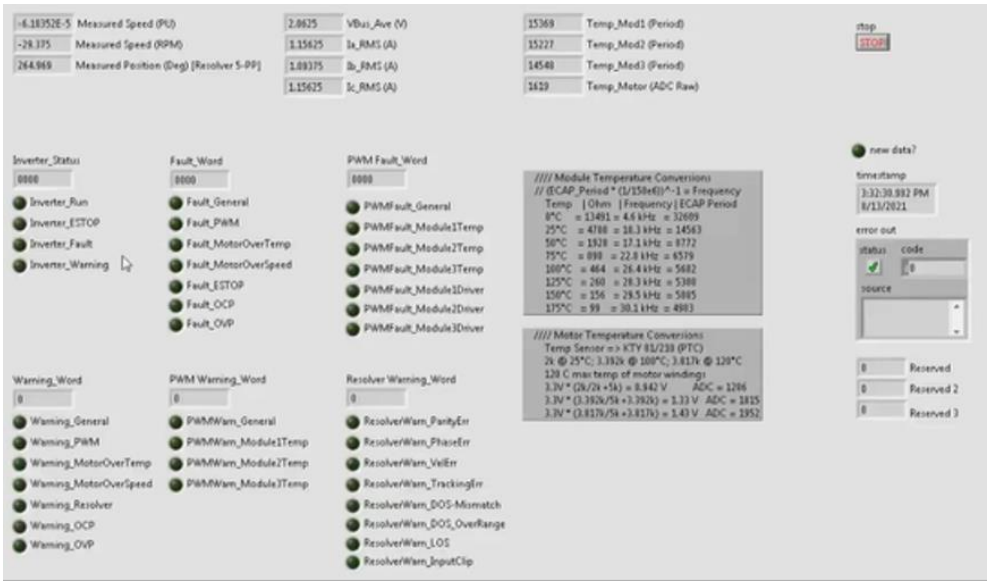

Figure 74. CAN communication interface

Table 9. Inverter threshold values (Warnings)

Warnings	Warning Level
PWM Driver Warning	5682 = 100 °C
DC Bus Over Voltage Warning	750 Vdc
Inverter Over Current Warning	250 Amps
Motor Temperature Warning	1815 = 100°C
Motor Over Speed Warning	2600 RPM

Table 10. Inverter threshold values (Fault)

Fault	Fault Level
WM Driver Fault	5300 = 125 °C
DC Bus Over Voltage Fault	820 Vdc
Inverter Over Current Fault	325 Amps
Motor Temperature Fault	1952 = 100°C
Motor Over Speed Fault	3000 RPM

7.9 References

[1] *Section 8.0 – Vibration test: DO-160*. DO160.org. (n.d.). Retrieved October 20, 2021, from https://do160.org/vibration/.

[2] *Section 7.0 – operational shocks and crash safety: DO-160*. DO160.org. (n.d.). Retrieved October 30, 2021, from https://do160.org/operational-shocks-and-crash-safety/.

[3] *Section 4.0 – temperature and altitude: DO-160*. DO160.org. (n.d.). Retrieved October 20, 2021, from https://do160.org/temperature-and-altitude/.

[4] *Section 5.0 – temperature variation: DO-160*. DO160.org. (n.d.). Retrieved November 1, 2021, from https://do160.org/temperature-variation/.

[5] *RTCA DO-160G for Airborne Equipment: DO-160*. DO160.org. (n.d.). Retrieved October 24, 2021, from https://do160.org/rtca-do-160g/.

CHAPTER 8

8.1 Conclusion

The University of Arkansas Power Electronics Research group met the object to design an inverter for a Cessna 337 Skymaster aircraft. This purpose of the inverter was to replace the engine that is located in the nose of the aircraft, converting the Cessna 337 to a hybrid electric aircraft. First the required specifications for the inverter were determined, either a 2-Level three phase inverter or a 3-Level three phase inverter. Based on the time frame of the project a contract manufactured 2-Level three phase inverter was designed. Next comparisons between different control methods for a PMSM was conducted. As a result of the study Field Oriented Control was chosen because it has a lot of advantages over both Scalar Control and Direct Torque Control such as efficiency and lower torque ripple. This is why Field Oriented Control was chosen for the scope of the thesis.

A custom controller board was designed for the contract manufactured 2-Level three phase inverter. After completion of the controller board, it was then integrated into the 2-Level three phase inverter. After integration in the inverter numerous Federal Aviation Administration (FAA)/DO-160G test procedures were conducted such as an Operational Shock and Crash Safety test, Robust Vibrational testing, and Temperature Variations testing. The purpose of the DO-160G test procedures is to determine the performance characteristics of the inverter in flight. After completion of the DO-160G test procedures the aerospace inverter was successfully delivered to Ampaire.

Best practices for PCB design

For an effective PCB design there are numerous tips that can improve the overall design. Component should be placed in a specific order, Connectors, Power circuits, Sensitive circuits, and all remaining components. If possible similar components should be orientated in the same

direction, this will reduce soldering errors. If Surface Mount Device components are used in the design, place these components on the same side of the board. The reason behind this is to eliminate the number of assembly steps and reduce the number of errors.

When routing power traces avoid creating daisy chains from component to component. Another important tip is to keep traces as short as possible. The rule is the faster the signal travels on the wire, the higher the priority and the shorter the trace length [1]. Whenever there are sensitive signals throughout the design ensure that these signals are shielded from noise sources. Implementation of Capacitor-Inductor-Capacitor (CLC) filters can be used to reduce the high frequency noise that can cause interference with sensitive components as well. Figure 84 shows the schematic diagram for a CLC filter. The first capacitor filters the majority of the ripple from the source, after this the LC filter attenuates the remaining noise.

8.2 References

[1] Baddeley, B. (2017, January 26). *PCB design guidelines to minimize RF transmissions*. Hackaday. Retrieved November 26, 2021, from https://hackaday.com/2017/01/26/pcb-design-guidelines-to-minimize-rf-transmissions/

Appendices

A. Layer by Layer Images

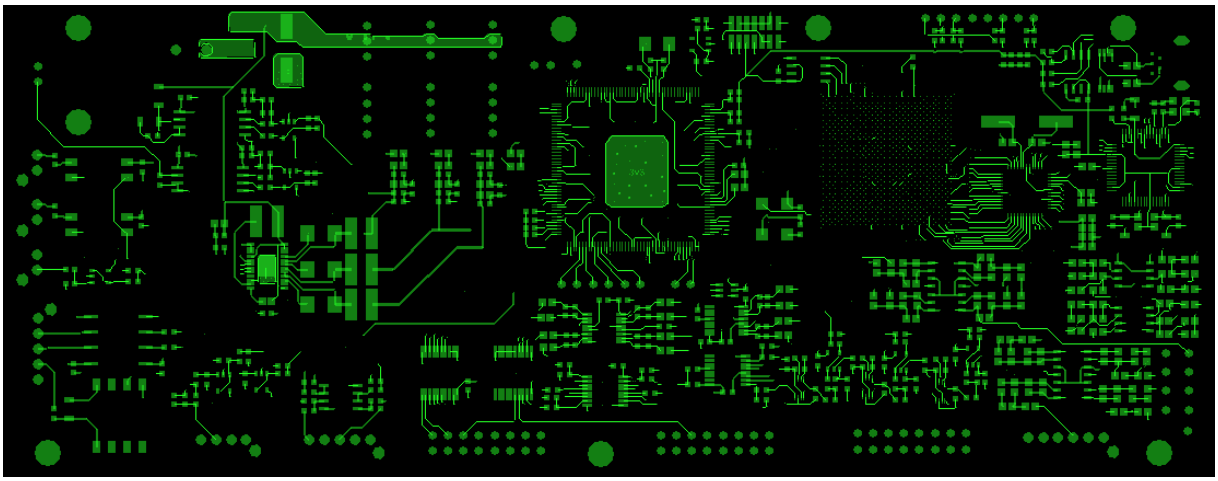

Figure 75. Layer 1 - Top Layer

Figure 76. Layer 2 – Ground Plane

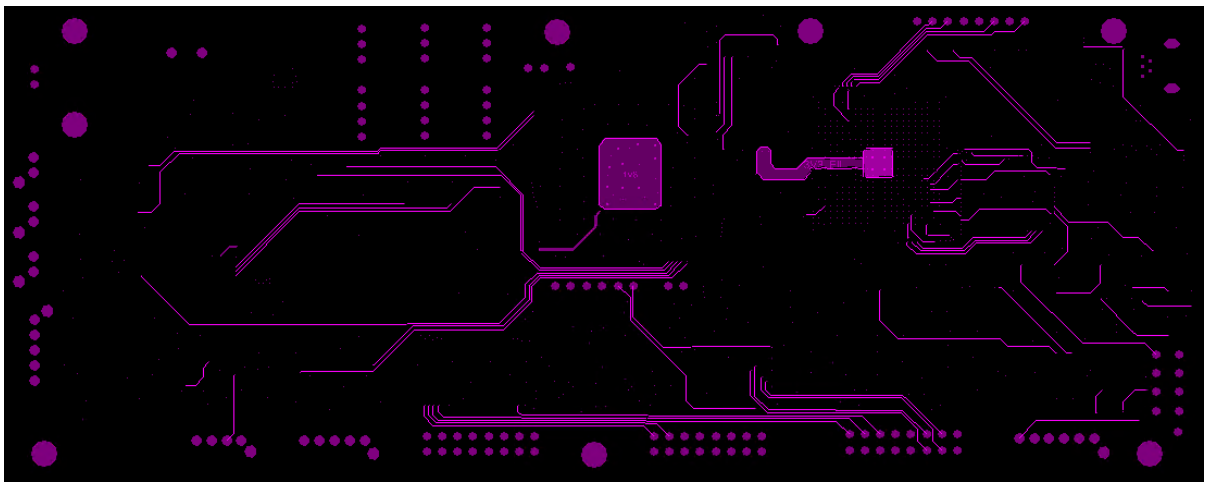

Figure 77. Layer 3 – Signal Layer

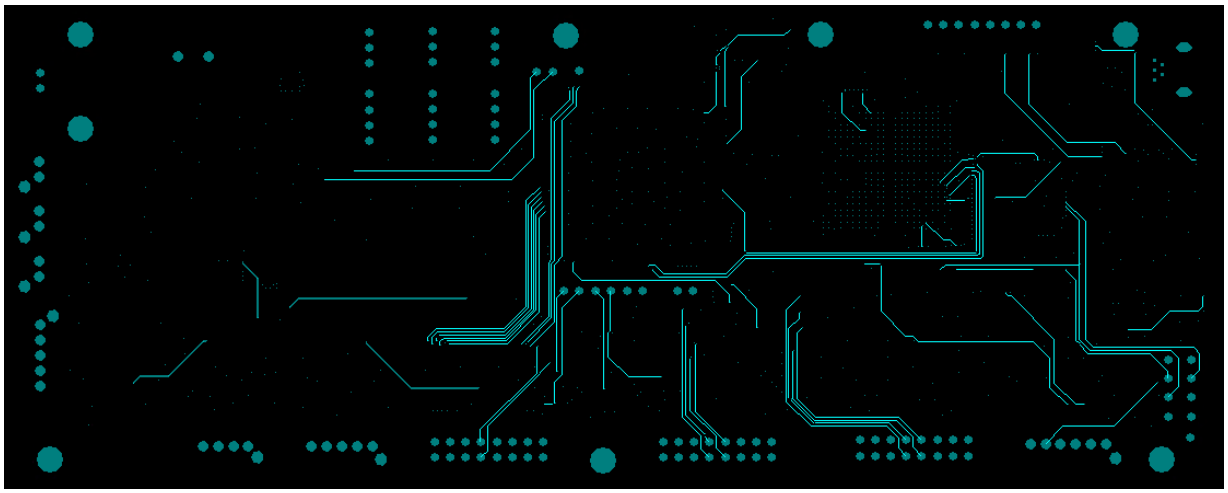

Figure 78. Layer 4 – Signal Layer

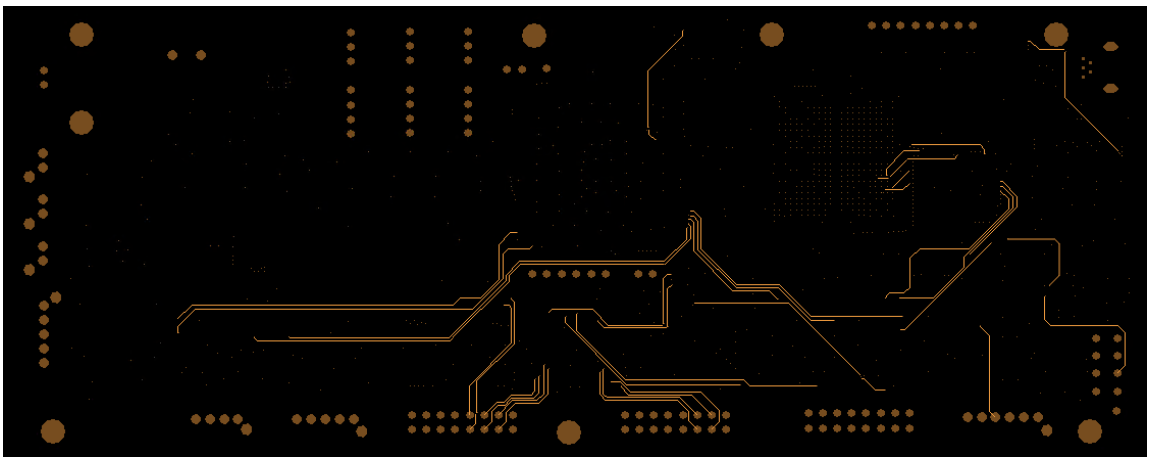

Figure 79. Layer 5 – Signal Layer

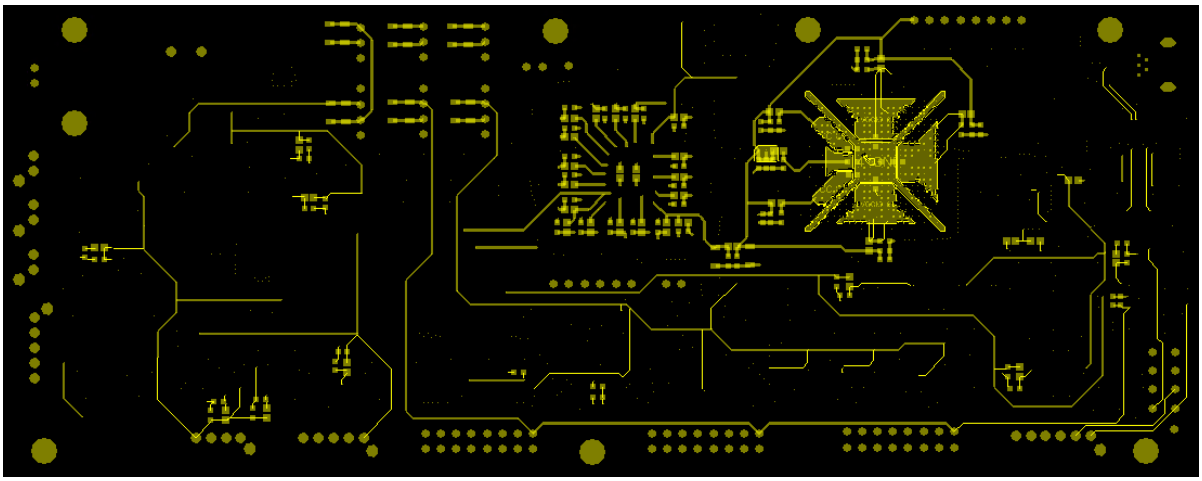

Figure 80. Layer 6- Ground Plane

Output Voltage Waveforms with different gate resistance

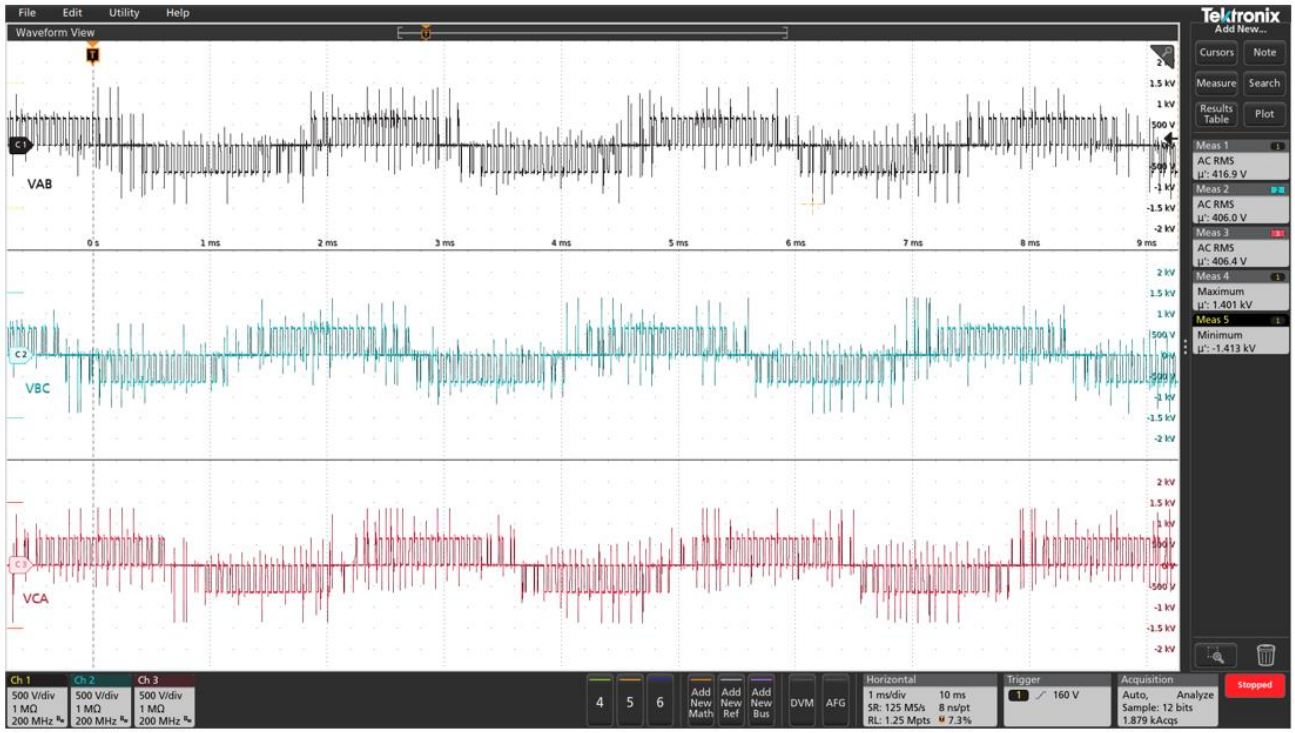

Figure 81. 650 Vdc Terminal Voltages 2040RPM Gate resistance 1.0 Ω

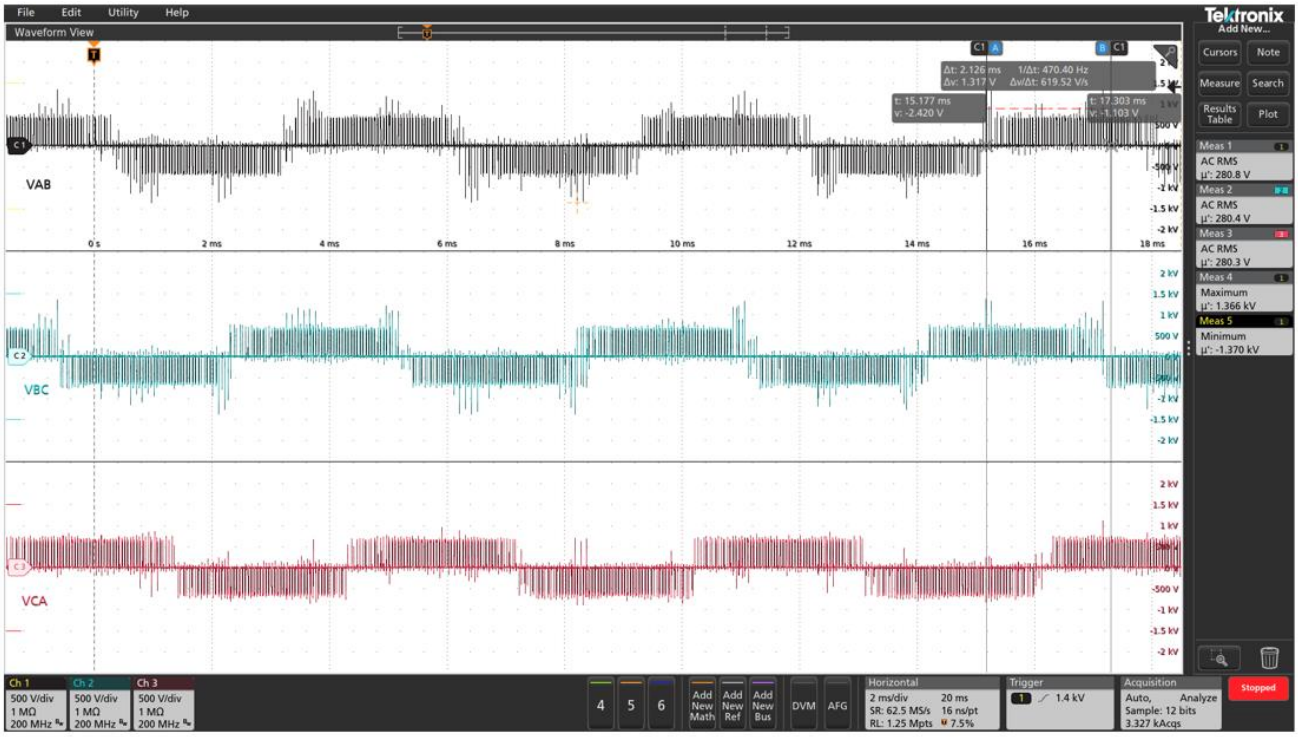

Figure 82. 650 Vdc Terminal Voltages 1020RPM Gate resistance 1.8 Ω

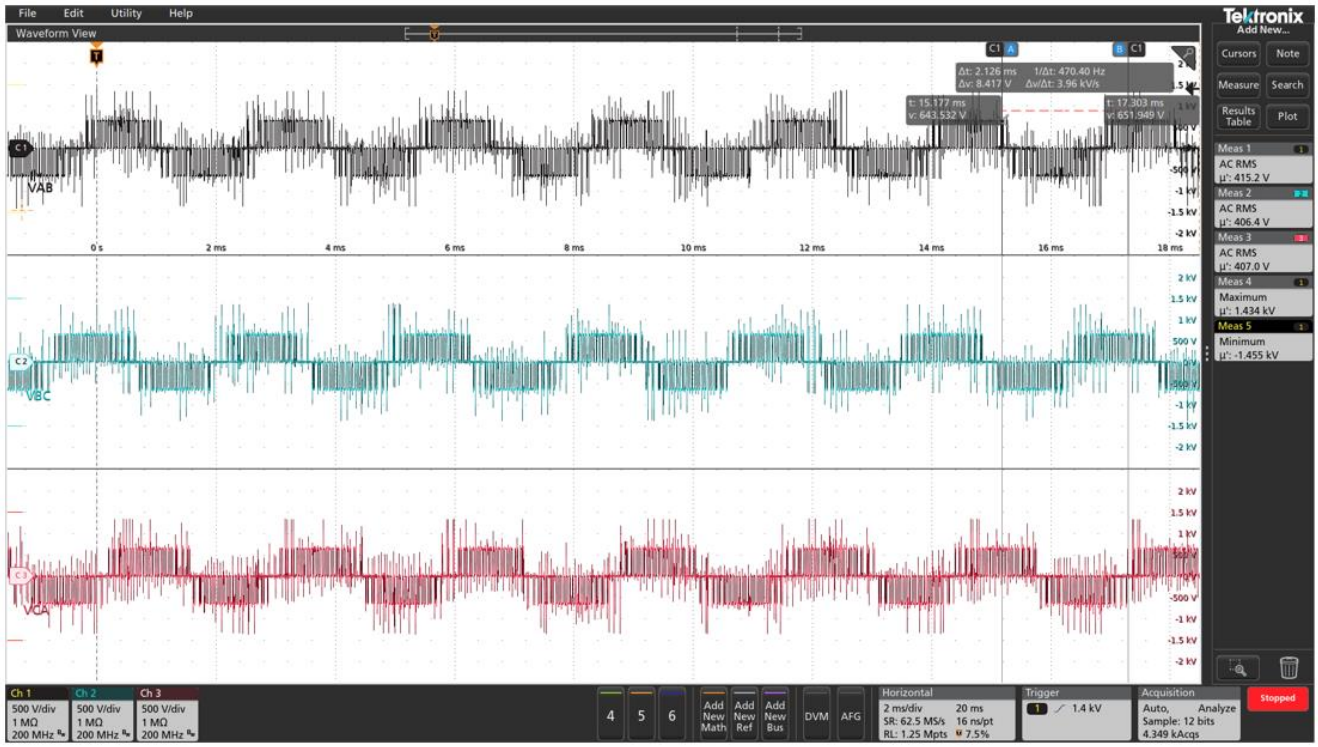

Figure 83. 650 Vdc Terminal Voltages 2040RPM Gate resistance 1.8 Ω

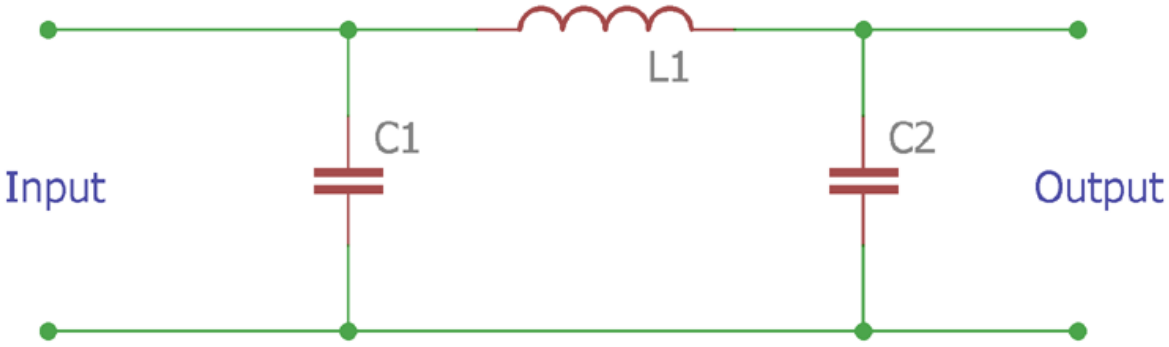

Figure 84. CLC Filter [1]