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High Power Density and High Efficiency Converter Topologies for Renewable Energy Conversion and EV Applications

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High Power Density and High Efficiency Converter Topologies for Renewable Energy Conversion and EV Applications

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ABSTRACT

This dissertation work presents two novel converter topologies (a three-level ANPC inverter utilizing hybrid Si/SiC switches and an Asymmetric Alternate Arm Converter (AAAC) topology) that are suitable for high efficiency and high-power density energy conversion systems. The operation principle, modulation, and control strategy of these newly introduced converter topologies are presented in detail supported by simulation and experimental results. A thorough design optimization of these converter topologies (Si/SiC current rating ratio optimization and gate control strategies for the three-level ANPC inverter topology and component sizing for the asymmetric alternate arm converter topology) are also presented.

Performance comparison of the proposed converter topologies with other similar converter topologies is also presented. The performance of the proposed ANPC inverter topology is compared with other ANPC inverter topologies such as an all SiC MOSFET ANPC inverter topology, an all Si IGBT ANPC inverter topology and mixed Si IGBT and SiC MOSFET based ANPC inverter topologies in terms of efficiency and cost. The efficiency and cost comparison results show that the proposed hybrid Si/SiC switch based ANPC inverter has higher efficiency and lower cost compared to the other ANPC inverter topologies considered for the comparison. The performance of the asymmetric alternate arm converter topology is also compared with other similar voltage source converter topologies such as the modular multilevel converter topology, the alternate arm converter topology, and the improved alternate arm converter topology in terms of total device count, number of switches per current conduction path, output voltage levels, dc-fault blocking capability and overmodulation capability. The proposed multilevel converter topology has lower total number of devices and lower number of devices per current conduction path hence it has lower cost and lower conduction power loss. However, it has lower number of output voltage

levels (requiring larger ac interface inductors) and lacks dc-fault blocking and overmodulation operation capabilities.

A converter figure-of-merit accounting for the hybrid Si/SiC switch and converter topology properties is also proposed to help perform quick performance comparison between different hybrid Si/SiC switch based converter topologies. It eliminates the need for developing full electro-thermal power loss model for different converter topologies that would otherwise be needed to carry out power loss comparison between different converter topologies. Hence it saves time and effort.

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First and foremost, I would like to express my sincere gratitude to my advisor, Prof. H. Alan Mantooth for his continued guidance, support, and mentorship during my PhD study and research. His tremendous research experience, broad knowledge, critical thinking, great leadership, and personality benefited me a lot to grow personally and academically. He is an inspiring role model that I look up to in my future career growth.

I am also very grateful to my other dissertation and advising committee members, Profs. Juan C. Balda, Yue Zhao, and David Huitink for their valuable suggestions and helpful discussion during my PhD study and research. I am also thankful to the NCREPT test engineers, Dr. Chris Farnell and Justin Jackson, for their technical support during testing at NCREPT. My appreciation also goes to all my colleagues with whom I have worked together on multiple projects and have had valuable discussion and collaboration with.

DEDICATION

This dissertation is dedicated to my parents and friends who helped me achieve this goal. My heartfelt gratitude goes to them for their continued support throughout my entire life.

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[1] D. Woldegiorgis, Y. Wu, Y. Wei and H. A. Mantooth, "A High Efficiency and Low Cost ANPC Inverter Using Hybrid Si/SiC Switches," in *IEEE Open Journal of Industry Applications*, vol. 2, pp. 154-167, 2021. (published). **(Chapter 2).**

[2] D. Woldegiorgis and H. A. Mantooth, "A Converter Figure-of-Merit Accounting for Hybrid Si/SiC Switches and Converter Topology Properties," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*. (under review). **(Chapter 3)**.

[3] D. Woldegiorgis and H. A. Mantooth, "A New Hybrid Voltage Source Converter with Reduced Active Switch Count for HVDC Applications," in *IEEE Transactions on Energy Conversion*, vol. 37, no. 1, pp. 612-622, March 2022. (published). **(Chapter 4).**

[4] D. Woldegiorgis and H. A. Mantooth, "Arm Energy Investigation and Submodule Capacitor Sizing for the Asymmetric Alternate Arm Converter Topology," in *IEEE Transaction on Power Electronics*. (under review). **(Chapter 5).**

CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Renewable Energy and Electric Vehicle (EV) Market Trends

With the increase in population and industrialization, the annual world energy consumption is also increasing constantly. Figure 1-1 shows the total world energy supply in EJ from 1971 to 2019 from conventional energy resources such as coal, oil, natural gas, nuclear, hydro and biofuels [1.1]. As can be seen from this figure, the world total energy supply from these energy resources is constantly increasing year to year and this trend is expected to continue in the years following 2019 [1.2]. Two factors attribute to this annual increase in world energy consumption: the increasing global industrialization and the increasing annual domestic electricity utilization. Prompted by the increase in world population, there has been a constant increase in industrial development around the world especially in developing countries to respond to the needs of the population [1.3], [1.4]. As a result, several new manufacturing, processing, and packaging industries have been built, and the capacity of some of the existing industries such as hotels, tourism, and leisure has been constantly growing over the last couple of decades. The second factor attributing to the annually increasing total energy demand is the annual increase in domestic energy

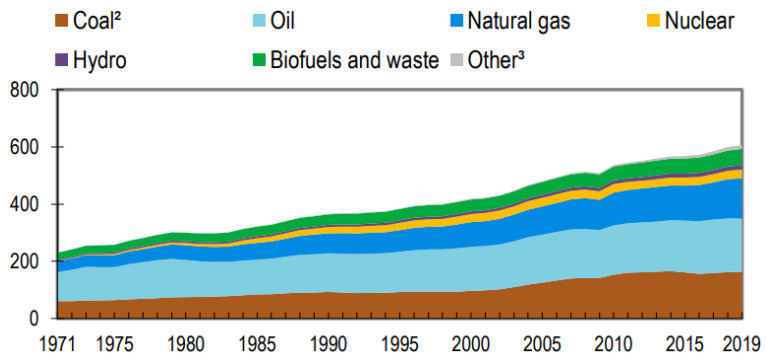

Figure 1-1 World total energy supply in EJ.

consumption [1.5]. The number and type of energy consuming home appliances such as refrigerators, entertainment, cooking, and cleaning appliances has been constantly increasing year to year especially in developed nations. Not only the number of these appliances is increasing, but also the amount of time they are being used is increasing. This is true especially after the change in lifestyle due to the COVID-19 pandemic [1.6].

The increasing energy consumption however has brought a significant challenge to the world. The annual CO_2 emission from industries and manufacturing plants into the atmospheric air is parallelly increasing as shown in Figure 1-2 [1.7]. This causes depletion of the ozone layer, which protects the earth from harmful ultraviolent radiations [1.8]. With the depleted ozone layer, the increased concentration of CO_2 and other greenhouse gases such as methane and Nitrous Oxide increases the absorption and emission of radiant energy from the environment causing an annual mean temperature increase to the world, a phenomenon called global warming. This phenomenon causes changing weather patterns such as extreme weather events, melting icebergs, and sea level rise. These changes affect the polar and marine ecosystems [1.9].

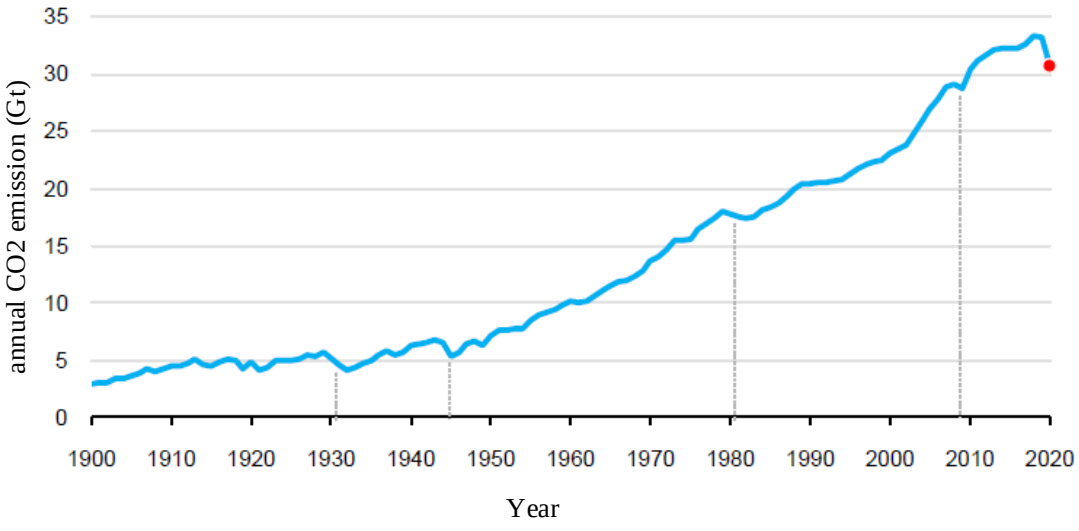

Figure 1-2 Global annual CO_2 emission.

To mitigate the harmful effect of CO_2 and other greenhouse gases, several actions have been taken by many stakeholders to reduce the emission of these harmful gases into the atmosphere. Following the Paris climate agreement in 2015, several nations pledged to reduce their CO_2 emission into the atmosphere by fostering the use of alternative clean and renewable energy resources such as Photovoltaic (PV), wind, geothermal, and hydropower through government incentives such as investment tax credits and lower tax rates [1.14], [1.15]. This brought forth a new era in the energy sector where renewable energy resources are increasingly being used.

Among the renewable energy resources, wind energy and Photovoltaic (PV) energy resources are the most widely harvested renewable energy resources in recent decades. Figure 1-3 for example shows the global cumulative wind energy installation from 2001 to 2016 [1.10]. As can be seen from the figure, the global annual installed wind energy capacity has been increasing exponentially and this trend has continued in the years following 2016 [1.11] – [1.13]. The high penetration of wind energy generation is primarily derived by several factors such as recent wind energy generation technology advancements, grid modernization, and government incentives [1.14] – [1.16]. The wind energy generation technology has been constantly advancing in the last couple of decades. The size of wind turbines and towers has been increasing year to year, new gearbox and coupling technologies have been introduced and improved generator technologies such as the doubly fed induction generator (DFIG) [1.17] have been developed allowing increased wind energy harvesting. The modernization of the grid such as the introduction of the distributed (non-centralized) grid concept allowing bidirectional power flows also promotes large scale deployment of wind energy generations [1.18], [1.19]. Government incentives through carbon credits and lower tax rates for renewable energy generations has also been one of the main drivers for the increased wind energy generation penetration worldwide [1.14], [1.15].

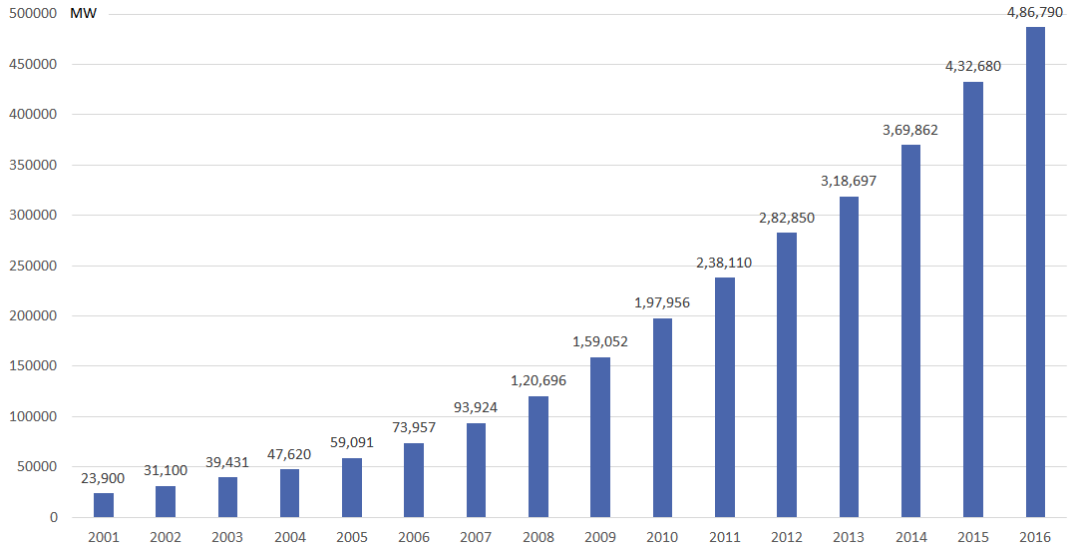

Figure 1-3 Global cumulative wind installation.

There has also been a rapid increase of Photovoltaic (PV) energy generation in the past couple of decades. As can be seen from Figure 1-4 [1.20], the world global annual installed solar energy capacity has been increasing exponentially, and this trend is expected to continue in the coming years [1.21]. In recent years, many countries especially China have bolstered their annual energy generation from solar energy to migrate from conventional energy resources into clean renewable energy resources to combat the detrimental effect of global warming. Despite its intermittent nature, the solar energy resource continues to be one of the most attractive renewable energy resources in the shift towards clean energy resources.

Several factors attribute to the rapid growth of solar energy generation in the last couple of decades. One of such factors is the continuous decline of the cost of solar panels. As can be seen from Figure 1-5 [1.22], the cost of solar panels is constantly dropping annually, and this trend is expected to continue in the coming years according to the US Solar Energy Technology Office

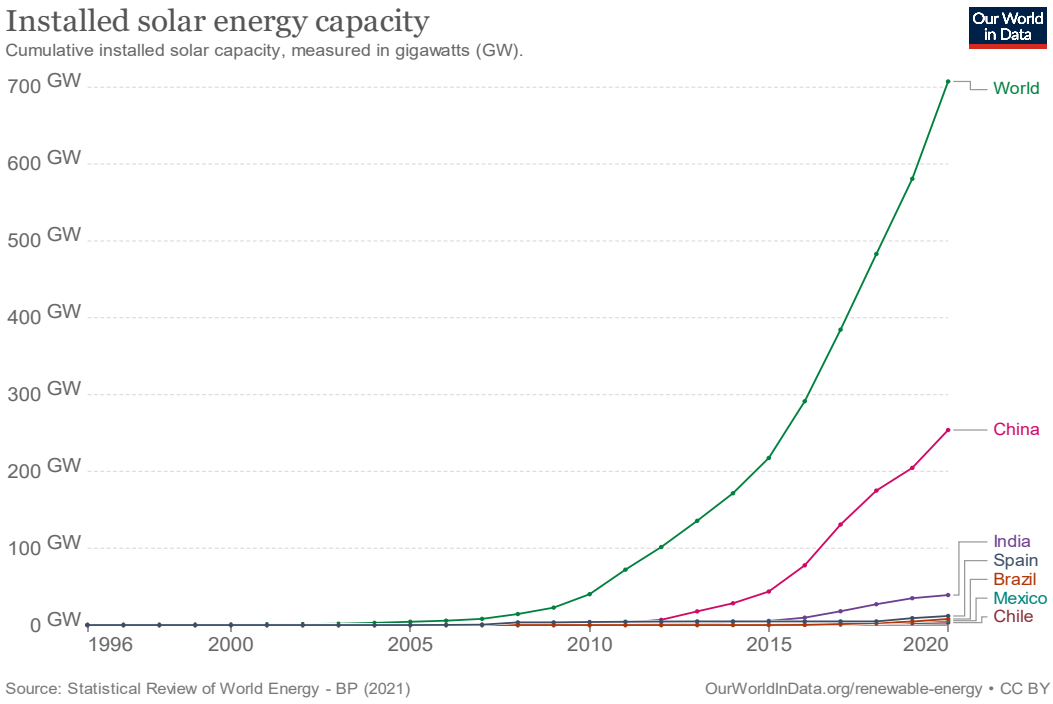

Figure 1-4 Global cumulative PV installation.

(SETO) 2020 Q1 Solar Photovoltaic System and Energy Storage Cost Benchmark [1.22]. The constant solar panel technology advancement and market competition between different manufacturers drives the solar panel cost reduction [1.23], [1.24].

Solar panel efficiency improvement is another factor promoting the increase of solar energy generation. In the last couple of decades, there has been a successful research and development effort that improved the energy conversion efficiency of solar panels. Figure 1-6 shows the achieved and expected solar panel efficiency improvement from 2010 to 2035 [1.25]. As can be seen from the figure, several new higher efficiency solar panel technologies are being introduced. New solar panel materials with lower losses (higher energy conversion efficiency) will continue to be introduced through government funded and industrial research and development programs.

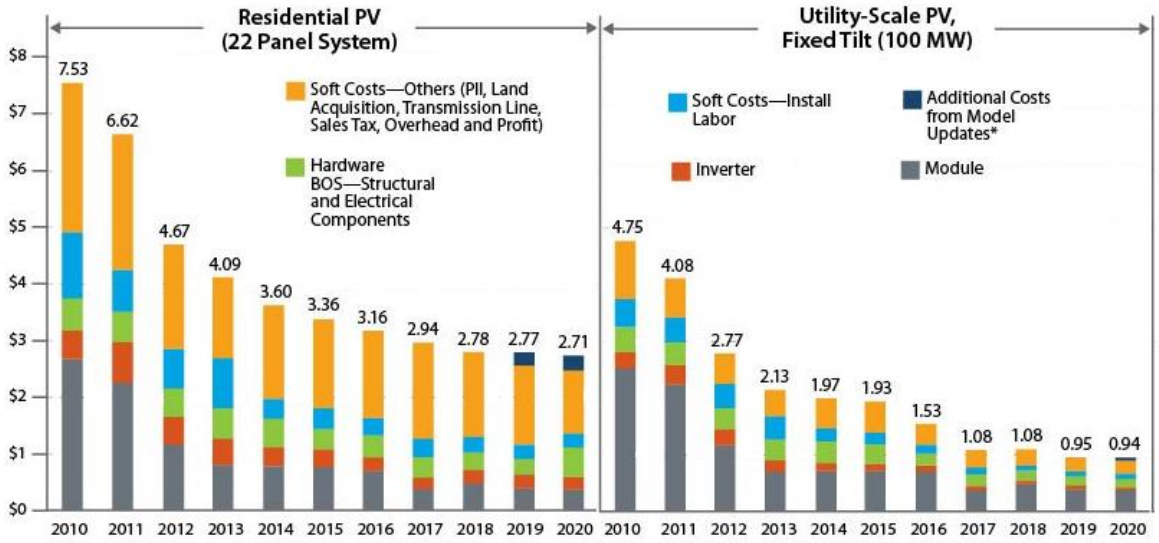

Figure 1-5 Annual PV system cost reduction.

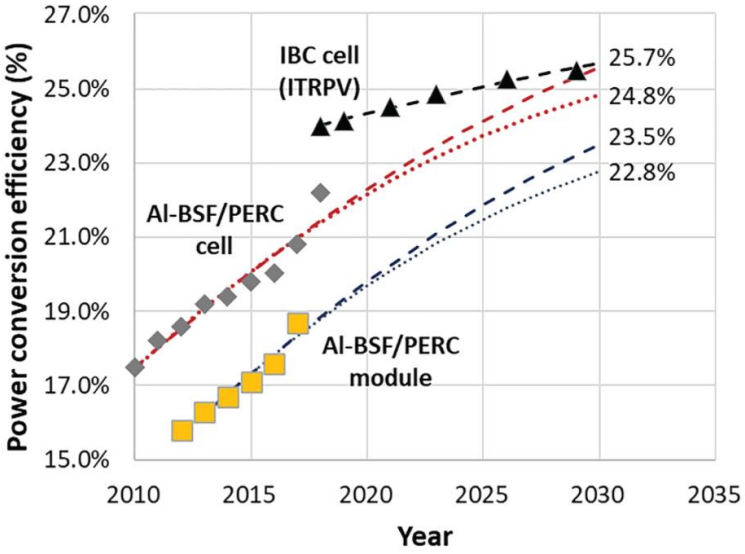

Figure 1-6 PV panel efficiency improvement.

The transportation sector is the next highest producer of greenhouse gases after coal power plants and industries. It produces about 25 percent of the annual greenhouse gases emitted into the atmosphere [1.26]. Therefore, like the energy sector, the transportation sector has also received attention in the last couple of decades in the effort to reduce greenhouse gas emission.

Promoted by government incentives such as investment tax credits, lower tax rates, and ample research and development funds, the last decade has seen increased electrification of the transportation sector starting from small passenger commuter cars to heavy-duty trucks and ships. Several research consortia such as the Center for Power Optimization of Electro-Thermal Systems (POETS), and research and development projects such as the More Electric Aircraft and Horizon 2020 have been established to accelerate the electrification of the transportation sector. As a result of this, automakers have already started cashing in a large amount of revenues annually.

Figure 1-7 shows the number of electric passenger-cars and light-duty vehicles sold annually in the last decade [1.27]. As can be seen from the figure, the number of small electric vehicles sold annually has increased exponentially starting from the birth of the business in 2010. China has the highest share of the market currently, but this is sure to change in the future as government regulation of the transportation sector starts to change in the other parts of the world especially in Europe and the USA.

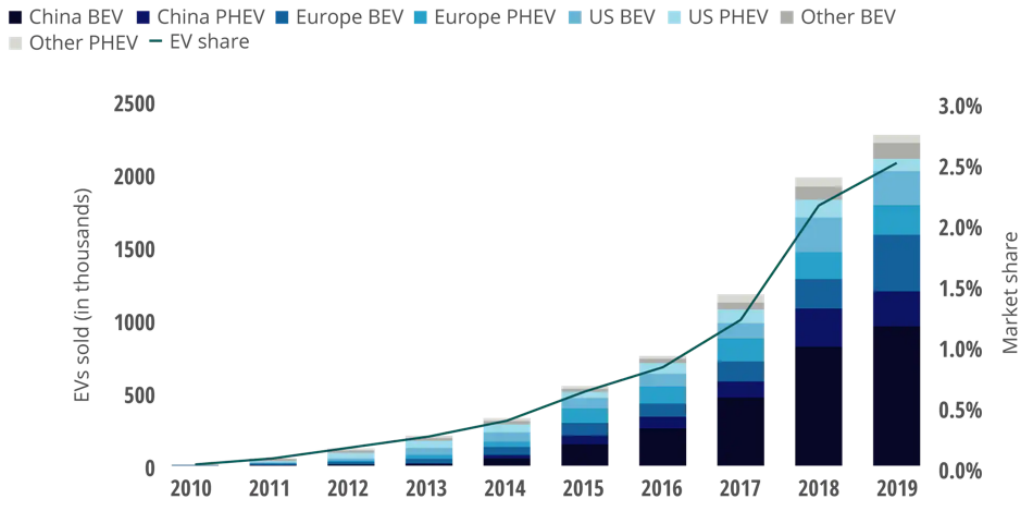

Figure 1-7 Annual passenger-car and light-duty vehicle sale.

Figure 1-8 shows the number of electric vehicles sold annually in the United States between 2010 and 2021, and the expected sale up to 2030 [1.28]. Like the rest of the world, the annual electric vehicles sale in the United States has also been increasing exponentially, and it is expected to maintain this trend in the coming years. The electric vehicle (EV) business started slowly in the US because of government reluctance to adopt policies and regulations favoring the EV market and scarcity of charging infrastructures. However, this has significantly changed in the second half of the last decade when states started to change their transportation and market regulations to favor EVs and more charging infrastructures are being built around the US.

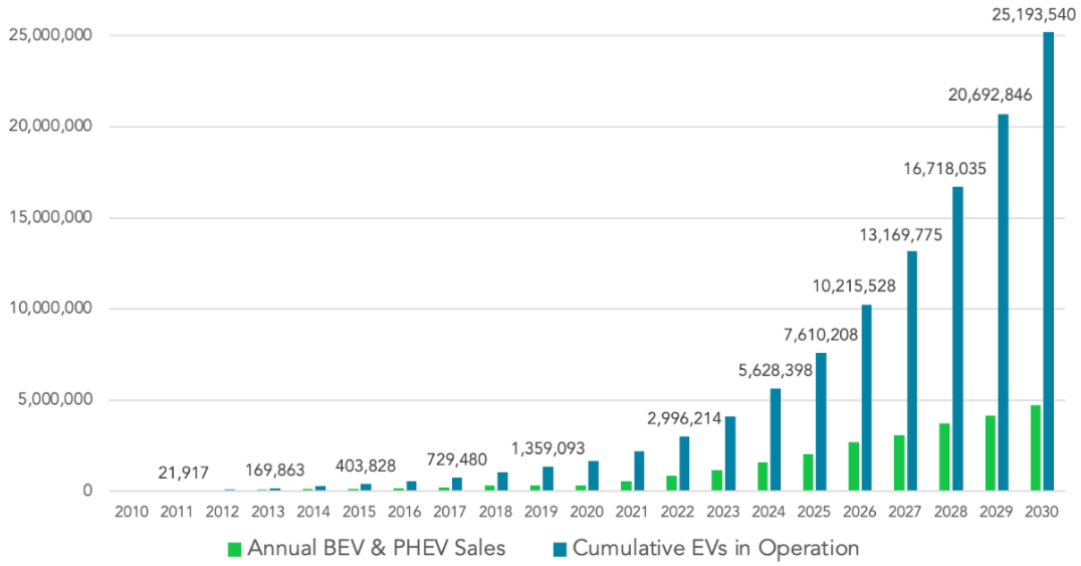

Figure 1-8 US actual and forecast EV sale.

1.2 Role of Power Electronics in Renewable Energy and EV Applications

Power electronics plays an integral role in renewable energy generation and electric vehicle applications. Because of their intermittent nature, renewable energy resources cannot be directly integrated into the electric grid. The daily and seasonal fluctuation in wind and solar energy resources causes fluctuation in the harvested energy from these renewable energy resources. This

energy fluctuation would cause voltage and frequency oscillation to the grid if directly integrated [1.29].

To mitigate this problem, renewable energy resources are usually integrated to the grid through power electronic converters as shown in Figure 1-9 to smooth out the power fluctuation injected into the grid from these energy resources [1.30]. Solar farms are connected to the grid via a front-end dc/dc converter which performs a Maximum Power Point Tracking (MPPT) functionality and a back-end dc/ac inverter which regulates the active and reactive power injected into the grid. Wind farms on the other hand are integrated to the grid through a front-end ac/dc rectifier which controls the pitch angle of the turbine blades to regulate the energy extracted from the wind and a back-end dc/ac inverter that regulates the active and reactive power injected into the grid.

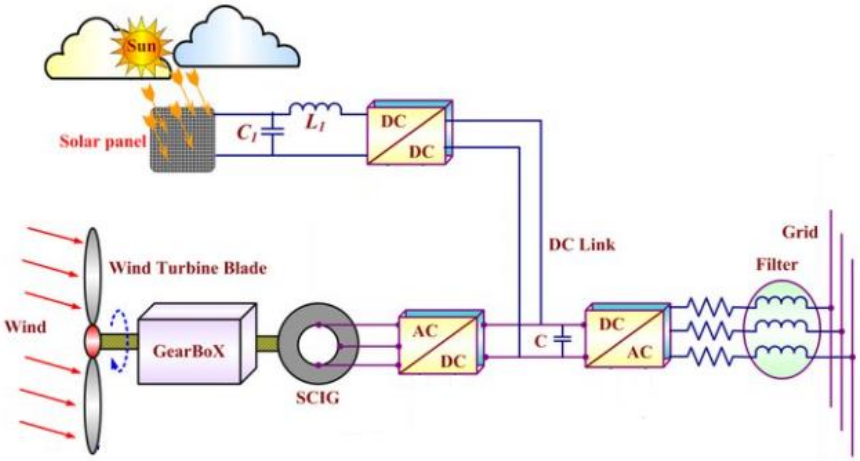

Figure 1-9 Integration of Wind and PV energy to the grid.

Power electronics is also an important component of an electric vehicle system. Figure 1-10 shows diagram of a passenger electric car system [1.31]. As can be seen from the diagram, an electric vehicle consists of several power electronic units such as the on-board charger, dc/dc converter and dc/ac inverter. The on-board charger regulates the charging profile of the battery

packs to ensure their safety and reliability. The dc/dc converter converts the dc voltage level of the battery packs into the different dc voltage levels required by the electric vehicle system. Three dc voltage levels may be present in a typical electric vehicle – a 12 V dc bus for the 12 V vehicle components, a 24 V dc bus for the 24 V vehicle components and an 800 V dc bus supplying the traction dc/ac inverter.

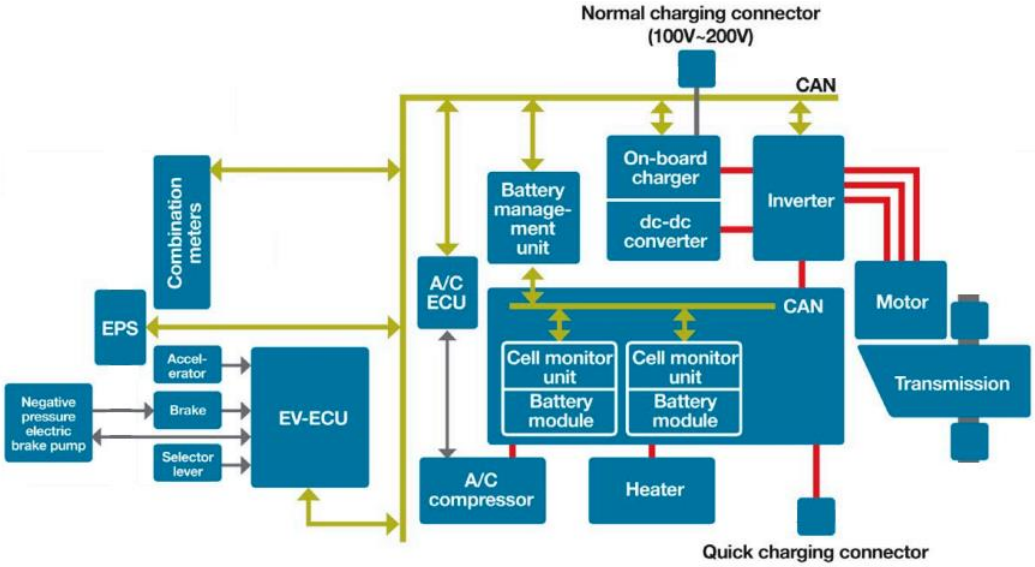

Figure 1-10 Diagram of typical electric vehicle system.

1.3 The Future Power Electronics Demand

The rapid penetration of renewable energy generation and the increasing electrification of the transportation sector in the last couple of decades, however, has brought a challenge to the design of energy conversion systems. Promoted by market competition and other system operational needs, the future power electronic systems need to be designed to offer high efficiency, high power density, high reliability, and lower cost.

1.3.1 High Efficiency and High-Power Density

Not only the penetration of renewable energy resources has been increasing in the last couple of decades but also the size of the generation plants has been continuously increasing. However, when the size of the energy generation plants increases, the power processing capability of the front-end power electronic converter needs to be increased as well. This presents a significant challenge to the design of the front-end converter. It needs to have high conversion efficiency to reduce the power losses in the converter. Otherwise, an advanced thermal management system needs to be employed to extract the heat generated by the semiconductor devices and other components in the converter. This increases the cost of the converter and reduces its power density.

Power density is another design challenge for future power electronic conversion systems, especially for applications where space is a premium such as offshore wind energy generation and electric vehicles. In these applications, the converter weight and volume are very significant. Even though significant progress has already been made in converter power density improvement as shown in Figure 1-11 [1.32], there is still a demand for further improvement especially for EV applications where the converter size and weight are critical design parameters.

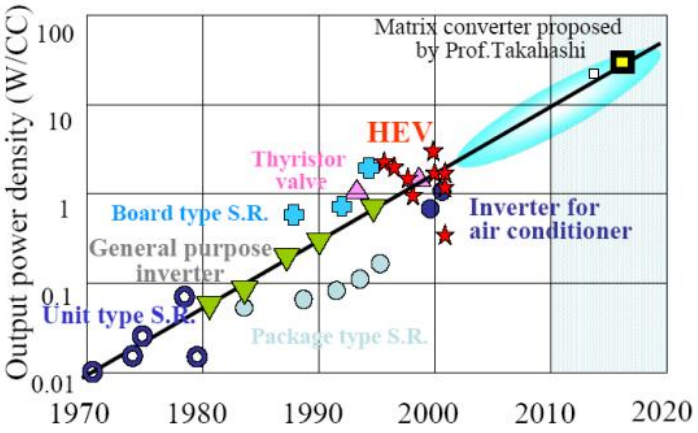

Figure 1-11 Converter power density improvement over time.

1.3.2 Low Cost

Another design need for the future power electronic conversion is cost reduction. This is primarily driven by market competition. In the early years of the last decade, government incentives through investment tax credits and lower tax rates were one of the main drivers of the rapid growth of the renewable energy and electric transportation markets [1.14], [1.15]. These incentives were primarily given to increase the awareness of customers on these market sectors and to help with their huge investment cost. However, as customers became more friendly with these new market sectors, the government incentives started to reduce and will likely be stopped entirely in the coming years [1.33]. Therefore, these market sectors need to be economically competitive with the conventional fuel-based energy and transportation sectors to keep their current market momentum. This requires cost reduction in renewable energy generation and electric vehicle systems.

Figure 1-12 shows the cost decline for small passenger electric vehicles with 200 miles battery capacity from 2014 to 2022 [1.34]. When passenger electric vehicles were initially introduced to market, they were quite expensive more so than the conventional Internal Combustion Engine (ICE) passenger vehicles, but their price has been dropping exponentially since then with the advancement in power converter technologies and the technology maturity. Currently, the price of an electric passenger car is almost equivalent to the price of a similarly sized ICE passenger car. However, more cost reduction is still expected for electric vehicles in the future. Unlike the ICE vehicle technology, the electric vehicle technology is not yet fully matured especially in the battery technology. There are still several research and development activities to improve the performance and reduce cost of EVs.

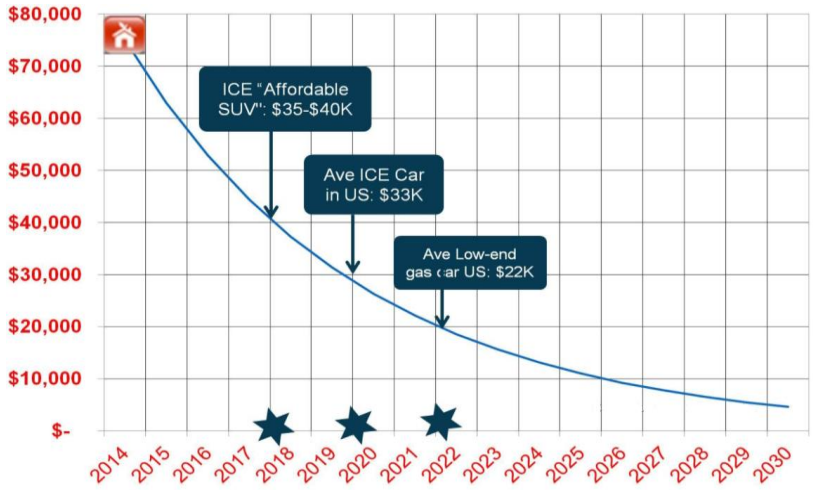

Figure 1-12 Cost decline for EVs with 200 miles battery capacity.

Figure 1-13 shows the cost decline in PV systems from 2010 to 2020 [1.22]. As can be seen from the figure, the Levelized Cost of Energy (LCOE) for PV systems has drastically reduced from 2010 to 2020. The introduction of new efficient solar panels and power converter topologies is the main drivers for this cost reduction. Despite the significant cost reduction that has already been recorded in PV systems, there is still a need for cost reduction to make this energy sector even more competitive. According to the US Solar Energy Technology Office (SETO) 2020 Q1 report [1.22], further cost decline of PV systems is still expected in 2030.

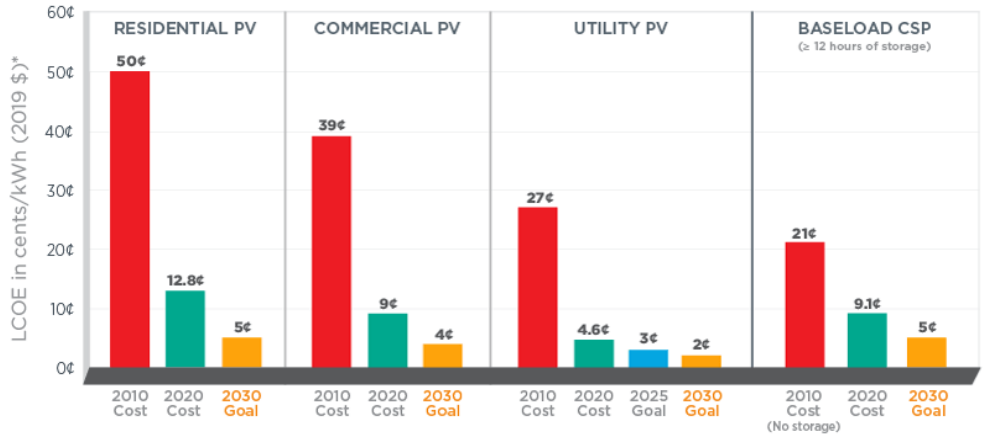

Figure 1-13 LCOE of PV systems: progress and goals.

1.4 Solutions for the Future Power Electronics Needs

1.4.1 Semiconductor Device Solutions

Silicon based semiconductor devices were the workhorse for power converters in many applications such as energy conversion, automotive, and industrial applications until the beginning of the 21st century. This semiconductor device technology is quite matured and converter design using these semiconductor devices is well established. Therefore, there is not much room for further performance improvement of power converters using silicon devices.

At the beginning of the 21st century, Wide Band Gap (WBG) semiconductor devices such as Silicon Carbide (SiC) MOSFETs and Gallium Nitride (GaN) devices have emerged as the next bricks for building power electronic converters. These semiconductor devices have superior performance indices compared to silicon devices as shown in Figure 1-14 [1.35]. They have a higher breakdown electric field offering lower on-state resistance, higher electron saturation velocity providing faster switching speed (higher switching frequency), higher bandgap energy allowing higher junction temperature operation capability, and higher thermal conductivity providing higher converter power density compared to silicon devices [1.36].

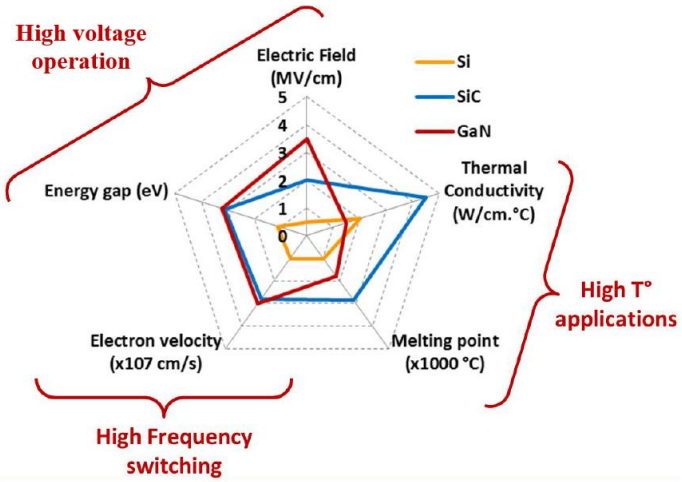

Figure 1-14 Physical properties of different semiconductor devices.

Because of their relative maturity compared to GaN devices, SiC devices are the primary pick for designing high efficiency and high power density power conversion systems. They provide significant switching loss reduction compared to silicon devices due to their higher switching speed and their very small reverse recovery loss (only due to the current needed to discharge their junction capacitor) [1.37]. Figure 1-15 for example shows the power loss comparison between Si IGBTs and SiC MOSFETs for a 2.5 kW dc/dc converter application [1.38]. For this application, SiC MOSFETs reduce the switching loss of the converter by about 73 percent. In addition, these devices can be operated at much higher switching frequency than silicon devices, hence the passive components can be designed much smaller than their silicon counterpart enabling compact and lower weight converter design for applications where space and weight is a premium such as aerospace applications. Moreover, combined with their excellent thermal conductivity, the reduced switching loss of SiC devices provides significant reduction in the thermal management of power converters employing SiC devices.

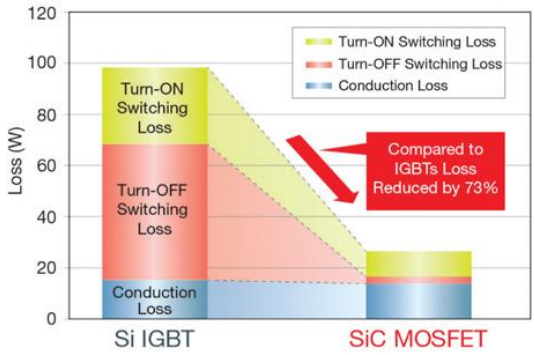

Figure 1-15 Power loss comparison between Si IGBT and SiC MOSFET.

The major drawback of SiC devices currently is their high cost. As shown in Figure 1-16, the investment cost of SiC devices for a power converter is almost seven times the cost of Si devices [1.39]. However, this is expected to change in the future with the advancement in SiC device

manufacturing technology and market competition between SiC device manufacturers. In addition, despite their high initial investment cost, SiC devices provide cost savings in the overall converter system due to the reduction in the cooling system requirement, passive components, and converter enclosure. They also provide indirect cost savings for consumers during operation. For Hybrid Electric Vehicles (HEV) and Electric Vehicle (EV), consumers will have savings from the fuel cost cutting and for renewable energy applications, higher conversion efficiency means higher annual energy yield so utility companies will see increased revenue when using SiC based power converters for renewable energy generation.

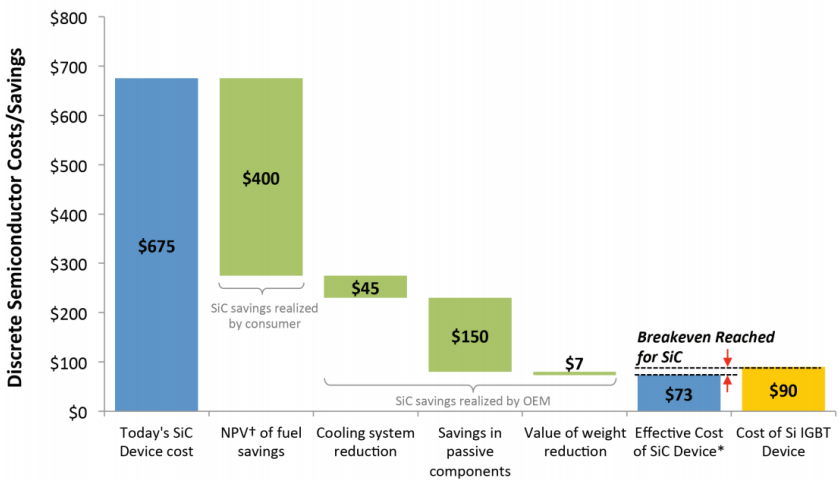

Figure 1-16 Si IGBT and SiC MOSFET cost comparison for EV application.

However, there are still several research and development activities to further improve the performance of wide band gap devices through new packaging and gate driver technologies as well as improvements in the voltage and current handling capabilities of the devices themselves especially for GaN devices. In addition, the performance benefits of new device configurations such as hybrid Si/SiC switches [1.40] – [1.42] also need to be well investigated and converter design methods suitable for these device configurations need to be developed.

1.4.2 Power Converter Topology Solutions

Another room for finding answer for the high efficiency and high-power density energy conversion system need is converter topology. Converter efficiency and power density depend on the converter topology structure and operation. The converter conduction power loss depends on the number of devices per current conduction path while its switching power loss depends on the converter blocking voltage requirement both of which in turn depend on the converter topology structure and operation [1.43], [1.44]. The converter power density on the other hand is dependent on the number, size, and weight of the components that the converter is made from [1.45]. These factors are also dependent on the converter topology structure and operation. The converter topology determines the total number of semiconductor devices and the size of its passive components (the size of the passive components depends on the effective switching frequency of the converter topology). Therefore, converter topology is critical for achieving the desired efficiency and power density target for energy conversion systems.

Figure 1-17 for example shows efficiency comparison of three converter topologies for a 10-kW motor derive application [1.46]. As can be seen from the figure, the Three-Level T-Type Converter ($3LT^2C$) has higher efficiency compared to the Three-Level Neutral-Point Clamp Converter ($3LNPC^2$) and the Two-Level Converter (2LC) for lower switching frequencies both for inverter and rectifier operation modes. For higher switching frequencies (> 35 kHz), the $3LNPC^2$ has higher efficiency compared to the other two converter topologies in both operation modes. On the other hand, the two-level converter (2LC) has the lowest efficiency compared to the other three-level converter topologies for both operation modes and wide switching frequency range. This shows conversion efficiency is dependent on the converter topology and its operating conditions such as switching frequency.

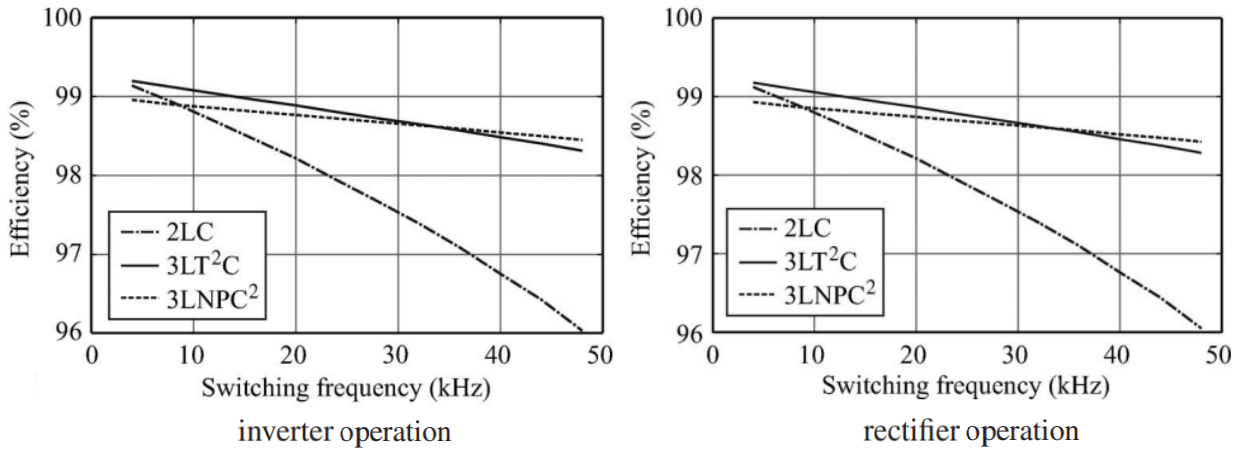

Figure 1-17 Efficiency comparison between different converter topologies.

The power density of a converter also depends on its topology structure as shown in Figure 1-18 [1.46]. The two-level converter (2LC) topology has the lowest total semiconductor chip area (higher power density) compared to the other two three-level converter topologies for low switching frequencies (< 20 kHz). For medium switching frequency values (between 20 kHz and 35 kHz), the three-level T-type converter offers the highest power density compared to the other two converter topologies and, for high switching frequency (> 35 kHz), the three-level NPC converter offers the highest power density compared to the other two converter topologies.

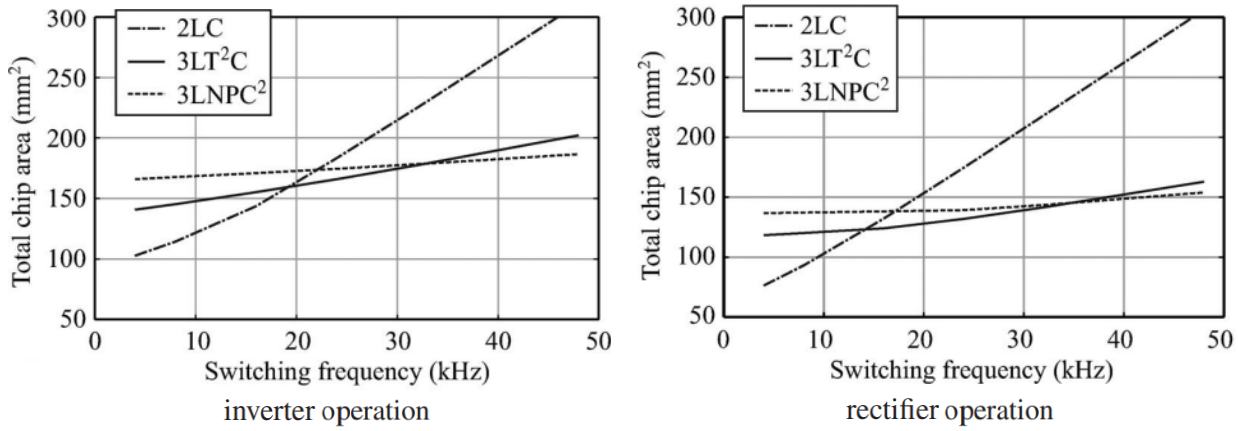

Figure 1-18 Total semiconductor chip area comparison for different converter topologies.

1.4.3 Passive Component Solutions

1.4.3.1 *Dc-link Capacitor Choice*

Different dc-link capacitor technologies have different physical and functional characteristics that play a great role in converter efficiency and power density. Figure 1-19 shows a comparison of three different dc-link capacitor technologies [1.47]. Ceramic capacitors are usually available in low capacitance and voltage rating, but they offer great energy density and very low Equivalent Series Resistance (ESR) compared to the other capacitor technologies [1.48]. Therefore, they are good choice to maximize converter efficiency and power density especially if they are used in conjunction with WBG devices.

Film capacitors on the other hand are available in relatively higher capacitance and voltage rating than ceramic capacitors. They also offer low ESR, and high energy density compared Aluminum Electrolytic capacitors [1.49]. Aluminum Electrolytic capacitors are probably the most matured capacitor technology. They are available in higher capacitance compared to the other two capacitor technologies. They also have good energy density. However, they have relatively higher ESR than Film and Ceramic capacitors especially at higher switching frequencies.

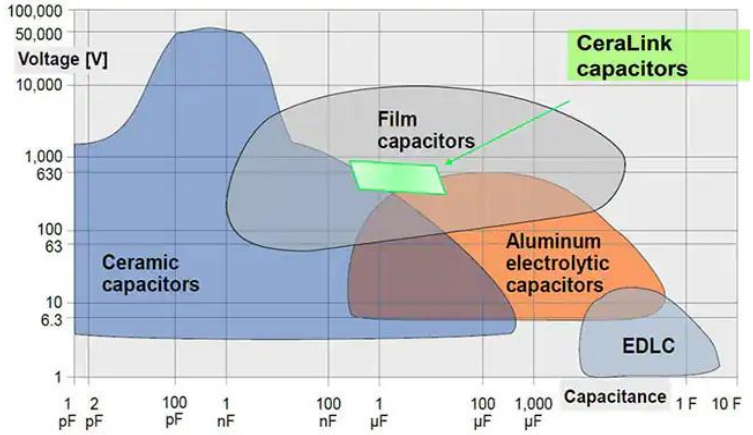

Figure 1-19 Dc-link capacitor technology comparison.

1.4.3.2 *Inductor Choice*

The choice of inductor also affects the efficiency and power density of a converter. Depending on the type of inductors used, different converter efficiency and power density can be achieved. The Quality factor (Q) of an inductor is a good indicator of the power loss of the inductor – a higher Q value indicates lower power loss and better high frequency stability [1.50], [1.51]. Figure 1-20 for example shows the Q-factor of three types of inductors [1.52]. As can be seen from the figure, winding inductors have higher Q-factor values especially at higher switching frequency hence they have lower power loss while thin film inductors have lower Q-factor or higher power loss compared to winding inductor and multilayer inductor technologies. The inductor core size is also important design parameter since it affects the power density of the converter.

However, inductors are primarily selected based on their functionality such as ripple current filtering or EMI suppression. The power loss and power density of the inductor comes next to these parameters and hence it very difficult to get a good tradeoff between their primary functionality, and converter efficiency and power density.

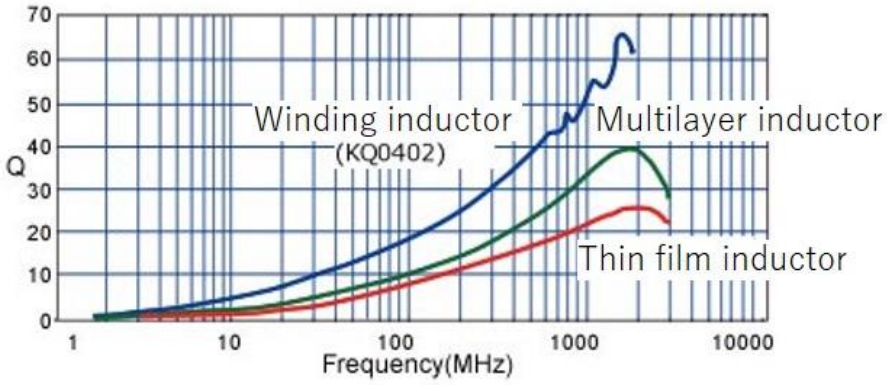

Figure 1-20 Comparison of different inductor technologies.

1.4.4 New Design Approaches

Another way forward for the future power electronics high efficiency and high-power density needs is a paradigm shift in converter design approach. Traditionally, the different converter design aspects such as the electrical design parameters, mechanical design parameters, and thermal design parameters are dealt separately and sequentially despite that these parameters are interrelated. This approach results in unoptimized converter performance in terms of the electrical, mechanical, and thermal aspects.

Recently, a new converter design approach has been introduced where the converter design space is expanded to include all the electrical, mechanical, and thermal aspects of the converter. Such design approach is called co-design or co-engineering [1.53], [1.54]. A co-design approach moves away from the conventional sequential design approach where the electrical design parameters, thermal design parameters, and mechanical design parameters are considered separately and replaces it with an approach where these design parameters are all simultaneously considered during the initial design. This design approach offers an optimized design in terms of the electrical, mechanical, and thermal performance of the converter.

However, the accuracy of this design approach depends on the design rules which defines the relationship between the electrical, thermal, and mechanical parameters of the converter [1.55]. Developing such design rule is not straightforward and it is a subject of the current research. But, with the ongoing research effort, simplified converter electrical, thermal, and mechanical models will surely be developed, and this design approach will soon be helpful.

1.5 Dissertation Objectives and Organization

Despite several converter topologies that have already been proposed to improve efficiency and power density of power converters, there is still much room for further improvement in terms of the tradeoff between efficiency, power density, and cost. Much effort is still expected to find a new converter topology with lower device count, lower power loss, and higher effective switching frequency to facilitate the tradeoff between efficiency, power density, and cost. This dissertation presents two novel high efficiency and high-power density converter topologies for renewable energy generation and EV applications. The first converter topology is a three-level ANPC inverter employing hybrid Si/SiC switches [1.56] and the second converter topology is a modified alternate arm converter topology termed as the Asymmetric Alternate Arm Converter (AAAC) topology [1.57]. The operation principle, control strategy and novel features of these converter topologies are discussed in detail and validated by both simulation and experimental results.

This dissertation is organized as follows. Chapter 2 presents the three-level ANPC inverter employing hybrid Si/SiC switches. The novel features of this topology, its operation and control strategy, and the converter design optimization in terms of the Si/SiC gate control and current rating ratio optimization are discussed in detail. Simulation and experimental results validating the operation and control strategies of the converter are also presented.

Chapter 3 introduces an improved converter Figure of Merit for hybrid Si/SiC switches combining the high-level semiconductor device properties such as on-state resistance and input/output capacitances and converter topology properties such blocking voltage and switching frequency. The detailed derivation of the proposed converter figure of merit is shown, and its accuracy is validated by experimental power loss and efficiency data using the hybrid Si/SiC switch ANPC inverter presented in Chapter 2.

Chapter 4 introduces a new hybrid voltage source converter topology termed as the Asymmetric Alternate Arm Converter (AAAC) that resembles the modular multilevel converter and the alternate arm converter topologies both in structure and operation. The structure, operation principle, control strategy, novel features, and design optimizations of this new converter topology are discussed in detail. Simulation and experimental results verifying the operation and control strategy of the proposed converter topology are also presented.

Chapter 5 presents the investigation of the converter arm energy for the topology presented in chapter 4 with aim of driving an expression of the maximum arm energy deviation of this converter topology that is needed to determine the minimum submodule capacitance of this converter topology. Validation of the derived maximum arm energy deviation equation with simulation and experimental results is also shown. In addition, arm energy deviation and the submodule capacitance requirement comparison between the proposed converter topology in Chapter 4 and other similar converter topologies is also given.

Chapter 6 presents conclusion to the work described in this dissertation and highlights the main future works for the topics discussed in the dissertation.

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CHAPTER 2

THE THREE-LEVEL ANPC INVERTER EMPLOYING HYBRID SI/SIC SWITCHES

2.1 Introduction to Three-level Inverter Topologies

Three-level inverter topologies have recently gained increased attention for high power energy conversion applications due to their benefits compared to two-level inverter topologies. Typical benefits of three-level inverter topologies over two-level inverter topologies are lower harmonic content in the output current waveform (requiring smaller filter components), reduced switching power loss, and reduced electromagnetic interference [2.1], [2.2]. The three-level T-type inverter topology shown in Figure 2-1 (a) is especially preferred for lower voltage applications because of its higher power conversion efficiency compared to other three-level inverter topologies, especially for low switching frequencies [2.3]. However, this topology is less economically attractive for high voltage applications since it requires higher blocking voltage rated semiconductor devices [2.4]. In addition, the T-type inverter topology suffers from imbalanced power loss distribution among the semiconductor devices due to the unequal voltage stress on the semiconductor devices [2.5]. The clamping leg devices (S_2 and S_3) have lower voltage stress hence lower switching power loss than the main leg devices (S_1 and S_4).

For high power applications, the three-level neutral point clamped (NPC) inverter topology shown in Figure 2-1 (b) is especially attractive due to its capability to handle higher voltage levels with lower voltage rated semiconductor devices [2.6], [2.7]. In this inverter topology, the semiconductor devices need to be rated for half of the input dc bus voltage. However, like the T-type inverter topology, it suffers from imbalanced loss distribution among its semiconductor devices [2.8], [2.9]. Depending on the load power factor, two kinds of switching loops exist in this inverter topology that results in imbalanced loss distribution among the semiconductor devices

[2.10]. When the load voltage and load current have the same polarity (rectifier operating mode), short commutation loops involving two switching devices exist. On the other hand, when the load voltage and load current have opposite polarity (inverter operating mode), long commutation loops involving four switching devices exist. These commutation loops result in different stray inductances hence different voltage stress and switching energy loss for the semiconductor devices.

Conversely, the Active Neutral Point Clamped (ANPC) inverter topology shown in Figure 2-1 (c) eliminates the problem of imbalanced semiconductor loss distribution among the semiconductor devices. This topology has two redundant neutral current paths that can be flexibly configured to balance the semiconductor device power losses irrespective of the load power factor [2.11] – [2.13]. The power loss of the semiconductor devices in ANPC inverter only depends on the modulation strategy unlike the NPC inverter which depends on the load power factor. In addition, like the three-level neutral-point clamped inverter topology, it requires low voltage rated semiconductors devices for high voltage applications. Therefore, it is a very attractive solution for high power energy conversion applications.

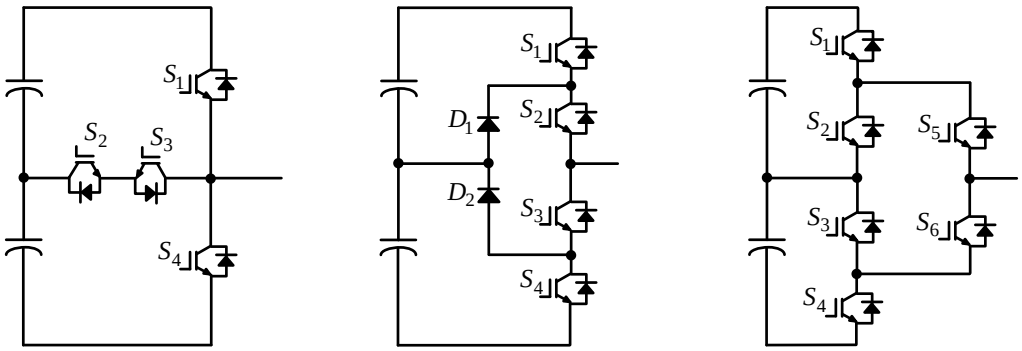

Figure 2-1 Three level voltage source inverter topologies: (a) T-type inverter, (b) Neutral Point Clamp (NPC) inverter, (c) Active Neutral Point Clamp (ANPC) inverter.

2.2 ANPC Inverter Modulation Strategies

Three-level ANPC inverter topology has four switching states: positive state (P), negative state (N) and two redundant neutral (O) states. The redundant neutral switching states increase the modulation freedom for this inverter topology since they can be flexibly configured to achieve different control objectives. Using this modulation flexibility, two major types of modulation strategies have been developed for ANPC inverter to optimize its switching performance and semiconductor device power losses. These modulation strategies differ from each other based on the neutral current path they are using during the positive and negative half cycle of the output voltage. However, these two neutral current paths result in different stress and loss for the semiconductor devices due to the difference in their switching loop stray inductances.

The first modulation type (modulation type I) [2.14], [2.15] uses the top neutral current path (S_2 and S_5) during the positive half cycle of the output voltage and the bottom neutral current path (S_3 and S_6) during the negative half cycle of the output voltage as shown in Figure 2-2. The switching states and corresponding gate signals for this modulation strategy are shown in Table 2-1 and Figure 2-3, respectively. The O^+ and O^- states in the switching table represent the O states during the positive and negative half cycle of the output voltage respectively. In this modulation strategy, the switches (S_1 - S_4) commutate at carrier frequency while the switches (S_5 - S_6) commutate at

Table 2-1 Switching table for modulation type I.

State	Output	S_1	S_2	S_3	S_4	S_5	S_6
P	$0.5V_{dc}$	1	0	0	0	1	0
O^+	0	0	1	0	0	1	0
O^-	0	0	0	1	0	0	1
N	$-0.5V_{dc}$	0	0	0	1	0	1

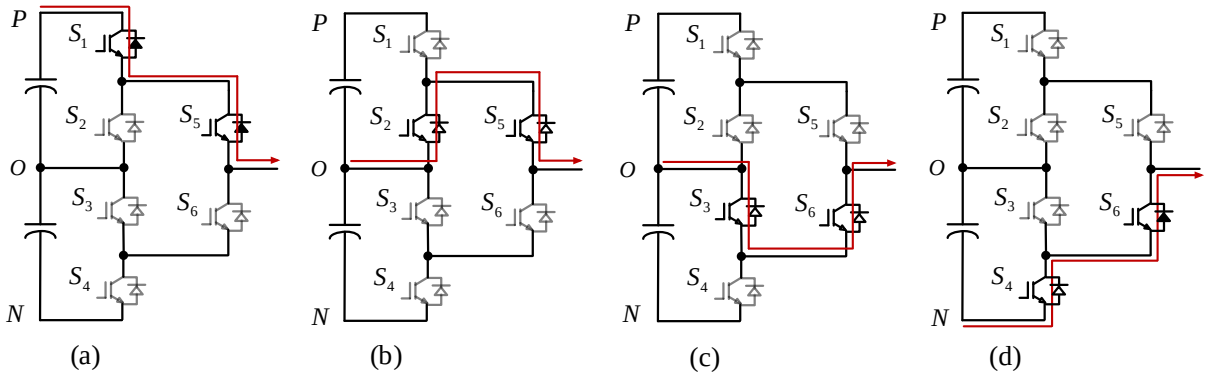

Figure 2-2 Switching diagram for modulation type I: (a) P state, (b) O+ state, (c) O- state, and (d) N state.

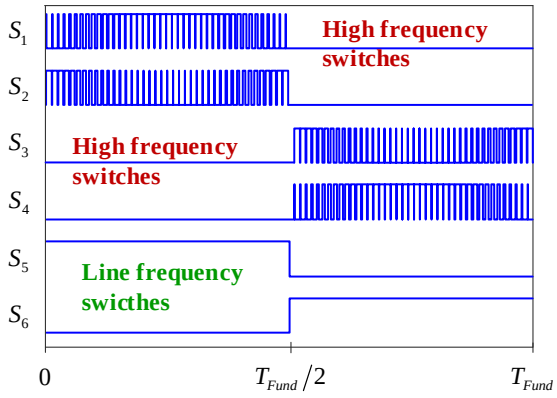

Figure 2-3 Gate signals for modulation type I.

fundamental line frequency. Therefore, it only involves short commutation loops consisting of two switching devices in all four operation quadrants resulting in lower voltage stress and switching power loss for the semiconductor devices.

The second modulation type (modulation type II) [2.16] – [2.18] uses the lower neutral current path (S_3 and S_6) during the positive half cycle of the output voltage and the upper neutral current path (S_2 and S_5) during the negative half cycle of the output voltage as shown in Figure 2-4. The switching states and corresponding gate signals for this modulation strategy are shown in Table 2-2 and Figure 2-5, respectively. In this modulation strategy, the switches (S_1 - S_4) are commutating

at fundamental line frequency while the switches (S_5 - S_6) are commutating at carrier frequency, hence it reduces the number of high frequency switches by half compared to the first modulation type. However, it results in long commutation loops consisting of four switching devices in all operation quadrants. Hence, it increases the parasitic inductance of the switching loops which in turn increases the voltage overshoot and switching energy loss of the semiconductor devices during switching. Therefore, the choice modulation strategy for the ANPC inverter depends on the design target (the tradeoff between cost, efficiency, and semiconductor device voltage stress) – one modulation strategy might be beneficial over the other for different applications.

Table 2-2 Switching table for modulation type II.

State	Output	S_1	S_2	S_3	S_4	S_5	S_6
P	$0.5V_{dc}$	1	0	1	0	1	0
O^+	0	1	0	1	0	0	1
O^-	0	0	1	0	1	1	0
N	$-0.5V_{dc}$	0	1	0	1	0	1

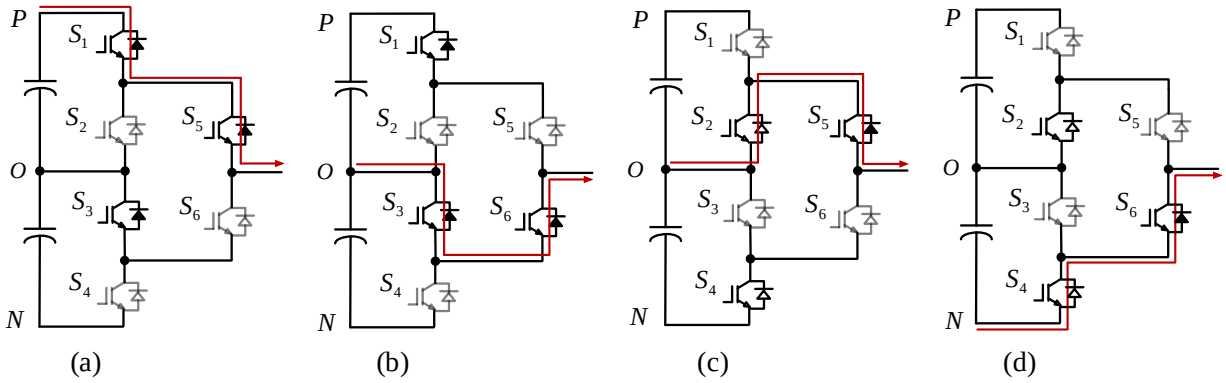

Figure 2-4 Switching diagram for modulation type II: (a) P state, (b) O^+ state, (c) O^- state, and (d) N state.

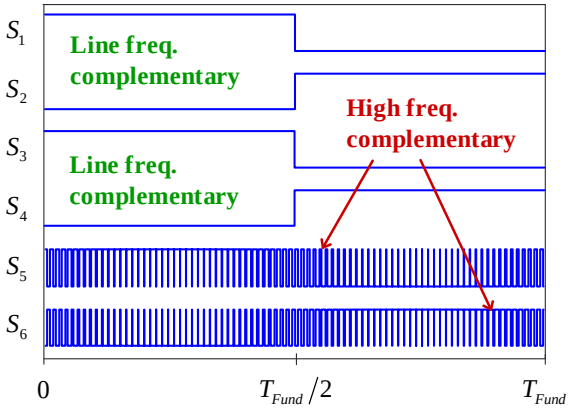

Figure 2-5 Gate signals for modulation type II.

2.3 State of the Art ANPC Inverter Topologies

The above ANPC inverter modulation strategies produce a cluster of low frequency switching devices switching at fundamental line frequency and high frequency switching devices switching at carrier frequency. This feature presents a good opportunity for ANPC inverter to optimize its cost, efficiency, and power density tradeoff. By using Si IGBTs for the low frequency switching devices and SiC MOSFETs for the high frequency switching devices, a good tradeoff between cost, efficiency, and power density can be achieved for this inverter topology. Si IGBTs have lower conduction power loss especially at higher current values and significantly lower cost compared to SiC MOSFETs [2.19] – [2.21]. On the other hand, SiC MOSFETs have much lower switching power loss and higher switching frequency and junction temperature operation capability compared to Si IGBTs [2.22], [2.23].

By leveraging this modulation flexibility, two semiconductor device configurations have been proposed for ANPC inverter to facilitate the tradeoff between efficiency, cost, and power density. In [2.14] and [2.15], the topology shown in Figure 2-6 (a) is proposed using modulation type I and

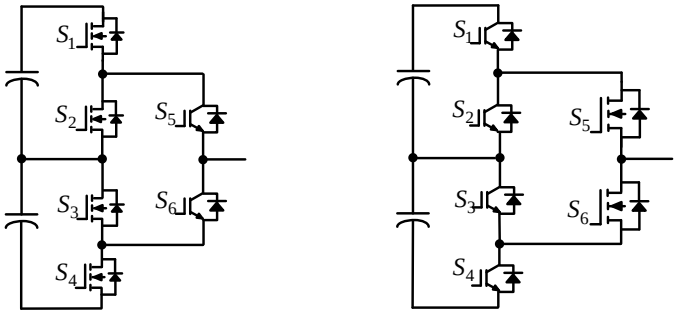

Figure 2-6 State of the art ANPC inverter topologies: (a) topology proposed in [2.14] and [2.15], (b) topology proposed in [2.16] and [2.17].

in [2.16] and [2.17], the topology shown in Figure 2-6 (b) is proposed using modulation type II. Compared to the topology shown in Figure 2-6 (a), the topology shown in Figure 2-6 (b) has better tradeoff in terms of cost and efficiency, since it has a lower number of high frequency switches. Since SiC MOSFETs are used for the high frequency switches, the higher number of high frequency switches will lead to higher inverter cost.

However, the topology in Figure 2-6 (b) has one significant drawback. It involves only a long commutation loop in all operation modes and power factor values. Hence, it has higher semiconductor device switching voltage stress and switching power loss compared to the topology shown in Figure 2-6 (a). To mitigate this problem, switching loop parasitic inductance reduction is proposed in [2.17] by using a decoupling capacitor between the high frequency switching stage and the low frequency switching stage. The decoupling capacitor splits the large commutation loop that this modulation strategy creates into two smaller commutation loops, hence, it reduces the voltage stress and switching energy loss of the high frequency switches.

These two semiconductor device configurations improve the efficiency and cost of an ANPC inverter significantly, they however still have a higher cost compared to their silicon counterpart. The efficiency of an ANPC inverter can be improved without significantly increasing the overall cost of the inverter by using hybrid Si/SiC switching devices for the high frequency switches. In [2.24] – [2.27], it is shown that the loss and cost of high frequency switches can be reduced by using hybrid Si/SiC switching devices compared to using a single SiC MOSFET. By using a higher current rated Si IGBT and a lower current rated SiC MOSFET, the static current sharing therefore the cost and conduction loss of the SiC MOSFET can be reduced. On the other hand, using appropriate gate sequence control, the turn-on and turn-off sequence of the Si IGBT and the SiC MOSFET can be regulated to optimize the switching loss of the Si IGBT.

2.4 The Proposed ANPC Inverter Employing Hybrid Si/SiC Switches

2.4.1 Modulation and Semiconductor Device Configuration

The proposed topology [2.28] – [2.30] uses modulation type II to reduce the number of high frequency switches to achieve a good tradeoff between the inverter cost and efficiency. As shown in Figure 2-7, it uses Si IGBTs for the low frequency switches (S_1 – S_4) to achieve low cost and low conduction power loss for these switching positions. For the high frequency switches (S_5 and S_6), it uses hybrid Si/SiC switches rather than SiC MOSFETs to reduce the cost and power loss of these switches compared to using a single SiC MOSFET. A high current rated Si IGBT and a low current rated SiC MOSFET are used for the hybrid Si/SiC switches to reduce the static current sharing and therefore the cost and conduction power loss of the SiC MOSFETs. Using appropriate gate sequence control for the hybrid Si/SiC switches, the switching loss of the Si IGBT in the hybrid Si/SiC switches is minimized. Therefore, the proposed semiconductor device configuration

provides higher efficiency compared to other ANPC inverter systems such as an all Si IGBT based ANPC inverter system, an all SiC MOSFET based ANPC inverter and mixed Si IGBT and SiC MOSFET based ANPC inverter systems.

Regarding cost, the proposed ANPC inverter system has lower semiconductor device cost compared to an all SiC MOSFET based ANPC inverter system and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems shown in Figure 2-6, while it has almost comparable cost with an all Si IGBT ANPC inverter system. It has lower semiconductor device cost compared to the mixed Si IGBT and SiC MOSFET ANPC inverter systems due to the use of a higher current rated Si IGBT and a lower current rated SiC MOSFET hybrid switches for the high frequency switches. On the other hand, it has lower passive component cost compared to an all Si IGBT ANPC inverter system due to its higher switching frequency operation capability.

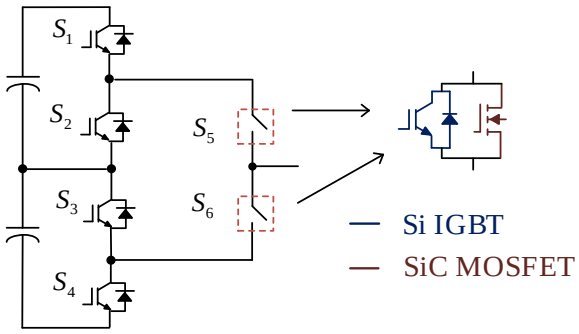

Figure 2-7 Hybrid Si/SiC switches based ANPC inverter topology proposed in this chapter.

2.4.2 Electro-thermal Power Loss Model

In order to demonstrate the efficiency improvement of the proposed hybrid Si/SiC switch based ANPC inverter compared to other similar ANPC inverter configurations such as the all Si IGBT ANPC inverter, the all SiC MOSFET ANPC inverter and the mixed Si IGBT and SiC MOSFET

based ANPC inverters, the theoretical power losses of the different ANPC inverter systems are investigated. The conduction power losses of the semiconductor devices for the different ANPC inverter systems are modeled using the well-known piecewise linear model shown in (2-1) [2.31] – [2.34].

$$P_{\text{cond}} = V_0 I_{\text{avg}} + r I_{\text{rms}}^2 \tag{2-1}$$

where V_0 is the on-state voltage drop of the device, I_{avg} is the average current through the device, r is the equivalent on-state resistance of the device and I_{rms} is the root-mean-square (*rms*) value of the current through the device. The on-state forward voltage (V_0) and the on-state resistance (r) for the semiconductor devices are extracted from their respective datasheet using piecewise linear approximation.

The turn-on energy loss (E_{on}) and the turn-off energy loss (E_{off}) of the semiconductor devices are also extracted from their datasheets. The reverse recovery energy loss of the diodes is already included into the turn-on energy loss (E_{on}) as described in the datasheet. Since the switching loss data provided in the device's datasheet is at a test condition different from the circuit operating condition, the turn-on and turn-off energy losses provided in the device's datasheet are scaled according to (2-2) – (2-3) using the voltage and current values of the datasheet test condition and the actual circuit operating conditions [2.35] – [2.37]. To simplify the switching loss modeling, switching losses are considered to be linear with the dc-link voltage. The switching voltage of three-level ANPC inverter is half of the dc-link voltage ($0.5U_{\text{dc}}$). The relationship between switching loss and the device current is derived by using curve-fitting tools. The total switching power loss of the semiconductor devices is then determined by integrating the total switching energy loss of one switching cycle over the full output fundamental cycle.

$$E_{\text{on}} = \frac{0.5U_{\text{dc}}E_{\text{on,test}}}{U_{\text{test}}} \cdot \frac{k_{2\text{on}}I_0^2 + k_{1\text{on}}I_0 + k_{0\text{on}}}{k_{2\text{on}}I_{\text{test}}^2 + k_{1\text{on}}I_{\text{test}} + k_{0\text{on}}} \tag{2-2}$$

$$E_{\text{off}} = \frac{0.5U_{\text{dc}}E_{\text{off,test}}}{U_{\text{test}}} \cdot \frac{k_{2\text{off}}I_0^2 + k_{1\text{off}}I_0 + k_{0\text{off}}}{k_{2\text{off}}I_{\text{test}}^2 + k_{1\text{off}}I_{\text{test}} + k_{0\text{off}}} \tag{2-3}$$

where $E_{\text{on,test}}$ and $E_{\text{off,test}}$ are the datasheet turn-on and turn-off energy losses, U_{test} and U_{dc} are the dc-link voltages of the datasheet test condition and the actual circuit operating condition, I_0 and I_{test} are the actual current going through the device and the datasheet test current, and k_{ion} and k_{ioff} (i = 0, 1, 2) are the turn-on and turn-off empirical fit coefficients.

The conduction behavior of the hybrid Si/SiC switches depend on the current sharing between the two devices and the polarity of the load voltage. During the positive half cycle of the load voltage, the Si IGBT and the SiC MOSFET conduct the load current. Therefore, the two devices share the load current according to their on-state resistance as shown in (2-4) and (2-5).

$$I_{\text{MOSFET}} = \frac{r_{\text{ce,IGBT}}}{r_{\text{ce,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{2-4}$$

$$I_{\text{IGBT}} = \frac{r_{\text{ds,MOSFET}}}{r_{\text{ce,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{2-5}$$

During the negative half cycle of the load voltage, the SiC MOSFET and the body diode of the Si IGBT conduct the load current. The body diode of the SiC MOSFET has high conduction loss due to its high forward voltage drop. Therefore, synchronous rectification is used for the SiC MOSFET in most cases. The current sharing between the SiC MOSFET and the body diode of the Si IGBT is given by (2-6) and (2-7).

$$I_{\text{MOSFET}} = \frac{r_{\text{bd,IGBT}}}{r_{\text{bd,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{2-6}$$

$$I_{\text{bd,IGBT}} = \frac{r_{\text{ds,MOSFET}}}{r_{\text{bd,IGBT}} + r_{\text{ds,MOSFET}}} I_{\text{load}} \tag{2-7}$$

The energy loss of the hybrid Si/SiC switches for the proposed ANPC inverter is also dependent on the Si/SiC gate control strategy (see section 2.4.3.1). When the Si IGBT and the SiC MOSFET turn on simultaneously as in the case of Option I and Option II, the turn-on loss of the Si IGBT can be ignored and the SiC MOSFET can be assumed to turn-on at the rated load current. This is because the turn on speed of the SiC MOSFET is much higher than the Si IGBT, so the SiC MOSFET turns on very quickly [2.19], [2.22]. The Si IGBT undergoes zero voltage switching for the most part. During turn off, both devices will experience turn-off energy loss proportional to their device current. On the other hand, when a delay time between the two gate signals is used as in the case of Option II – IV, the device which turns on or turns off first handles the full load current and the device which turns on or turns off later handles zero voltage or zero current during switching.

The accuracy of the switching loss model is first verified using measured switching loss data. The test is conducted at room temperature (T_j = 25 ^oC) but it will not lose too much accuracy for elevated temperatures since the switching energy losses are hardly dependent on temperature [2.37]. Table 2-3 shows the specifications of the converter for this test. An Infineon 650 V, 70 A Si IGBT (IRGP4069DPBF) and a ROHM 650 V, 70 A SiC MOSFET (SCT3030ALGC11) are used for the switches. The theoretically estimated and the measured switching energy losses of these switches are shown in Figure 2-8. As can be seen from the figure, the estimated switching energy losses are very close to the measured energy losses and hence the switching loss model is acceptable. This switching energy loss model has also been proved acceptable in [2.38] and [2.39].

Table 2-3 Converter specification.

Parameter	**Value**
Rated output power, P_{rated}	10 kW
Dc-link voltage, U_{dc}	800 V
Output voltage, V_{out}	480 V
Dc-link capacitor	350 μF
Switching frequency	50 kHz

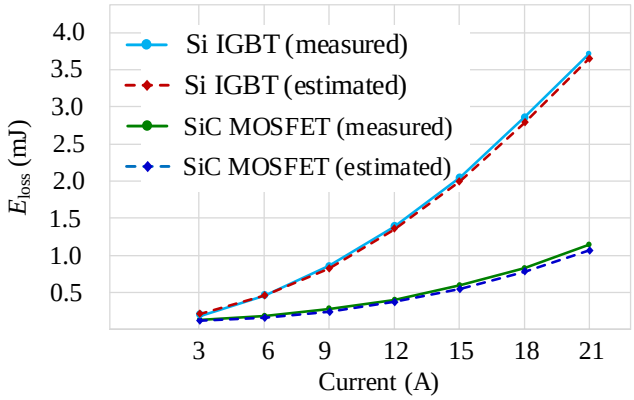

Figure 2-8 Estimated and measured switching energy losses of the Si IGBT and the SiC MOSFET (T_j = 25 °C, V_{GE} = 15 V, $R_{G,\ IGBT}$ = 10 Ω, V_{GS} = 18 Ω, $R_{G,\ MOSFET}$ = 0 Ω).

The overall power loss model is then verified using experimental efficiency data. The theoretical power stage efficiency of the proposed inverter is calculated for different load conditions and is compared with the measured power stage efficiency values. For the hybrid Si/SiC switches, the full current rated Si IGBT (IRGP4069DPBF) and the full current rated SiC MOSFET (SCT3030ALGC11) are initially used for the power loss model validation. The optimal current rating ratio between the Si IGBT and SiC MOSFET for the hybrid Si/SiC switches is later determined in Section 2.4.3.2 based on the power loss model and the Si/SiC current ratio optimization algorithm. The theoretical switching power loss of the devices is calculated from the

energy losses provided in their datasheet at room temperature. Switching energy losses hardly depend on junction temperature [2.37] so this will not compromise the accuracy of the switching power loss calculation for other junction temperature values.

Conduction power loss is however dependent on the junction temperature of the devices. Therefore, the conduction power loss and junction temperature of the devices are calculated iteratively. First, the conduction power losses of the devices are calculated using (2-1) from the datasheet parameters at room temperature (T_j = 25 ^{o}C), and the total power losses of the switches are then calculated from their switching and conduction power losses. The junction temperature of the devices is then calculated from the total power loss, junction to case thermal impedance ($Z_{th,(j-c)}$), and case temperature (T_c) using the thermal model in (2-8). The case temperature of the devices is measured using a thermal image camera for the power loss model validation but for the performance comparison between the different inverters, a reasonable case temperature value can be assumed since this is dependent on the cooling approach. Using the newly calculated junction temperature value, the devices on-state resistance (r) and on-state voltage (V_0) are then calculated as in (2-9) – (2-12) assuming linear relationship between these parameters and junction temperature [2.37].

$$T_j = \left(P_{cond} + P_{sw}\right) \cdot Z_{th,(j-c)} + T_c \tag{2-8}$$

$$r(T_j) = r(T_1) + \sigma_r (T_j - T_1) \tag{2-9}$$

$$V_0(T_j) = V_0(T_1) + \sigma_v (T_j - T_1) \tag{2-10}$$

$$\sigma_r = \frac{r(T_2) - r(T_1)}{T_2 - T_1} \tag{2-11}$$

$$\sigma_v = \frac{V_0(T_2) - V_0(T_1)}{T_2 - T_1} \tag{2-12}$$

where, T_j is the junction temperature of the current iteration, σ_r and σ_v are on-state resistance and on-state voltage temperature dependency coefficients, and T_1 and T_2 are the junction temperatures used for test in the device datasheet (usually 25 ^oC and 125 ^oC or 150 ^oC).

Then, using the newly calculated on-state resistance and on-state voltage values, the new conduction power loss is calculated using (2-1) again, and the entire process is repeated until the junction temperatures of two consecutive iterations are sufficiently close to each other. After the conduction power loss and junction temperature calculation iteration is completed, the power stage efficiency is then calculated from the total conduction and switching power losses. Figure 2-9 shows the measured and calculated efficiencies of the proposed ANPC inverter system. A resistive load bank (SIMPLEX ELECTRA-700) is used as a load while HIOKI power analyzer (PW6001) is used for the power stage efficiency measurement. The slight difference between the two efficiency values is due to losses in PCB parasitic elements and connection wires which are not accounted for in the inverter theoretical loss estimation.

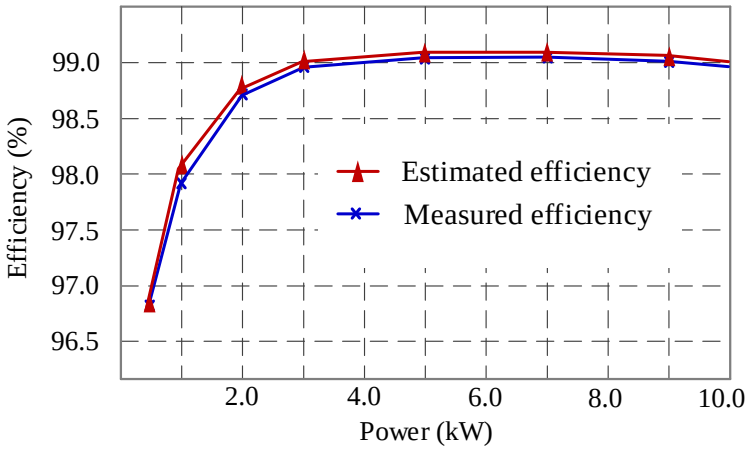

Figure 2-9 Comparison of measured and calculated efficiency for the proposed ANPC inverter for different power levels.

2.4.3 Hybrid Si/SiC Switch Design Considerations

2.4.3.1 Si/*SiC Switch Gate Control Strategies*

Four gate control options are proposed for the hybrid Si/SiC switches in [2.40] – [2.44]. These options differ from each other in the relative switching on and switching off timing of the Si IGBT and the SiC MOSFET. Figure 2-10 shows the gate control options. In the first option (Option I), both the Si IGBT and the SiC MOSFET switch on and switch off simultaneously. This option does not provide significant switching loss reduction since the Si IGBT will still have substantial turn-off energy loss due to its tail current. In the second gate control option (Option II), both devices turn on at the same time, but the Si IGBT turns off before the SiC MOSFET. This option eliminates the turn-off energy loss of the Si IGBT since it is switching off at zero voltage. In the third gate control option (Option III), the Si IGBT turns on after the SiC MOSFET completely turns on and it turns off before the SiC MOSFET turns off. In this gate control option, the SiC MOSFET handles the switching dynamics alone (the Si IGBT switches on and off at zero voltage). Therefore, the switching loss of the Si IGBT is eliminated. In the fourth gate control option (Option IV), the Si IGBT turns on and turns off before the SiC MOSFET. This gate control option eliminates the turn-off energy loss of the Si IGBT, but its turn-on energy loss still exists.

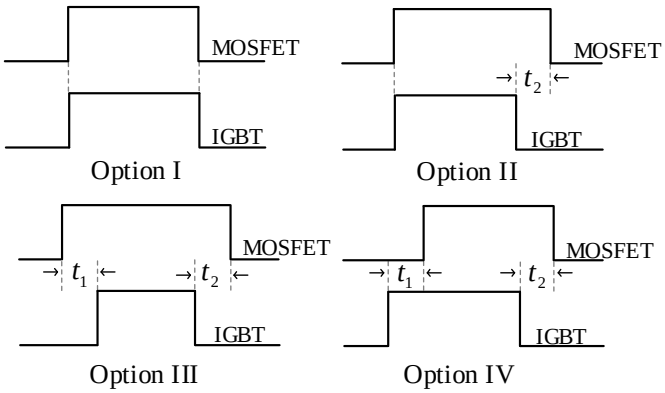

Figure 2-10 Gate control options for hybrid Si/SiC switches.

To ensure the switching loss reduction benefits of hybrid Si/SiC switches, the gate delay between the Si IGBT and SiC MOSFET, (t_1) and (t_2), must be greater than the turn on and turn off times of these devices. The turn on and turn off times also depend on the parasitic elements present in the switching loop. Therefore, it requires careful tuning of the above time difference values to ensure soft switching for the Si IGBT.

2.4.3.2 *Si/SiC Switch Current Rating Ratio Optimization*

Using a low current rated SiC MOSFET and a high current rated Si IGBT for the hybrid Si/SiC switches reduces the cost and conduction loss of the SiC MOSFET. However, smaller current rating means smaller die area (higher thermal resistance). Therefore, a transient temperature peak that could exceed the maximum permissible temperature of the SiC MOSFET will occur during switching if a very small current rated SiC MOSFET is used. If the junction temperature of the SiC MOSFET repeatedly exceeds its maximum permissible value, its material layer will degrade leading to total device failure. This will lead to a subsequent failure of the Si IGBT since it will be subjected to excessive switching loss at high switching frequency when the SiC MOSFET fails. Therefore, the minimum current rating for the SiC MOSFET that ensures a safe operation without its transient peak temperature exceeding its maximum permissible value must be determined to achieve the best tradeoff between cost, loss, and reliability.

The optimal Si/SiC current rating ratio that achieves minimum cost and loss with safe operation is determined using the optimization algorithm shown in Figure 2-11 which was first proposed in [2.24] for dc/dc converters. The algorithm determines the maximum junction temperature of the SiC MOSFET from its junction-to-case thermal impedance and total power losses for different Si/SiC current ratios and gate control options for a given inverter operation conditions. The algorithm begins with a higher Si/SiC current ratio value (smaller SiC MOSFET current rating)

and reduces the current ratio until the maximum junction temperature of the SiC MOSFET is below its maximum permissible value. The switching power loss of the SiC MOSFET is calculated from its energy losses extracted from its datasheet at room temperature, while the conduction and junction temperature of the SiC MOSFET are calculated iteratively as described in section 2.4.2. The optimization algorithm ends when the estimated junction temperature of the SiC MOSFET is lower than its maximum permissible value which is typically 175°C [2.45].

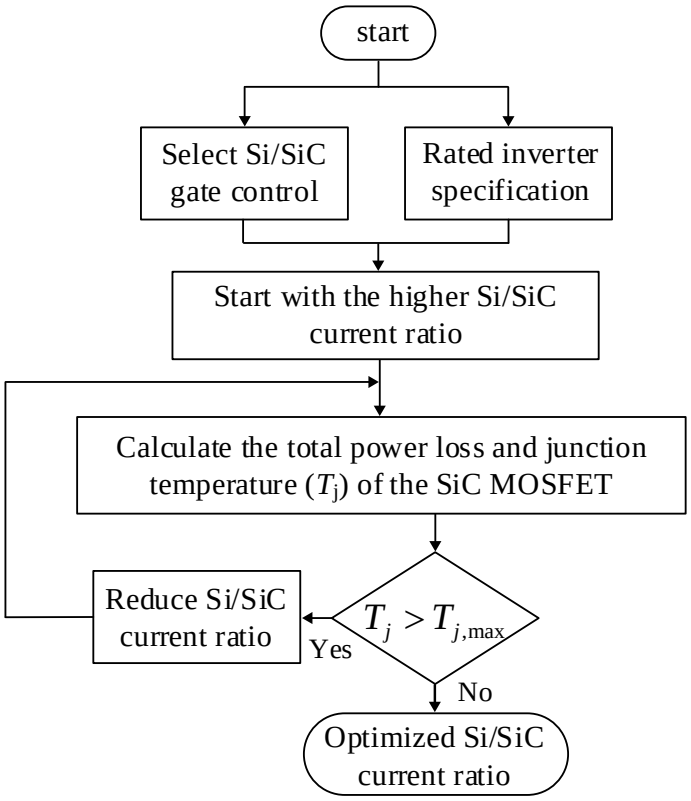

Figure 2-11 Si/SiC current rating ratio optimization algorithm.

When gate control option III is used, the SiC MOSFET carries the full load current during the time durations t_1 and t_2. Therefore, it will be periodically stressed with pulsed currents having a peak value over its rating. The current optimization algorithm uses this gate control option as a worst-case scenario to determine the minimum Si/SiC current ratio since it produces the highest

junction temperature for the SiC MOSFET. Having known the gate control option for the hybrid Si/SiC switches, the second set of data required for the current optimization algorithm is the inverter rated specification. To demonstrate the current optimization algorithm, a 10 kW 480 V (*rms*) inverter system shown in Figure 2-12 is developed. Table 2-4 shows four different sets of Si/SiC switch combinations that can be used for the hybrid switches for this inverter system. These devices are selected solely based their current rating to demonstrate the current ratio optimization algorithm. In practice, several device figure of merits such as cost, power loss, and availability should be considered when selecting the devices.

Figure 2-12 Experimental prototype picture of a 10-kW hybrid Si/SiC switch based ANPC inverter.

Table 2-4 Devices selected for current ratio optimization.

Ratio	**Si IGBT**	**SiC MOSFET**
85:15	IXGR24N60CD1 (600 V, 42.5 A)	SCT2450KEC (650 V, 7.5 A)
80:20	HGTG20N60B3 (600 V, 40 A)	SCT2280KEC (650 V, 10 A)
70:30	RGCL80TK60DGC11 (600 V, 35 A)	SCT3120ALHRC11 (650 V, 15 A)
60:40	IRGPC40S (600 V, 30 A)	SCT3080ALHRC11 (650 V, 20 A)

Figure 2-13 shows the estimated peak junction temperature of the SiC MOSFET for different Si/SiC current ratios and different cooling approaches. For light cooling (for example natural air cooling), a 60:40 Si/SiC current ratio is the optimal choice, whereas a 70:30 Si/SiC current ratio is the optimal choice for heavy cooling (for example liquid cooling), to attain the best tradeoff between cost, loss, and safe operation. The transient peak junction temperature of the Si IGBT can also be determined using the above optimization algorithm. For the Si IGBT, the highest stress occurs when the first gate control option is used. When this gate control option is used, the Si IGBT experiences hard switching under high switching frequency. Therefore, it will face higher stress compared to other gate control options.

Figure 2-14 shows the estimated peak junction temperature of the Si IGBT for different Si/SiC current ratios and different cooling methods. The peak junction temperature of the Si IGBT is lower than the typical maximum permissible value for all Si/SiC current ratios and cooling media. Therefore, the SiC MOSFET is the critical component for determining the Si/SiC current ratio. Light cooling (air cooled heatsink) is considered for this design, so the 60:40 Si/SiC current ratio is chosen.

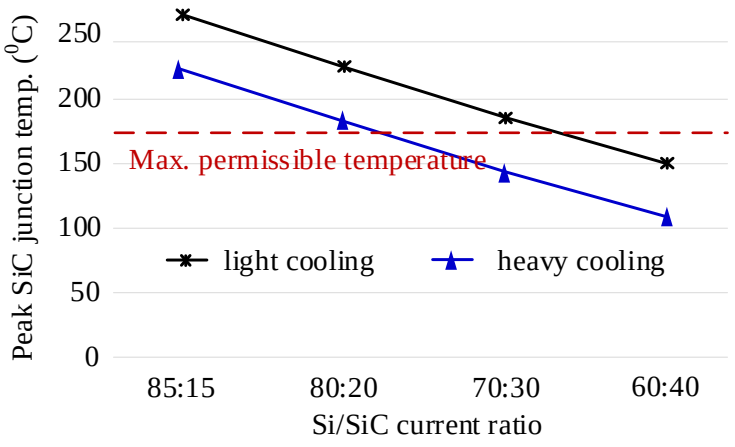

Figure 2-13 Peak junction temperature of the SiC MOSFET for different Si/SiC current ratios.

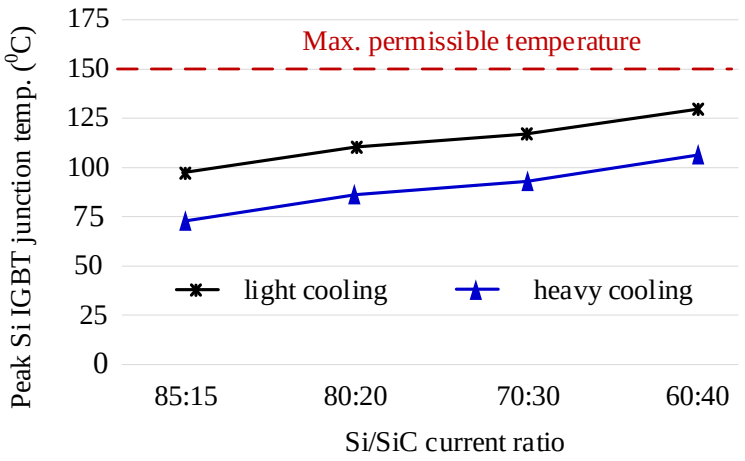

Figure 2-14 Peak junction temperature of the Si IGBT for different Si/SiC current ratios.

2.5 Performance Comparison with Other ANPC Inverter Topologies

The performance of the proposed ANPC inverter system is compared with other similar ANPC inverter systems: (a) an all Si IGBT ANPC inverter system, (b) a mixed Si IGBT and SiC MOSFET ANPC inverter system shown in Figure 2-6 (a), (c) a mixed Si IGBT and SiC MOSFET ANPC inverter system shown in Figure 2-6 (b), and (d) an all SiC MOSFET ANPC inverter system in terms of inverter efficiency and cost. The inverter system specifications for the performance comparison are shown in Table 2-5. The semiconductor device power loss for the different ANPC inverter systems is compared for different power factor and modulation index values. The cost of the semiconductor devices and the associated gate driving circuitry is also compared for the different ANPC inverter systems to assess the efficiency and cost benefit of the proposed ANPC inverter compared to other ANPC inverter systems. Only the cost of the power stage is considered for the cost comparison in order to have a universal cost comparison for different applications such as motor drives and renewable energy conversion applications.

Table 2-5 Converter specification for performance comparison.

Parameter	**Value**	**Cost**
Rated power	10 kW	
Dc-link voltage	800 V	
Output voltage	480 V (*rms*)	
Switching frequency	50 kHz	
Full current Si IGBT	IRGP4069DPBF	$7.02
Full current SiC MOSFET	SCT3030ALGC11	$26.23
Hybrid Si/SiC switches	Si IGBT: IRGPC40S	$5.23
	SiC MOSFET: SCT3080ALHRC	$16.73

2.5.1 Power Loss and Efficiency Comparison

With the data derived from the device datasheet and the help of the power loss model, the power loss of the different ANPC inverter systems is investigated for different operating conditions. To have fair comparison with the proposed ANPC inverter, similar modulation strategy (modulation type II) is used for the other ANPC inverter systems except for the ANPC inverter in Figure 2-6 (a). The semiconductor device configuration for this topology is based on modulation type I hence its efficiency-cost benefits will be discarded if modulation type II is applied.

The power loss distribution of the semiconductor devices for the different ANPC inverters is investigated first under different operating conditions. Since the power loss of an ANPC inverter is symmetrical, only the power loss of the upper half devices (S_1, S_2 and S_5) are shown. Figure 2-15 shows the power loss distributions for the different ANPC inverter systems under unity power factor. As can be seen from the figure, the low frequency switches (S_5 for the topology in Figure 2-6 (a), and S_1 and S_2 for the other topologies) have negligible switching loss since they commutate at fundamental line frequency. Conduction loss is the dominant one for these devices, hence using

Si IGBTs for these switches provides lower conduction losses compared to SiC MOSFETs since Si IGBTs have lower conduction losses compared to SiC MOSFET especially for high output current [2.19], [2.21]. For the high frequency switches (S_1 and S_2 for the topology in Figure 2-6 (a), and S_5 for the other topologies), SiC MOSFETs provide much lower switching loss at the expense of higher conduction loss as can be seen from the power loss of S_5 for the all-Si IGBT, all-SiC MOSFET topologies and the topology in Figure 2-6 (b). In the proposed ANPC inverter, hybrid Si/SiC switches are used for the high frequency switches. Therefore, it combines the benefits of both Si IGBT (lower conduction power loss) and SiC MOSFET (lower switching power loss). This is evident from the power loss of S_5; it has lower overall loss compared to the topologies using SiC MOSFET for this switching position.

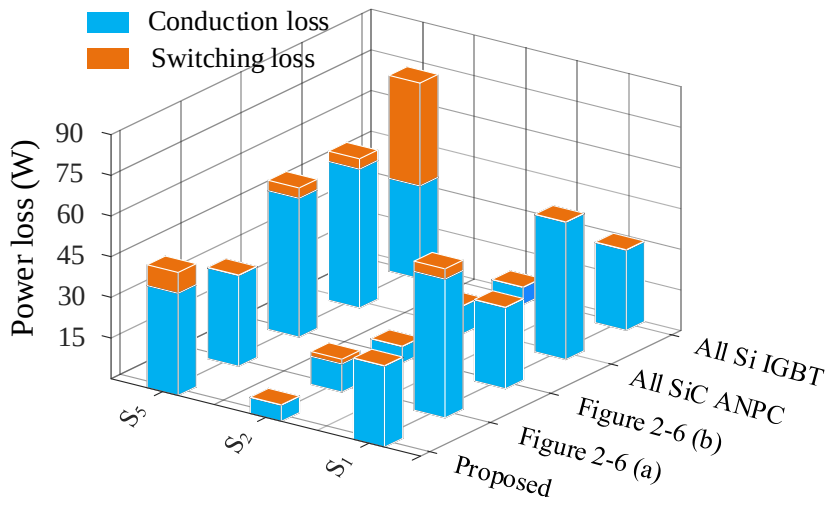

Figure 2-15 Power loss distribution for the different ANPC inverter topologies under unity power factor.

Figure 2-16 shows the power loss distributions for the different ANPC inverter systems for low power factor values. When the power factor is reduced, the inner switches (S_2 and S_3) will have higher power loss due to their higher switching current stress than that of higher power factor

values. The phase leg power loss of the inverter shifts more to the inner switches with decreasing power factor value (this topic is investigated in detail in [2.10], [2.18]). But this does not affect the overall power loss of the proposed ANPC inverter. The proposed ANPC inverter system still has lower power loss (hence higher efficiency) compared to the other ANPC inverters. The switching power loss of the inner switches with Si IGBTs would have increased for low power factor values if they were commutating at carrier frequency. Since they are commutating at fundamental line frequency, their switching loss is negligible.

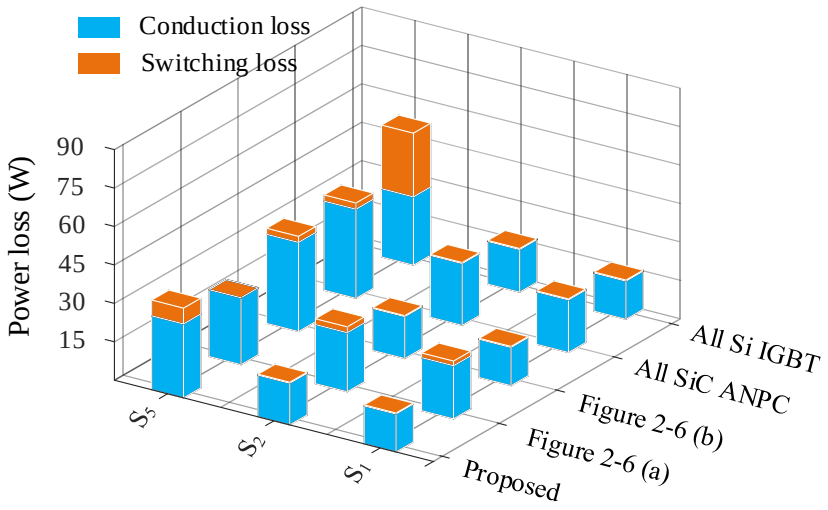

Figure 2-16 Power loss distribution for the different ANPC inverter topologies for low power factor (pf = 0.6).

Figure 2-17 shows the power loss distribution of the different ANPC inverter topologies for low modulation indices. The power loss of the different ANPC inverter systems is investigated for a modulation index of 0.4 as an example to demonstrate the power losses of the different ANPC inverter systems for low modulation indices. When the modulation index is reduced, the output voltage and current of the inverter reduces hence the output power and the power loss of the semiconductor devices reduces too. But, as can be seen from the figure, the proposed ANPC

inverter system still has lower overall power loss (hence higher efficiency) compared to the other ANPC inverters for this modulation index value. But the power loss reduction benefit of the proposed ANPC inverter system is lower for lower modulation indices compared to that for higher modulation indices. This is because the conduction power loss benefits of Si IGBTs compared to SiC MOSFET reduces with lower current and for very low output current Si IGBTs actually have higher conduction power loss than SiC MOSFETs [2.19] – [2.23]. Therefore, the proposed ANPC inverter system will have slightly higher power loss (lower efficiency) than the all-SiC MOSFET topology and the topology in Figure 2-6 (a) for very small modulation indices. However, power converters commonly operate at high modulation index, so this is not necessarily a drawback for the proposed ANPC inverter.

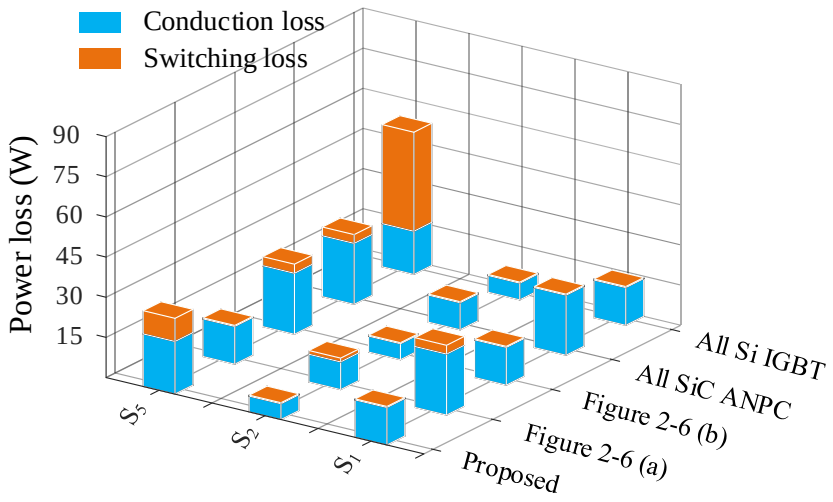

Figure 2-17 Power loss distribution for the different ANPC inverter topologies for low modulation index (m_a = 0.4).

The efficiency of the different ANPC inverter systems is shown in Figure 2-18 and Figure 2-19 for different power levels for both inverter and rectifier operation. As can be seen from these figures, the proposed ANPC inverter system achieves higher efficiency compared to the all Si

IGBT based ANPC inverter system, the all SiC MOSFET based ANPC inverter system, and the mixed Si IGBT and SiC MOSFET based ANPC inverter systems for different power levels. As it is evident from the above power loss analysis, the proposed ANPC inverter system also has higher efficiency compared to the other ANPC inverter systems for low power factor and modulation index values.

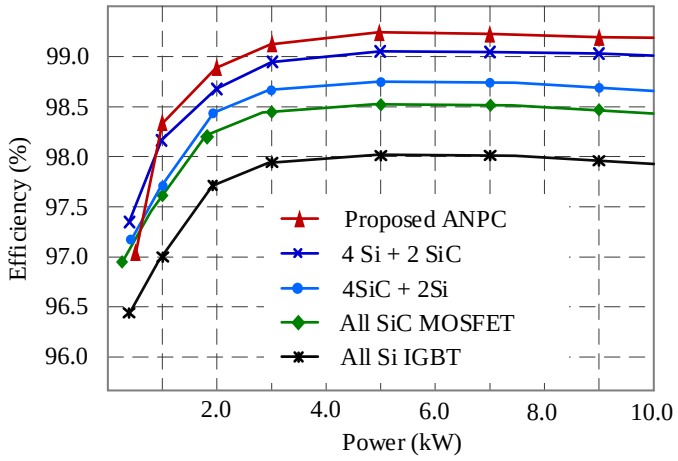

Figure 2-18 Efficiency comparison between the proposed ANPC inverter and other ANPC inverters for inverter operation.

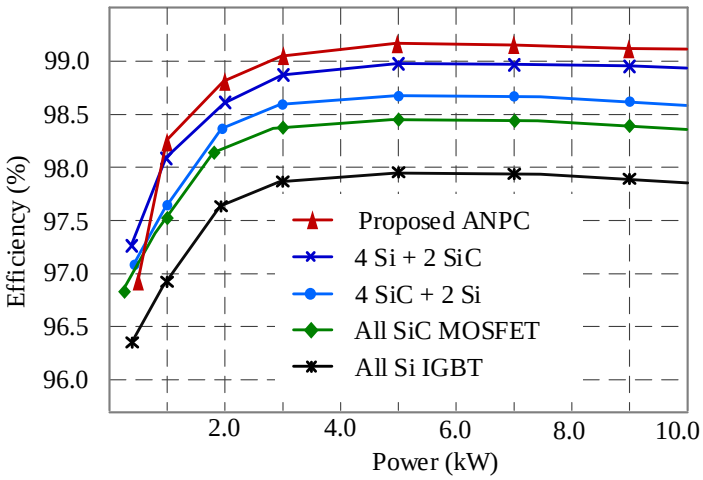

Figure 2-19 Efficiency comparison between the proposed ANPC inverter and other ANPC inverters for rectifier operation.

2.5.2 Cost Comparison

The inverter cost for the different semiconductor device configurations is estimated using off-the-shelf component prices as shown in Table 2-5 obtained from the Digikey website. The cost of the inverter PCB, housing, and cooling system is generally fixed and accounts for approximately 50 percent of the total inverter cost [2.46]. Therefore, the cost of these components is not considered for the cost comparison between the different ANPC inverter systems; only the semiconductor devices and their associated gate driving circuitry cost are considered. Figure 2-20 shows the estimated semiconductor device and gate driver costs for the different ANPC inverter systems. The figure shows the proposed ANPC inverter system has a comparable semiconductor device cost with an all Si IGBT based ANPC inverter system and lower semiconductor device cost compared to the mixed Si IGBT and SiC MOSFET ANPC inverter systems and the all SiC MOSFET ANPC inverter system. The proposed ANPC inverter system however has a slightly higher gate driving circuit cost. This is because the hybrid Si/SiC switches are currently individually driven by a separate gate driver. However, research is underway to reduce the cost and complexity of gate drivers for hybrid Si/SiC switches. In [2.47] and [2.48] a single gate driver

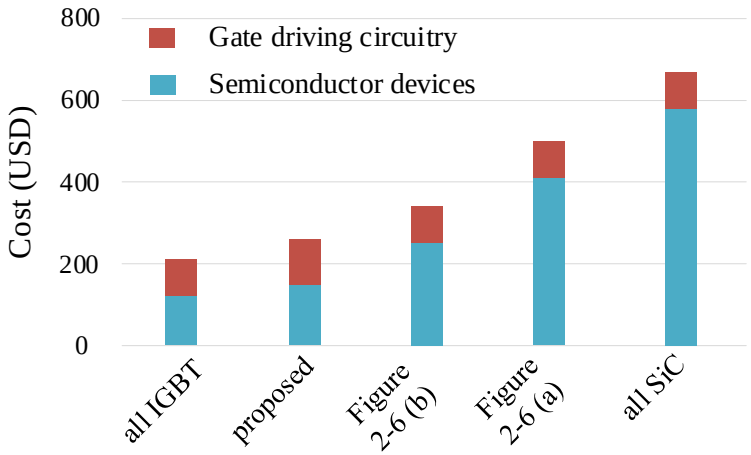

Figure 2-20 Variable inverter cost comparison for different ANPC inverter configurations.

For the hybrid Si/SiC switches is designed and experimentally validated. It features lower cost and lower complexity when compared to the conventional gate driving approach for hybrid Si/SiC switches. Therefore, the slightly higher gate driving circuit cost of the proposed ANPC inverter will not necessarily be a drawback in the future.

2.6 Experimental Validation

The operation of the proposed ANPC inverter is validated by experimental test. A double-pulse test (DPT) experiment is first conducted on the actual inverter phase leg to validate the switching characteristics and current sharing of the hybrid Si/SiC switches. The device currents for the Si IGBT and SiC MOSFET are measured using Tektronix Ultra Mini Rogowski current probe (TRCP0300). This current measurement technique is suitable for TO-247 packaged devices since it can easily clamp around the device legs. The forward voltage is measured using an active differential voltage probe (THDP0200). It should be noted that this voltage measurement technique is not the best choice since it introduces additional loop inductance and hence pronounces the measured voltage overshoot. It is used for this test due to its simplicity and availability.

Gate control option III is used for the hybrid Si/SiC switches to enable soft switching for the Si IGBT. In this gate control strategy, the Si IGBT is turned on after the SiC MOSFET is fully turned on. The SiC MOSFET is turned off after the Si IGBT is fully turned off as shown in Figure 2-23 to achieve zero voltage switching (ZVS) for the Si IGBT. However, to guarantee ZVS for the Si IGBT, the gate turn on delay time (T_{on_delay}) between the Si IGBT and the SiC MOSFET gate signals must be greater than the turn on time (t_{on}) of the SiC MOSFET and the gate turn off delay time (T_{off_delay}) between the Si IGBT and the SiC MOSFET. The gate signals must be greater than the turn off time (t_{off}) of the Si IGBT. The turn on and turn off times of the SiC MOSFET and the

Si IGBT can be extracted from their datasheet by applying current and voltage scaling factor as shown (2-13) and (2-14).

$$t_{on} = t_{d(on)} + \left(\frac{I_L}{I_0}\right) t_{ri} + \left(\frac{V_L}{V_0}\right) t_{fv} \tag{2-13}$$

$$t_{off} = t_{d(off)} + \left(\frac{I_L}{I_0}\right) t_{fi} + \left(\frac{V_L}{V_0}\right) t_{rv} \tag{2-14}$$

where $t_{d(on)}$ and $t_{d(off)}$ are the turn on and turn off delay time of the SiC MOSFET and the Si IGBT, I_L and V_L are the load current and load voltage of the specific application, I_0 and V_0 are the test current and test voltage of the datasheet, t_{ri} and t_{rv} are the current and voltage rise times, t_{fi} and t_{fv} are the current and voltage fall times.

However, the actual turn on and turn off times of the Si IGBT and SiC MOSFET depend on the parasitic inductance of the converter circuit. Large parasitic inductance decreases the switching speed of the devices hence the required turn on and turn off delay time would be greater than the turn on and turn off times calculated from the SiC MOSFET and Si IGBT datasheets. Therefore, the actual turn on time of the SiC MOSFET and turn off time of the Si IGBT are experimentally measured using a double-pulse test to determine the optimum turn on and turn off delay times between the Si IGBT and the SiC MOSFET gate signals required for this specific application. Based on the measured turn on time of the SiC MOSFET and turn off time of the Si IGBT, a turn on delay time of 500 ns and a turn off delay time of 1 μs are used. The turn on delay time is smaller than the turn off delay time since the former depends on the turn on speed of the SiC MOSFET and the later depends on the turn off speed of the Si IGBT.

Figure 2-21 shows the turn on characteristics of the hybrid Si/SiC switches. During the turn on transient of the SiC MOSFET, the gate voltage (V_{GE}) of the Si IGBT should be zero. However,

there will be a small oscillatory voltage (as shown in the figure) induced in the gate voltage of the Si IGBT due to the parasitic crosstalk effect of the SiC MOSFET and the Si IGBT. The fast changing SiC MOSFET gate current induces a ringing voltage on the Si IGBT gate voltage. In order to make sure this phenomenon does not cause false triggering for the Si IGBT, a negative gate driving voltage (-4V) is used. The value of the negative gate driving voltage depends on the magnitude of the ringing voltage (which in turn depends on the parasitic inductance of the converter circuit) and the threshold voltage of the Si IGBT. Larger negative gate driving voltage provides higher noise immunity, but it increases the switching energy loss of the Si IGBT since it increases the gate driver swing voltage. Figure 2-22 shows the turn off characteristics of the hybrid Si/SiC switches.

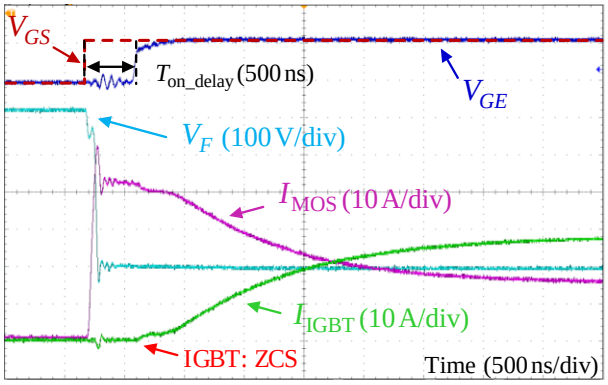

Figure 2-21 Turn on characteristics of the hybrid Si/SiC switches.

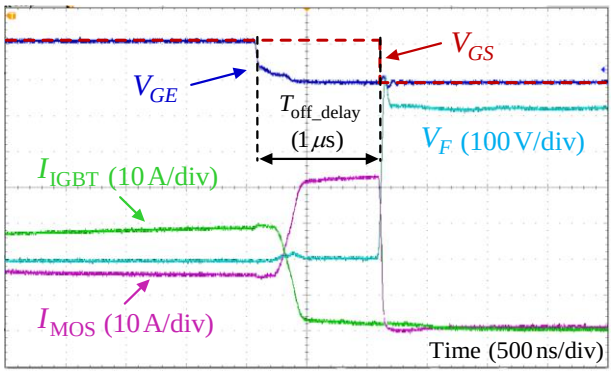

Figure 2-22 Turn off characteristics of the hybrid Si/SiC switches.

Figure 2-23 shows the conduction (static) characteristics of the hybrid Si/SiC switches. When gate control Option III is used, the SiC MOSFET carries the full forward current during the turn on and turn off process, but during conduction, the forward current is shared between the two devices according to their current rating. Based on the Si/SiC current rating optimization algorithm, the Si IGBT is designed to conduct 60 percent of the forward current and the SiC MOSFET is designed to conduct 40 percent of the forward current for the application considered in this design. For other power levels and operating conditions, the optimal current sharing between the Si IGBT and the SiC MOSFET should be determined using the Si/SiC current ratio optimization algorithm.

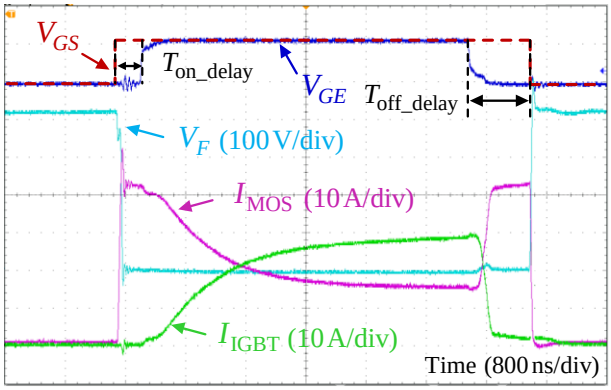

Figure 2-23 Switching and conduction characteristics of the hybrid Si/SiC switches.

To verify the thermal performance of the hybrid Si/SiC switches, the case temperature of the hybrid Si IGBT and SiC MOSFET devices is measured using an infrared thermal image camera (FLIR C2) because of the difficulty of measuring the junction temperature of discrete power devices. The respective junction temperature value of the Si IGBT and SiC MOSFET is then estimated from the measured case temperature value using the device power loss and thermal model. Figure 2-24 shows the measured case temperature and the estimated junction temperature of the hybrid Si IGBT and SiC MOSFET switches for different power levels. The figure shows

the junction temperature of the hybrid Si/SiC switches is below their respective maximum permissible values for the different power levels. Therefore, the hybrid Si/SiC switch design is reliable.

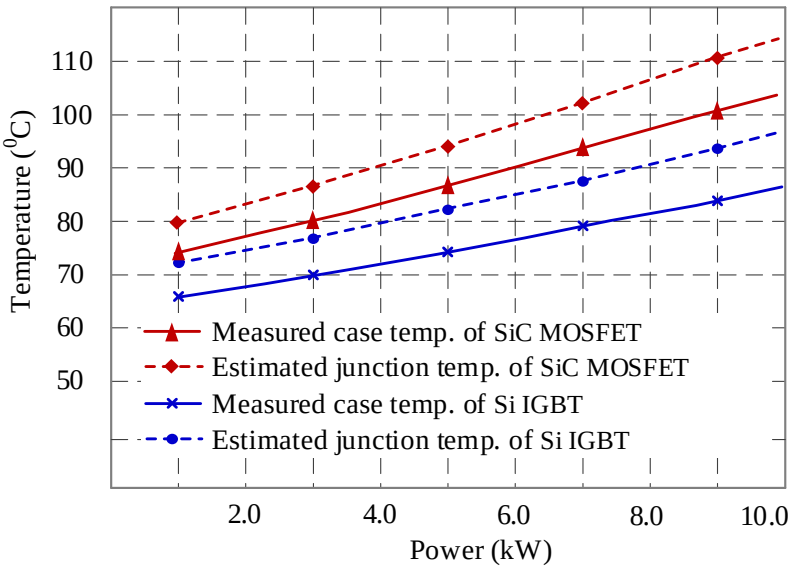

Figure 2-24 Measured case temperature and estimated junction temperature for the hybrid Si/SiC switches for different power levels.

The overall operation of the inverter is also tested. In terms of the overall operation of the inverter, using hybrid Si/SiC switches will not affect the operation of the inverter with respect to the output voltages and currents of the inverter since the operation of power converters fundamentally depends on the modulation (control) strategy and the output filter of the converter. Figure 2-25 shows the three-phase output voltages of the inverter and Figure 2-26 shows the line-to-line output voltage and three phase output currents of the inverter. The slightly higher ripples in the output current waveform are due to the output filter. Only one three phase reactor of 170 μH is used for the test just to verify the output waveforms of the inverter. In practice, a load side inductor and parallel capacitor would be required to eliminate these high frequency ripples. Figure 2-27 shows the dc-link capacitor voltage waveforms along with the inverter phase voltage and

current waveforms. The carrier-based dc-link capacitor voltage balancing strategy presented in [2.49] is used to achieve dc-link capacitor voltage balancing.

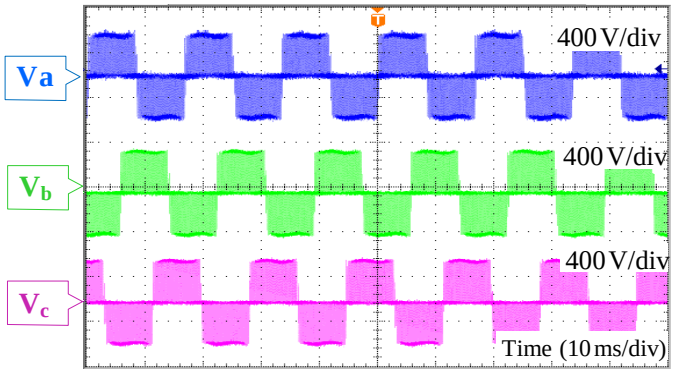

Figure 2-25 Inverter phase output voltage waveforms.

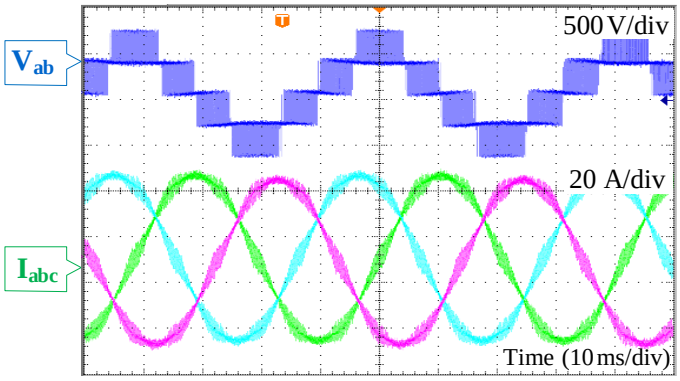

Figure 2-26 Inverter output line-to-line voltage and three-phase to output current waveforms.

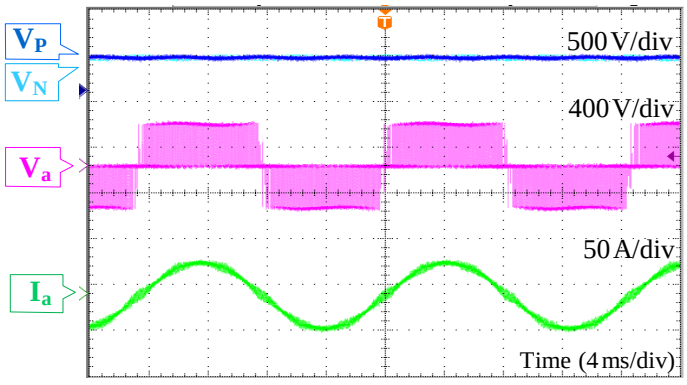

Figure 2-27 Dc-link capacitor voltages, output voltage and output current waveforms.

2.7 Conclusion

This chapter presented the design and validation of a high efficiency and low cost three-level Active Neutral Point Clamped (ANPC) inverter employing hybrid Si/SiC switches. It uses a modulation strategy that creates a group of low frequency switches commutating at fundamental line frequency and high frequency switches commutating at carrier frequency to enable the use of hybrid Si/SiC switches. Si IGBTs are used for the low frequency switches, while hybrid Si/SiC switches are used for the high frequency switches to reduce the cost and power loss of the inverter. In order to fully leverage the benefits of hybrid Si/SiC switches while guaranteeing safe operation, an Si/SiC current ratio optimization algorithm is presented. The optimization algorithm determines the minimum Si/SiC current rating ratio that provides low cost, low loss, and safe operation based on the inverter specifications and Si/SiC gate control strategy.

The proposed ANPC inverter system provides higher efficiency compared to a Si IGBT based ANPC inverter system, a SiC MOSFET based ANPC inverter system and a mixed Si IGBT and a SiC MOSFET based ANPC inverter systems for different power levels and operation modes. On the other hand, the semiconductor device cost of the proposed ANPC inverter system is comparable with an ANPC inverter system containing only Si IGBTs and much lower than an ANPC inverter system consisting only of SiC MOSFETs or mixed Si IGBT and SiC MOSFETs. The gate driver cost for the proposed ANPC inverter system is currently slightly higher. But research is underway to reduce the cost and complexity of the gate driver for hybrid Si/SiC switches, and there are positive results in literature already. Therefore, this is not necessarily a drawback in the future.

2.8 Reference

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CHAPTER 3

FIGIRE OF MERIT FOR HYBRID SI/SIC SWITCHES

3.1 Introduction

Despite several investigations that have already been carried out on the operation, control, and characteristics of hybrid Si/SiC switches, research on the figure-of-merit of these type of switches is still scarce. Semiconductor device figures-of-merit serve as a quick tool to assess the performance merits of different semiconductor devices across similar or different technology types, packaging techniques, and device parameters [3.1] – [3.4]. Hence, they facilitate the design and optimization of converter topologies by eliminating the need for developing a full converter power loss model that would otherwise be required for the power loss and efficiency estimation of different semiconductor devices for a specific converter topology to perform the converter design optimization. As a result, this research topic has been one of the hottest research topics that has attracted increased attention recently especially with the increasing renewable energy and electric transportation market.

Several material figures-of-merits (M-FOM) have been proposed in literature for semiconductor devices by considering their material properties such as electron mobility, critical electric field, and thermal conductivity [3.5] – [3.8]. These types of figures of merits facilitate the research and development of new types of semiconductor device technologies with better performance indices since they are primarily an indicator of the performance of the materials that semiconductor devices are made from. Another type of semiconductor device figures of merit is device figures-of-merit (D-FOM) that are derived by considering the higher-level device parameters such as equivalent gate charge, equivalent output capacitance, and on-state resistance of the semiconductor devices [3.9] – [3.11]. These types of figures of merits help to compare the performances of semiconductor devices

of different technology, manufacturer, and device ratings. They are the ones that designers mostly use to perform converter design optimization in terms of converter efficiency and power density tradeoff [3.2], [3.11]. This is because the high-level semiconductor device properties such as on-state resistance, input capacitance and output capacitance are the prime determinants of the converter conduction and switching power losses along with its operating conditions such as operating voltage, current, and switching frequency.

Several material and device figures of merits have already been proposed in literature, they are primarily applicable for single type devices – either Si IGBTs or SiC MOSFETs. They cannot be used for hybrid Si/SiC switches in their entirety since the conduction and switching characteristics of hybrid Si/SiC switches are distinct from that of single Si IGBT and SiC MOSFET devices. Therefore, it is necessary to revise the existing semiconductor device figures of merits to account for the operating characteristics of hybrid Si/SiC switches and drive an improved figure of merit for these new types of switches to facilitate the design optimization of different converter topologies employing hybrid Si/SiC switches.

This chapter introduces an improved converter figure of merit (C-FOM) for hybrid Si/SiC switches combining the device properties of the individual switches such as on-state resistance and output capacitance with the converter topology properties such as blocking voltage and switching frequency to precisely forecast the efficacy of hybrid Si/SiC switches for different converter topologies. To arrive at the improved figure of merit, the existing device figures of merits for single-technology devices (Si IGBT and SiC MOSFET) are first revised in Section 3.2 and the parameters that differ for hybrid Si/SiC switches are identified. An improved device figure of merit (D-FOM) for hybrid Si/SiC switches is then derived to facilitate performance comparison between different hybrid Si/SiC switch combinations for a specific converter application. The improved device figure

of merit is then extended to incorporate the converter topology operating parameters and arrive at the improved converter topology and semiconductor device figure of merit for hybrid Si/SiC switches (C-FOM). The proposed converter figure of merit enables quick performance comparison between different converter topology and hybrid Si/SiC switch combinations hence helps designers to perform rapid design optimizations of converters employing these types of switches.

3.2 Review of Semiconductor Device Figure of Merits

The most common material figures of merits are the Johnson figure of merit (JFOM) [3.6] and the Keyes Figure of Merit (KFOM) [3.7]. The JFOM claims the ultimate performance of semiconductor devices depend on the critical electric field (E_C) and the minority carrier saturation velocity (v_s) to arrive at the figure of merit shown in (3-1). The Johnson figure of merit implies an inverse relationship between power and frequency irrespective of thermal dissipation.

$$\text{JFOM} = \frac{E_c v_s}{2\pi} \tag{3-1}$$

In subsequent research work, Keyes however argued that the performance of semiconductor devices depends on the thermal conductivity of the material and thereby proposed a new material figure of merit termed as Keyes' Figure of Merit (KFOM) given by (3-2).

$$\text{KFOM} = \lambda \frac{c v_s}{4\pi\varepsilon_r} \tag{3-2}$$

where λ is the thermal conductivity of the semiconductor material, c is the velocity of light in free space and ε_r is the dielectric constant of the semiconductor material.

Recently, two specialized material figures of merits have also been proposed for the performance comparison of wideband gap semiconductor materials namely the Huang Material Figure of Merit (HMFOM) given in (3-3) and the Huang Thermal Figure of Merit (HTFOM) given in (3-4) [3.8].

The HMFOM is derived for the power loss comparison of different wideband gap semiconductor materials, while the HTFOM is derived for the thermal performance comparison of different wideband gap semiconductor materials.

$$\text{HMFOM} = E_C\sqrt{\mu} \tag{3-3}$$

$$\text{HTFOM} = \sigma_{\text{th}}/\varepsilon E_{\text{C}} \tag{3-4}$$

where μ is carrier mobility of the semiconductor material, ε the dielectric constant of the semiconductor material, and σ_{th} is the thermal conductivity of the semiconductor material.

Apart from the semiconductor material properties, the performance of semiconductor devices also depends on the manufacturing process, the device structure, and packaging technology [3.2], [3.10], [3.12] hence material figures of merits do not precisely indicate the performance of semiconductor devices. Therefore, by rather considering the higher-level semiconductor device properties such as on-state resistance and input/output capacitance, device figures of merits are also proposed to better serve the design optimization of power converters in terms of efficiency and power density tradeoff.

In 1989, Baliga proposed a new device figure of merit termed as the Baliga High Frequency Figure of Merit (BHFFOM) [3.9] shown in (3-5). This considers both the conduction and switching power loss of semiconductor devices. He argued the converter conduction and switching power losses are inversely dependent on the specific on-state resistance and specific input capacitance of the semiconductor devices at high switching frequencies.

$$\text{BHFFOM} = \frac{1}{R_{\text{on,sp}}C_{\text{in,sp}}} \tag{3-5}$$

where $R_{\text{on,sp}}$ is the specific on-state resistance and $C_{\text{in,sp}}$ is the specific input capacitance of the semiconductor devices.

The switching power loss of semiconductor devices however depends not only on the input capacitance of the devices but also on their output capacitances [3.22] – [3.24]. Therefore, the BHFFOM is not an accurate indicator of semiconductor device power losses. In subsequent research work Kim [3.10] proposed an improved device figure of merit for high frequency applications shown in (3-6) by rather considering the specific on-state resistance and specific output capacitance of the semiconductor devices.

$$\text{NHFFOM} = \frac{1}{R_{\text{on,sp}} C_{\text{oss,sp}}} \tag{3-6}$$

where $C_{\text{oss,sp}}$ is the specific output capacitance of semiconductor devices. As backed by the investigation in [3.12], [3.22] – [3.24], this device figure of merit provides better insight into the conduction and switching power loss of semiconductor devices in hard-switched power electronic circuit applications. The output capacitance rather than the input capacitance of semiconductor devices is the dominant factor determining capacitive switching power losses for hard-switched power electronic converters [3.22] – [3.24].

However, (3-6) cannot be used for hybrid Si/SiC switches in its entirety. The conduction power loss of the hybrid Si/SiC switches depend on the current sharing between the two internal devices. Their switching energy loss on the other hand depends on the equivalent output capacitance of the internal devices (the output capacitances of the internal devices add up due to their parallel configuration). In addition, the switching power loss of hybrid Si/SiC switches also depend on the gate control strategy between the two internal devices. Therefore, (3-6) needs to be revised to account the conduction and switching characteristics of hybrid Si/SiC switches as well as their gate control strategies to come up with an improved figure of merit that is effective for the design optimization of converter topologies employing hybrid Si/SiC switches.

3.3 Improved Figure of Merit for Hybrid Si/SiC switches

3.3.1 Improved Device Figure of Merit

In order to derive a figure of merit expression for hybrid Si/SiC switches, it is first important to explore the conduction and switching power loss of these types of switches. The conduction and switching power loss of hybrid Si/SiC switches are widely investigated in [3.14] – [3.17]. To avoid unnecessary repetition, only the relevant expression needed towards deriving the figure of merit expression for hybrid Si/SiC switches are presented here.

The conduction loss of the hybrid Si/SiC switches can be calculated as in (3-7) [3.18] – [3.21].

$$P_{\text{cond}} = R_{\text{eq}} I_{\text{rms}}^2 \tag{3-7}$$

where R_{eq} is the equivalent on-state resistance of the hybrid Si/SiC switches given by (3-8) and I_{rms} is the root-mean-square (rms) value of the load current.

$$R_{\text{eq}} = \frac{R_{\text{on\_IGBT}} R_{\text{on\_MOS}}}{R_{\text{on\_IGBT}} + R_{\text{on\_MOS}}} \tag{3-8}$$

where $R_{\text{on\_IGBT}}$ is the collector-to-emitter equivalent on-state resistance of the Si IGBT and $R_{\text{on\_MOS}}$ is the drain-to-source on-state resistance of the SiC MOSFET.

The switching power loss of the semiconductor devices on the other hand depends on many parameters such as the semiconductor device material type, the device structure, the packaging technique, the gate driver parameters, and the converter circuit parasitic elements [3.22] – [3.24]. It is therefore very difficult to come up with an accurate switching power loss model for semiconductor devices that accounts for all of these factors. Usually, a simplified switching power loss model is used depending on the purpose of the investigation. To assess the performance of the semiconductor devices and compare among each other, a precise switching power loss model is not usually necessary. The minimum hard-switching energy losses that indicate the maximum

achievable converter efficiency is normally used to derive a figure of merit expression for semiconductor devices [3.12], [3.25], [3.26]. This is especially valid for hard-switched high-frequency converter applications where the switching currents are typically much smaller than the load current [3.12], [3.23], [3.24]. For these applications, the $V - I$ overlap period is very small, and therefore the capacitive switching energy losses are dominant.

The minimum hard-switching energy dissipated per switching cycle can be given by (3-9) [3.27].

$$E_{\mathrm{sw}} = C_{\mathrm{oss}} U_{\mathrm{dc}}^2 \tag{3-9}$$

where C_{oss} is the equivalent output capacitance of the semiconductor devices and U_{dc} is the dc bus voltage of the application. For hybrid Si/SiC switches, (3-9) can be rewritten as in (3-10) considering the C_{oss} of the internal Si/SiC switches.

$$E_{\mathrm{sw}} = \left(C_{\mathrm{oss\_IGBT}} + C_{\mathrm{oss\_MOS}} \right) U_{\mathrm{dc}}^2 \tag{3-10}$$

The switching energy loss of hybrid Si/SiC switches also depends on the Si/SiC gate control strategy. The different gate control strategies have their own benefits and drawbacks as presented in Section 2.4.3.1, gate control option II is the preferred gate control strategy for switching loss reduction of hybrid Si/SiC switches. Since the switching speed of the SiC MOSFET is much higher than the Si IGBT, the SiC MOSFET turns on very quickly and handles the majority of turn-on current by itself [3.28] – [3.30]. The Si IGBT on the other hand undergoes zero voltage turn on for the most part of its turn on process, hence it has a very small turn on energy loss. However, Si IGBT devices have large turn off energy loss due to their tail current [3.31] – [3.33]. If the Si IGBT turns off simultaneously with the SiC MOSFET, the hybrid Si/SiC switches will have a large turn off loss. On the other hand, if the Si IGBT turns off before the SiC MOSFET does, the Si IGBT will undergo a zero voltage turn off, hence its turn off loss can be reduced or even eliminated. However,

large turn off delay time between the Si IGBT and the SiC MOSFET will increase the conduction power loss of the SiC MOSFET and ultimately the total power loss of the hybrid Si/SiC switches. Therefore, an optimal turn off delay time that reduces the switching energy loss of the Si IGBT without increasing the conduction power loss of the SiC MOSFET must be used.

The effect of the turn-off delay time on the switching energy loss of the hybrid Si/SiC switches is investigated in [3.17], [3.34] – [3.36] for dc/dc applications. In this chapter, the investigation is extended to an inverter application using the three-level ANPC inverter topology utilizing hybrid Si/SiC switches introduced in Chapter 2. Figure 3-1 shows the typical turn off characteristics of hybrid Si/SiC switches when gate turn off delay time is applied. As can be seen from the figure, the SiC MOSFET carries the full load current during the turn off delay time. Therefore, it experiences an additional conduction loss ($\Delta E_{\text{cod\_MOS}}$) during this period.

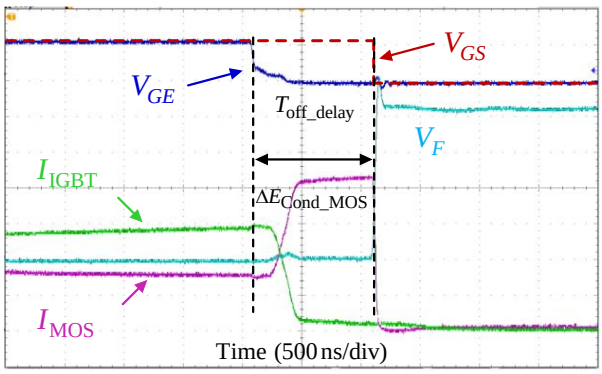

Figure 3-1 Turn-off characteristics of hybrid Si/SiC switches with turn-off delay time.

Accounting for the gate turn off delay time, the switching energy loss of the hybrid Si/SiC switches can be modeled as (3-11) – (3.13) [3.17], [3.36].

$$E_{\text{sw}} = E_{\text{sw\_MOS}} + E_{\text{sw\_IGBT}} \tag{3-11}$$

where, $E_{\text{sw\_MOS}}$ is the switching energy loss of the SiC MOSFET given by (3-12) and $E_{\text{sw\_IGBT}}$ is the switching energy loss of the Si IGBT given by (3-13). The righthand side expression in (3-12)

represents the additional conduction loss of the SiC MOSFET during the turn off delay time. It is modeled as switching energy loss for convenience [3.17], [3.36].

$$E_{\text{sw\_MOS}} = E_{\text{sw\_hard\_MOS}} + R_{\text{ds\_MOS}} \cdot T_{\text{off\_delay}} \cdot I_{\text{rms}}^2 \tag{3-12}$$

$$E_{\text{sw\_IGBT}} = E_{\text{sw\_hard\_IGBT}} \cdot e^{-\delta \cdot T_{\text{off\_delay}}} \tag{3-13}$$

where $E_{\text{sw\_hard\_MOS}}$ and $E_{\text{sw\_hard\_IGBT}}$ are the hard-switching energy losses of the SiC MOSFET and the Si IGBT respectively given by (3-9) and δ is exponential time constant for the dependency of the switching energy loss of the Si IGBT on the gate turn off delay time. Combining (3-9), (3-11), (3-12) and (3-13), the minimum hard switching energy loss of the hybrid Si/SiC switches will be as shown in (3-14).

$$E_{\text{sw}} = U_{\text{dc}}^2 \cdot \left(C_{\text{oss\_MOS}} + C_{\text{oss\_IGBT}} \cdot e^{-\delta \cdot T_{\text{off\_delay}}} \right) + R_{\text{on\_MOS}} \cdot T_{\text{off\_delay}} \cdot I_{\text{rms}}^2 \tag{3-14}$$

As can be seen from (3-14), the minimum hard-switching energy loss of the hybrid Si/SiC switches has exponential dependency on the gate turn off delay time. Therefore, there exists an optimal gate turn off delay time ($T_{\text{off\_delay\_opt}}$) that results in minimum hard-switching energy loss for the hybrid Si/SiC switches. This optimal gate turn off delay time value can be determined by taking the derivative of (3-14) with respect to the turn off delay time and equating it to zero as shown in (3-15) and (3-16).

$$\frac{\mathrm{d}}{\mathrm{d}T_{\text{off\_delay}}} \left(\begin{array}{c} U_{\text{dc}}^2 \cdot \left(C_{\text{oss\_MOS}} + C_{\text{oss\_IGBT}} \cdot e^{-\delta \cdot T_{\text{off\_delay}}} \right) \\ + R_{\text{on\_MOS}} \cdot T_{\text{off\_delay}} \cdot I_{\text{rms}}^2 \end{array} \right) = 0 \tag{3-15}$$

$$T_{\text{off\_delay\_opt}} = \frac{1}{\delta} \ln \left(\frac{R_{\text{on\_MOS}} I_{\text{rms}}^2}{C_{\text{oss\_IGBT}} U_{\text{dc}}^2} \right) \tag{3-16}$$

Eq. (3-16) shows the optimal gate turn off delay time is not purely a function of the semiconductor device parameters but also depends on the converter parameters such as the dc bus

voltage and the load current. Therefore, in order to derive a figure of merit that solely depends on the semiconductor device parameters (device figure of merit), the switching energy loss dependency on the gate turn off delay time can be first neglected. This will be reconsidered when we drive an improved converter figure of merit for hybrid Si/SiC switches combining the properties of the semiconductor devices and the specific converter topology operating properties in Section 3.3.2.

From (3-7), (3-8), and (3-10), it can be observed that the power loss of the hybrid Si/SiC switches increases when the on-state resistance and output capacitance of the internal switches (the Si IGBT and the SiC MOSFET) increases. Therefore, with the goal of reducing the power loss of the hybrid Si/SiC switches, a better Si/SiC switch combination would have lower equivalent on-state resistance ($R_{\text{on,eq}}$) and lower equivalent output capacitance ($C_{\text{oss,eq}}$). Hence, the device figure of merit shown in (3-17) can be derived for hybrid Si/SiC switches.

$$\text{D-FOM} = \frac{1}{R_{\text{on,eq}} C_{\text{oss,eq}}} \tag{3-17}$$

where $R_{\text{on,eq}} = (R_{\text{on\_IGBT}} R_{\text{on\_MOS}}) / (R_{\text{on\_IGBT}} + R_{\text{on\_MOS}})$ and $C_{\text{oss,eq}} = (C_{\text{oss\_IGBT}} + C_{\text{oss\_MOS}})$.

The power loss of semiconductor devices also depends on the converter operating parameters, such as switching frequency and device blocking voltage apart from the semiconductor device properties. Therefore, the device level figure of merit in (3-17) falls short in revealing the performance of hybrid Si/SiC switches for different converter topologies and operating conditions. Designers usually explore for a combination of different semiconductor devices and converter topologies in search of an optimized converter solution in terms of performance for a specific application. This process requires estimating the power loss of the converter either by using analytical power loss model or electro-thermal circuit simulation [3.38], [3.39]. Alternatively, a converter figure of merit that combines the semiconductor device properties and the converter

topology operating conditions such as [3.12] can be used to quickly assess the performance of different semiconductor device and converter topology combinations. In the following section, an improved hybrid Si/SiC switch converter figure of merit (C-FOM) combining the semiconductor device properties of hybrid Si/SiC switches and the converter operating conditions is proposed.

3.3.2 Converter Figure of Merit

The first step towards deriving a converter figure of merit that combines the properties of the semiconductor devices and the converter topology is to investigate the dependency of the semiconductor device properties on the blocking voltage of the converter topology. This is because different converter topologies have different semiconductor device blocking voltage requirements. For example, the semiconductor devices in a two-level converter topology need to block the full dc bus voltage while the semiconductor devices in a three-level ANPC converter topology need to only block one-half of the dc bus voltage [3.40]. The higher voltage that the semiconductor devices need to block, the higher their switching energy loss will be. The lower their figure of merit should be. Therefore, in order to develop a precise figure of merit for semiconductor devices that is valid for different converter topologies, the semiconductor devices blocking voltage requirement must be considered. In [3.12], a detailed investigation with physics-based derivation of the dependencies of the semiconductor devices' on-state resistance and output capacitance with blocking voltage is presented. To avoid unnecessary repetitions, only the relevant expressions needed for deriving the improved converter figure of merit for hybrid Si/SiC switches are presented in this chapter. Readers can refer to [3.12] for detailed derivations and analysis of the dependencies of the semiconductor devices' on-state resistance and output capacitance on the semiconductor devices' blocking voltage.

The semiconductor devices on-state resistance (R_{on}) can be written as a function of a technology-specific constant (α_R) and the device blocking voltage (U_B) [3.12], [3.25], [3.41].

$$R_{on}(U_B) = \alpha_R U_B^2 \tag{3-18}$$

The value of the technology-specific scaling constant (α_R) can be derived by empirical fitting from the on-state resistance and blocking voltage rating values of different commercially available semiconductor devices. This value is approximated as 4.8×10^{-4} for the Si IGBT devices and 7.2×10^{-3} for the SiC MOSFET devices in [3.12] using this approach.

Like the on-state resistance, the charge equivalent output capacitance (C_{oss}) can also be written as a function of the blocking voltage of the semiconductor devices (U_B) and the technology-specific constant (α_c) as shown in (3-19) [3.12], [3.25].

$$C_{oss}(U_B) = \frac{\alpha_C}{U_B} \tag{3-19}$$

The value of the technology specific scaling constant (α_c) can be similarly determined by empirically fitting the relationship between the output capacitance and blocking voltage rating of different commercially available semiconductor devices. This value is again approximated as 2.4×10^{5} for the Si IGBTs and 1.6×10^{4} for the SiC MOSFETs in [3.12].

Knowing the relationship between the on-state resistance and output capacitance of the semiconductor devices with the devices' blocking voltage rating, the next step towards deriving an extended converter figure of merit for hybrid Si/SiC switches is determining the power loss of the converter topology utilizing hybrid Si/SiC switches. Combining (3-7), (3-14), (3-18), and (3-19), the conduction and switching power loss of the converter can be rewritten as (3-20) and (3-21).

$$P_{cond} = I_{rms}^2 R_{eq}(U_B) = I_{rms}^2 \left(\frac{R_{on\_IGBT}(U_B) R_{on\_MOS}(U_B)}{R_{on\_IGBT}(U_B) + R_{on\_MOS}(U_B)} \right) \tag{3-20}$$

$$P_{sw} = f_{sw} U_{dc}^2 \cdot \left(C_{oss\_MOS}(U_B) + C_{oss\_IGBT}(U_B) \cdot e^{-\delta \cdot T_{off\_delay}} \right) + R_{on\_MOS}(U_B) \cdot T_{off\_delay} \cdot I_{rms}^2 \quad (3\text{-}21)$$

where f_{sw} is the switching frequency of the converter. Substituting the optimal gate turn off delay time in (3-16) that yields the lowest switching energy loss for the hybrid Si/SiC switches in to (3-21), the optimal switching power loss shown in (3-22) can be obtained for a converter utilizing hybrid Si/SiC switches.

$$P_{sw} = f_{sw} U_{dc}^2 \cdot \left(C_{oss\_MOS}(U_B) + \frac{C_{oss\_IGBT}(U_B)}{e^{\ln\left(\frac{R_{on\_MOS}(U_B) I_{rms}^2}{C_{oss\_IGBT}(U_B) U_{dc}^2}\right)}} \right) + R_{on\_MOS}(U_B) \cdot \frac{1}{\delta} \ln\left(\frac{R_{on\_MOS}(U_B) I_{rms}^2}{C_{oss\_IGBT}(U_B) U_{dc}^2} \right) \cdot I_{rms}^2 \quad (3\text{-}22)$$

From (3-20) and (3-22), we can observe the following points:

- The converter overall power loss increases with increasing equivalent on-resistance and equivalent output capacitance of the hybrid Si/SiC switches.
- The converter power loss depends on its switching frequency, dc bus voltage and output current. But the dc bus voltage and output current are fixed for specific application, not a degree freedom. The switching frequency of the converter on the other hand can be utilized for design optimization – when the switching frequency of the converter increases, its switching power loss increases [3.39], [3.40].
- When the ratio of the on-state resistance of the SiC MOSFET to the output capacitance of the Si IGBT ($R_{on\_MOS}(U_B)/ C_{oss\_IGBT}(U_B)$) increases, the first part of (3-22) decreases while the second part of (3-22) increases. However, the dc bus voltage of a converter is normally much larger than its current, hence the first part of (3-22) is much larger than the second part. Therefore, the converter switching power loss has an overall inverse relation with the ratio ($R_{on\_MOS}(U_B)/ C_{oss\_IGBT}(U_B)$).

Combining the above three points, an improved converter figure of merit accounting for the semiconductor device properties and converter topology properties can be derived for converter topologies employing hybrid Si/SiC switches. With the aim of maximizing the performance of the converter, a better hybrid Si/SiC switch combination would result in lower converter power loss. Hence, the converter figure of merit (C-FOM) shown in (3-23) can be derived.

$$\text{C-FOM} = \frac{1}{f_{\text{sw}} R_{\text{on,eq}} C_{\text{oss,eq}}} \left(\frac{R_{\text{on\_MOS}}(U_{\text{B}})}{C_{\text{oss\_IGBT}}(U_{\text{B}})} \right) \tag{3-23}$$

This converter figure of merit facilitates the design optimization of converter topologies utilizing hybrid Si/SiC switches by eliminating the need for a full converter electro-thermal power loss model to estimate the converter efficiency for different Si/SiC switch combinations and converter operating points.

3.4 Experimental Validation

The simplified switching energy loss model in (3-14) that represents the minimum hard-switching energy losses of the hybrid Si/SiC switches is first validated by experimentally measured switching energy losses. Figure 3-2 shows the comparison of the estimated minimum hard-switching energy losses and the measured switching energy losses of the hybrid Si/SiC switches for different gate turn off delay time values. For the hybrid Si/SiC switches, a 600 V, 30 A Si IGBT (IRGPC40S) and a 650 V, 20 A SiC MOSFET (SCT3080ALHRC11) are used. Two things can be observed from this figure. One, the switching energy loss of the Si IGBT decreases as the gate turn off delay time increases while the opposite happens for the SiC MOSFET. Two, the estimated switching energy loss of the Si IGBT and the SiC MOSFET are less than the actual measured switching energy losses. This is because (3-12) and (3-13) represent only the minimum hard-switching energy losses of the Si IGBT and the SiC MOSFET. The purpose of these simplified

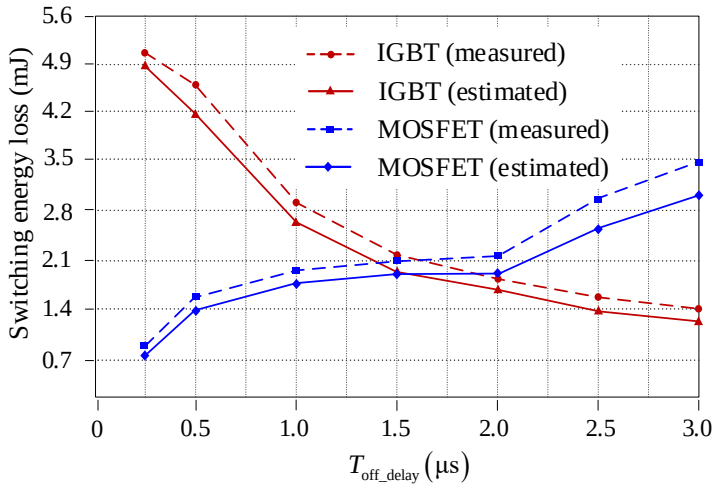

Figure 3-2 Comparison of measured and estimated minimum hard-switching energy loss for the hybrid Si/SiC switches.

switching energy loss models is to help derive a simplified device figure of merit for converter topologies employing hybrid Si/SiC switches to enable the comparison of various hybrid Si/SiC switch combinations for a specific application. It is not intended to derive a precise power loss model for hybrid Si/SiC switches which is rather covered in detail in [3.17] and [3.36]. The key thing to observe here is the trend between the estimated minimum hard-switching energy losses and the actual measured switching energy losses of the hybrid Si/SiC switches. The estimated minimum hard-switching energy losses of the hybrid Si/SiC switches follow a similar trend with the actual measured switching energy losses of these switches except a small offset between them. Hence, the simplified switching energy loss model is adequate for the sake of deriving device figure of merit to help perform a comparison between different hybrid Si/SiC switches devices for different converter topologies.

The dependency of the switching energy loss of the hybrid Si/SiC switches on the gate turn off delay time is also investigated experimentally. Figure 3-3 shows the measured switching energy losses of the hybrid Si/SiC switches for different gate turn off delay time values. As can be seen

from the figure, the total switching energy loss of the hybrid Si/SiC switches has almost a parabolic relationship with the gate turn off delay time.

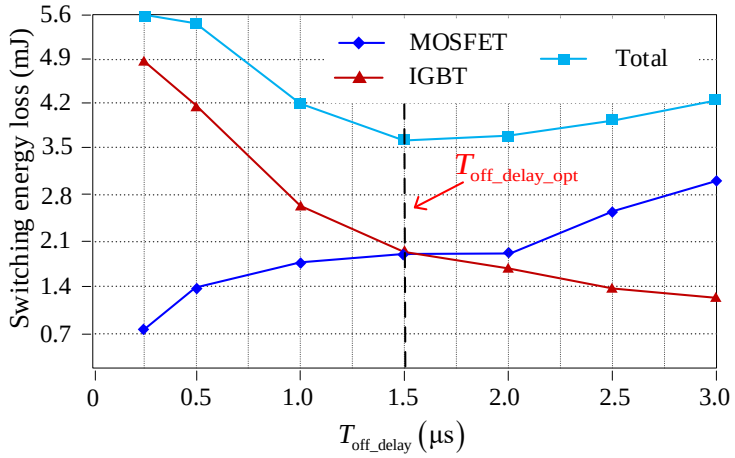

Figure 3-3 Switching energy loss dependency on gate turn-off delay time for hybrid Si/SiC switches.

To validate the accuracy of the C-FOM theory, the semiconductor device conduction and switching energy power loss models that are used to derive the device and the converter figure of merit are verified by measured experimental device power losses. The 10 kW, 480 V three-level ANPC inverter utilizing hybrid Si/SiC switches introduced in Chapter 2 is used for the experimental test. Table 3-1 shows the converter specifications for the experimental test. The Si/SiC gate control Option II (see Section 2.4.3.1) where both devices turn on simultaneously, but the Si IGBT turns off before the SiC MOSFET is used for the hybrid Si/SiC switches with a gate turn off delay time of 1.5 μs. As shown in Figure 3-3, this gate turn off delay time is the optimal value that yields the lowest switching energy loss for the hybrid Si/SiC switches.

The switching energy loss of the hybrid Si/SiC switches is measured using a double pulse test experiment for different load conditions. The experimental test is conducted at room temperature (T_j = 25 ºC), but switching energy losses hardly depend on the junction temperature of the

semiconductor devices [3.42]. Hence, this will not compromise the accuracy of the measurement for higher junction temperature values. Figure 3-4 shows comparison of the estimated switching energy losses (estimated using (3-14)) and the measured switching energy losses of the hybrid Si/SiC switches for different load conditions. As can be seen from the figure, the measured switching energy losses are higher than the estimated switching energy losses. This is because (3-14) represents only the minimum hard-switching energy losses of semiconductor devices neglecting the $V - I$ overlap losses. The difference between the measured and the estimated switching energy losses represents the $V - I$ overlap losses. These switching energy losses are dependent on many parameters such as gate voltage, gate resistance, and gate loop inductance [3.17], [3.36]. Hence, to simplify the switching energy loss modeling, these switching energy losses are not accounted for in (3-14), since the purpose of this switching energy loss model is not to accurately model the switching energy losses of semiconductor devices but rather to help derive a figure of merit that enables performance comparison between different semiconductor device and converter topology combinations. The important thing to note here is the measured and the estimated switching energy losses have a similar trend, therefore the switching energy loss model is acceptable for the purpose of relative performance comparison of different semiconductor devices.

Table 3-1 Converter specification.

Parameter	**Value**
Rated output power	10 kW
Dc-link voltage	800 V
Output voltage	480 V
Dc-link capacitor	350 μF
Switching frequency	50 kHz
Switches ($S_1 - S_4$)	IRGP4069DPBF
Si/SiC switches (S_5, S_6)	Si IGBT: IRGPC40S SiC MOS: SCT3080ALHRC

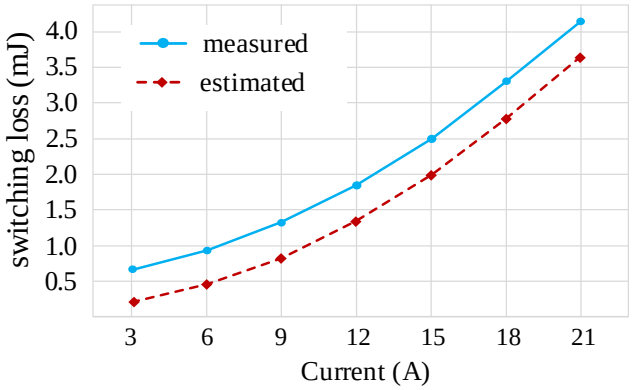

Figure 3-4 Comparison of measured and estimated minimum hard-switching energy losses for the hybrid Si/SiC switches.

Figure 3-5 shows a comparison of the estimated and measured efficiency of the converter for different load conditions. As can be seen in the figure, the estimated converter efficiency values are higher than the measured converter efficiency values. But again, the estimated and the measured converter efficiency values have a similar trend (with just small offset), so the semiconductor power loss model used to derive the device and converter figure of merit is acceptable. This semiconductor power loss model is also proved acceptable in [3.12] for the sake of deriving a figure of merit for semiconductor devices.

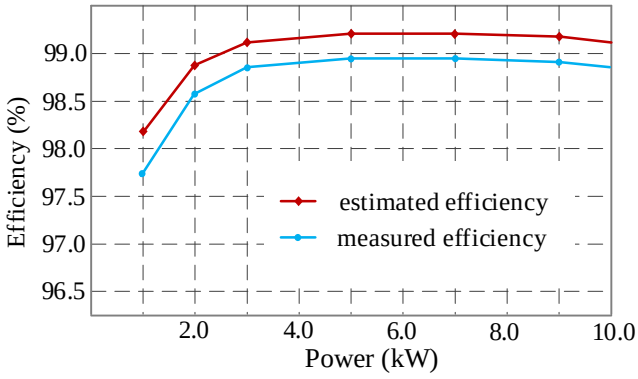

Figure 3-5 Comparison of measured and estimated converter efficiency.

3.5 Demonstration of the Applicability of the Proposed Figures of Merits

To demonstrate the applicability of the improved device figure of merit for hybrid Si/SiC switches, different Si/SiC device pairs that can be used for a 20-kW, 480 V ANPC inverter system (shown in Figure 3-6 (d)) are selected from commercially available devices. The devices are selected based on their current rating ratio (a smaller current rated SiC MOSFET, and a higher current rated Si IGBT are selected in different current rating proportions to meet the rated load current requirement). Table 3-2 shows list of the selected devices, their important device parameters and corresponding device figure of merits.

Table 3-2 D-FOM of selected hybrid Si/SiC switches for 10 kW ANPC inverter.

pair	Devices	R_{on}	C_{oss}	D-FOM
1	Si IGBT: STGW60V60DF	4.6 mΩ	280 pF	$7.2x10^{11}$
	SiC MOS: SCT3080ARC14	80 mΩ	39 pF	
2	Si IGBT: IXGH30N60C2D1	3.2 mΩ	140 pF	$1.9x10^{12}$
	SiC MOS: C3M0120065D	80 mΩ	35 pF	
3	Si IGBT: STGW45HF60WD	2.8 mΩ	260 pF	$1.2x10^{12}$
	SiC MOS: SCT2280KEC	280 mΩ	27 pF	

Pair 1 represents an Si/SiC current rating ratio of 80:20, pair 2 represents an Si/SiC current ratio of 70:30, and pair 3 represents an Si/SiC current ratio of 60:40. In [3.43], an Si/SiC current rating ratio optimization algorithm is presented ,and it is shown that when the current rating of the SiC MOSFET is reduced the power loss of the hybrid Si/SiC switches will also reduce. According to this, one would expect pair 1 to have the lowest power loss or the highest figure of merit. But the new hybrid Si/SiC switch device figure of merit reveals that pair 2 actually has the highest figure of merit or the lowest power loss of the three Si/SiC device pairs considered. This is because of the difference in the device parameters (on resistance and output capacitance) across devices of

different manufacturers or device generations due to the difference in packaging techniques and manufacturing process.

To similarly demonstrate the applicability of the proposed converter figure of merit, a 10 kW, 800 V dc bus, 480 V inverter system is considered. Two inverter topologies with two different semiconductor device configurations as shown in Figure 3-6 are considered for the application to assess the benefits of using hybrid Si/SiC switches for the different converter topologies. For two-level inverter topology, the SiC based configuration, Figure 3-6 (a), is proved to have better performance compared to its silicon counterpart [3.40]. Therefore, this inverter configuration is chosen for a performance comparison with a two-level topology utilizing hybrid Si/SiC switches shown in Figure 3-6 (b) [3.16]. Similarly, for the three-level inverter, the increasingly popular three-level ANPC inverter topology utilizing mixed Si IGBT and SiC MOSFET devices, Figure 3-6 (c), [3.44] is chosen. It uses a modulation strategy [3.45] that produces a group of low frequency switches commutating at fundamental line frequency (S_1 – S_4), and a group of high frequency

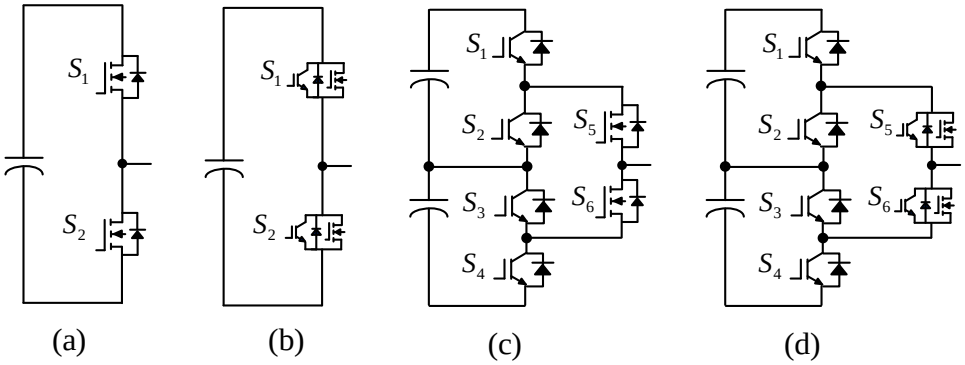

Figure 3-6 Topologies considered for comparison: (a) two-level SiC MOSFET inverter, (b) two-level hybrid Si/SiC switch inverter [3.16], (c) three-level mixed “Si+SiC” switch ANPC inverter [3.44], (d) three-level hybrid Si/SiC switch ANPC inverter [3.37].

switches commutating at carrier frequency (S_5 and S_6) hence enabling a mixed semiconductor device configuration. The hybrid Si/SiC switch based ANPC inverter topology, Figure 3-6 (d), recently proposed in [3.37] based on the same modulation strategy as the ANPC topology in Figure 3-6 (c) is also considered for the performance comparison.

For the non-hybrid switches (the switches in Figure 3-7 (a) and (c), and $S_1 – S_4$ in Figure 3-8 (d)), the device figure of merit (D-FOM) and the converter figure of merit (C-FOM) are calculated by using the on-state resistance and output capacitance of the single devices in (3-17) and (3-23) in place of the equivalent on-state resistance and equivalent output capacitance of the hybrid Si/SiC switches. In addition, the MOSFET on-state resistance to IGBT output capacitance ratio term ($R_{\text{on\_MOS}}(U_{\text{B}})/ C_{\text{oss\_IGBT}}(U_{\text{B}})$) in (3-23) is ignored for these switches. This ratio term models the effect of the gate turn off delay time on the switching power loss of the hybrid Si/SiC switches and is valid only for such kind of switches and gate control strategy.

Table 3-3 shows the semiconductor device parameters selected for the different converter topologies and their corresponding estimated device figure of merit (D-FOM) and converter figure of merit (C-FOM). Since the semiconductor devices in two-level inverter topologies need to block the full dc bus voltage, 1200 V devices are selected for these topologies. On the other hand, the semiconductor devices in three-level ANPC inverter topologies need to block only half of the dc bus voltage, hence 650 V devices are selected for these topologies. The power loss of semiconductor devices in converters also depends on the switching frequency of the converter. To make a fair semiconductor device power loss comparison between the two-level and three-level inverter topologies, the same switching frequency (50 kHz) at the output node is used for both type of inverter topologies. However, it is important to note that the effective switching frequency of

Table 3-3 Device parameters for C-FOM comparison of different converter topologies.

	Type	Part number	U_B (V)	R_{on} (mΩ)	C_{oss} (pF)	D-FOM	*C-FOM	C-FOM
2L VSC	SiC	NVHL040N120SC1	800	40	140	$1.31x10^{10}$	$2.01x10^{6}$	$2.01x10^{6}$
	Si/SiC	Si: IRGP30B120KD	800	3.4	165	$1.46x10^{10}$	$2.23\ x10^{6}$	$2.93\ x10^{6}$
		SiC: E3M0075120D	800	75	58			
3L ANPC	Si	IRGP4069DPBF	400	4.2	197	$1.34x10^{10}$	$4.61x10^{6}$	$3.21x10^{6}$ (Si+SiC)
	SiC	SCT3030ALGC11	400	40	245	$1.42x10^{10}$	$2.04x10^{6}$	
	Si/SiC	Si: IXGH30N60C2	400	3.2	140	$1.58x10^{10}$	$2.38x10^{6}$	$4.43x10^{6}$ (Si+Si/SiC)
		SiC: C3M0120065D	400	80	35			

*C-FOM represents the converter figure of merit if only one type of device is used for the converter. C-FOM on the other hand represents the combined converter figure of merit for the converter topologies using mixed semiconductor device configurations (Si IGBT + SiC MOSFET (Fig. 9 (c)), Si IGBT + Si/SiC switches (Fig. 9 (d))). C-FOM is calculated as the average of the *C-FOM of the devices the converter topology consists of.

three-level inverter topologies at the output node is twice the switching frequency of the individual switches [3.12], since these inverter topologies are a family of multilevel inverter topologies which have a frequency multiplication benefit at the output node.

Looking at the D-FOM of the semiconductor devices, the hybrid Si/SiC switches both in the two-level and three-level inverter topologies have higher D-FOM than the non-hybrid switches. Because of their parallel configuration, the equivalent on-state resistance of the hybrid Si/SiC switches is lower than that of the internal switches. But their equivalent output capacitance is higher than that of the internal switches. This shows that the effect of the on-state resistance of semiconductor devices (conduction power loss) is more dominant than the effect of the output capacitance of the semiconductor devices (switching power loss). This is however valid only for low switching frequency applications as in Baliga's figure of merit (BFOM) [3.5]. For high switching frequency applications, the semiconductor devices' switching power losses could be

more dominant than their conduction power losses. Therefore, D-FOM is not an accurate predictor of the performance of semiconductor devices for different converter applications. Another point to note regarding the D-FOM of the semiconductor devices is the semiconductor devices for a three-level inverter topology have higher D-FOM than those for a two-level inverter topology because of the lower blocking voltage requirement of three-level inverter topologies.

With respect to the *C-FOM of the semiconductor devices, we can see that the *C-FOM of the three-level inverter devices is higher than that of the two-level inverter devices. This is again because of the lower blocking voltage requirement and higher effective switching frequency of three-level inverter topologies. The effective switching frequency of three-level inverter topologies at the output node is twice the switching frequency of the semiconductor devices, while it is the same as the switching frequency of the semiconductor devices for two-level inverter topologies [3.12]. Therefore, despite the two topologies having the same switching frequency at the output node, the semiconductor devices in the three-level inverter topology have half the switching frequency of the semiconductor devices in two-level inverter topology. Moreover, the hybrid Si/SiC switches have higher *C-FOM than SiC MOSFETs both for two-level and three-level inverter topologies. This is because of the lower power loss of hybrid Si/SiC switches compared to SiC MOSFETs.

With respect to the C-FOM of the semiconductor devices, two important points can be observed. The first point is, the C-FOM of the two-level inverter increases by about 50 percent, and the C-FOM of the three-level ANPC inverter increases by about 40 percent when the SiC MOSFETs are replaced by hybrid Si/SiC switches. This indicates about 50 percent power loss reduction for the two-level inverter and about 40 percent power loss reduction for the three-level ANPC inverter. This agrees with the performance improvements of hybrid Si/SiC switches for

two-level and three-level ANPC inverters reported in [3.16] and [3.37]. The second point to note is, the C-FOM of the three-level ANPC inverter is higher than the C-FOM of the two-level inverter (about 60 percent higher for the ANPC inverter utilizing hybrid Si/SiC switches for the high frequency switches (Figure 3-9 (d)) and about 40 percent higher for the ANPC inverter using SiC MOSFETs for the high frequency switches (Figure 3-10 (c)) compared to the SiC MOSFET based two-level inverter). This shows about 50 percent power loss reduction on the average for the three-level ANPC inverter compared to the two-level inverter – very close agreement with the findings of [3.12] and [3.40]. In these articles, it is reported that three-level inverter topologies in general have about 55 percent lower semiconductor power loss compared to two-level inverter topologies keeping the same output filter stress (same switching frequency at the output node).

3.6 Conclusion

This chapter presented a new converter figure of merit for hybrid Si/SiC switches that combines the high-level properties of the semiconductor devices such as on-state resistance and output capacitance and the converter topology operating properties such as blocking voltage and switching frequency. The proposed converter figure of merit (C-FOM) serves two benefits: facilitating the performance comparison of different Si/SiC switch combinations for a specific converter topology and facilitating performance comparison between different converter topology and semiconductor device combinations. The converter figure of merit is derived based on a simplified power loss model accounting for only the conduction and the minimum hard-switching energy losses of the semiconductor devices. However, this does not compromise the accuracy of the proposed converter figure of merit. The power loss model is validated by experiment – the estimated and measured switching energy losses have a similar trend despite a small offset, hence the power loss model is

acceptable for relative performance comparison between different semiconductor device and converter topology combinations.

The applicability of the proposed converter figure of merit (C-FOM) is demonstrated using two-level and three-level inverter topologies utilizing different semiconductor device configurations. The C-FOM showed that hybrid Si/SiC switches have higher performance in terms of reducing semiconductor device power loss compared to SiC MOSFETs both for two-level and three-level inverter topologies. In addition, the C-FOM showed that three-level inverter topologies have about 50 percent lower power loss when compared to two-level inverter topologies keeping the same output filter stress, a benefit which is validated by many published literatures.

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CHAPTER 4

THE ASSYMETRIC ALTERNATE ARM CONVERTER (AAAC) TOPOLOGY: A NEW MULTILEVEL CONVERTER TOPOLOGY FOR HVDC APPLICATIONS

4.1 Introduction

Several research and development activities have been performed to improve the power transfer capability of HVDC transmission systems and to reduce their associated cost, power loss and converter footprint. Various converter topologies and control strategies have been introduced in this effort. Current Source Converter (CSC) topologies [4.1], [4.2] are well established and more efficient for HVDC applications. However, they have some drawbacks such as limited active and reactive power control capability, lack of black start capability (ability to support ac networks containing only passive loads) and inability to support Multi-terminal DC (MTDC) applications [4.3] – [4.5]. Voltage source converters (VSCs) on the other hand eliminate the drawbacks of current source converters and become preferable for HVDC applications. These converter topologies have lower converter footprint (requiring minimal space for converter installation), full active and reactive power control capability and black start capability. Therefore, they are suitable for applications where space is a critical design constraint such as offshore wind energy generation plants and today's diversified energy resource power systems where quick active and reactive power control capability is mandatory to provide fast response to power transients and faults. In addition, in power systems containing bulk wind energy generation plants, black start capability (ability to start without reactive power support) is a necessity to enable wind farms starting from parking without drawing excessive reactive power from the grid. These and other factors make voltage source converter topologies key to the advancement of renewable energy generation and transmission systems.

Several voltage source converter topologies have been proposed for HVDC applications [4.6] – [4.8], but the most widely used topology is the Modular Multilevel Converter (MMC) topology [4.9], [4.10] proposed in 1998 for STATCOM applications and in 2003 for HVDC applications. This topology replaces the series connected switches in each arm of the two-level voltage source converter topology by stack of half-bridge submodules consisting of two switches and a charged capacitor. Therefore, it is modular and scalable in structure. In addition, it provides higher converter efficiency compared to cascaded two-level and three-level voltage source converter topologies since it does not rely on high frequency modulation for its output voltage synthesis [4.11]. However, it has some drawbacks that hamper its large-scale utilization for high voltage applications. Because of its distributed sub-module capacitors, it requires complex control strategy to regulate the submodule capacitor voltages and the circulating current between the two converter arms [4.12]. In addition, the submodule capacitors are large and bulky increasing the converter footprint and cost.

Hybrid voltage source converter topologies that combine the features of modular multilevel converter topologies and other voltage source converter topologies also have been proposed to improve the waveform fidelity of modular multilevel converter topologies. In [4.13], a hybrid combination of soft switched H-bridge cells and hard switched MMC cells is proposed to reduce the current stress of the MMC cells and to improve the converter efficiency. The H-bridge cells are operating at fundamental line frequency; therefore, they have very low switching loss. In [4.14], [4.15], a new hybrid voltage source converter topology termed as the Alternate Arm Converter (AAC) is proposed which is a hybrid topology between the modular multilevel converter topology and two-level voltage source converter topology. Like the modular multilevel converter, it is modular and scalable in structure providing easy extension to higher voltage and power levels. But it retains the operation of two-level voltage source inverters through the director switches in each

arm. The upper and lower arm submodules alternatively conduct the ac current regulated by the director switches hence it can switch the dc bus in reverse polarity. In [4.16], a series hybrid converter topology consisting of three-level T-type converter topology and modular multilevel converter topology is proposed to reduce the semiconductor loss of the converter. The three-level converter operates at fundamental line frequency and serves as input voltage polarity selector while the MMC converter connected in series with the three-level converter generates multilevel output voltage. All the above topologies have one common drawback: they have higher number of devices due to the additional switches they use in conjunction with the conventional MMC structure. Therefore, they have higher converter footprint and cost.

In an effort to reduce the device count and footprint of hybrid voltage source converter topologies, asymmetric alternate arm converter topologies consisting of strings of diodes/IGBTs in the upper converter arms and chain of submodules in the lower converter arms are also proposed [4.17], [4.18]. These topologies reduce the number of submodules hence significantly reduce the converter cost and footprint compared to the conventional hybrid voltage source alternate arm converter topologies that contain chain of submodules in both converter arms. This chapter presents a new voltage source converter topology with reduced submodule (cell) count which belongs to the family of asymmetric alternate arm hybrid voltage source converter topologies [4.19], [4.20]. It consists of switching blocks (IGBTs/MOSFETs) in its upper converter arms and cascaded half-bridge cells in its lower converter arms. Compared to other similar voltage source converter topologies for HVDC application, the proposed converter topology has lower number of submodules hence it has lower converter footprint and cost. In addition, it has lower number of switches in the current conduction path and lower semiconductor device blocking voltage

requirement. Therefore, it can provide higher converter efficiency compared to other voltage source converter topologies with similar structure and operation.

4.2 Topology Structure and Operation

The proposed hybrid voltage source converter topology is shown in Figure 4-1. It consists of switch blocks in the upper converter arms and cascaded half-bridge cells in the lower converter arms. The type of switches required for the upper converter arms depends on the intended functionality of the converter. If the converter is to be used as an HVDC rectifier, the power flow will be unidirectional from the ac input to the dc output. Therefore, line commutated devices such as diodes and thyristors can be used. However, if bidirectional power flow is required, active switches such as IGBTs and MOSFETs must be used. The cascaded half-bridge cells in the lower converter arms contain two switches and one capacitor. Table 4-1 shows the switching states of this submodule structure. The two switches (S_1 and S_2) switch in complementary fashion. When the switch (S_1) is ON and the switch (S_2) is OFF, the output voltage of the submodule cell will be equal to the cell capacitor voltage (E). On the other hand, when the switch (S_1) is OFF and the switch (S_2) is ON, the output voltage of the cell will be zero. Therefore, this submodule structure can produce two output voltage levels (0 and E). By cascading multiple half-bridge submodules together, a multilevel output voltage can be achieved like in the case of the modular multilevel converter topology to achieve higher voltage levels.

Table 4-1 Switching state of half-bridge submodule.

S_1	S_2	Output
0	1	0
1	0	E

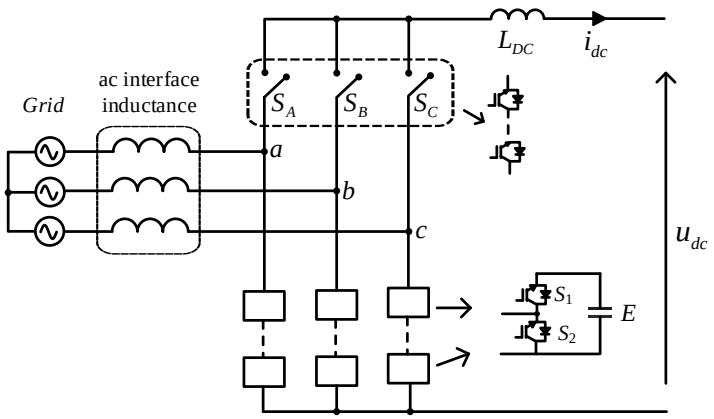

Figure 4-1 Proposed hybrid voltage source converter topology.

The proposed converter topology has three operation modes determined by the relative magnitude of the input line-to-neutral voltages as shown in Figure 4-2. The first operation mode (M_1) is represented by the duration when the phase A line-to-neutral voltage (u_{an}) is greater than the other two line-to-neutral phase voltages (u_{bn} and u_{cn}). During this operation mode, the upper arm switches in Phase A (S_A) are conducting the dc current while the upper arm switches in the other two phases are off. The voltage across the lower arm submodules and the current through them can be derived as shown in (4-1) using Kirchhoff's voltage and current laws from the equivalent circuit of the converter during this operation mode as shown in Figure 4-3.

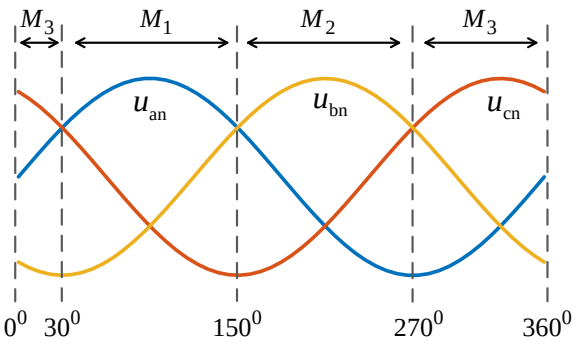

Figure 4-2 Conduction intervals for upper arm switches.

$$\begin{cases} u_{\text{arm}}^{\text{a}} = u_{\text{dc}} \\ u_{\text{arm}}^{\text{b}} = u_{\text{dc}} - u_{\text{ab}} \\ u_{\text{arm}}^{\text{c}} = u_{\text{dc}} - u_{\text{ac}} \end{cases}, \quad \begin{cases} i_{\text{arm}}^{\text{a}} = i_{\text{a}} - i_{\text{dc}} \\ i_{\text{arm}}^{\text{b}} = i_{\text{b}} \\ i_{\text{arm}}^{\text{c}} = i_{\text{c}} \end{cases} \tag{4-1}$$

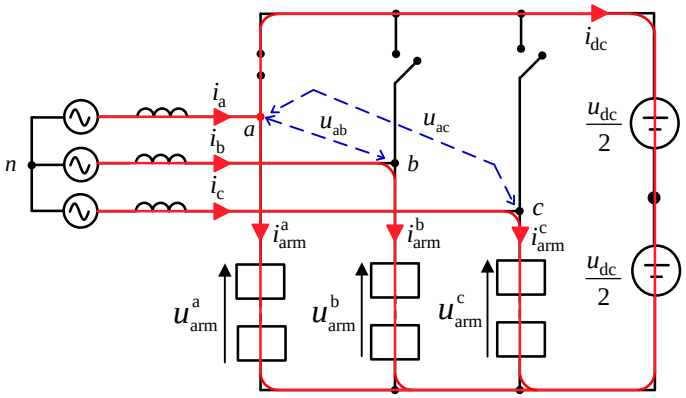

Figure 4-3 Converter equivalent circuit during operation mode I.

The second operation mode (M_2) is represented by the duration where the phase B line-to-neutral voltage (u_{bn}) is greater than the other two line-to-neutral phase voltages (u_{an} and u_{cn}). During this operation mode the upper arm switches in Phase B (S_{B}) are conducting the dc current while the upper arm switches in the other two phases are off. The equivalent circuit of the converter during this operation mode is shown in Figure 4-4. The output voltages of the lower arm submodules and the current through them during this operation mode is given by (4-2).

$$\begin{cases} u_{\text{arm}}^{\text{a}} = u_{\text{dc}} + u_{\text{ab}} \\ u_{\text{arm}}^{\text{b}} = u_{\text{dc}} \\ u_{\text{arm}}^{\text{c}} = u_{\text{dc}} - u_{\text{bc}} \end{cases}, \quad \begin{cases} i_{\text{arm}}^{\text{a}} = i_{\text{a}} \\ i_{\text{arm}}^{\text{b}} = i_{\text{b}} - i_{\text{dc}} \\ i_{\text{arm}}^{\text{c}} = i_{\text{c}} \end{cases} \tag{4-2}$$

The third operation mode (M_3) is represented by the duration where the phase C line-to-neutral voltage (u_{cn}) is greater than the other two line-to-neutral phase voltages (u_{an} and u_{bn}). During this operation mode, the upper arm switches in Phase C (S_{C}) are conducting the dc current while the upper arm switches in the other two phases are off. Figure 4-5 shows the equivalent circuit of the

converter during this operation mode. From the equivalent circuit of the converter, the output voltages and currents of the lower arm stack of submodules can be expressed as in (4-3).

$$\begin{cases} u_{\text{arm}}^{\text{a}} = u_{\text{dc}} + u_{\text{ac}} \\ u_{\text{arm}}^{\text{b}} = u_{\text{dc}} + u_{\text{bc}} \\ u_{\text{arm}}^{\text{c}} = u_{\text{dc}} \end{cases}, \quad \begin{cases} i_{\text{arm}}^{\text{a}} = i_{\text{a}} \\ i_{\text{arm}}^{\text{b}} = i_{\text{b}} \\ i_{\text{arm}}^{\text{c}} = i_{\text{c}} - i_{\text{dc}} \end{cases} \tag{4-3}$$

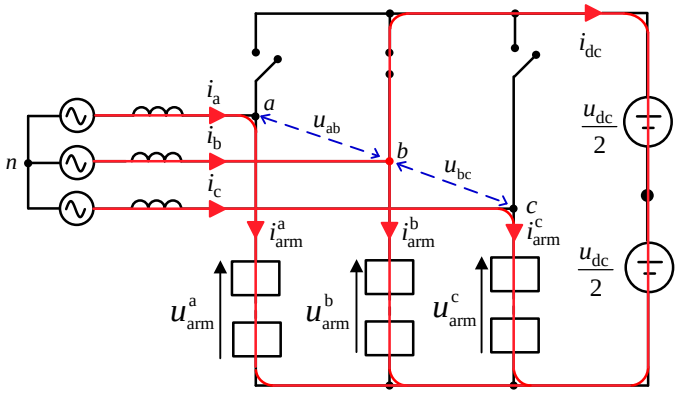

Figure 4-4 Converter equivalent circuit during operation mode II.

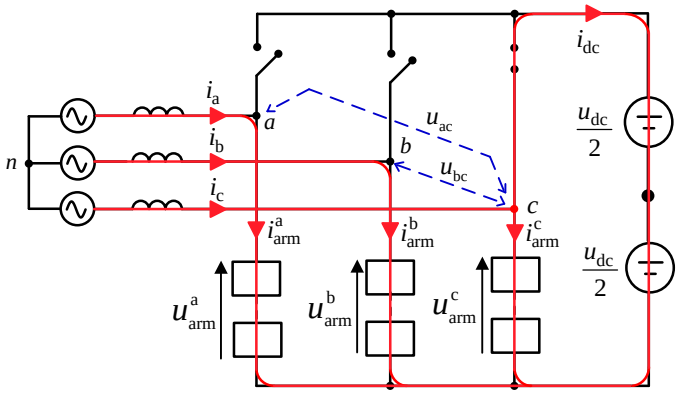

Figure 4-5 Converter equivalent circuit during operation mode III.

Generally, only one of the three upper arm switching blocks are conducting the dc current during each operation modes; the other two upper arm switch blocks are off. In addition, each of the upper arm switching blocks are conducting for one-third of the fundamental line period to maintain energy balance between the converter phase legs.

4.3 Modulation and Control Strategy

The overall control strategy of the proposed converter topology is shown in Figure 4-6. The ac side control regulates the power exchange between the ac network and the converter while the dc side control regulates the power exchange between the converter and the dc network. The carrier sorting and rotation scheme on the other hand ensures capacitor voltage balancing for the converter lower arm submodules.

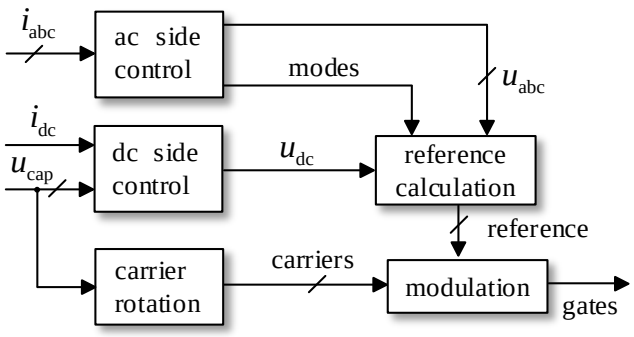

Figure 4-6 Overall converter control strategy.

4.3.1 Ac Side Control Strategy

This control part regulates the input ac currents to their reference values. The conventional synchronous reference frame voltage orientated grid current control strategy as shown in Figure 4-7 [4.22], [4.23] is used to achieve this control task. The current controller is designed based on the relationship between the ac input voltages and currents of the converter in synchronous reference frame as shown in (4-4).

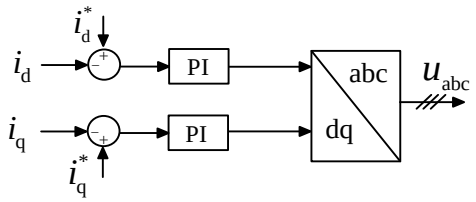

Figure 4-7 Ac side converter control strategy.

$$\begin{bmatrix} u_{\mathrm{d}} \\ u_{\mathrm{q}} \end{bmatrix} = L_{\mathrm{ac}} \frac{d}{dt} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} + R_{\mathrm{ac}} \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \end{bmatrix} + \omega L_{\mathrm{ac}} \begin{bmatrix} -i_{\mathrm{q}} \\ i_{\mathrm{d}} \end{bmatrix} + \begin{bmatrix} e_{\mathrm{d}} \\ e_{\mathrm{q}} \end{bmatrix} \tag{4-4}$$

where:

- u_{d} and u_{q} are the d-axis and q-axis components of the converter input voltages.
- i_{d} and i_{q} are the d-axis and q-axis components of the converter input currents.
- e_{d} and e_{q} are the ac grid voltage feedforward terms to compensate grid voltage drop.
- L_{ac} and R_{ac} are the equivalent inductance and resistance of the ac interface inductors.
- ω is the ac grid angular frequency.

The controller parameters are designed based on the plant transfer function shown in (4-5). The d-axis and q-axis current references are calculated from the synchronous reference frame instantaneous power equations as shown in (4-6). From the output voltages of the ac side control, the three converter operation modes are determined based on the relative magnitude of the line-to-neutral values as shown in Table 4-2.

$$\frac{i(s)}{u(s)} = \frac{1}{R_{\mathrm{ac}} + L_{\mathrm{ac}} s} \tag{4-5}$$

$$\begin{cases} P = \frac{3}{2}\left(u_{\mathrm{d}} i_{\mathrm{d}} + u_{\mathrm{q}} i_{\mathrm{q}}\right) \\ Q = \frac{3}{2}\left(u_{\mathrm{q}} i_{\mathrm{d}} - u_{\mathrm{d}} i_{\mathrm{q}}\right) \end{cases} \tag{4-6}$$

Table 4-2 Determination of the Converter Operation Modes.

Mode	Conducting phase	Condition
1	Phase A	($u_{\mathrm{an}} > u_{\mathrm{bn}}$) and ($u_{\mathrm{an}} > u_{\mathrm{cn}}$)
2	Phase B	($u_{\mathrm{bn}} > u_{\mathrm{an}}$) and ($u_{\mathrm{bn}} > u_{\mathrm{cn}}$)
3	Phase C	($u_{\mathrm{cn}} > u_{\mathrm{an}}$) and ($u_{\mathrm{cn}} > u_{\mathrm{bn}}$)

4.3.2 Dc Side Control Strategy

The dc side control part regulates the total energy of the converter to its nominal value to ensure the converter is not sourcing or absorbing any net energy in order to maintain the power balance between the ac network and dc network. Figure 4-8 shows block diagram of the dc side control strategy. The energy of the converter is calculated from the measured submodule capacitor voltages and is compared with its nominal value. The energy difference is compensated using a PI controller designed according to (4-7) – (4-10).

$$P_{ac} = P_{dc} \tag{4-7}$$

$$\frac{dw_c(t)}{dt} = u_{dc} \cdot i_{dc}(t) \tag{4-8}$$

$$\frac{w_c(s)}{i_{dc}(s)} = \frac{u_{dc}}{s} \tag{4-9}$$

$$\frac{i_{dc}(s)}{u_{offset}(s)} = \frac{1}{R_{dc} + L_{dc}s} \tag{4-10}$$

where P_{ac} and P_{dc} are the input ac power and output dc power of the converter, w_c is the converter energy, u_{dc} and i_{dc} are the output dc voltage and current of the converter, R_{dc} and L_{dc} are the equivalent resistance and inductance of the output inductance.

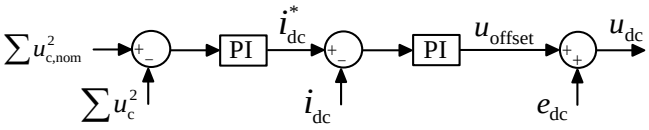

Figure 4-8 Converter energy and output dc current control strategy.

The converter energy control loop produces current reference for the subsequent dc current control loop. The dc current control loop then produces an offset voltage (u_{offset}) that needs to be added to the nominal dc output voltage (e_{dc}) to maintain the power balance between the ac network and dc network.

The reference voltages for the converter modulation are then calculated from the outputs of the ac side and dc side control loops according to (4-1) – (4-3) as shown in Table 4-3. When the upper arm switches are conducting, the corresponding converter lower arm submodules need to produce a voltage equal to the output dc output voltage. Therefore, the reference signal should be equal to the output dc voltage during this period. When the upper arm switches are not conducting, the corresponding lower arm submodules need to produce a voltage equal to the difference of the output dc voltage and the line-to-line voltage between the corresponding phase and the conducting phase. Therefore, the reference signal will be equal to the difference between the output dc voltage and the line-to- line voltage between the respective phase and the conducting phase during this period.

Table 4-3 Reference Voltages for Converter Modulation.

Mode	$\boldsymbol{u}^{\mathbf{a}}_{\mathbf{m}}$	$\boldsymbol{u}^{\mathbf{b}}_{\mathbf{m}}$	$\boldsymbol{u}^{\mathbf{c}}_{\mathbf{m}}$
1	u_{dc}	$u_{\mathrm{dc}}+u_{\mathrm{ab}}$	$u_{\mathrm{dc}}+u_{\mathrm{ac}}$
2	$u_{\mathrm{dc}}-u_{\mathrm{ab}}$	u_{dc}	$u_{\mathrm{dc}}+u_{\mathrm{bc}}$
3	$u_{\mathrm{dc}}-u_{\mathrm{ac}}$	$u_{\mathrm{dc}}-u_{\mathrm{bc}}$	u_{dc}

4.3.3 Modulation Strategy

There are two types of carrier-based sinusoidal pulse width modulation schemes for multilevel converters: phase-shifted carrier modulation scheme and level-shifted carrier modulation scheme [4.24]. In phase-shifted carrier modulation scheme shown in Figure 4-9 (a), the triangular carrier signals have the same peak-to-peak amplitude and frequency, but they are horizontally shifted by a phase-shift angle of ($360^{o}/(m$-1)) degrees. Since the PWM signals produced by this modulation scheme have equal effective duty ratio, it has intrinsic voltage balancing capability for multilevel

converter topologies constituting cascaded submodules [4.25]. However, it has lower waveform fidelity (higher output current harmonic distortion).

In level shifted sinusoidal pulse width modulation, the triangular carrier signals are vertically displaced as shown in Figure 4-9 (b). However, they have the same frequency and peak-to-peak amplitude. Depending on the phase-shift between the carriers, this multicarrier modulation scheme can be subcategorized into three: In-phase Disposition (IPD), where all carriers are in phase with each other; (b) Alternative Phase Opposite Disposition (APOD), where all carriers are alternatively in opposite disposition with each other; and (c) Phase Opposite Disposition (POD), where all carriers above the zero reference are in phase with each other but in opposition with those below the zero reference. The IPD is however the most preferable due to its best harmonic profile compared to the other two level shifted multicarrier modulation schemes [4.26].

Level-shifted carrier modulation however has a problem of submodule capacitor voltage imbalance [4.27]. In this modulation scheme, the bottommost triangular carrier signal produces a gate signal with the highest duty ratio while the topmost triangular carrier signal produces a gate signal with the lowest duty ratio. Therefore, when this modulation scheme is used, the submodule capacitors will have unequal charging and discharging times. The submodule which the bottommost triangular carrier signal is assigned to will have the longest charging and discharging time while the submodule which the topmost triangular carrier signal is assigned to will have the quickest charging and discharging time. Therefore, the submodule capacitor voltages will diverge overtime. Unbalanced capacitor voltage deteriorates the waveform fidelity of the converter output voltages and currents and results in unbalanced voltage stress on the semiconductor devices [4.28].

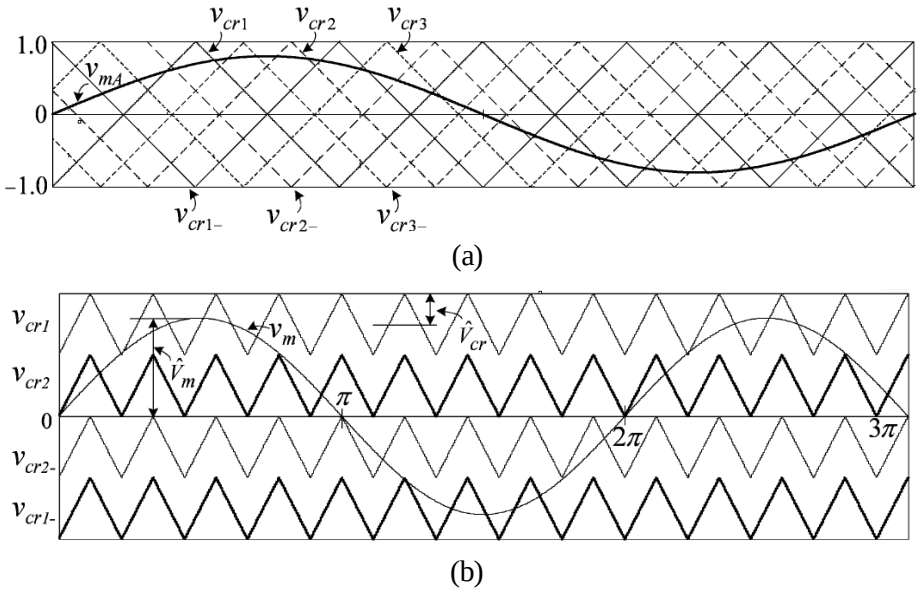

Figure 4-9 Multicarrier modulation strategies: (a) phase shifted carrier modulation, (b) level shifted carrier modulation strategies.

4.3.4 Submodule Capacitor Voltage Balancing Strategy

Submodule capacitor voltage balancing is achieved by the well-known submodule selection method shown Figure 4-10 during the transition between two output voltage levels [4.29], [4.30]. When the arm current is in charging direction and one submodule is needed to be added to the arm, the submodule with the lowest voltage is added. On the other hand, when one submodule is needed to be removed from the arm and the arm current is in charging direction, the submodule with the highest voltage is removed. The reverse action is taken when the arm current is in discharging direction. When one submodule is needed to be added to the arm, the submodule with the highest voltage is added while the submodule with the lowest voltages is removed when one submodule is needed to be removed.

This submodule capacitor voltage balancing strategy is realized through carrier sorting and rotation algorithm. The submodule capacitor voltages are measured and then sorted in ascending or

descending order depending on the direction of the arm current. Based on the precedence of the sorted submodule capacitor voltages, submodule indices indicating the virtual locations of the submodules within the converter arm are assigned. Carrier signals are then assigned to the submodules based on the indices of the submodules and the direction of the submodule capacitors current. When the submodule capacitors are charging, the carrier signal which produces the highest duty ratio (the bottommost carrier signal) will be assigned to the submodule with the lowest voltage and the carrier signal which produces lowest duty ratio (the topmost carrier signal) will be assigned to the submodule with the highest voltage. On the other hand, when the submodule capacitors are discharging, the carrier signal which produces the lowest duty ratio (the topmost carrier signal) will be assigned to the submodule with the lowest voltage and the carrier signal which produces the highest duty ratio (the bottommost carrier signal) will be assigned to the sub-module with the highest voltage. This ensures the submodules in each phase have a similar average duty over a period of time hence it equally distributes capacitor voltage deviations among the submodules.

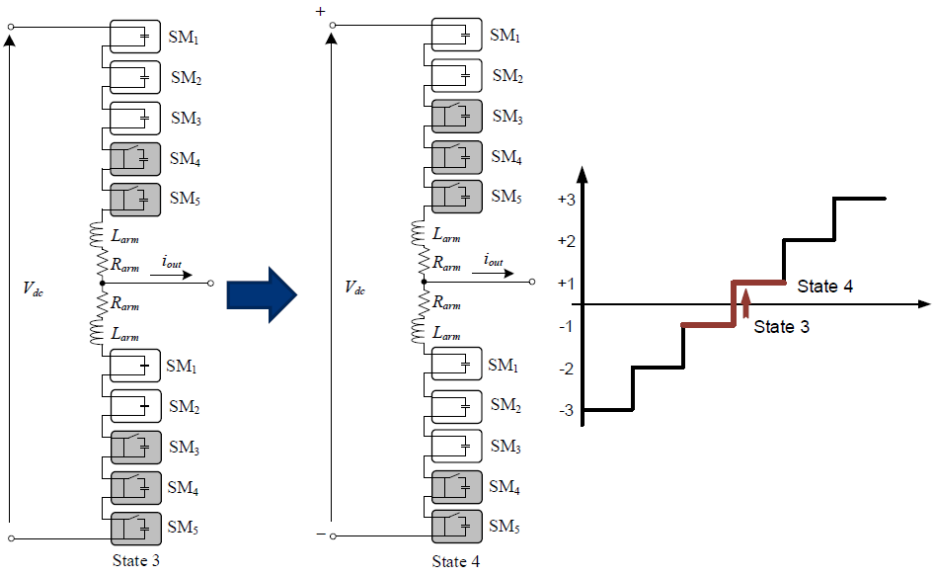

Figure 4-10 Sorting and rotation algorithm for submodule capacitor voltage balancing.

4.4 Converter Dimensioning

4.4.1 Number of Devices

Similar to MMC, the lower converter arm chain-link cells in the proposed VSC converter need to support the dc link voltage at all times. Therefore, the number of submodules (N_{SM}) required for a given dc-link voltage (V_{dc}) can be calculated as in (4-11).

$$N_{SM} = 3\left(\frac{V_{dc}}{V_{SM}}\right) \tag{4-11}$$

where V_{SM} is the rated voltage of the submodules which depends on the available rating of the semiconductor devices and submodule capacitors.

The upper arm switches are only responsible for switching conduction of the dc current from one converter phase to another. Therefore, the maximum blocking voltage requirement of the upper arm switches is determined by the peak ac voltage of the converter. Since the minimum voltage of the converter arm is the difference between the dc output voltage and the adjacent line-to-line ac input voltage as shown in (4-1) – (4-3), the maximum ac voltage of the converter will be

$$\hat{V}_{ac} = \frac{V_{dc}}{\sqrt{3}} \tag{4-12}$$

Since there are two switches in each half-bridge submodules, the number of active switches (with antiparallel diodes) required for the proposed VSC converter then can be calculated as (4-13) considering the total number of half-bridge submodules in the lower converter arms and the maximum blocking voltage requirement of the upper arm switches. The number of switches in the converter upper arms depends on the upper arm blocking voltage requirement and the blocking voltage of the submodules (switches).

$$N_{SW} = 6\left(\frac{V_{dc}}{V_{SM}}\right) + 3\left(\frac{V_{dc}}{\sqrt{3}V_{SM}}\right) = \left(6 + \frac{3}{\sqrt{3}}\right) N_{SM} \tag{4-13}$$

The number of submodule capacitors required for the proposed voltage source converter is equal to the number of submodules in the lower arms of the converter.

4.4.2 Submodule Capacitor Sizing

The minimum capacitance of the submodule capacitors can be determined using (4-14) based on the worst-case energy perturbation method [4.31].

$$C_{\mathrm{SM}} = \frac{2\Delta E_{\mathrm{arm}}}{N_{\mathrm{SM}}\Delta V_{\mathrm{SM}}^2} \tag{4-14}$$

where ΔE_{arm} is the worst-case converter arm energy deviation, and ΔV_{SM} is the allowed voltage deviation of the submodules.

The converter arm energy deviation is determined by ideal circuit simulation where the converter lower arm submodule stacks are represented by a controlled voltage source given by (4-1) – (4-3). In Chapter 5, a simplified arm energy analytical expression will be derived. The converter arm energy is estimated by integrating the product of the arm voltage and arm current. Figure 4-11 shows the ideal converter arm energy for the converter system shown in Table 4-4. The minimum submodule capacitance then can be calculated from the converter arm energy deviation (ΔE_{arm}) and the allowed submodule capacitor voltage deviation (ΔV_{SM}) using (4-14).

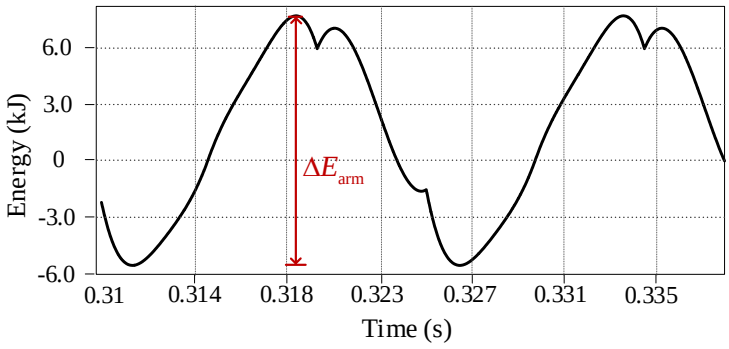

Figure 4-11 Simulated converter arm energy using ideal circuit simulation.

4.5 Simulation and Experimental Results

The operation of the proposed hybrid voltage source converter topology and the associated control strategy that regulates the power exchange between the ac/dc network and the proposed converter is investigated in MATLAB/SIMULINK simulation. The specification of the simulation setup is as shown in Table 4-4. An ac interface reactor and transformer leakage inductance of 12% of the nominal impedance is used for the simulation which is the typical value for VSC converters in HVDC applications [4.32]. The number of submodules required for the lower arms of the converter is calculated using (4-11). Four submodules are required in each lower arm of the converter for this HVDC system. The size of submodule capacitors is determined using (4-14) for the worst-case power factor value of 0 (full reactive power processing). The worst-case power factor value is the value that produces the largest energy deviation for the stacks of submodules in the lower arm of the converter (this is elaborated in Chapter 5).

Table 4-4 Specification for Performance Comparison.

Parameter	**Value**
rated Power	1 MW
dc bus voltage	6.0 kV
ac voltage, line to line	3.3 kV
nominal submodule voltage	1.5 kV
switching frequency	3 kHz
submodule capacitor	4.5 mF
ac interface inductor	3.5 mH
dc interface inductor	6.5 mH
switching device (active)	FZ400R17KE4
switching device (diode)	BYM600A170DN2

Figure 4-12 shows the control (modulating) signals of the converter and the current through the upper and lower arm switches. When the upper arm switches are conducting, the lower arm

submodules need to produce a voltage equal to the dc bus voltage. On the other hand, when the upper arm switches are not conducting, the lower arm submodules need to produce a voltage equal to the difference of the dc output voltage and the line-to-line voltage between the corresponding phase and the conducting phase. The upper arm switches are alternatively conducting the dc current producing three operation modes for the converter. Figure 4-13 shows the simulation results of the converter input ac currents, the converter phase and phase-to-phase voltages and the converter output dc current waveforms.

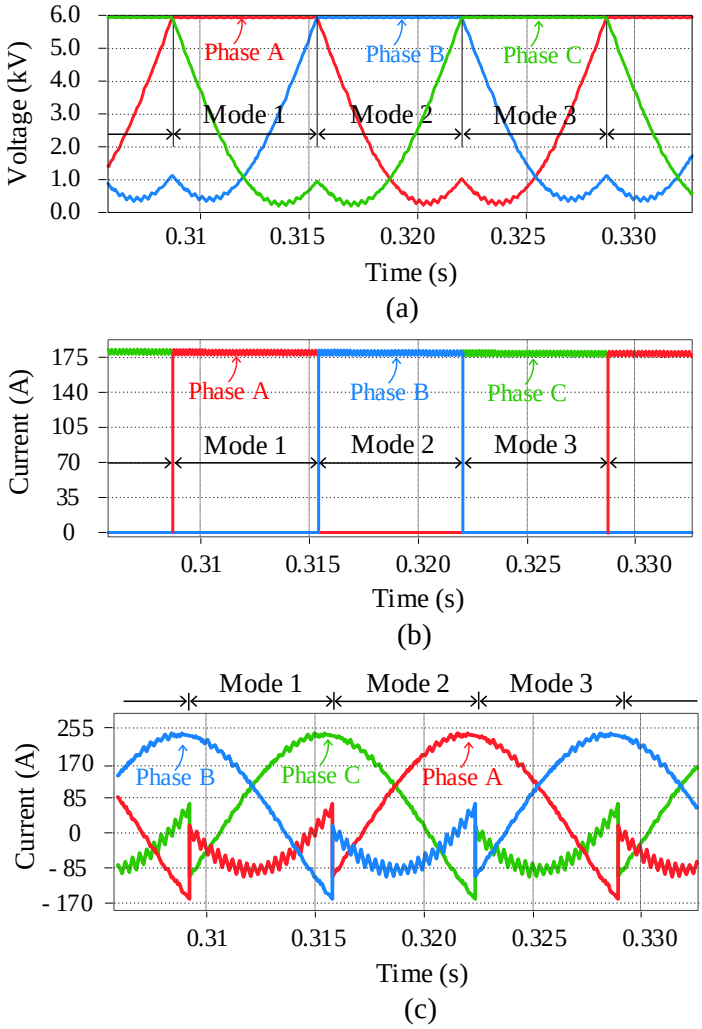

Figure 4-12 (a) converter modulating signals, (b) current through the upper converter arms, (c) current through the lower converter arms.

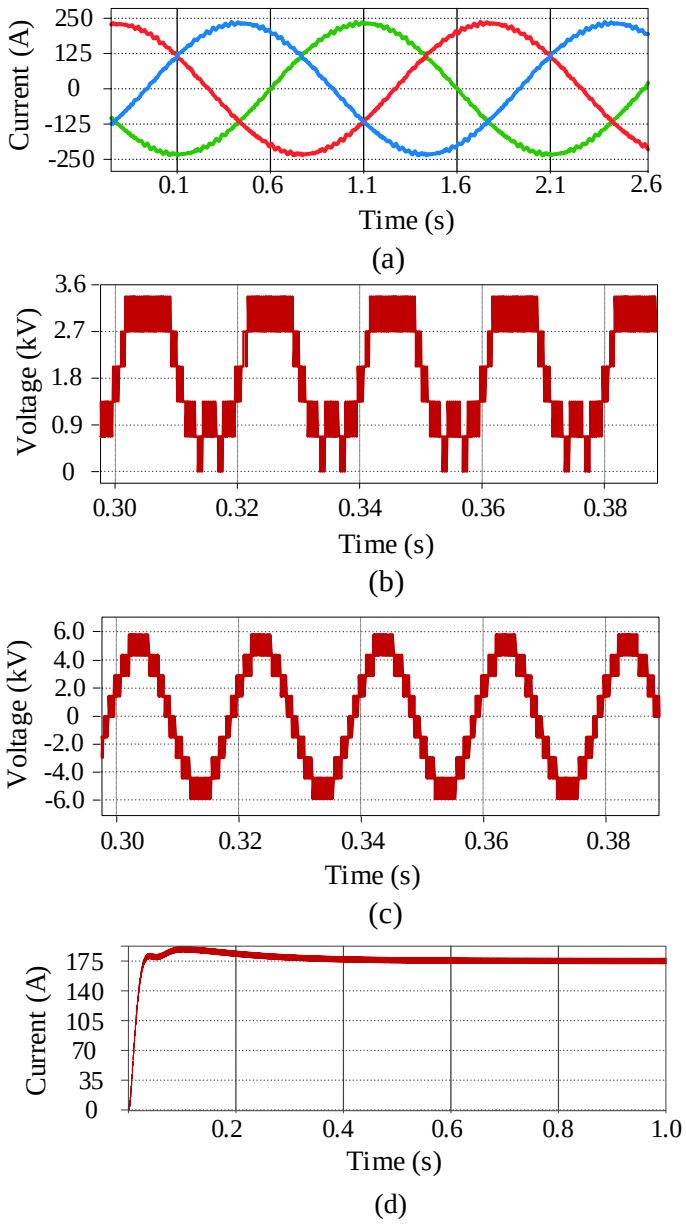

Figure 4-13 Simulation results of the converter operation: (a) input ac currents, (b) output phase voltage, (c) output phase-to-phase voltage, and (d) output dc current.

The operation of the proposed converter is also verified using small scale experimental prototype shown in Figure 4-14. The specification of the prototype is P_{rated} = 2 kW, V_{dc} = 200 V, V_{ac} = 110 V (*rms*, line-to-line). Two submodules with rated voltage of 100 V and capacitance of 50 μF are used in the lower converter arms. Sinusoidal pulse width modulation with modulation index of 0.8 is

used. The control is implemented in Texas Instruments Delfino microcontroller (TMS320F28335). Figure 4-15 shows the gate voltages of the converter upper arm switches. As can be seen from this figure, the upper arm switches of the converter operate alternatively only for one-third of the fundamental line period and none of the upper arm switches operate simultaneously. The converter input ac voltage and current waveforms are shown in Figure 4-16, and the converter submodule capacitor voltages and phase-to-phase voltages are shown in Figure 4-17. These experimental results validate the control and operation of the proposed hybrid voltage source converter topology.

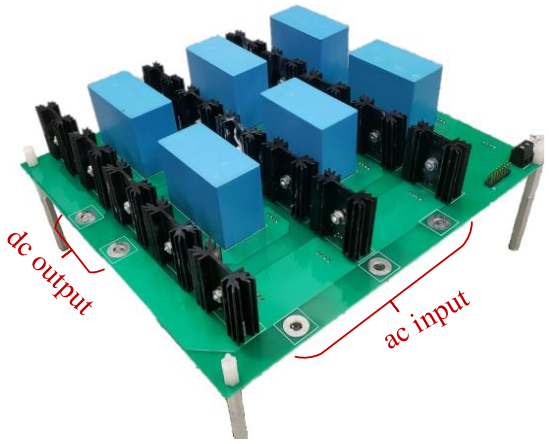

Figure 4-14 Experimental prototype picture of the proposed hybrid voltage source converter topology.

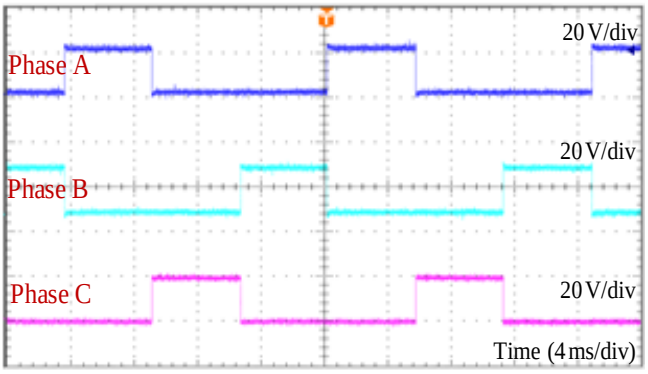

Figure 4-15 Experimental results of the gate voltages for the converter upper arm switches.

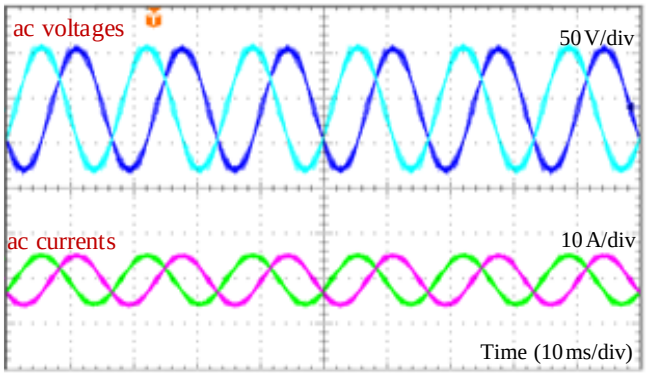

Figure 4-16 Experimental results of the converter input ac voltages and ac currents.

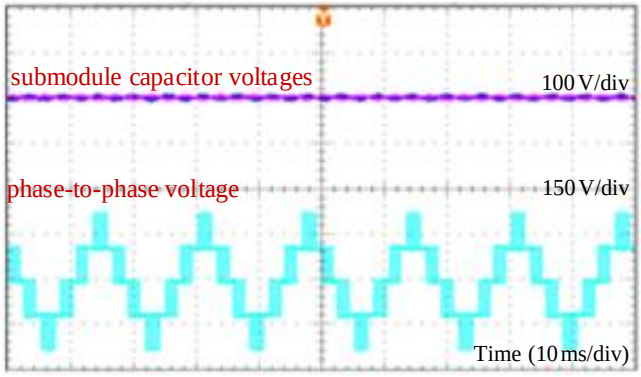

Figure 4-17 Experimental results of the converter submodule capacitor voltages and the converter phase to phase voltage.

4.6 Performance Comparison with Other Similar HVDC Converter topologies

By modifying the structure of the basic submodules (half bridge and full bridge submodules), several variants of modular multilevel converter topologies have been introduced in literature for HVDC applications. Some of these enhanced submodule structures are diode clamped submodule [4.33], T-submodule [4.34], single/double clamped submodule [4.35], cross-connected submodule [4.36] and asymmetrical submodule [4.37]. Compared to the basic modular multilevel converter submodules, these enhanced submodule cells provide improved waveform fidelity and added functionality such as dc fault blocking capability and ac fault rid though capability for the modular multilevel converter topology. However, they increase the converter part count hence the converter

cost and footprint due to their additional active switch, diode, or passive element. Therefore, the merits and demerits of the proposed hybrid voltage source converter topology is compared with other modular multilevel converter topologies containing the basic submodules as shown in Figure 4-18 to make fair comparison in terms of converter part count, cost, and power loss.

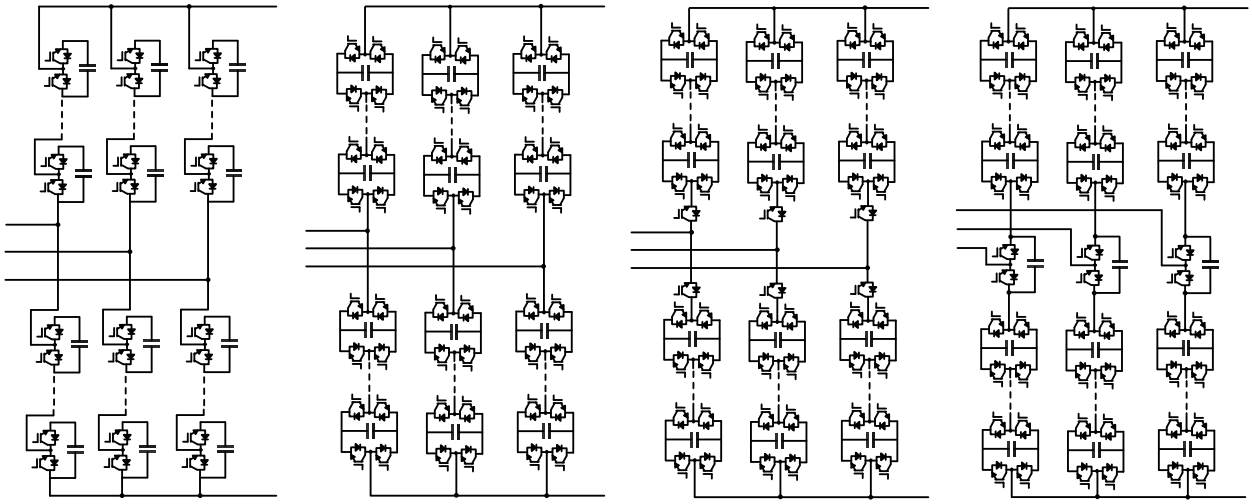

Figure 4-18 Modular Multilevel Converter topologies based on the basic switching cells: (a) Half bridge MMC (HB MMC), (b) Full bridge MMC (FB MMC), (c) Alternate Arm Converter (AAC), (c) Improved Alternate Arm Converter (IAAC).

Table 4-5 summarizes comparison of the general features of the proposed hybrid voltage source converter topology with other similar modular multilevel converter topologies such as Half Bridge MMC (HB MMC) [4.38], Full Bridge MMC (FB MMC) [4.39], Alternate Arm Converter (AAC) [4.14] and Improved Alternate Arm Converter (IAAC) [4.40]. In the table V_{dc} refers to the nominal dc bus voltage, V_{SM} refers to the rated voltage of the submodules and N_{SM} refers to the number of submodules per converter arm. For AAC and IAAC topologies, the director switches are assumed to have same voltage rating as the submodule switches and for the proposed converter topology,

the upper arm switches are assumed to have the same voltage rating as the lower arm submodule switches.

In terms of the number of devices, the proposed hybrid voltage source converter topology requires 35 percent lower number of devices compared to the HB MMC, 67 percent lower number of devices compared to the FB MMC and 57 percent lower number of devices compared to the AAC and IAAC topologies. The proposed converter topology also reduces the number of submodule capacitors by 50 percent compared to the HB MMC and FB MMC topologies and by about 25 percent compared to the AAC and IAAC topologies. Therefore, it provides significant reduction in terms of converter footprint, cost, and power loss. Converter footprint and cost are two of the essential design features required for high efficiency and high power density energy conversion systems hence this topology is very attractive for such application.

Table 4-5 Comparison of the Proposed Converter with Other Similar MMC Converters.

	HB MMC [4.38]	**FB MMC [4.39]**	**AAC [4.14]**	**IAAC [4.40]**	**Proposed**
No. of active switches	$12V_{dc}/V_{SM}$	$24V_{dc}/V_{SM}$	$18V_{dc}/V_{SM}$	$18V_{dc}/V_{SM}$	$7.7V_{dc}/V_{SM}$
No. of diodes	0	0	0	0	0
No. of capacitors	$6V_{dc}/V_{SM}$	$6V_{dc}/V_{SM}$	$4V_{dc}/V_{SM}$	$(4V_{dc}/V_{SM})+3$	$3V_{dc}/V_{SM}$
Voltage stress of switches	V_{dc}/N_{SM}	V_{dc}/N_{SM}	$0.632V_{dc}/N_{SM}$	$0.632V_{dc}/N_{SM}$	V_{dc}/N_{SM}
No. switches in conduction path	$6V_{dc}/V_{SM}$	$12V_{dc}/V_{SM}$	$5.5V_{dc}/V_{SM}$	$9V_{dc}/V_{SM}$	$3.7V_{dc}/V_{SM}$
Voltage levels	$N+1$	$2N+1$	$2N+1$	$2N+1$	$N+1$
Over modulation	No	Yes	Yes	Yes	No
Dc fault tolerance	No	Yes	Yes	Yes	No

The voltage stress of the lower arm devices for the proposed hybrid voltage source converter topology is the same as the half bridge MMC and full bridge MMC topologies. However, it is slightly higher than the alternate arm converter topologies. The alternate arm converter topologies have lower device voltage stress due to their unique operation. In these topologies, the converter arms need to block the maximum ac voltage of the converter which is lower than the dc bus voltage [4.14], [4.15] which the half bridge MMC, full bridge MMC and the proposed converter topology arms need to block. The upper arm devices of the proposed hybrid voltage source converter need to block the maximum ac output voltage similar to the alternate arm converter topologies. On the other hand, the proposed converter topology has significantly lower number of devices per current conduction path compared to the other converter topologies. Therefore, it achieves lower semiconductor device power loss hence higher efficiency than the other converter topologies.

The proposed hybrid voltage source converter topology however produces lower voltage levels compared to the FB MMC and the alternate arm converter topologies (AAC and IAAC). But this is not necessarily a drawback. The number of output voltage levels can be increased by using additional submodules in the lower arms of the converter if desired. In order to produce the same number of output voltage levels as the FB MMC and the alternate arm converter topologies, the proposed converter topology would require twice the number of devices of that would be needed for $N+1$ voltage levels. However, the number of devices is still lower than that of the FB MMC, AAC and IAAC topologies. Besides, the blocking voltage requirement of the devices will be reduced when additional submodules are used to increase the output voltage levels. Similarly, the proposed hybrid voltage source converter topology requires additional submodules in the lower converter arms or third harmonic injection to achieve over modulation, but the number of devices is still lower than that of the other converter topologies with over modulation capability.

The proposed hybrid voltage source converter topology however has some drawbacks. One such drawback is its inability to block dc faults. The chain of submodules in the lower arms of the proposed hybrid voltage source converter topology produces unipolar output voltages as shown in Figure 4-13 (b) making this converter topology incapable to block dc faults. As described in [4.41], the converter phases need to produce a bipolar output voltage to have dc-fault blocking capability. Otherwise, the converter will not have the capability to switch reverse voltage when dc-fault occurs to respond to the need for negative stack voltage. The FB MMC, AAC and IAAC topologies on the other hand contain full bridge submodules that can produce bipolar output voltage and hence enable dc fault blocking capability.

The power loss of the different converter topologies is also investigated in PLECS electro-thermal simulation using the converter specifications shown in Table 4-4. Sinusoidal pulse width modulation (modulation index = 0.8) is used for all converter topologies without third harmonic injection. This power loss estimation method is described in detail in [4.42] and it is used for power loss and efficiency estimation of power converters in [4.43] and [4.44]. It uses a power loss lookup table approach where the conduction and switching loss of the semiconductor devices are estimated from the devices simulated voltage, current and junction temperature using prepopulated power loss lookup tables. The power loss lookup table for the semiconductor devices can be constructed by measuring the conduction and switching energy losses of the semiconductor devices for different voltage, current and junction temperature values by experiment or by digitizing the datasheet energy loss curves of the devices. However, most semiconductor device manufacturers also provide PLECS power loss lookup table for their devices. In this case, the manufacturer's power loss lookup table can be used. For this investigation, the power loss lookup table of the devices is downloaded from the manufacturer's website. Since the power loss and junction temperature of the

semiconductor devices are dependent on each other, the power loss and junction temperature of the semiconductor devices are determined iteratively using the thermal model of the devices as described in [4.45].

Figure 4-19 shows the estimated semiconductor device losses of the different converter topologies. As can be seen from the figure the proposed converter topology has significantly lower conduction and switching losses compared to the other converter topologies. This is because the proposed converter topology has lower number of submodules and active switches (resulting in lower switching loss) and lower number of devices in current conduction path (reducing conduction loss). Figure 4-20 shows the power losses of the different converter topologies for different power factor values. The figure shows the proposed hybrid voltage source converter topology has lower semiconductor device power loss compared to the other converter topologies for a wide range of power factor values.

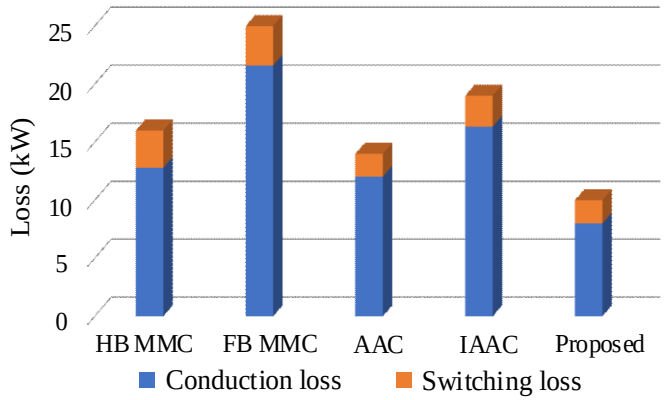

Figure 4-19 Conduction and switching losses of the semiconductor devices for the different HVDC converter topologies.

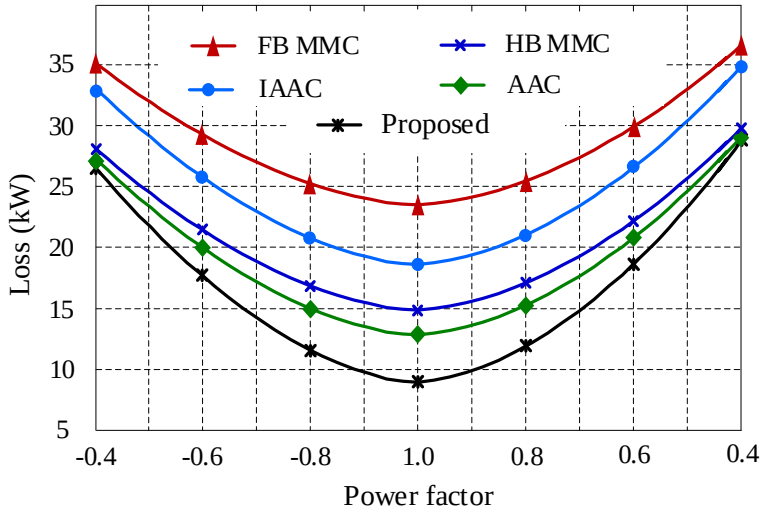

Figure 4-20 Semiconductor device power loss for the different converter topologies for different power factor values.

4.7 Conclusion

This chapter presented a new hybrid voltage source converter topology for HVDC applications featuring reduced submodule (device) count. It consists of strings of switches (IGBT/MOSFET) in the upper arms of the converter and cascaded half-bridge submodules in the lower arms of the converter. The cascaded half-bridge submodules in the lower arms of the converter produce multilevel output voltages while the switching blocks in the upper arms of the converter perform waveform steering (dc current conduction). The upper arm switches conduct the dc current alternatively for one-third of the fundamental line period. The conduction period of the upper arm switches depends on the relative magnitude of the input ac line-to-neutral voltages.

The control of the proposed converter is based on energy balance principle. It regulates the power exchange between the ac network, the converter, and the dc network so that the converter is not sourcing or absorbing any net energy. It consists of three control parts: ac side control, dc side control and submodule capacitor voltage balancing. The ac side control part regulates the power

exchange between the ac network and the converter. This control part is similar to the conventional grid current control strategy for grid-connected converters. The dc side control part regulates the power exchange between the converter and the dc network by controlling the total energy of the converter to its nominal value. The submodule capacitor voltage balancing makes sure the voltages of the submodule capacitors is balanced.

The proposed hybrid voltage source converter topology has superior performance features compared to other similar converter topologies. In terms of the number of devices, the proposed hybrid voltage source converter topology requires 35 percent lower number of devices compared to the HB MMC, 67 percent lower number of devices compared to the FB MMC and 57 percent lower number of devices compared to the AAC and IAAC topologies. Therefore, it has lower converter footprint and cost making it preferable for applications such as offshore HVDC converter stations. In addition, it has more than 50 percent lower number of devices per current conduction path and lower semiconductor device blocking voltage requirement providing higher efficiency compared to other similar HVDC converter topologies. The main drawbacks of the proposed converter are its lack of dc fault blocking capability due to unipolar phase output voltages and lack of over modulation operation capability.

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CHAPTER 5

PRACTICAL SUBMODULE DESIGN CONSIDERATIONS FOR DIFFERENT HVDC CONVERTER TOPOLOGIES

5.1 Introduction

Multilevel converter topologies such as the Modular Multilevel Converter (MMC) [5.1] – [5.3], the Alternate Arm Converter (AAC) [5.4] – [5.6] and the Asymmetric Alternate Arm Converter (AAAC) [5.7] – [5.10] topologies rely on charged submodule capacitors for the generation of multilevel output voltage waveform. The submodule capacitors of these converter topologies need to be charged to their nominal voltage that they are designed for in order to guarantee the proper operation and reliability of the converter. If the submodule capacitors are overcharged, the capacitor voltage may go beyond the rated voltage of the capacitors, causing accelerated fatigue and risk of failure to the submodule capacitors. On the other hand, if the submodule capacitors are undercharged, the converter would not provide its maximum voltage capability, leading to a potential instability of the converter operation and other power system components connected to the converter. The overall control of these converter topologies also depends on the converter arm energy hence submodule capacitor under voltage or overvoltage will lead to loss of arm energy control, causing system instability [5.11] – [5.15].

The generation of multilevel (staircase) output voltage waveform requires insertion and removal of the stacked submodules to the converter arm current path depending on the magnitude of the required output voltage [5-16] – [5.18]. When a submodule is inserted to the arm current path, its capacitor will charge or discharge depending on the direction of the arm current. Hence the submodule capacitor voltage will increase or decrease. On the other hand, if a submodule is removed from the converter arm current path, its capacitor will not charge, or discharge and its

voltage will stay at its current value. This phenomenon causes submodule capacitor voltage fluctuation which in turn causes converter arm energy fluctuation. The submodule capacitor voltage fluctuation can be suppressed by using large submodule capacitors [5.19], [5.20]. But this will increase the converter cost and footprint. In most power electronic converter applications such as offshore wind energy generations, lower converter cost and footprint is a required converter feature hence using large submodule capacitors is not an attractive solution. Therefore, in order to assess the relative benefits and drawbacks of the different HVDC converter topologies in terms of converter cost and footprint, it is first important to investigate their arm energy and submodule capacitor voltage deviation to know the minimum submodule capacitance requirement of these converter topologies. The modular multilevel converter and the alternate arm converter topologies are relatively matured, and their corresponding submodule capacitor voltage and arm energy deviation has been well investigated in [5.21] – [5.29]. The arm energy deviation and minimum submodule capacitance requirement of the asymmetric alternate arm converter topology on the other hand has yet not been investigated.

This chapter presents an investigation of the converter arm energy and submodule capacitor sizing of the asymmetric alternate arm converter topology using the analytical model of the converter. A mathematical model of the converter arm energy is derived using the converter arm voltage and arm current expressions derived in Section 4.2 and then a simplified mathematical expression is derived to determine the minimum submodule capacitance from the maximum arm energy deviation over a line period and the maximum allowed capacitor voltage deviations. To compare the minimum submodule capacitance requirement of the asymmetric alternate arm converter topology with other similar HVDC converter topologies, the arm energy deviation, and

submodule capacitor voltage oscillation of the modular multilevel converter topology and the alternate arm converter topology are first reviewed in the next section.

5.2 Arm Energy Deviation of Existing Common HVDC Converter Topologies

A widely used submodule capacitance sizing method for multilevel converter topologies is based on the investigation of the converter arm energy over one line cycle [5.21], [5.22], [5.23], [5.24]. Such investigation reveals the energy storage requirements of the converter necessary to keep the power balance between the ac and dc side of the converter. Based on the steady state operating equations (considering the circulating currents and common mode voltage if any) of the converter, the maximum converter arm energy deviation over one line cycle is calculated and the required submodule capacitance is then determined from the maximum arm deviation, the maximum allowed submodule capacitor voltage deviation and the number of submodules per converter arm [5.21], [5.22], [5.24]. The minimum required submodule capacitance (C_{SM}) of the converter arm can be determined using the worst-case energy perturbation method from the converter maximum arm energy deviation (ΔE_{arm}), and the converter maximum allowable submodule capacitor voltage deviation (ΔV_{SM}) as shown in (5-1).

$$C_{SM} = \frac{2\Delta E_{arm}}{N_{SM}\Delta V_{SM}^2} \tag{5-1}$$

The converter arm energy deviation (ΔE_{arm}) depends on the converter topology operation principle and control strategy. Hence it is important to investigate the arm energy deviations of different converter topologies to determine their minimum required submodule capacitance.

5.2.1 Arm Energy Deviation of the MMC Converter Topology

The energy storage requirement and submodule capacitance sizing procedure of the modular multilevel converter topology is extensively investigated in several literatures based on the

analytical model of the converter topology. In [5.22], an analytical submodule capacitance sizing technique for the modular multilevel converter topology is proposed based on the analytical solution of the submodule capacitor voltage ripple equations. The submodule capacitor voltage ripple equations are constructed based on the knowledge of the external voltage/current magnitudes considering all the passive elements of the converter, the injected common-mode voltage, and the circulating current of the converter. The maximum arm energy deviation of the converter is then determined based on the analytical converter equations using computer simulation software since these equations are rather cumbersome for hand calculation.

In [5.23], another analytical submodule capacitance sizing method for the modular multilevel converter topology is proposed using the steady state model of the converter. The submodule capacitance is determined from the amplitudes of the arm voltage harmonic components for a desired dc voltage fluctuation range as shown in (5-2).

$$C = \frac{2}{4\omega\Delta u_{\mathrm{C}}}\left(\hat{u}_{\mathrm{C1}} + \hat{u}_{\mathrm{C3}}\right)\cos\varphi \tag{5-2}$$

where Δu_{c} is the maximum allowed submodule capacitor voltage deviation, ω is the angular frequency of the arm voltage, φ is the power factor angle and u_{c1} and u_{c3} are the first and third harmonic components of the submodule capacitor voltage respectively. The harmonic components of the submodule capacitor voltage are determined from the steady state analytical equations of the converter using computer simulation.

In [5.24], optimal submodule capacitance sizing method is proposed for the modular multilevel converter topology for high voltage variable speed drive applications. The submodule capacitor is estimated from the drive system parameters, the injected common-mode voltage and the maximum allowed submodule capacitor voltage deviation as shown (5-3).

$$C_{\mathrm{SM}} = \frac{\int\left(\frac{1}{2}V_{\mathrm{dc}} - u_0 - u_{\mathrm{com}}\right)\left(i_{\mathrm{Z}}\left(u_{\mathrm{com.ref}},\ u_{\mathrm{o.ref}},\ V_{\mathrm{dc}},\ i_0\right) + \frac{1}{2}i_0\right)dt}{\Delta V_{\mathrm{div}} \cdot V_{\mathrm{dc}}} \tag{5-3}$$

where V_{dc} is the dc bus voltage of the converter, u_{o} is the rated output voltage of the converter, u_{com} is the injected common mode voltage of the converter, i_{z} is the injected common mode current of the converter and i_{o} is the rated output voltage of the converter.

In [5.25], the relationship between the submodule capacitance and the power transfer capability of the modular multilevel converter topology is investigated. The authors highlighted that the power transfer capability of the converter is dependent on the maximum allowed submodule capacitor voltage deviation, the power factor of the converter and its submodule capacitance.

5.2.2 Arm Energy Deviation of the AAC Converter Topology

The arm energy and submodule capacitance requirement of the alternate arm converter is also addressed in several literatures. In [5.28], the arm energy and submodule capacitance requirement of the alternate arm converter is investigated for "short-overlap" operation mode using the Fourier Series expressions of the converter arm voltage and arm current expressions shown in (5-4) and (5-5). The converter arm energy is determined by integrating the product of the converter arm voltage and arm current for one fundamental line cycle and then the minimum required submodule capacitance is determined from the maximum arm energy deviation and the maximum allowed submodule capacitor voltage oscillation.

$$i_{\mathrm{arm}}(t) = \begin{cases} \frac{I_0}{2}\sin\left(\omega_0 t + \varphi\right) + I_{\mathrm{cir}}, & \text{if} \quad \frac{2\pi - \varphi - \psi/2}{\omega_0} < t \le \frac{-\varphi - \psi/2}{\omega_0} \\ I_0 \sin\left(\omega_0 t + \varphi\right), & \text{if} \quad \frac{-\varphi - \psi/2}{\omega_0} < t \le \frac{\pi - \varphi - \psi/2}{\omega_0} \\ 0, & \text{if} \quad \frac{\pi - \varphi - \psi/2}{\omega_0} < t \le \frac{\pi - \varphi + \psi/2}{\omega_0} \end{cases} \tag{5-4}$$

$$u_{\text{arm}}(t)=\begin{cases}\dfrac{V_{\text{DC}}}{2}-V_0\sin(\omega_0 t+\varphi), & \text{if} \quad \dfrac{-\varphi-\psi/2}{\omega_0}<t\le\dfrac{\pi-\varphi+\psi/2}{\omega_0}\\ 0, & \text{if} \quad \dfrac{\pi-\varphi+\psi/2}{\omega_0}<t\le\dfrac{2\pi-\varphi-\psi/2}{\omega_0}\end{cases} \tag{5-5}$$

where V_0 and I_0 are the converter output voltage and output current, V_{DC} is the converter dc bus voltage, ω_o is the angular frequency of the output voltage, φ is the power factor angle, I_{cir} is the converter circulating dc current, and ψ is the angular duration of the "overlap" state.

In [5.29], the arm energy deviation of the alternate arm converter is similarly investigated, and a mathematical model is developed to help the submodule capacitance sizing of this converter topology. The converter arm power is first determined by multiplying the converter arm voltage and arm current as shown in (5-6) and then the converter arm energy is calculated by integrating the arm power over fundamental line cycle as shown in (5-7).

$$P_{\text{arm}}(t)=V_{\text{arm}}(t)I_{\text{arm}}(t)=\frac{S}{3}\left(\cos\varphi-\cos(2\omega t+\varphi)-\frac{\pi}{2k_{\text{AC}}}\sin(\omega t+\varphi)\right) \tag{5-6}$$

$$E_{\text{arm}}(t)=\frac{S}{6\omega K_{\text{AC}}}\left(\cos(\omega t+\varphi)(\pi-2K_{\text{AC}}\sin\omega t)-\cos\varphi(\pi-2K_{\text{AC}}\omega t)\right) \tag{5-7}$$

where S is the rated apparent power of the converter, φ is the power factor angle, ω is the angular frequency of the output voltage and K_{AC} is the maximum allowed ac voltage fluctuation.

Despite the converter arm energy and submodule capacitor sizing of the modular multilevel converter and the alternate arm converter is well investigated, the operation of the asymmetric alternate arm converter topology is slightly different from the operations of the modular multilevel converter topology and the alternate arm converter topology. Both the upper and lower converter arms of the modular multilevel converter topology are simultaneously used for the entire line period while the alternate arm converter topology alternately uses the upper and lower converter

arms for half of the line period. The asymmetric alternate arm converter topology on the other hand simultaneously uses all the lower converter arms for the entire line period like the modular multilevel converter topology but it alternates the three upper converter arms in each one-third of the line period. Therefore, the converter arm energy over a line cycle hence the submodule capacitance requirement of the asymmetric converter arm converter topology is different from that of the modular multilevel converter and the alternate arm converter topologies. But no literature has been reported on this until now despite this is significant for the converter design and comparison with other similar converter topologies. Therefore, the arm energy deviation and submodule capacitor sizing of the alternate arm converter topology is discussed in the following section.

5.3 Arm Energy Deviation of the AAAC Topology

5.3.1 Analytical Arm Energy Derivation

The arm energy deviation and energy storage requirement of the asymmetric alternate arm converter topology is also investigated using the same approach as the modular multilevel converter and the alternate arm converter topologies. The converter arm power is first calculated by multiplying the converter arm voltage and arm current expressions and then the converter arm energy is determined by integrating the converter arm power over one line cycle. The arm voltage and arm current expressions of the converter phase A, shown in (5-8) and (5-9), are used for the investigation of the converter arm power and arm energy based on the steady state operating equations of the converter presented in Section 4.2.

$$u_{\text{arm}}^{\text{a}}(t)=\begin{cases} V_{\text{dc}}, & \pi/6<\omega t\le 5\pi/6 \\ V_{\text{dc}}+u_{\text{ab}}(t), & 5\pi/6<\omega t\le 3\pi/2 \\ V_{\text{dc}}+u_{\text{ac}}(t), & 3\pi/2<\omega t\le 13\pi/6 \end{cases} \tag{5-8}$$

$$i_{arm}^{a}(t)=\begin{cases} i_a(t)-i_{dc}, & \pi/6<\omega t\le 5\pi/6 \\ i_a(t), & 5\pi/6<\omega t\le 3\pi/2 \\ i_a(t), & 3\pi/2<\omega t\le 13\pi/6 \end{cases} \tag{5-9}$$

where V_{dc} is the dc output voltage, u_{ab}(t) and u_{ac}(t) are the input line-to-line voltages of the converter given by (5-10) and (5-11), i_a(t) is the phase A input ac current of the converter given by (5-12) and i_{dc} is the dc current of the converter given by (5-13).

$$u_{ab}(t)=V_s\sin(\omega t)-V_s\sin(\omega t-2\pi/3) \tag{5-10}$$

$$u_{ac}(t)=V_s\sin(\omega t)-V_s\sin(\omega t+2\pi/3) \tag{5-11}$$

$$i_a(t)=I_s\sin(\omega t-\varphi) \tag{5-12}$$

$$i_{dc}=\frac{3v_s i_s\cos(\varphi)}{2u_{dc}} \tag{5-13}$$

where V_s and I_s are the input ac peak voltage and current, v_s and i_s are the input rms voltage and current and φ is the power factor angle.

The converter arm energy can then be determined by integrating the product of the converter arm voltage and arm current as shown in (5-14). By substituting the expressions (5-10) – (5-13) into (5-14) and evaluating the integrals, the simplified arm energy expression shown in (5-15) can be derived. Equation (5-15) shows the converter arm energy is dependent on the load power factor angle (φ). The power factor angle value that yields the maximum arm energy deviation can be determined by taking the derivative of the arm energy expression with respect to the power factor angle (φ) and equating it with zero. Doing so reveals the maximum arm energy deviation occurs at a power factor of 0.925 leading. Figure 5-1 shows the normalized converter arm energy for this power factor value.

$$E_{\text{arm}}(t)=\begin{cases}\int V_{\text{dc}}\cdot\left(i_{\text{a}}(t)-i_{\text{dc}}\right)dt, & \pi/6<\omega t\le 5\pi/6\\ \int\left(V_{\text{dc}}+u_{\text{ab}}\left(t\right)\right)\cdot i_{\text{a}}(t)\,dt, & 5\pi/6<\omega t\le 3\pi/2\\ \int\left(V_{\text{dc}}+u_{\text{ac}}\left(t\right)\right)\cdot i_{\text{a}}(t)\,dt, & 3\pi/2<\omega t\le 13\pi/6\end{cases} \tag{5-14}$$

$$E_{\text{arm}}(t)=\begin{cases}\left(\dfrac{-V_{\text{dc}}I_{\text{s}}\cos(\omega t-\varphi)}{2\omega}\right., & \pi/6<\omega t\le 5\pi/6\\ \left(\dfrac{-V_{\text{dc}}I_{\text{s}}\cos(\omega t-\varphi)}{2\omega}+\dfrac{V_{\text{s}}I_{\text{s}}\sin(2\omega t-\varphi-2\pi/3)}{4\omega}\right., & 5\pi/6<\omega t\le 3\pi/2\\ \left(\dfrac{-V_{\text{dc}}I_{\text{s}}\cos(\omega t-\varphi)}{2\omega}-\dfrac{V_{\text{s}}I_{\text{s}}\sin(2\omega t-\varphi+2\pi/3)}{4\omega}\right., & 3\pi/2<\omega t\le 13\pi/6\end{cases} \tag{5-15}$$

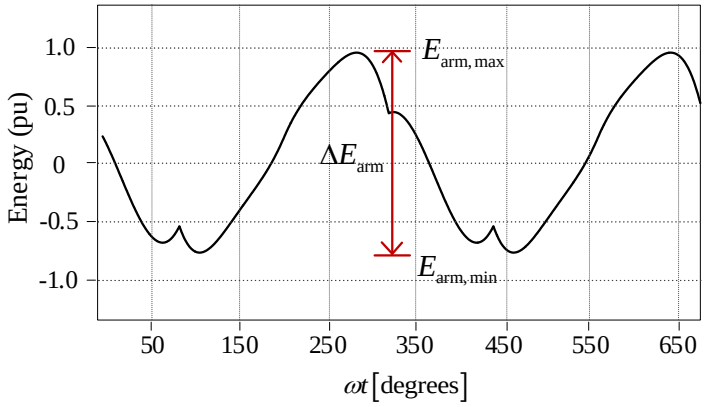

Figure 5-1 Normalized converter arm energy for power factor of 0.925 leading.

The maximum arm energy deviation (ΔE_{arm}) needed to calculate the minimum required submodule capacitance for the converter can then be determined by using (5-16).

$$\Delta E_{\text{arm}}=E_{\text{arm, max}}-E_{\text{arm, min}} \tag{5-16}$$

The required minimum submodule capacitance is then determined from the maximum arm energy deviation and the maximum and minimum allowable submodule capacitor voltages as shown in (5-17).

$$C_{\mathrm{SM}} = \frac{2\Delta E_{\mathrm{arm}}}{N\left(V_{\mathrm{SM,max}}^2 - V_{\mathrm{SM,min}}^2\right)} \tag{5-17}$$

where $V_{\mathrm{SM,max}}$ and $V_{\mathrm{SM,min}}$ are the maximum and minimum allowed submodule capacitor voltages and N is the number of submodules per converter arm. Given the maximum allowed submodule capacitor voltage ripple factor (k_{r}) and the nominal submodule capacitor voltage value (V_{nom}), the maximum and the minimum allowable submodule capacitor voltages can be expressed as in (5-18) and (5-19). Equation (5-17) can then be simplified into (5-20) by substituting (5-18) and (5-19) into (5-17).

$$V_{\mathrm{SM,max}} = \left(1 + k_{\mathrm{r}}\right)V_{\mathrm{nom}} \tag{5-18}$$

$$V_{\mathrm{SM,min}} = \left(1 - k_{\mathrm{r}}\right)V_{\mathrm{nom}} \tag{5-19}$$

$$C_{\mathrm{SM}} = \frac{\Delta E_{\mathrm{arm}}}{2Nk_{\mathrm{r}}V_{\mathrm{nom}}^2} \tag{5-20}$$

5.3.2 Arm Energy Model Validation

To validate the accuracy of the derived arm energy expression and submodule capacitance sizing method, the theoretically estimated converter arm energy is first compared with the simulated converter arm energy values using the converter specification shown in Table 5-1. An ideal converter circuit simulation is first performed to investigate the converter arm energy variation over one line cycle. Figure 5-2 shows the ideal converter simulation configuration in MATLAB/SIMULINK. The cascaded submodules in the lower converter arms are represented by controlled voltage sources given by (4-1) – (4-3). The gate signals for the upper arm switches are

generated based on the converter operating modes (determined by the relative magnitude of the input line-to-neutral voltages) as shown in Figure 5-3. The converter arm energy is calculated by integrating the product of the converter arm voltage and arm current waveforms in MATLAB.

Table 5-1 Converter specification for simulation.

Parameter	**Value**
rated power	1 MW
dc bus voltage	6 kV
ac voltage, line-to-line	3.3 kV
nominal submodule voltage	1.5 kV
ac interface inductor (L_{ac})	3.5 mH
dc interface inductor (L_{dc})	6.5 mH
dc interface resistor (R_{dc})	0.3 Ω

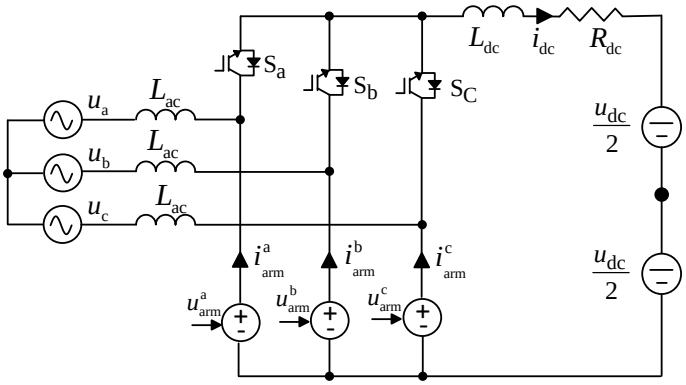

Figure 5-2 Ideal converter topology simulation configuration.

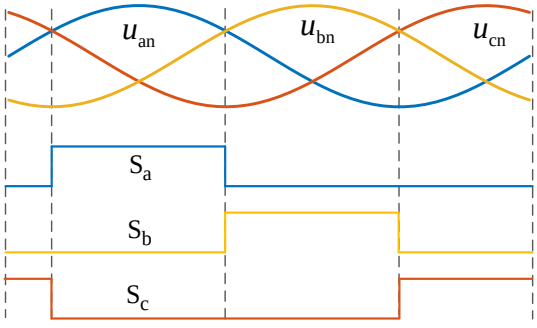

Figure 5-3 Gate signals for the converter upper arm switches.

Figure 5-4 shows comparison of the theoretically estimated converter arm energy and the ideally simulated converter arm energy values. As can be seen from the figure the theoretically estimated converter arm energy and the ideally simulated converter arm energy values have a very close agreement. This validates the mathematical correctness of the converter arm energy derivation process outlined in Section 5.3.1. The minimum submodule capacitance required for the lower converter arms then can be determined from the maximum arm energy deviation, the number of submodules required in the lower converter arms and the maximum allowable submodule capacitor voltage fluctuation. Since the lower converter arms need to always support the dc bus [5.9], [5.15], four submodules are required for each converter legs. From the figure, the maximum converter arm deviation can be calculated to be about 10.8 kJ. Considering a peak maximum allowable submodule capacitor voltage ripple factor of 10 percent, the minimum submodule capacitance required for the lower converter arms then will be 6 mF.

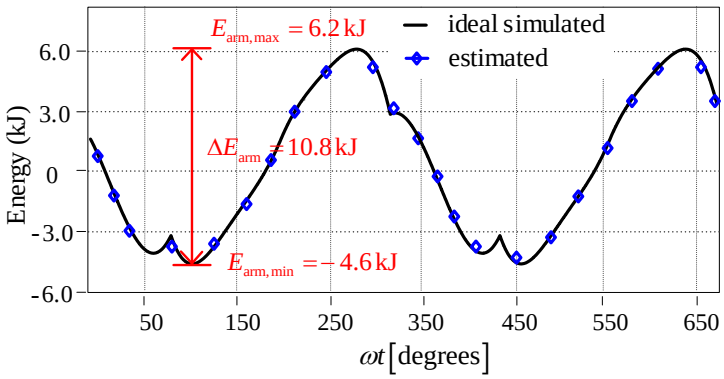

Figure 5-4 Comparison of theoretically estimated and ideally simulated converter arm energy values.

The ideal submodule capacitor voltage waveform can also be determined from the calculated submodule capacitance and the converter arm current as shown in (5-21).

$$u_c(t) = \frac{1}{C_{SM}} \int i_{arm}(t) \mathrm{dt} \tag{5-21}$$

Figure 5-5 shows the theoretically estimated submodule capacitor voltage waveform. From the figure, the maximum submodule capacitor voltage fluctuation can be calculated to be 300 V which is about 20 percent of the nominal submodule capacitor voltage value – the design requirement for the submodule capacitors (10 percent peak or 20 percent peak-to-peak submodule capacitor voltage ripple).

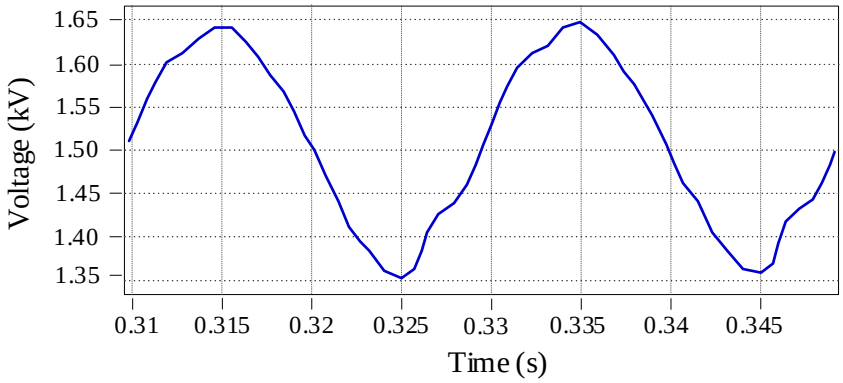

Figure 5-5 Theoreticallty estimated submodule capacitor voltage waveform.

To further verify the converter arm energy calculation and submodule capacitor sizing procedure, the full switching model of the converter is developed in MATLAB/SIMULINK using the calculated submodule capacitor value and the converter specifications given in Table 5-1. Four cascaded half bridge submodules are used for the lower converter arms while IGBTs are used for the upper converter arms. Level-shifted carrier pulse width modulation with the sorting and rotation algorithm presented in [5.30], [5.31] for submodule capacitor voltage balancing is used for the converter modulation. The converter arm energy is similarly determined by integrating the product of the converter arm voltage and the converter arm current waveforms. Figure 5-6 shows comparison of the theoretically estimated and the simulated converter arm energy values. It can again be seen from the figure that the theoretically estimated converter arm energy and the simulated converter arm energy values have a good agreement with each other further validating

the accuracy of the derived converter arm energy expression. Figure 5-7 shows comparison of the simulated submodule capacitor voltage waveforms (u_{c1}, u_{c2}, u_{c3} and u_{c4} represent the capacitor voltages of the four submodules in the lower converter arms) and the theoretically estimated submodule capacitor voltage waveform. As can be seen from the figure, the simulated submodule capacitor voltage waveforms closely resemble the theoretically estimated submodule capacitor voltage waveform both in shape and magnitude.

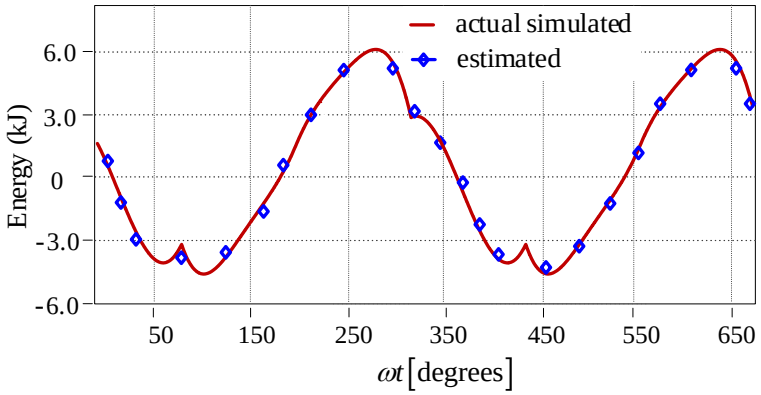

Figure 5-6 Comparison of the theoretically estimated and actual simulated converter arm energy values.

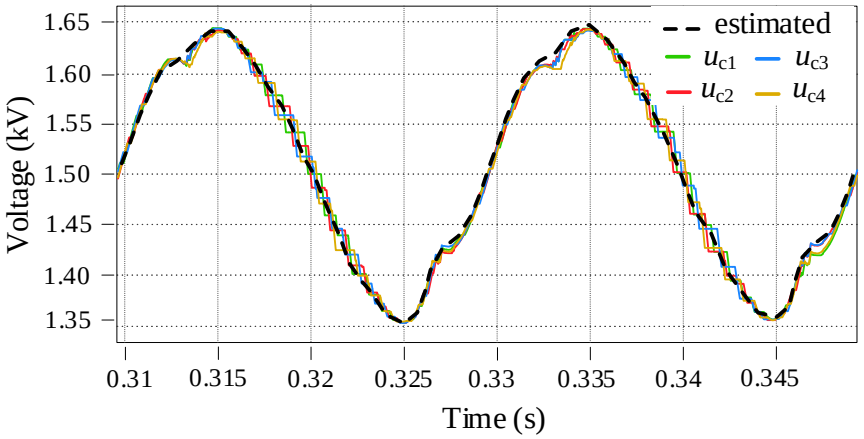

Figure 5-7 Estimated and simulated submodule capacitor voltage waveforms.

The accuracy of the derived converter arm energy expression and the submodule capacitor sizing method is also validated by experimental test. A scale-down experimental prototype with the converter specifications shown in Table 5-2 is built and used for the experimental investigation. Half bridge submodules are used for the lower converter arms and discrete IGBTs are used for the switches in the upper converter arms. Since the stack of submodules in the lower converter arms need to always support the dc voltage for proper operation of this converter topology, two submodules are required for each converter phase legs (the number of submodules required in the lower converter arms is equal to the ratio of the dc bus voltage to the nominal submodule capacitor voltage [5.32] – [5.34]).

Table 5-2 Converter specification for the experimental prototype.

Parameter	**Value**
rated power	2 kW
dc bus voltage	200 V
ac voltage, line-to-line	110 V
nominal submodule voltage	100 V
Submodule capacitance	50 μF

Using the converter specification shown in Table 5-2 and the arm energy expression in (5-15), the converter arm energy is computed in MATLAB for the worst-case power factor value determined in the previous section and the computed arm energy values are plotted as shown in Figure 5-8. From this result, the maximum arm energy deviation required for the submodule capacitance sizing is calculated using (5-16) and the minimum submodule capacitance required for the lower arm submodules is then determined using (5-20). A maximum (peak) allowed capacitor voltage ripple of 10 percent of the nominal submodule capacitor value is considered for

the capacitance calculation. But a slightly higher value of capacitance is then chosen based on availability and to allow an extra safety margin.

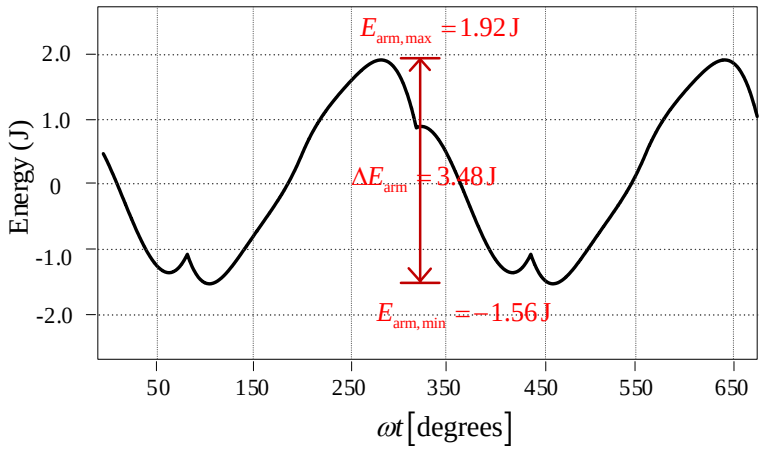

Figure 5-8 Estimated converter arm energy.

The full switching model of the converter is also developed in MATLAB/SIMULINK with the specifications shown in Table 5-2 to compare the estimated converter arm energy with the simulated converter arm energy and the experimentally measured converter arm energy values. Level-shifted carrier pulse width modulation with the sorting and rotation algorithm presented in [5.30], [5.31] for submodule capacitor voltage balancing is used to control the operation of the converter as described in [5.9], [5.15]. The simulated converter arm energy is determined by integrating the product of the converter arm voltage and arm current and the experimental converter arm energy is similarly determined by integrating the product of the measured arm voltage and arm current waveforms. Figure 5-9 shows the experimental results of the converter arm voltage and arm current waveforms. Figure 5-10 shows the experimental results of the converter arm current and arm energy waveforms. Figure 5-11 shows comparison of the theoretically estimated converter arm energy, the simulated converter arm energy, and the measured converter arm energy values. It can be seen from the figure that the theoretically

estimated converter arm energy matches with the simulated and measured converter arm energy values indicating that the derived arm energy expression has good accuracy.

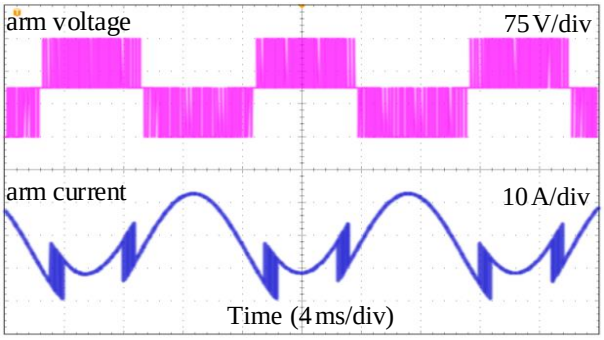

Figure 5-9 Experimental results of converter arm voltage and converter arm current.

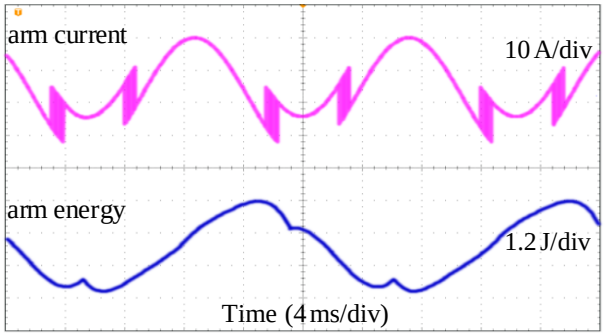

Figure 5-10 Experimental results of converter arm current and arm energy.

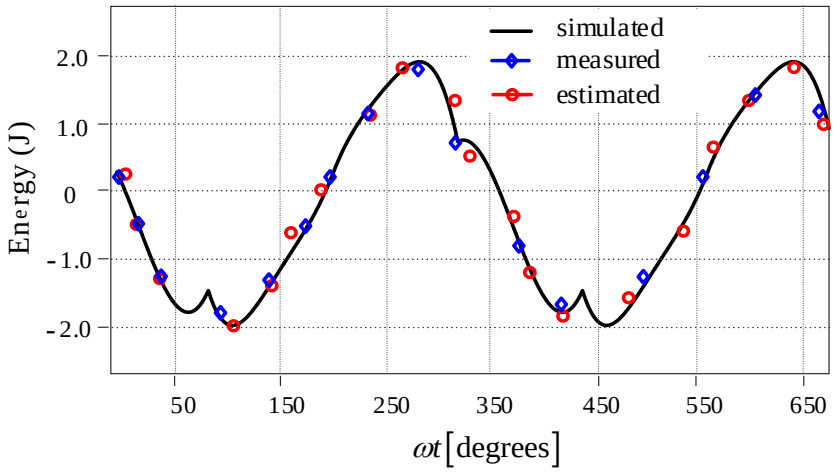

Figure 5-11 Comparison of the estimated converter arm energy, simulated converter arm energy and experimentally measured converter arm energy.

5.4 Energy Storage requirement Comparison for Different HVDC Converters

To demonstrate the applicability and usefulness of the derived converter arm energy expression and submodule capacitance sizing method, a comparison of the energy storage requirements of different converter topologies that have similar structure as the asymmetric alternate arm converter topology is performed and presented in this section. The modular multilevel converter topology and the conventional (symmetric) alternate arm converter topology are considered for this comparison primarily because of their resemblance in structure and operation with the asymmetric alternate arm converter topology. The arm energy expressions derived in [5.27], [5.29] for the modular multilevel converter topology shown in (5-22) and the alternate arm converter topology shown in (5-23) are used for this comparison. The maximum arm energy deviation for the modular multilevel converter occurs for a power factor angle of 90 degree while the maximum arm energy deviation for the conventional alternate arm converter topology occurs at a power factor angle of 74 degree [5.29]. Therefore, (5-22) and (5-23) are evaluated for these power factor angle values respectively.

$$E_{\text{arm,MMC}} = \frac{V_s I_s}{8\omega}\left(-\cos(\omega t-\varphi)-2\cos(\varphi)+(3-\sin(\omega t))\cdot(\cos(\omega t+\varphi))\right) \tag{5-22}$$

$$E_{\text{arm, AAC}} = \frac{V_s I_s}{4\omega}\left(\cos(\omega t+\varphi)\cdot(\pi-2\sin(\omega t))-(\cos(\varphi))\cdot(\pi-2\omega t)\right) \tag{5-23}$$

The arm energy for the different converter topologies is investigated in MATLAB using the specification in Table 5-1. Figure 5-12 shows the estimated arm energy for the different converter topologies. As can be seen from the figure, the alternate arm converter topologies have lower energy storage requirements compared to the modular multilevel converter topology. However, it is important to note that the arm energy deviation for the conventional (symmetric) alternate arm converter topology depends on the modulation index [5.4]. Equation (5-23) is derived for a

modulation index of 0.64 corresponding to the preferred operation of the converter termed as the "sweet spot" where the ac side and the dc side energy of the converter are equal. For the asymmetric alternate arm converter topology, the converter power factor and modulation index are interrelated since the converter control is based on energy balance between the ac side and dc side of the converter as described in [5.9], [5.34]. Therefore, the worst-case power factor value determined in this paper represents the worst-case modulation index.

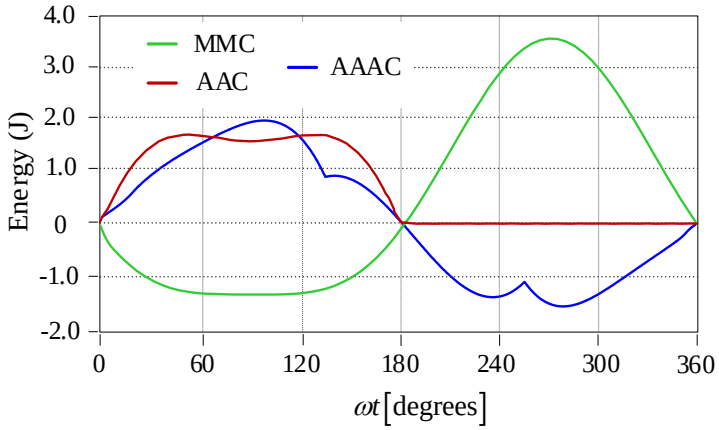

Figure 5-12 Comparison of energy storage requirement for different HVDC converter topologies.

5.5 Conclusion

This chapter presented a detailed investigation of the arm energy of the asymmetric alternate arm converter topology. The converter arm energy is determined by integrating the converter arm power which is the product of the converter arm voltage and arm current expressions. Using the derived converter arm energy expression, the maximum arm energy deviation of the converter is investigated for the worst-case power factor value which gives the maximum arm energy deviation for this converter topology. Then the required minimum submodule capacitance of the converter is determined from the maximum arm energy deviation and the maximum allowed submodule

capacitor voltage oscillation and the number of submodules per converter arm using the worst-case energy perturbation approach.

The derived converter arm energy and submodule capacitor sizing expression enables energy storage comparison of the asymmetric alternate arm converter with other similar HVDC converter topologies such as the modular multilevel converter and the symmetric (conventional) alternate arm converter topologies. The converter arm energy deviation determines the minimum submodule capacitance required for the converter which indirectly determines the cost and footprint of the converter. Converter cost and footprint are two of the essential converter features required for HVDC converters. This is especially true for offshore wind energy generation stations where space is a premium.

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CHAPTER 6

SUMMARY AND FUTURE WORK

6.1 Summary

This dissertation work presents two novel converter topologies (a three-level ANPC inverter utilizing hybrid Si/SiC switches and a new multilevel converter topology termed as the Asymmetric Alternate Arm Converter (AAAC) topology) that are suitable for high efficiency and high-power density energy conversion systems. The operation principles, modulation, and control strategies of these newly introduced converter topologies are presented in detail supported by simulation and experimental results. A thorough design optimization of these converter topologies is also presented. In addition, a new converter figure of merit accounting for the hybrid Si/SiC switch and the converter topology properties is proposed to facilitate the performance comparison of different converter topologies utilizing hybrid Si/SiC switches.

Performance comparison of the proposed converter topologies with other similar converter topologies is also presented. The hybrid Si/SiC switch based ANPC inverter has superior performance in terms of semiconductor device cost and inverter efficiency compared to an all SiC MOSFET ANPC inverter topology, an all Si IGBT ANPC inverter topology and mixed Si IGBT and SiC MOSFET based ANPC inverter topologies. However, it has slightly higher gate driver cost since the Si/SiC switches are currently driven by two separate gate drivers. Similarly, the asymmetric alternate arm converter topology has lower device count, lower number of devices per current conduction path, and a lower device blocking voltage requirement when compared to the modular multilevel converter and the conventional (symmetric) alternate arm converter topologies. Hence it has lower cost, lower power loss, and a lower converter footprint. However, it has lower

number of output voltage levels (requiring larger ac interface inductors) and lacks dc-fault blocking and overmodulation operation capabilities.

6.2 Future work

The application of hybrid Si/SiC switches can also be extended to other converter topologies with high switching frequency operation capabilities to optimize the converter efficiency and cost. However, their benefits and drawbacks for the specific converter topology and application need to be well investigated. The proper Si/SiC gate control strategy and current ratio between the internal devices must be chosen to maximize the benefits of these switches. In addition, new single chip gate driving approaches with lower cost and lower complexity must be developed to fully leverage the benefits of these switches. Another area of future work for hybrid Si/SiC switches is packaging and integration to reduce the parasitic interconnect inductance mismatch between the two internal devices. Currently, the hybrid Si/SiC switch concept is being validated using two discrete devices. This approach however results in a parasitic inductance mismatch between the two devices, which in turn results in switching voltage ringing and increased switching energy loss for these devices.

The asymmetric alternate arm converter topology proposed in this dissertation lacks the dc-fault blocking and overmodulation operation capability since the stacks of submodules in the lower converter arms only generate positive arm voltage. This issue could be addressed by using full bridge submodules for the lower converter arms, but the converter part count will be increased if these submodule structures are used. Hence, either a new low device count submodule structure with dc-fault blocking capability or a new control strategy with dc-fault blocking capability would be necessary to keep the lower cost and lower footprint benefits of this HVDC converter topology, while enabling dc-fault blocking and overmodulation operation capability.