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Junction Temperature Estimation of Silicon Carbide Power Module using Internal Gate Resistance as Temperature Sensitive Electrical Parameter

Michael Sykes
University of Arkansas, Fayetteville

Junction Temperature Estimation of Silicon Carbide Power Module using Internal Gate Resistance as Temperature Sensitive Electrical Parameter

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Michael Sykes
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This thesis is approved for recommendation to the Graduate Council.

_____
Yue Zhao, Ph.D.
Thesis Director

_____
Roy McCann, Ph.D.
Committee Member

_____
Zhong Chen, Ph.D.
Committee Member

ABSTRACT

The junction temperature of a power module is measured non-intrusively and uninterrupted in its application by analyzing the dependency of gate resistance to temperature. The circuit configuration proposed consists of altering the gate loop path and adding a basic peak detection circuit with an added low-pass filter to accurately measure the small differences seen during a temperature change on the internal gate resistance. The testing on this Silicon Carbide power module shows that the internal gate resistance has a positive temperature coefficient. This causes the current and the voltage drop on the gate loop sensing resistance to reduce as the temperature rises. The voltage drops on the sensing resistance forms a steady downward linear slope that is used to establish an accurate estimation of the junction temperature. This implementation has future implications on a smart gate-driver board that can actively measure the junction temperature of the Silicon Carbide power module and shut off the module when approaching a critical failing temperature.

ACKNOWLEDGMENTS

I would like to thank my advisor Dr. Yue Zhao for his expertise and guidance while working under him as a research student. Through his instruction I was able to complete projects and learn invaluable knowledge that I will use throughout my career as an Electrical Engineer.

The support of my family, friends, and lab mates also made this process possible as they too have taught me more than I could have imagined and supported me immensely while pursuing this degree.

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CHAPTER 1

INTRODUCTION

1.1 Importance of Modern-Day Power Modules

Power semiconductor devices such as metal oxide field effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs) are essential power components used in a variety of electrical applications such as motor drives, power supplies, and inverters [1]. By packaging multiple of these respective devices together, certain circuits can be formed, otherwise known as a topology, to obtain a switching characteristic for a specific application. These topologies can provide constant uninterrupted power, protection, improved power density, increased efficiency, and are more reliable. The power modules also have other built-in components to provide protection, to limit voltage overshoots, and thermistors to measure internal temperatures [2].

The history behind power modules is a rather short one as they were first introduced into the market by Semikron in 1975. Innovations and upgrades have been added to these devices to improve their power density, cost, reliability, and protection. Along with changes in topology, these devices have come a long way, however even that first module is still used today showing the reliability of these packages [3]. As power demands have increased over the last 50 years these devices have been improved to adapt to these new requirements and applications but the significant jumps in the technology have only been introduced in the last 20 years. These jumps come at the base level of these modules, which is the design of the MOSFET/IGBT. The latest materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have improved power density and switching speeds over the traditional substrate Silicon (Si). There are several benefits to using SiC over Si. For example, SiC has a lower on-state resistance which decreases the losses during operation. Additionally, SiC can operate at much higher voltages, reduced leakage

current, and improved thermal conductivity in removing heat from the device, which this issue can lead to failure in any device if not properly regulated [4].

1.2 Silicon-Carbide Power Modules

Silicon Carbide power modules are slowly replacing their silicon counterparts as they are vastly superior options for high voltage and high current applications. With all the benefits of SiC over Si, there are drawbacks that pertain to SiC that must be addressed when these devices are used. With the significant advantage of being able to switch at much higher frequencies than Si, SiC devices tend to generate more heat and the improved thermal conductivity is not enough to counter this significant increase in heat generation [4]. This requires sensitive and more improved methods of junction temperature (T_J) monitoring in order to prevent failure and damage to the power module made of SiC semiconductor devices. Some modules have NTC thermistors already installed which can estimate T_J of a power module, but these components are typically non-linear, unstable when introduced to higher temperatures, and only have a narrow range of temperatures that can accurately be estimated [5]. Other methods have been introduced to measure T_J of a SiC power module, such as infrared cameras, a direct contact to the inside of the power module, and temperature sensitive electrical parameters (TSEP). All these methods are viable in determining what T_J is and when the device may fail, however these methods all have their drawbacks. The infrared camera is very expensive and might not be as accurate as a direct contact relation. A direct contact relation will give an accurate estimation of T_J but could easily affect the operation of the power module and requires exposing the module which could have adverse effects to the power module overall [6]. The last method of using a TSEP might not necessarily be as accurate as some of these other methods, but it can be very cost-effective, relatively accurate, and does not affect the normal operation of the device which makes it an

ideal candidate in being used as the method to measure T_J and monitor when failure may occur on the device. There are other problems that SiC devices have such as increased electro-magnetic interference (EMI) which can affect other measured values by adding noise to the signal. The scope of this project does not cover reducing EMI for the device, however improved shielding and adopting other techniques to reduce EMI would provide improved waveforms and more accurate temperature estimation.

1.3 Temperature Sensitive Electrical Parameters

The use of temperature sensitive electrical parameters as a means of measuring T_J of the power module have become more applicable as technology has evolved to obtain more sensitive fluctuations. These parameters typically only fluctuate in a miniscule amount, in the hundredths or thousandths range, thus requiring sensitive equipment with good resolution to obtain an accurate measurement and estimation of T_J. Many of these parameters have accurate linear relationships with T_J and hold their value much better than other methods. The TSEP methods can be more cost-effective than that of other methods depending on the parameter that is used to estimate the temperature and the sensitive equipment required for the measurement. These TSEPs can be classified into two different categories, static and dynamic. Dynamic TSEPs are parameters that are taken during the on/off transition of the module while static measurements are taken during the on/off state. In Table 1 below, a list of common TSEPs can be seen and are classified in their respective categories of static or dynamic [7].

Table 1: Static vs Dynamic TSEPs [7]

TSEPs	
Static	**Dynamic**
Short Circuit Current I_{sc}	Miller Plateau Voltage V_{gp}
Saturation Current I_{sat}	Threshold Voltage V_{th}
Leakage Current I_{lk}	Maximum Voltage Rate dV/dt_{max}
Saturation Voltage V_{sat}	Maximum Current Rate dI/dt_{max}
Voltage at High Current $V_{ce(on)}$	Internal Gate Resistance Rg_{Int}

Knowing when these electrical parameters occur are important in determining when the measurement should take place. However, there are still many parameters to be considered at this point, thus it helps to narrow down the list even further. A TSEP with a dependency only on T_J would be the ideal choice for estimation. If a TSEP had another dependency, then every time that other specific variable would change the TSEP relationship with T_J could change in unforeseen ways. This does not mean that these TSEPs do not work, but that if any of the other dependencies changed then the relationship established would change and a new relationship would have to be researched and established to accurately measure T_J. Based on the dependency table below in Table 2, there are two TSEPs that fit our definition of an ideal parameter in the estimation of T_J, threshold voltage and the internal gate resistance.

Table 2: Dependencies of Various TSEPs [8]

TSEP	**Dependencies**
Short Circuit Current	T_J, V
Saturation Voltage	T_J, I
Threshold Voltage	T_J
Turn-on Delay	T_J, V, R_g
Turn-off Delay	T_J, V, I, R_g
Internal Gate Resistance	T_J
Rise-Time/Fall-Time	T_J, V, I, R_g
Saturation Current	T_J, V
Maximum Voltage/Current Rate	T_J, V, I, R_g

Along with this dependency table, it is also pertinent to look at what the typical relationship with these TSEPs and T_J are. In Table 3, threshold voltage has good linearity, sensitivity, and online measurement is feasible. The peak gate current, which changes based on the internal gate resistance fluctuating because of T_J shifting, is dependent upon the design of the gate and the module being used. Other TSEPs are listed as a comparison, but when the sensitivity is only good at slow switching, it defeats the purpose of having a SiC power module which is why those TSEPs were not considered.

Table 3: TSEP Linearity and Sensitivity [9]

TSEP	Linearity	Sensitivity	Online Measurement
Threshold Voltage	Good	Good	Feasible
Internal Gate Resistance	Good	Good	Feasible
Turn-on *di/dt*	Intermediate	Good at Slow Switching	Feasible
Turn On Delay	Good	Good at Slow Switching	Feasible
Turn Off Delay	Good	Good at Slow Switching	Feasible

In the subsequent sections below, the threshold voltage and the internal gate resistance will be considered in determining the optimal choice of accurately determining the junction temperature of a SiC power module non-intrusively and without changing the operation of the module.

1.3.1 Threshold Voltage

The threshold voltage is the required voltage on the gate needed to form a channel between the drain and source to conduct current. This method is classified as a dynamic parameter and must be acquired during a turn-on state which can present acquisition challenges. This parameter must be measured at a precise time with a precise measurement otherwise it could completely skew the relationship of T_J. Certain measurement concepts have been researched, introduced, and proven to work. Methods researched used the voltage drop over the parasitic inductance between Kelvin and the power source as the trigger for the data acquisition unit (DAQ). Along with that triggering system other electrical equipment was added to prevent

false triggering since the circuit would be switching on and off at a very high frequency and could be susceptible to electro-magnetic interference (EMI) causing a false trigger. A D-flip flop can reduce the chances of a false trigger significantly and can be adjusted to change the voltage trigger of the measurement. This method also has high sensitivity as compared to other TSEP methods with a negative coefficient of 2-15 mV per degree of Celsius depending on the module. An example of this method can be viewed below where a differential probe is waiting for a voltage drop over the Kelvin to Power Source inductance to trigger and to pass through a D-flip flop that closes the circuit. The signal is then passed on to the microcontroller to take the measurement at that exact moment when the channel is formed [10].

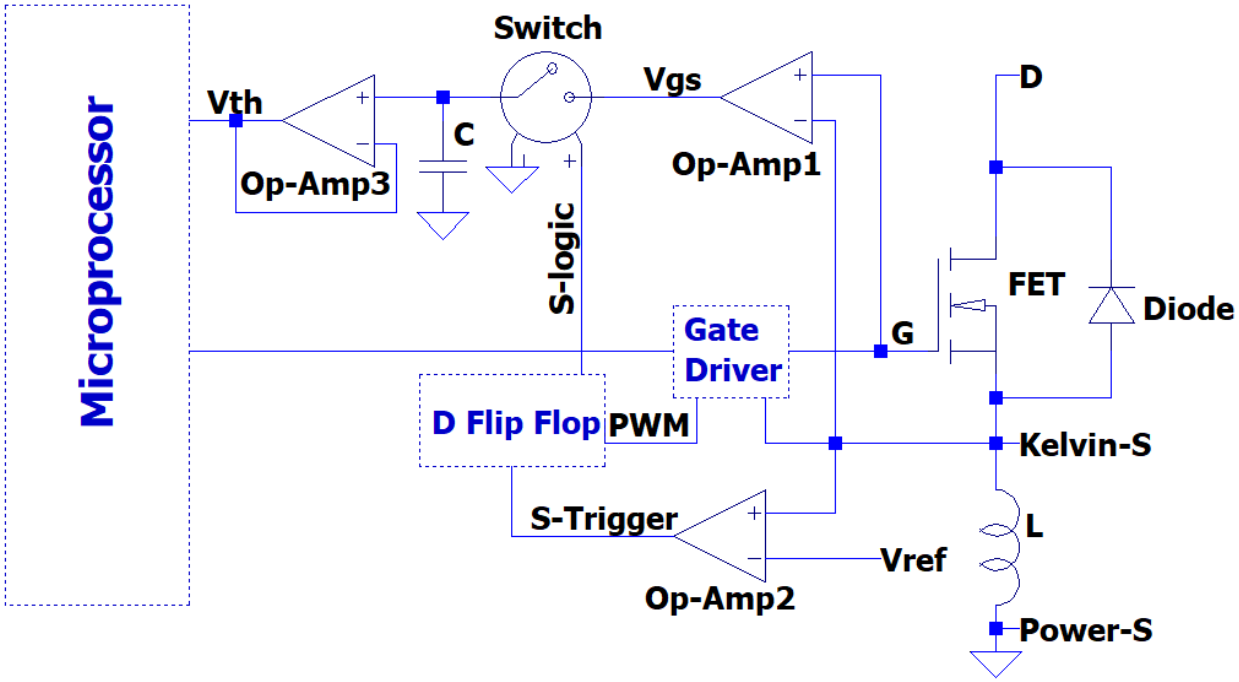

Figure 1: Example of Threshold Voltage TSEP [10]

Another representation of when the threshold measurement would be taken can be seen below. This figure is taken directly from a switching test on the power module being used in this test. The threshold voltage would be taken during the specific time as indicated on the figure.

This is when the voltage applied forms the channel for current to pass from the gate to the source of the MOSFET.

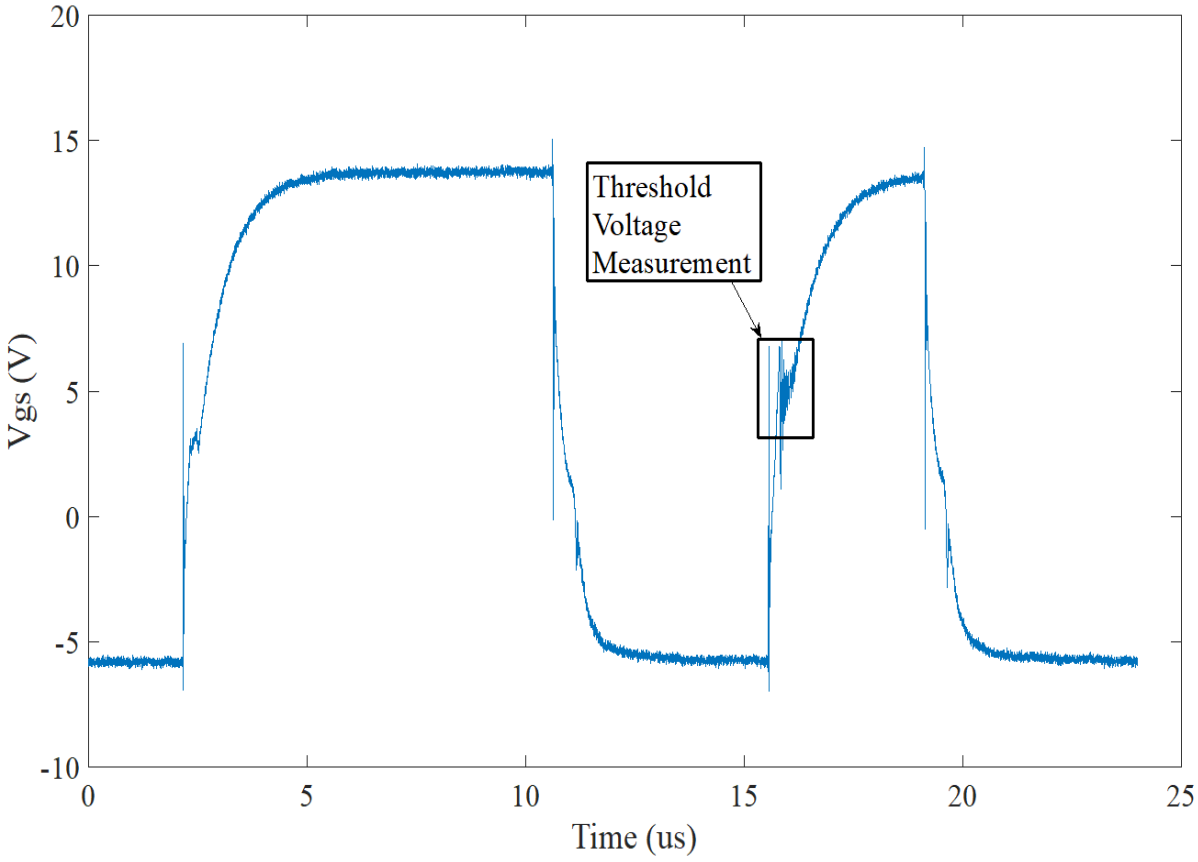

Figure 2: Threshold Voltage Measurement Acquisition

1.3.2 Internal Gate Resistance

The internal gate resistance (R_{gINT}) of a power module changes with respect to T_J. This TSEP method is also classified as dynamic meaning that the acquisition of this circuit will happen during on/off transitions during operation of the power module. However, a significant advantage is the acquisition of the measurement of this method over the threshold voltage TSEP. This method requires the peak value of the voltage drop or gate current over the external gate resistance (R_{gEXT}) which significantly reduces the effort put forth on timing a measurement. In the circuit below, when the semiconductor device is conducting, the resistor R_{gINT} forms a series

circuit with R_{gEXT}, the capacitance between the gate and source (C_{ge} in the figure below), and the gate driver [11].

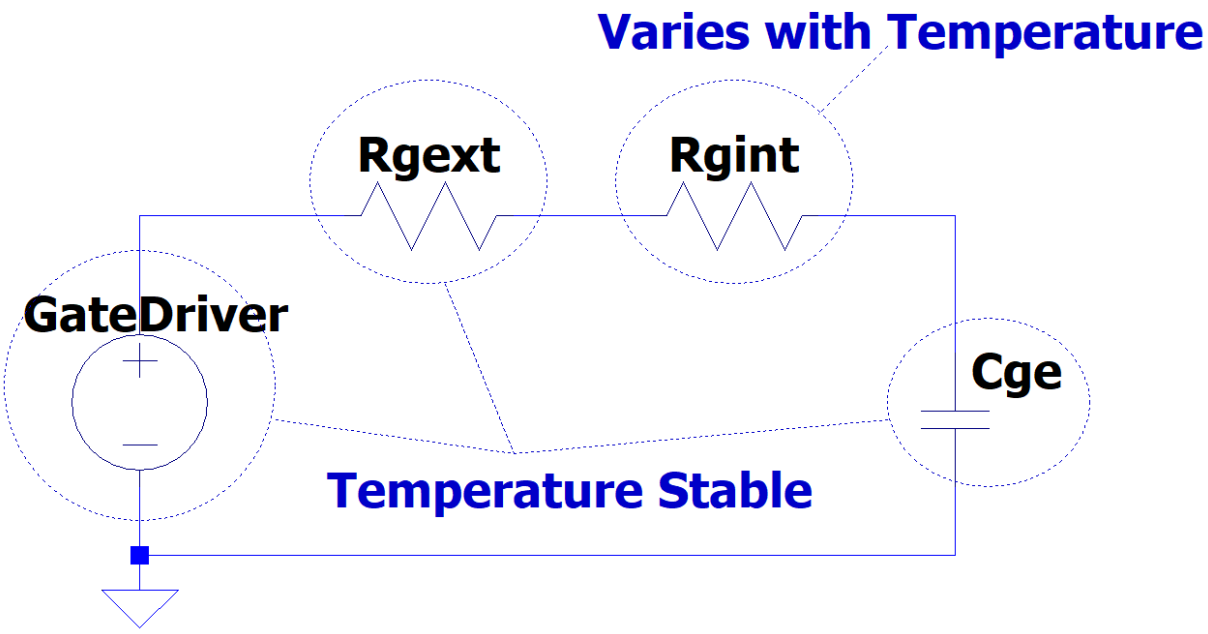

Figure 3: Internal Gate Resistance TSEP Gate Loop Path [11]

Three out of the four of these components are stable with respect to temperature and therefore as the temperature within the module changes it will alter R_{gINT}. When R_{gINT} is adjusted, the total closed loop resistance changes. This makes it possible for the relationship of T_J to R_{gINT} to be related to R_{gEXT} or the gate current (Ig) instead. The parameter R_{gEXT} will have a small change in the voltage drop over it as the total resistance of the circuit changes with respect to T_J. This change will also affect the peak current being supplied at the gate during turn-on of the MOSFET, thus relationships between T_J and the voltage drop on R_{gEXT} (V_{RgEXT}) or the peak gate current ($I_{g\text{-}peak}$) can be established. These parameters are much easier to accurately measure during the operation of the power module and the peak value is required for comparison instead of a specific value at a specific time as seen in the acquisition of the threshold voltage. The T_J can be related to R_{gINT} also but would require using Ohm's Law to determine the resistance. This

would be adding more steps to estimate the temperature and establish a relationship, but whether the variable is a voltage, current, or resistance, all of them provide the same relationship. This method provides a resolution of 2-5 mV change per degree Celsius for V_{RgEXT}, a 1-3 mΩ change per degree Celsius for R_{gINT}, or a 0.5-1 mA change per degree Celsius for $I_{g\text{-}peak}$ [11].

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CHAPTER 2

Temperature Sensitive Electrical Parameter Measurement Viability

2.1 Simulated Viability of TSEP

Although other papers reported on the viability of internal gate resistance as a TSEP, a simulated and experimental study to determine this was still required in order to confirm their results. It was also important to make sure the module being used behaves the same as other power modules since TSEP testing has not been attempted on this power module. A simulation was implemented using a SiC discrete switch by Wolfspeed that included temperature dependent parameters. The power module being experimentally tested on is a HT-3234 SiC 1.7kV MOSFET made by Wolfspeed, so a model similar to that and made by the same company was used because Wolfspeed did not have a model readily available to simulate the exact module being used in the experiment. This simulated setup can be analyzed below in Figure 5, showing an increasing temperature jump of 25 ˚C from 0 ˚C to 150 ˚C as V_{RgEXT} is analyzed.

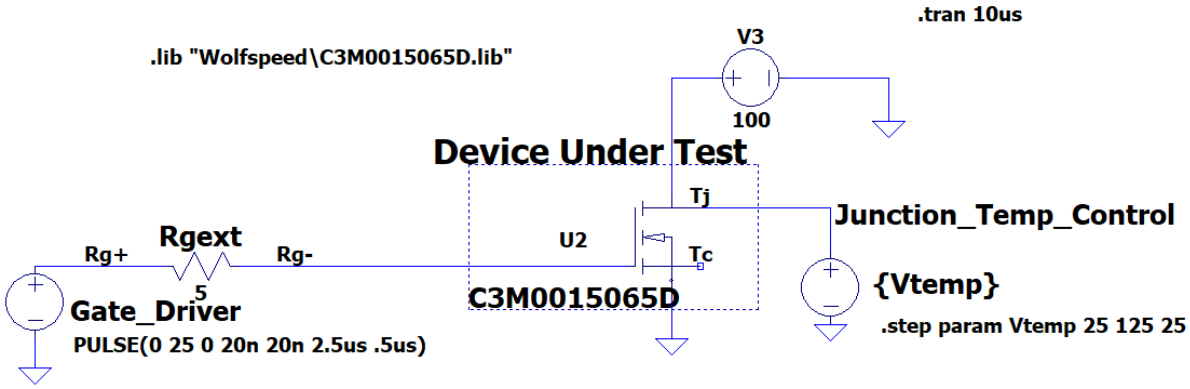

Figure 4: Gate Resistance TSEP Simulation Using LTspice

Using LTspice as the circuit simulation software, the voltage drops over R_{gEXT} were simulated as the device was turned on and off and produced results that can be seen below in Table 3. Along with the voltage drop, the peak gate current at that time was extrapolated by dividing the peak voltage drop by the resistor value of 5 Ω.

Table 4: Simulated Gate Resistance TSEP Results

Junction Temperature (°C)	Peak Voltage Drop on Rgext (V)	Peak Gate Current (A)
0	1.9719	0.39438
25	1.8771	0.37542
50	1.7846	0.35692
75	1.6979	0.33958
100	1.6168	0.32336
125	1.5365	0.3073
150	1.4630	0.2926
Relationship	-3.393 mV/°C	-0.679 mA/°C

The relationship established by the simulated results follow the experimental results reported previously in section 1.3.2 of a 2-5 mV/˚C or a 0.5 – 1 mA/˚C [1]. This relationship also showed an accurate and steady linear relationship with an R^2 value of 0.99 shown below in Figure 5.

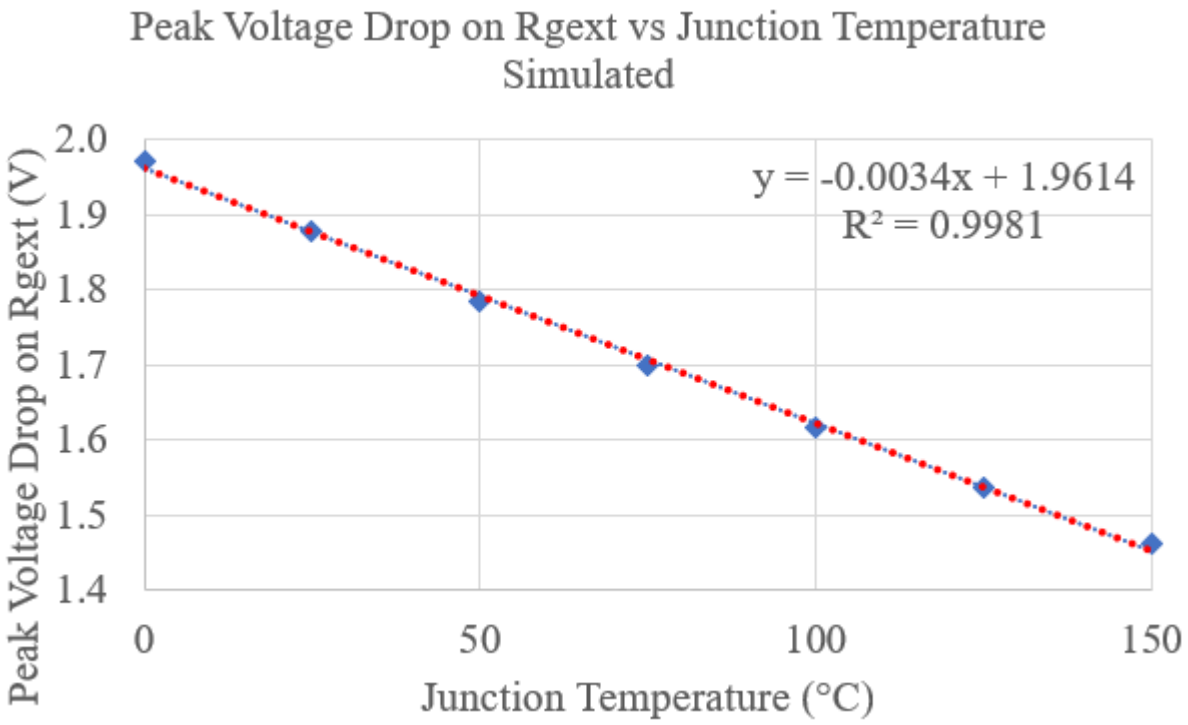

Figure 5: Simulated V_{RgEXT} and T_J Relationship

This means the estimated value obtained in relation to T_J would be a very accurate and linear estimation in the simulation. The peak gate current would also have the same approximate relationship since that value can easily be extrapolated from the peak voltage drop and is only 5 times smaller. In terms of measurement in experimental terms it would be easier to obtain the peak voltage drop over the peak current. The peak voltage drop will also have better resolution than the peak current because it is five times larger. The threshold voltage was not simulated but was considered in the initial viability of TSEP experimentally.

2.2 Test Setup and Assembly

The measurements obtained in this initial experiment were performed using a Double Pulse Test (DPT) and recorded with a Tektronix 6-Channel Oscilloscope. The DPT was setup through MATLAB Simulink and sent to a Digital Signal Processor (DSP) where the commands were then sent to the ITGD2-3011 gate driver made by Wolfspeed. A DPT is the preferred method for measuring the switching parameters of a MOSFET or IGBT. It consists of two pulses sent to the gate of the MOSFET. This type of testing is very controlled and can test the operating conditions of the module and the efficiency [2]. This method was also chosen because of its short testing time thus reducing the amount of heat generated solely by operation, giving a much more reliable temperature estimate. The DPT is ideal considering the parameter being measured happens only during the switching transition. It can be understood that this testing method is best for obtaining a relationship of this TSEP because it does not generate heat and reliably obtains the switching parameters of the module. However, the end result will be operated continuously and the DPT is used for characterization with temperatures for accurate estimation. A hot plate was used to set the case temperature and the module sat on the plate for roughly five to ten minutes before each test was ran. The amount of time the module stays on the hot plate before a

test allows the case temperature and junction temperature to be approximated to the same temperature. The power module used for this experiment was the HT-3234 SiC 1.7kV MOSFET from Wolfspeed. The hot plate used in this experiment is a Cole-Parmer Stable Temp Ceramic Hot Plate. Safety requirements were also thoroughly followed as this test was ran at 1.2 kV and 250 A of current. The test-setup can be viewed in Figure 6 below and points out all equipment relevant to the test.

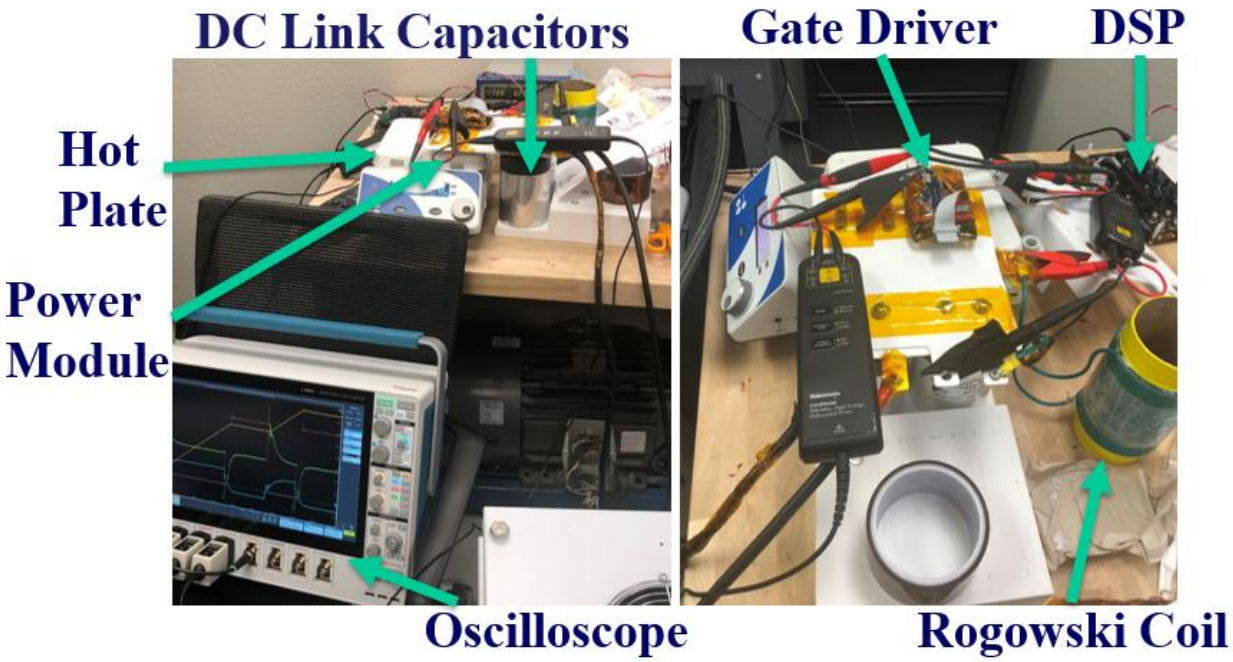

Figure 6: Experimental Test Setup for Viability of TSEP

During the test, probes were connected to measure V_{gs}, V_{RgEXT}, V_{ds}, and I_{Load}, which respectively are known as the gate-to-source voltage, the voltage drop over external gate resistance, the drain-to-source voltage, and the load current. With these parameters the internal gate resistance and threshold voltage were both tested as viable TSEPs and related to the junction temperature. The measurements took place in intervals of 15 ˚C starting at 25 ˚C and ending at 100 ˚C. Three separate DPT tests were performed at each temperature and a moving average was established on the results through MATLAB to obtain smooth and clear results with no

significant and abrupt voltage spikes that could skew the results. These voltage spikes that were smoothed out were most likely a result of EMI due to the high frequency switching of the power module.

2.3 Results of Viability

While analyzing the results there was a clear linear pattern established by the results for the peak of V_{RgEXT}. As the temperature was rising the voltage was falling at a rate of -3.973 mV/˚C. These results align closely with the simulation that was performed which fell at a rate of -3.393 mV/˚C. The experiment performed better with higher resolution which could be the difference between the discrete switch and the power module used. These results can be analyzed below in Figure 7 and Table 5 which display the peak averaged voltage drop values. Figure 8 show the peak V_{RgEXT} versus T_J and a clear linear trendline is established with an R^2 value of 0.99 as also seen in the simulated results.

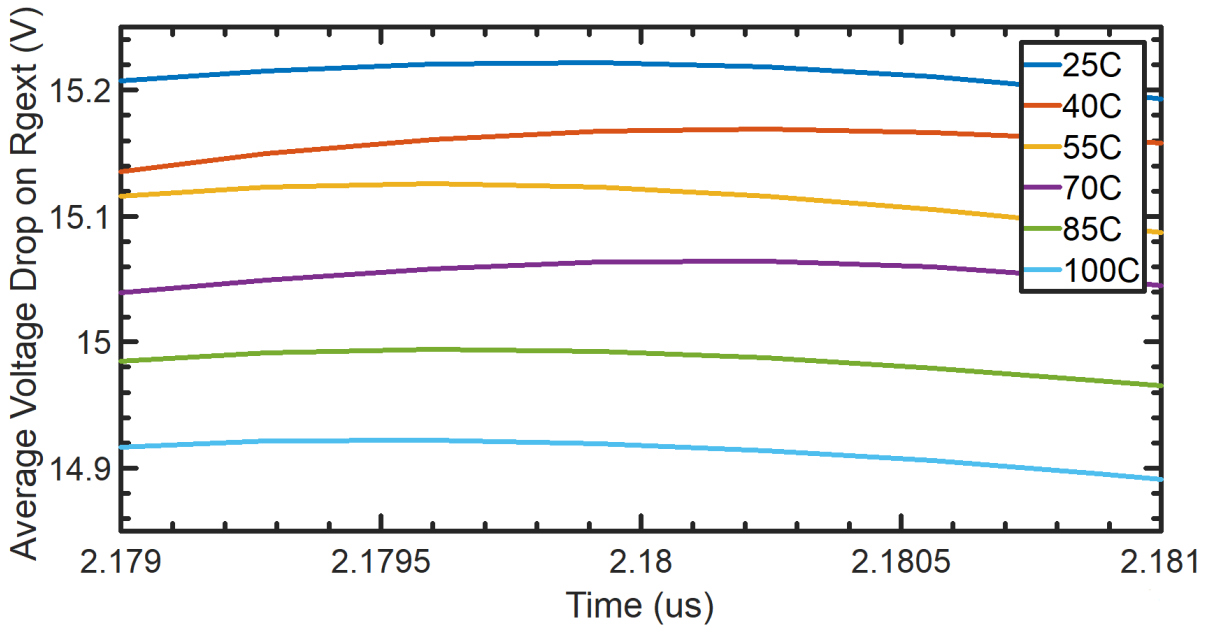

Figure 7: Experimental Results of Peak V_{RgEXT} vs Time with Varying Temperature

Table 5:Experimental Results of V_{RgEXT} and I_g Across Temperature

Junction Temperature (°C)	Peak Voltage Drop on Rgext (V)	Peak Gate Current (A)
25	15.2219	3.0444
40	15.1689	3.0338
55	15.1258	3.0252
70	15.0644	3.0129
85	14.9939	2.9988
100	14.9220	2.9844
Relationship	-3.973 mV/°C	-0.795 mA/°C

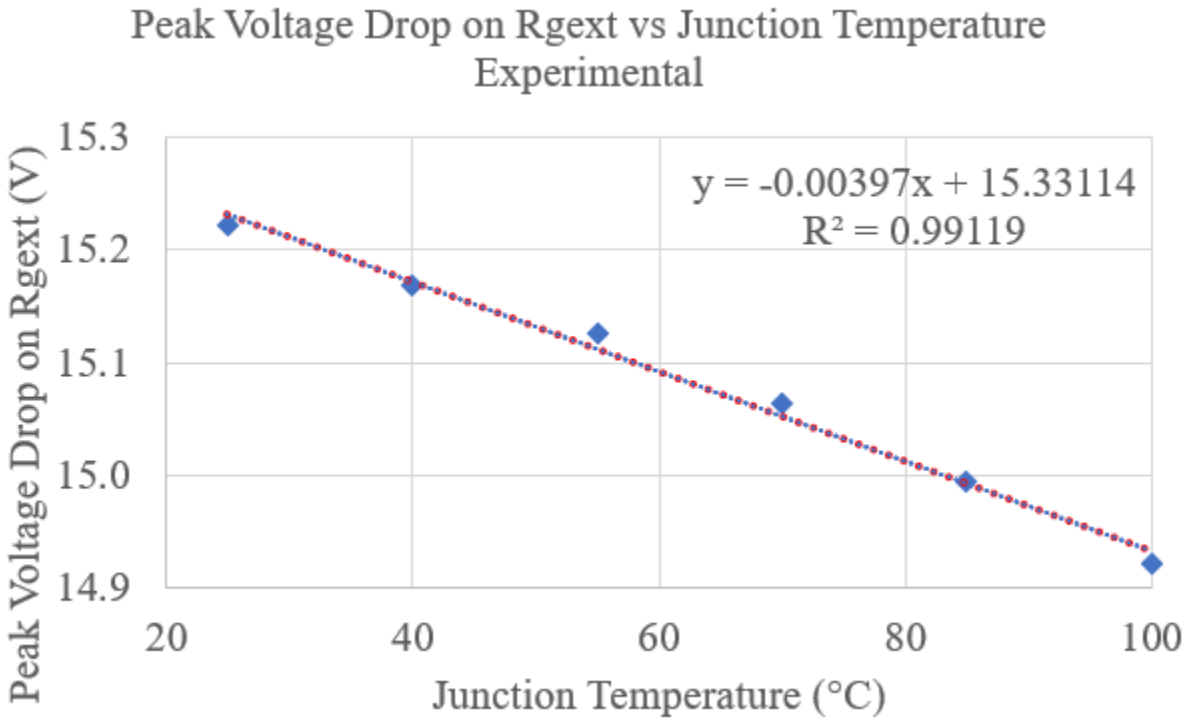

Figure 8: Viability Experiment of V_{RgEXT} vs T_J Relationship

From these same results the viability of the threshold voltage was also considered. The graphs had to be visually inspected, and values adjusted to determine the threshold voltage at each temperature because it would form the channel at different times due to the change in the junction temperature.

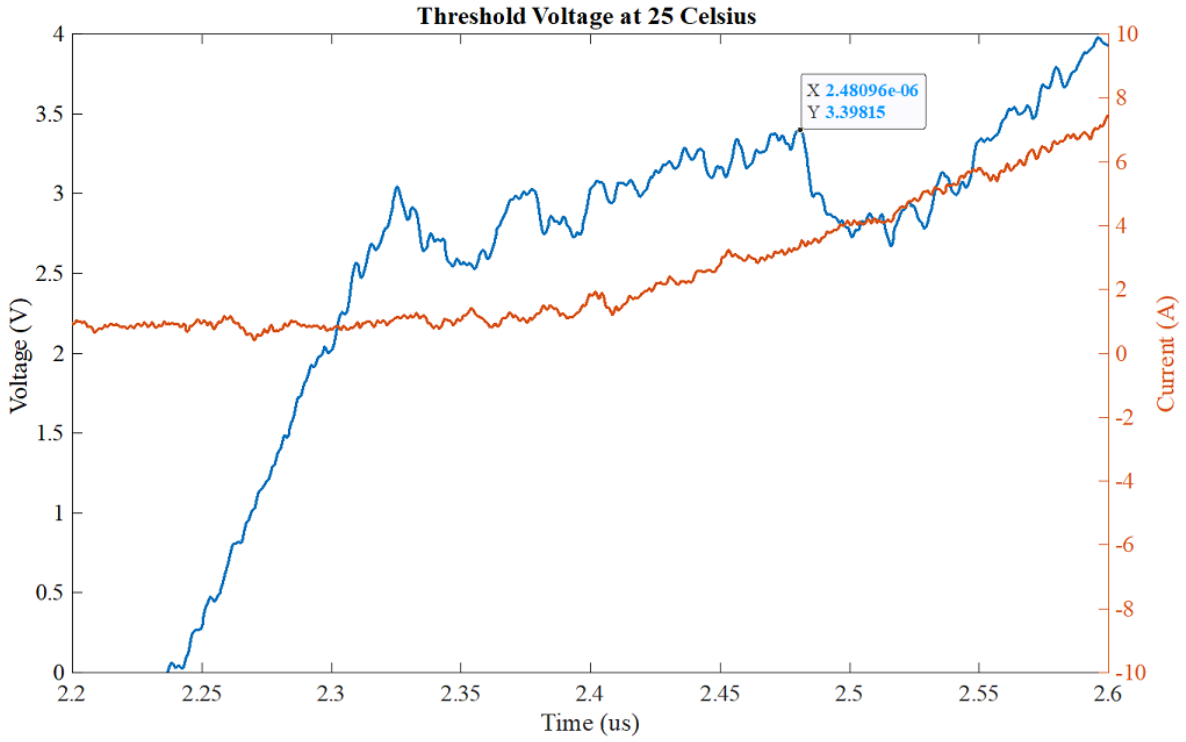

Figure 9: Viability of Threshold Voltage 25˚C

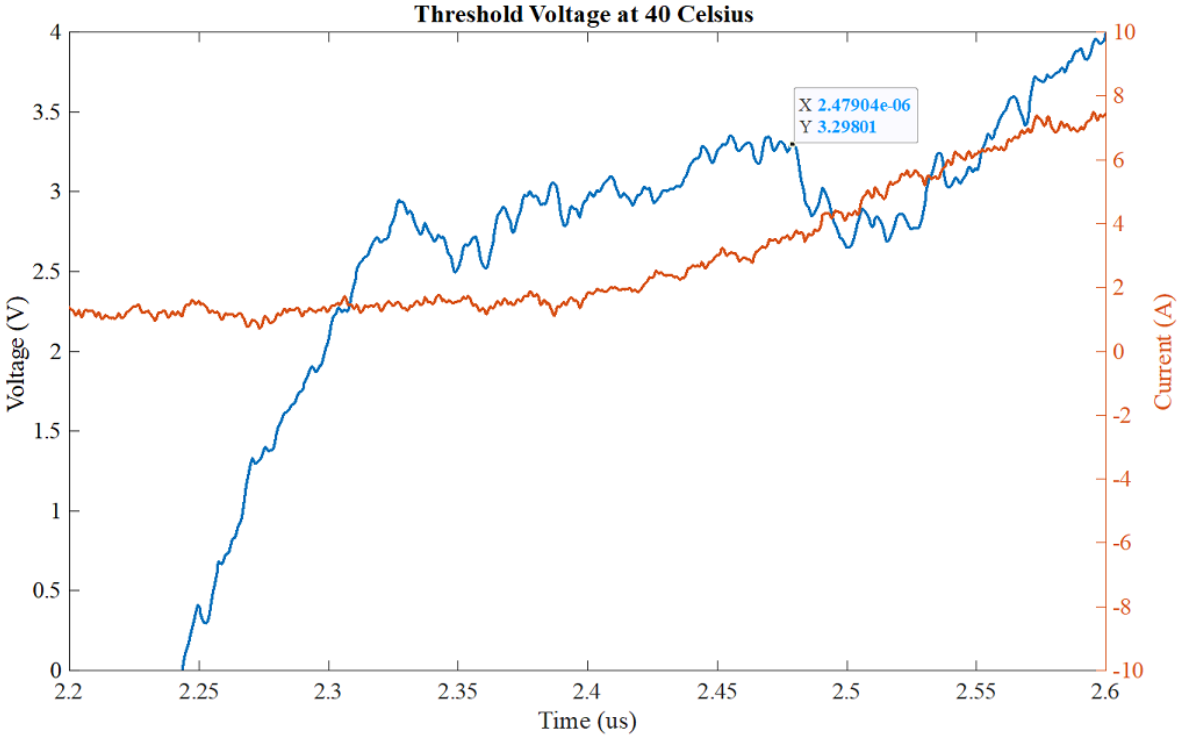

Figure 10: Viability of Threshold Voltage 40˚C

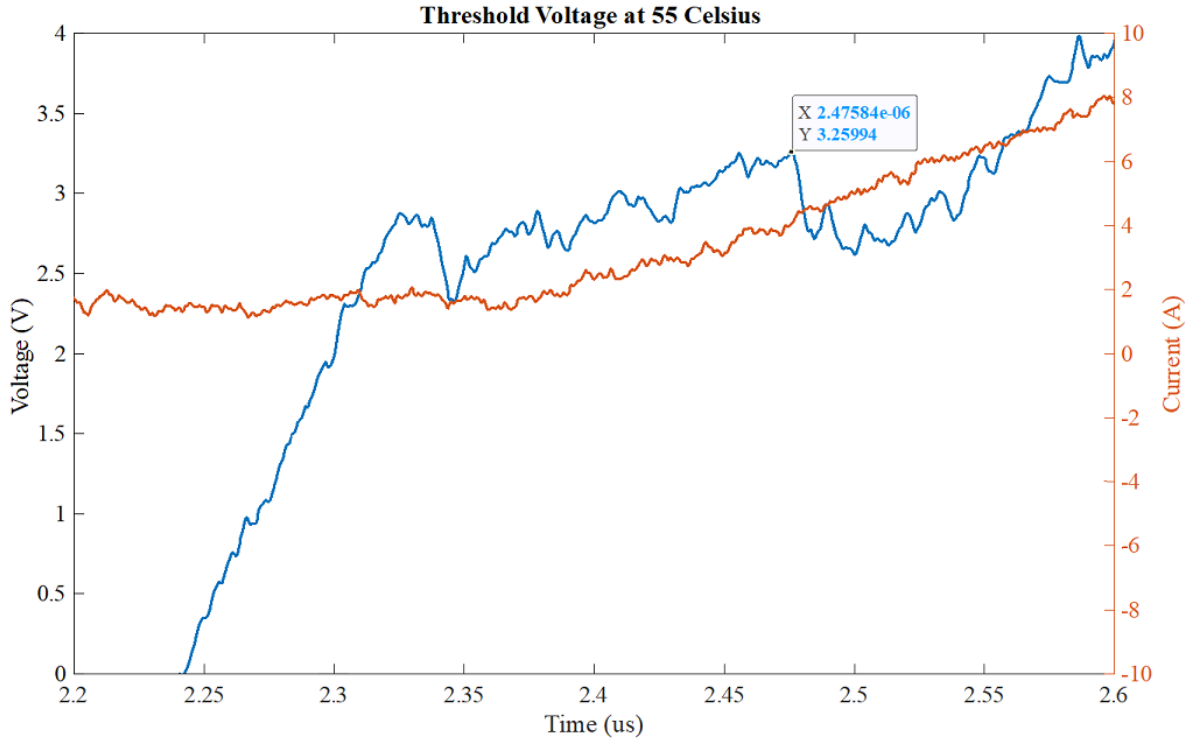

Figure 11: Viability of Threshold Voltage 55˚C

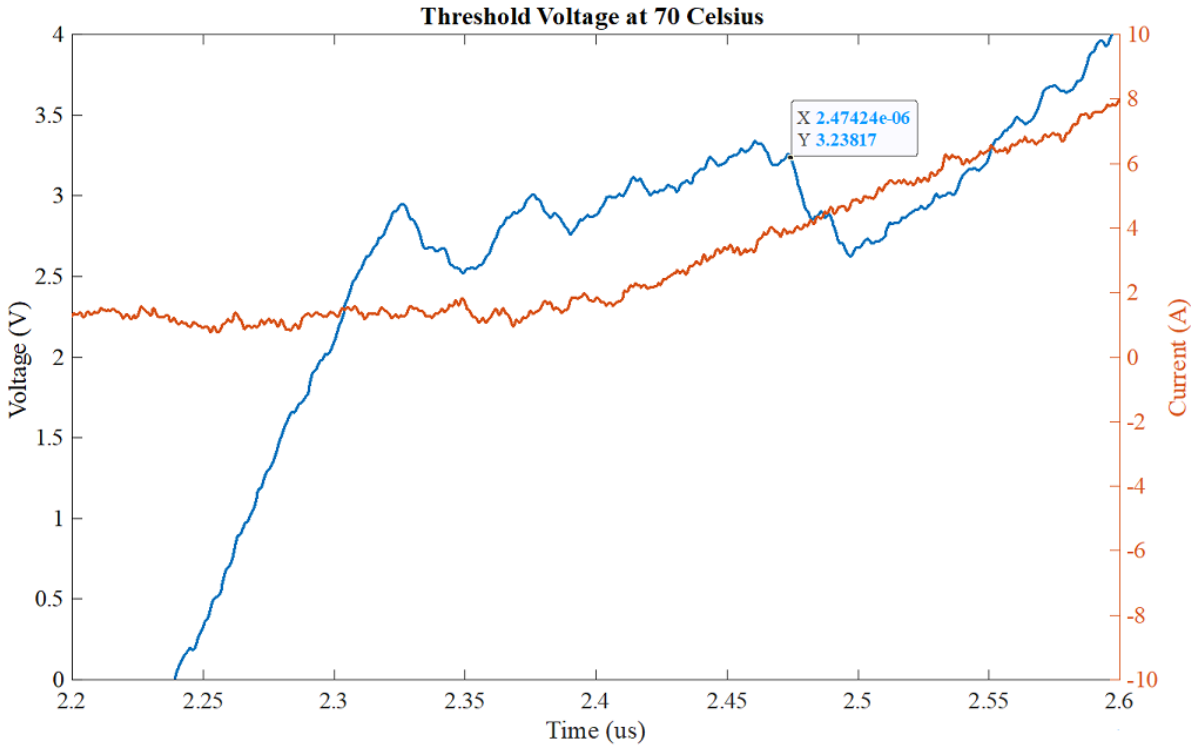

Figure 12: Viability of Threshold Voltage 70˚C

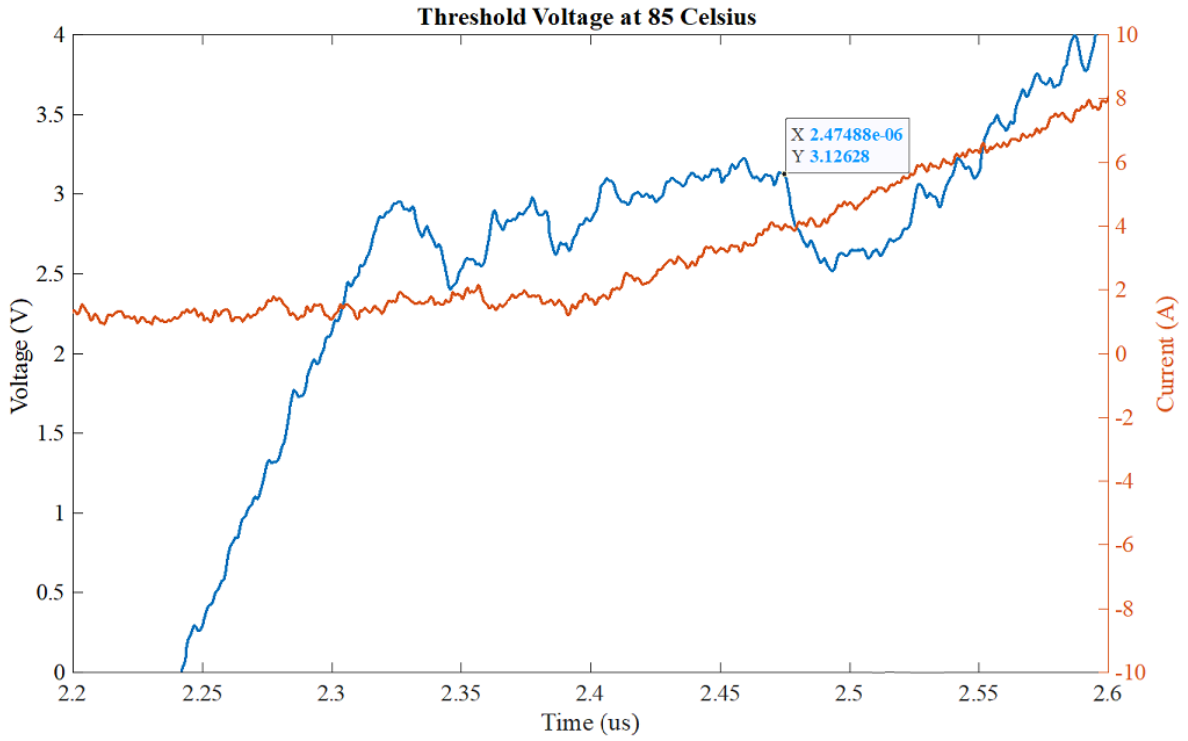

Figure 13: Viability of Threshold Voltage 85˚C

Table 6: Threshold Voltage vs Temperature

Junction Temperature (°C)	**Threshold Voltage (V)**
25	3.39815
40	3.29801
55	3.25994
70	3.23817
85	3.12628
Relationship	-4.02387 mV/°C

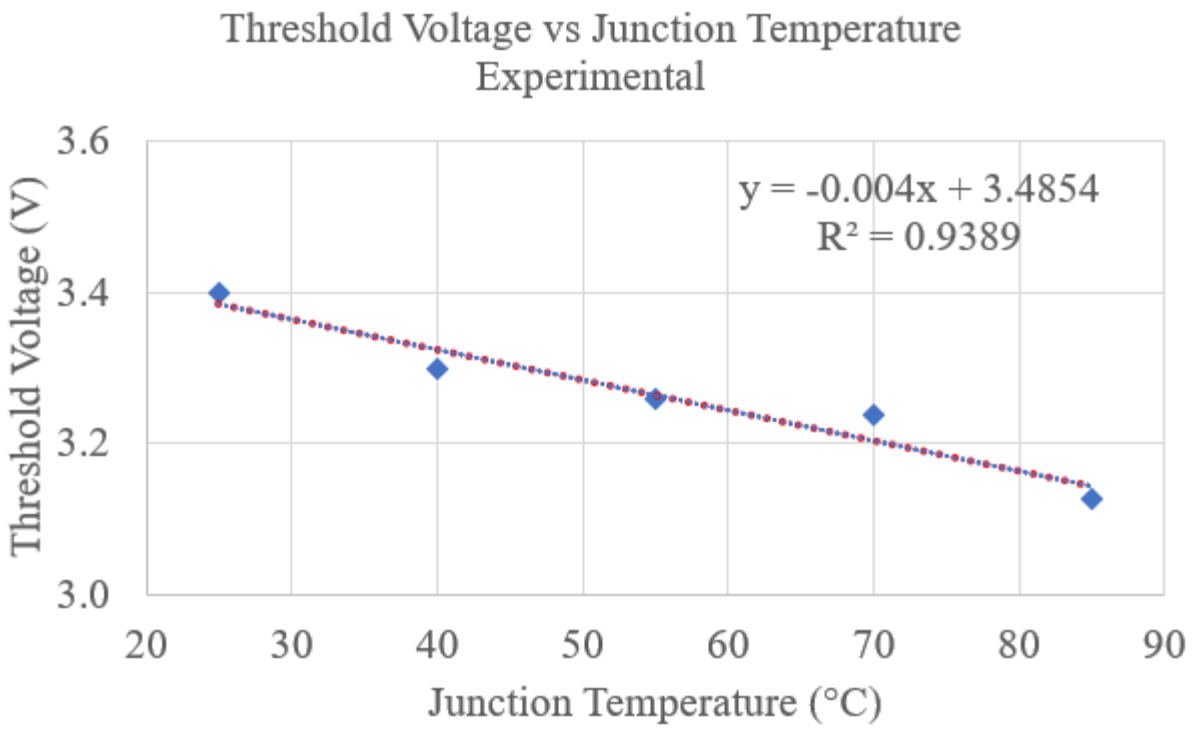

Figure 14: Viability Experiment of V_{TH} vs T_J Relationship

From the experimental results, values had to be estimated and determined for the threshold voltage as seen in Figures 9-13. These values, that are reported in Figure 14, show that the threshold voltage linearity was not as accurate as the internal gate resistance, and it could have human error incorporated in the results as all data points were general estimation from the graphs. These data points were not triggered from the voltage drop of the kelvin to power source inductance, as seen in Figure 1, which would have given more consistency and less guess work of the value. Although the measurement for both TSEPs happen at specific times, it is much easier to tell when a value is at its maximum versus in the middle of a rising voltage waveform when the MOSFET starts conducting. The R^2 values for the gate resistance TSEP was 0.99 while the R^2 value for threshold voltage TSEP was only 0.94. Both R^2 values are very close to 1, but the gate resistance TSEP shows a more consistent linearity which is essential for a more accurate junction temperature estimation. Using the internal gate resistance as the TSEP has easier

acquisition, better linearity, and is more accurate. The only advantage threshold voltage had over the internal gate resistance in experimentation is the resolution was slightly higher at -4.02387 mV/˚C, which follows the 2-15 mV/˚C discovered in research, but human estimation and error play a significant part in that value [3]. In the end, the internal gate resistance was chosen over threshold voltage as the TSEP to be pursued in this experiment because of its easier acquisition, greater linearity, and greater accuracy.

2.4 References

[1] N. Baker, S. Munk-Nielsen, F. Iannuzzo and M. Liserre, "Online junction temperature measurement using peak gate current," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1270-1275, doi: 10.1109/APEC.2015.7104511.

[2] H. Al Fahel, “Evaluate Power Device Efficiency with Double-Pulse Testing Using an AFG,” Power Electronics, 05-Dec-2019. [Online]. Available: https://www.powerelectronics.com/technologies/power-management/article/21864518/evaluate-power-device-efficiency-with-doublepulse-testing-using-an-afg. [Accessed: 2021].

[3] H. Yu, X. Jiang, J. Chen, J. Wang and Z. J. Shen, "A Novel Real-Time Junction Temperature Monitoring Circuit for SiC MOSFET," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 2605-2609, doi: 10.1109/APEC39645.2020.9124486.

CHAPTER 3

Initial Daughterboard Circuitry and Design

3.1 Peak Detection Circuitry

The end goal of this experiment is to find a reliable addition to the gate driver that can accurately and non-intrusively measure T_J. With this process in mind certain design implications are considered before even starting on how to measure V_{RgEXT}. Since the possibility of integration with the gate driver board in the future must be considered, the board must be powered by the same voltage as the gate driver board. This means the power voltage applied to any integrated circuits (ICs) on the board would be a max of 12 V, the same as what powers the gate driver. The signal being measured is specifically the voltage drop over a resistor so that voltage value must be isolated before the peak value is measured. When it was measured by the oscilloscope for viability, a differential probe was used to isolate the signal. Instead of a differential probe a differential operational amplifier (OP amp) was used in its place to isolate the voltage drop signal for the board. The voltage drop recorded during the viability test of the TSEP showed that the voltage maximum was higher than 14 volts. With the design implication of a 12 V power supply on the ICs, the voltage drop must be reduced so it can properly be processed through the ICs on the board. In this case the voltage drop signal must be reduced before the output of the differential amplifier, so a resistor network is applied so that the differential OP amp cuts the signal in half [1]. The downside to cutting this signal in half is that it also reduces the resolution in half. In determination of the differential OP amp that must be used to isolate the signal, other factors must be included before selection of the component. One important factor is the speed of the signal. Since the module in question is a SiC power module, the switching frequency can get very high and thus an OP amp with a very high slew rate must

be used to keep up with the higher frequency switching which results in a faster than normal spike in voltage than traditional OP amps can handle. In the initial circuitry design of this board, the peak detection circuit was considered and then modified to achieve the goals of this experiment. First, the operation of a simple peak detection circuit is considered. The original peak detection circuit consists of a diode and a capacitor as pictured below in Figure 15.

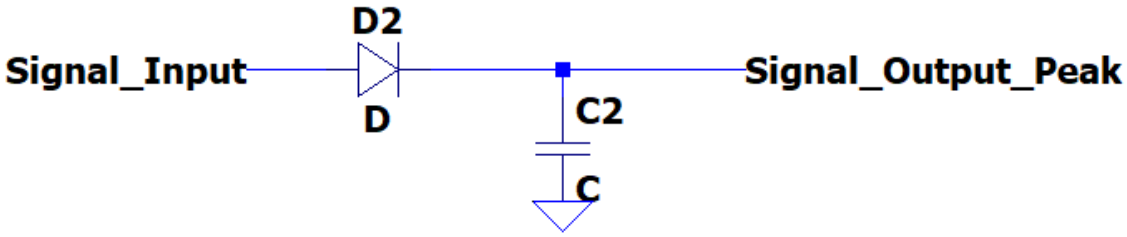

Figure 15: Basic Peak Voltage Detector Circuit

When the diode is conducting, the peak value of the signal is being held on the capacitor. When the voltage signal goes lower than the peak value already on the capacitor, the cathode is then higher than the anode on the diode and it stops conducting. The diode then only conducts when the anode has a higher voltage value than the cathode. However, this method will not hold the exact peak as there is a voltage drop over the diode, so the peak value held by the capacitor is the input voltage minus the voltage drop over the diode [2]. The diode selected is a Schottky diode as to assure a fast response time from the component since it is an integral part in the peak detection process, and it typically has a low voltage drop of around 0.3V. At the output of the diode is a capacitor that holds the peak value. When that capacitance is paired with a resistance as seen in Figure 16, the time it takes for the voltage to discharge off the capacitance can be calculated with the RC time constant, τ, which the equation can be found below the previously mentioned figure [3].

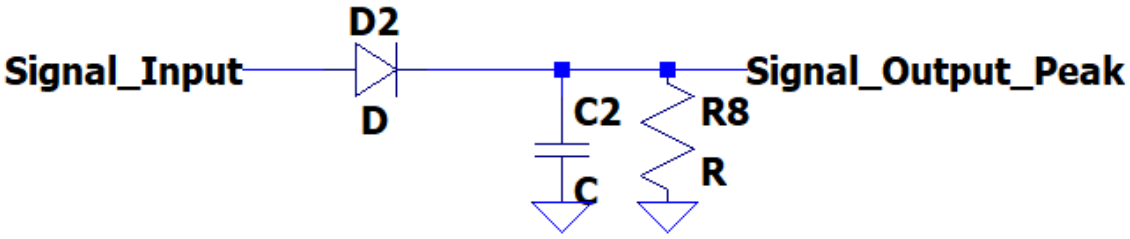

Figure 16: Peak Voltage Detection Circuit with Discharging Resistor

$$\tau = RC = \frac{1}{2\pi f_c} \quad (1)$$

The time in seconds it takes the capacitor to charge or discharge up to 63.2% of a DC voltage applied is equivalent to the equation above. For the capacitor to be considered fully charged or to fully discharge takes approximately five times the time constant that was calculated and the capacitor then holds 99.3% of the DC voltage applied which is approximately 100%. When choosing the time constant needed for this application, you take the time it takes for the peak drop to happen on the resistor and divide that time value by five to acquire the time constant needed [3]. This voltage held on the capacitance needs to bleed off because of the relationship between T_J and the peak voltage. A lower temperature will show a higher peak voltage drop so the circuit cannot hold the peak voltage indefinitely otherwise it would never be able to detect a lower peak voltage drop indicating a higher temperature. The capacitor and the resistor had to be carefully chosen to provide a time constant that was short enough to charge up to the desired peak in time but also to discharge so a new peak value could be obtained on the next switching cycle. A voltage follower was applied after the capacitor so the output would have a constant resistance as to not alter the RC time constant depending on what the output of the peak detector circuit was connected to. The OP amp used for the voltage follower had a constant input resistance in parallel with a load resistance that was used to set the time constant. It must be considered that since this prototype board is used for characterization of the

relationship of T_J to V_{RgEXT}, that the time constant needs to be small so the peak detector can reach steady state with as few pulses as possible and hold the peak voltage long enough for characterization. The time constant on the prototype board is around 1µs and with the high frequency switching that is seen by this module, this time constant should be ideal for holding a continuous peak voltage on the output with variations coming from the change in temperature. An OP amp was added as a voltage follower before the diode to create a "super-diode", which in theory results in no drop on the diode, so the modified peak detector circuit shown below in Figure 17 should truly hold the peak value with no drop from the diode [4].

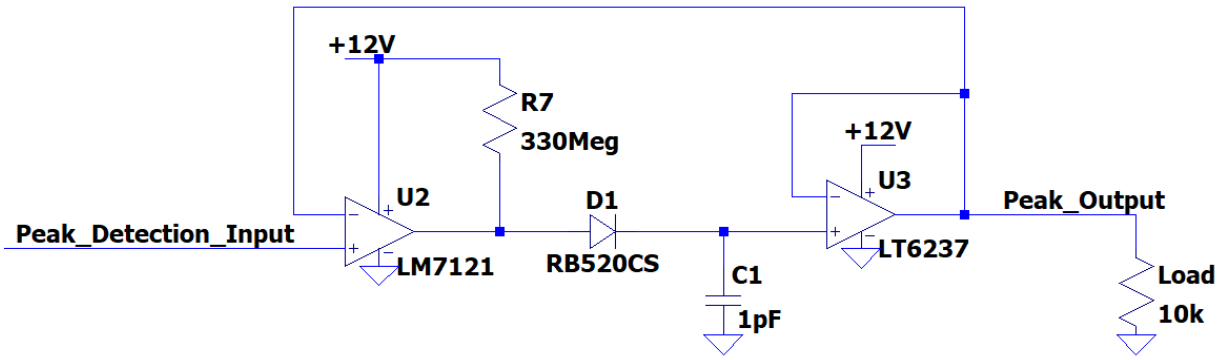

Figure 17: Modified Peak Voltage Detector

All components used in this circuit had to have a fast-operating speed to ensure the peak voltage was being detected. The high frequency applications for these modules require high slew rate OP amps, fast response Schottky diodes, and a small RC time constant in order to process the necessary information and can adjust and change if the peak value lowers.

3.2 Design of Printed Circuit Board

The first version of the prototype board included the circuits mentioned previously with a high-slew rate differential OP amp to isolate the drop on the gate resistor. The second version of the prototype board incorporated a different but very similar peak detection circuit that was mentioned before. The major differences between the versions were the OP amp located before

the diode to create the “super-diode” in version one was removed in version two, no RC filter was on the output of version one, and there was no isolation on the output of version one also, so a differential probe had to be used to measure the results. In Figure 19 below, the high-side circuitry of the first iteration of the board is shown which includes the super-diode concept, a power source with resistor to help the OP amp sync current for the diode faster, lack of a RC filter, and lack of an isolation module.

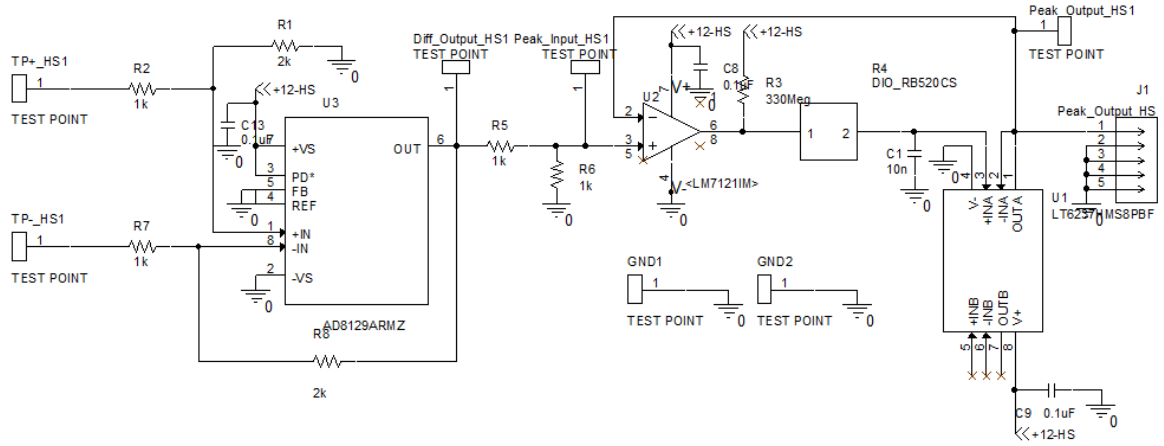

Figure 18: Version One of PCB Circuitry

These changes were made for various reasons. The “super-diode” concept was removed because the op amp was having major ripple issues on the output causing peak values that skewed the data. OP amps not receiving a constant voltage but would see significant switching waveforms tend to have more problems associated with them, so it was decided that a constant small voltage drop would be acceptable losses since that diode drop would be consistent across all measurements. Another notable issue with the “super-diode” concept is the OP amp involved would go into negative saturation and needed time to recover, which it never got, and that resulted in the multitude of issues seen with that OP amp. The RC filter was added on the second version of the prototype board because there was so much ripple on the output of the first prototype that the results were useless. A filter was added to the output of the peak detection

circuit to counter any extraneous noise that could cause the signal to be unreadable. These extraneous signals that could disrupt the peak output could be from the OP amp noise or ringing, noise generated from the module, and any additional noise or spikes not foreseen. Both the filter and the RC time constant introduce a delay issue which will take several pulses for the peak value to be reached, therefore a DPT is not plausible in the actual application but rather a multi-pulse test so the additional circuitry can reach steady state. The delay cannot be helped cause the peak value needs to be held to be able to determine the temperature and the filter is required to make the results readable. Lastly, an isolation module was added to the output of the peak detection and before the BNC connector to ensure that the BNC cable could be used to measure the peak value on the oscilloscope. This provides proper protection to the oscilloscope and the measurement becomes more accurate with improved resolution as a differential probe rated for 1.5 kV would not be used anymore to measure an output that only reaches a maximum of 10V. Other small considerations were introduced from version one to version two such as different connectors to improve ease of assembling and disassembling the test setup, bypassing certain sections of the peak detection circuitry to ensure ease of troubleshooting, and reducing the circuitry down to one peak detector instead of two as to not waste time since it is currently a testing prototype board. The circuit was also designed to be able to test two separate OP amps used in the isolation of the V_{RgEXT} because they were also experiencing ripple and distortion issues in the previous version. This gave more options for troubleshooting the board before having to redesign. The concept of this board would be integrated into the gate driver and would incorporate two separate isolated peak detection circuits to measure the high and low side of the power module.

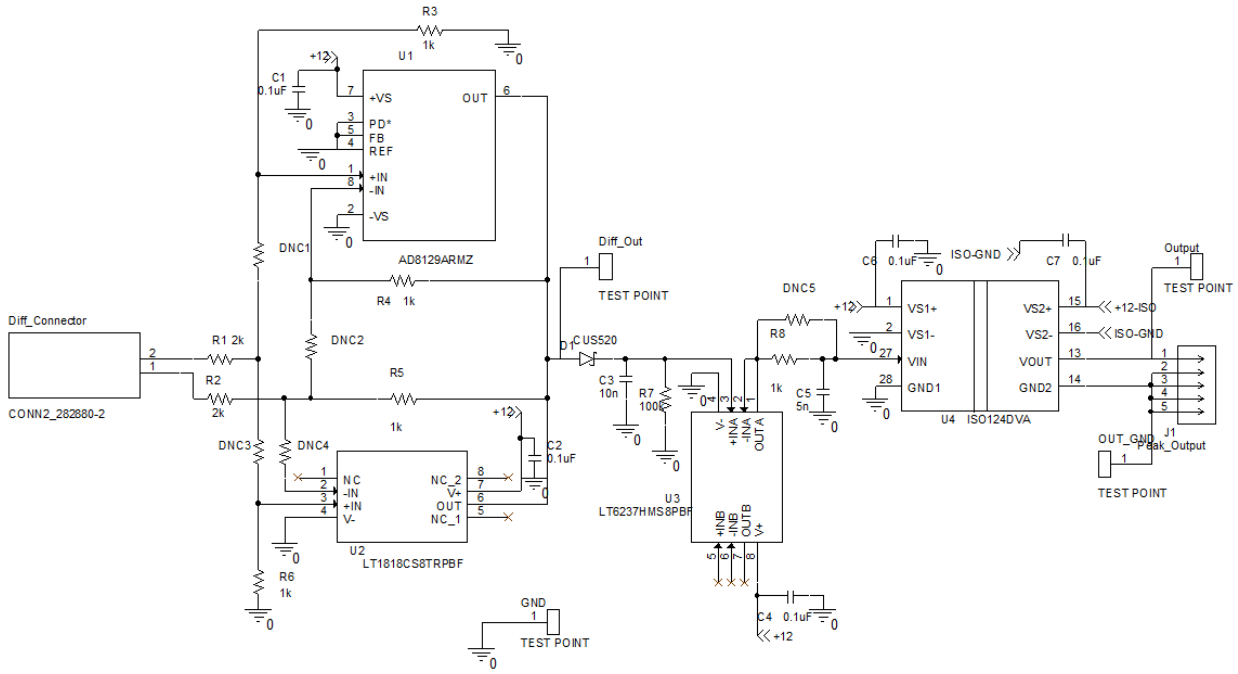

Figure 19: Version Two of PCB Circuitry

During the design of the board, testing was in consideration when looking at the dimensions of the board and how it would be incorporated as a separate entity to the gate driver board. The circuit would be directly implemented on the gate driver in the future as previously stated but since this is the prototyping and design phase, the board was made the same size as the gate driver board with identical holes in each corner so the board could be mechanically fixed above the gate driver board. This along with Kapton tape would keep the boards from touching and possibly shorting. Throughout PCB versions, the holes ended up being omitted as they were not used because of frequent moving of the board for testing and changing of components and the Kapton tape proved sufficient to prevent shorting. In the next two figures, the first version of the PCB is shown and then the second version of the PCB with the changes as mentioned above.

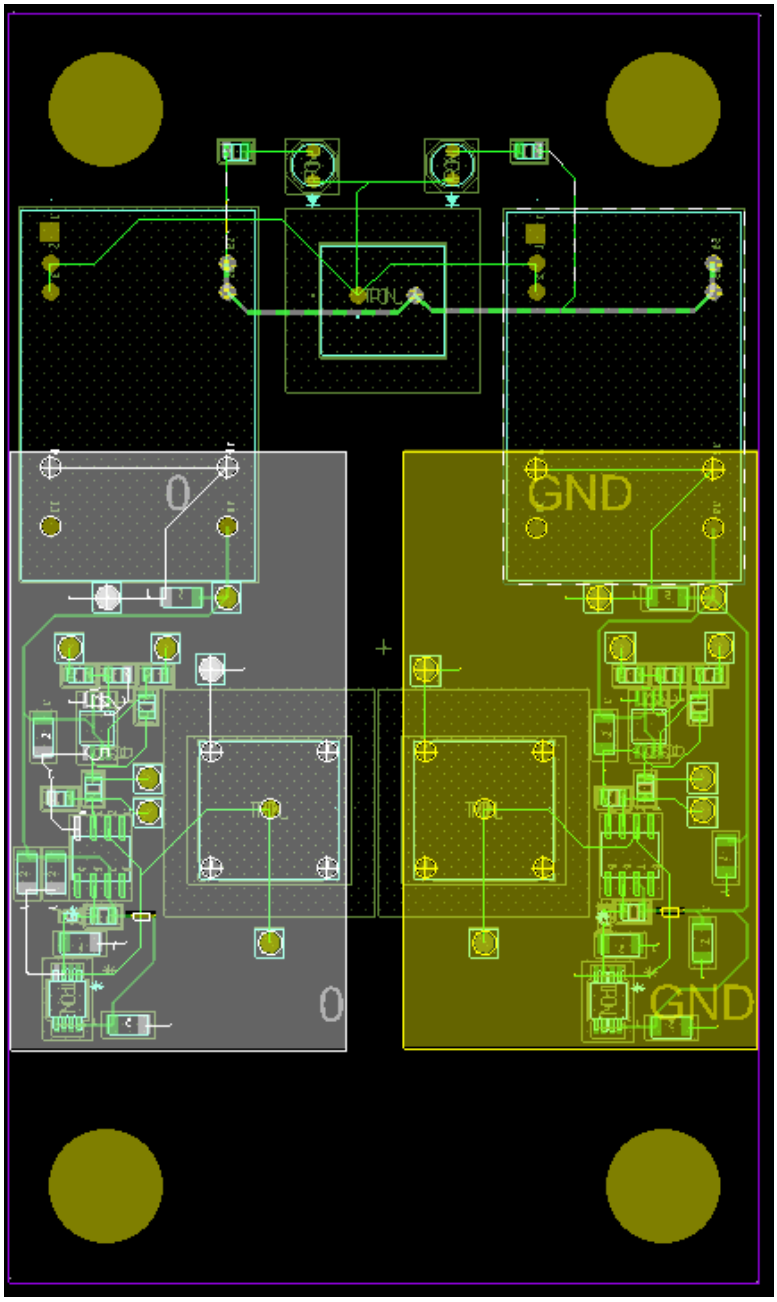

Figure 20: PCB Routed Board Version One

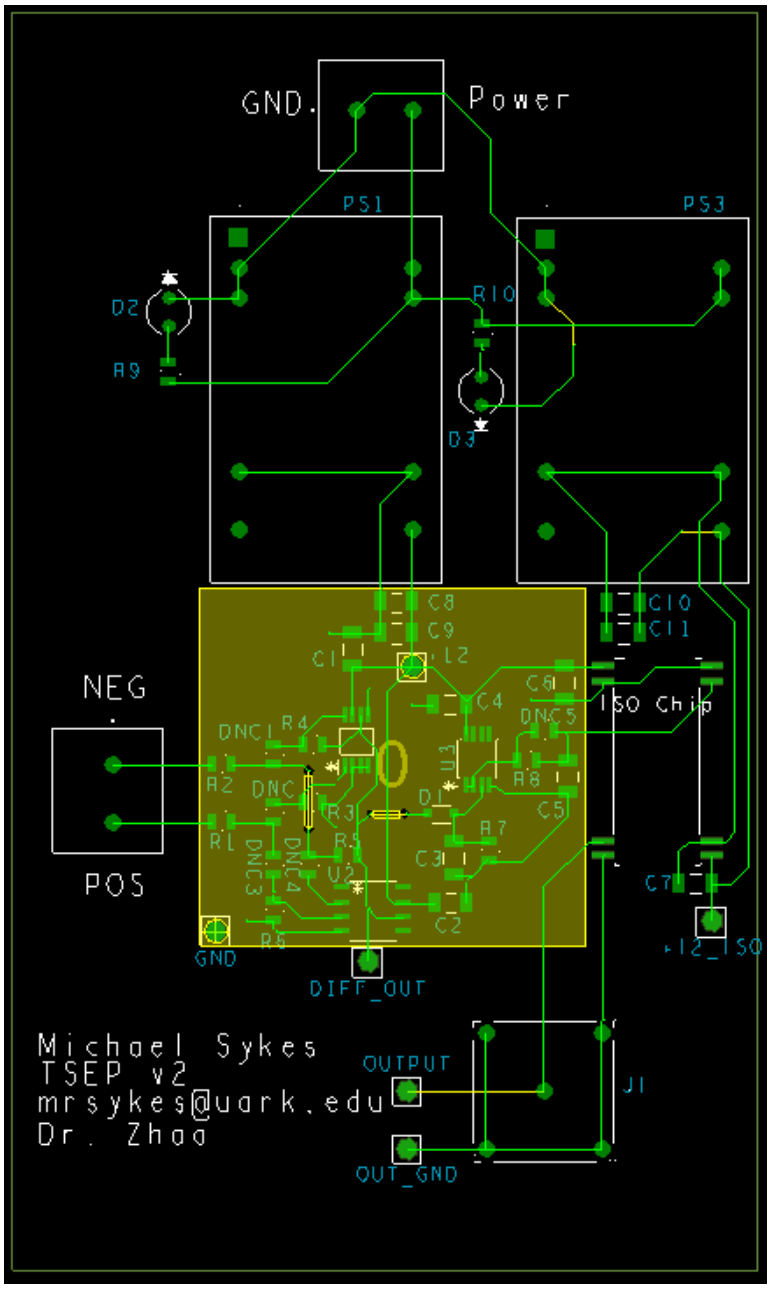

Figure 21: PCB Routed Board Version Two

3.3 References

[1] R. Teja, “OP amp differential amplifier circuit: Voltage Subtractor,” Electronics Hub, 05-Oct-2021. [Online]. Available: https://www.electronicshub.org/differential-amplifier/. [Accessed: 2021].

[2] “Peak Detector Circuit Explained,” Youtube, 03-Aug-2018. [Online]. Available: https://www.youtube.com/watch?v=w4531AVjBYY. [Accessed: 2021].

[3] “RC Charging Circuit Tutorial & RC time constant,” Basic Electronics Tutorials, 26-Aug-2020. [Online]. Available: https://www.electronics-tutorials.ws/rc/rc_1.html. [Accessed: 2021].

[4] R. Keim, “When a diode simply isn't good enough: The superdiode - technical articles,” All About Circuits, 08-Feb-2018. [Online]. Available: https://www.allaboutcircuits.com/technical-articles/when-a-diode-simply-isnt-good-enough-the-superdiode/. [Accessed: 2021].

CHAPTER 4

Analysis of Experimental Performance

4.1 Test Assembly

The test assembly consisted of everything seen from the first test-setup with the added component of the PCB board created to hold the peak output value. From Chapter 2, Temperature Sensitive Electrical Parameter Measurement Viability, the test-setup used there ended up proving that using the peak value from the voltage drop on the external gate resistor provided enough resolution and results to accurately estimate the junction temperature. With that in mind, most of the equipment was kept the same and the board's sole purpose is to make acquisition of the peak voltage easier to obtain. All the components on the board were rated well over the needed requirements that were seen from initial testing. The traces on the PCB were sufficiently large enough to pass the current required for the board to function properly.

4.2 Analysis of Initial Results

Channel 2 (light blue) is the actual voltage drop on R_{gEXT} before it goes through a voltage divider and the differential amplifier. Channel 3 (purple) is the output of the differential amplifier that isolates the voltage drop on R_{gEXT} after it is respectively cut in half by the voltage divider. Channel 4 (green) is the peak detector holding the output of V_{RgEXT}.

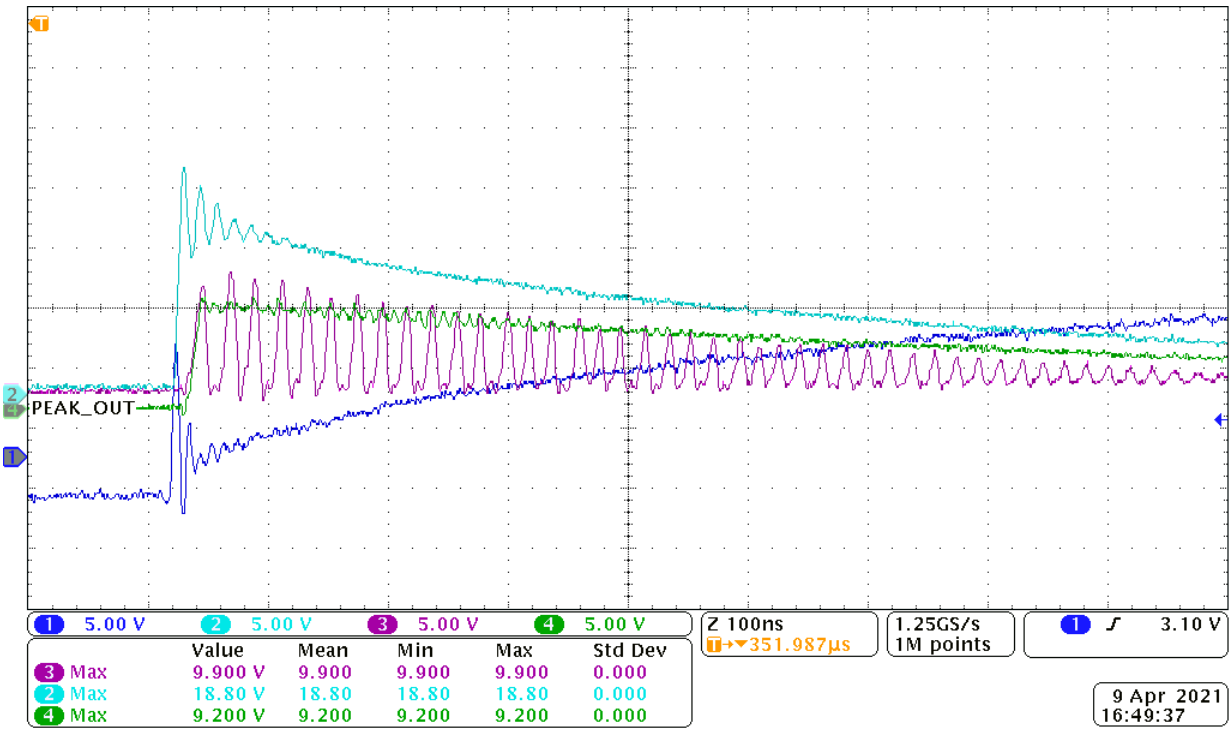

Figure 22: Initial Experiment 25˚C Results

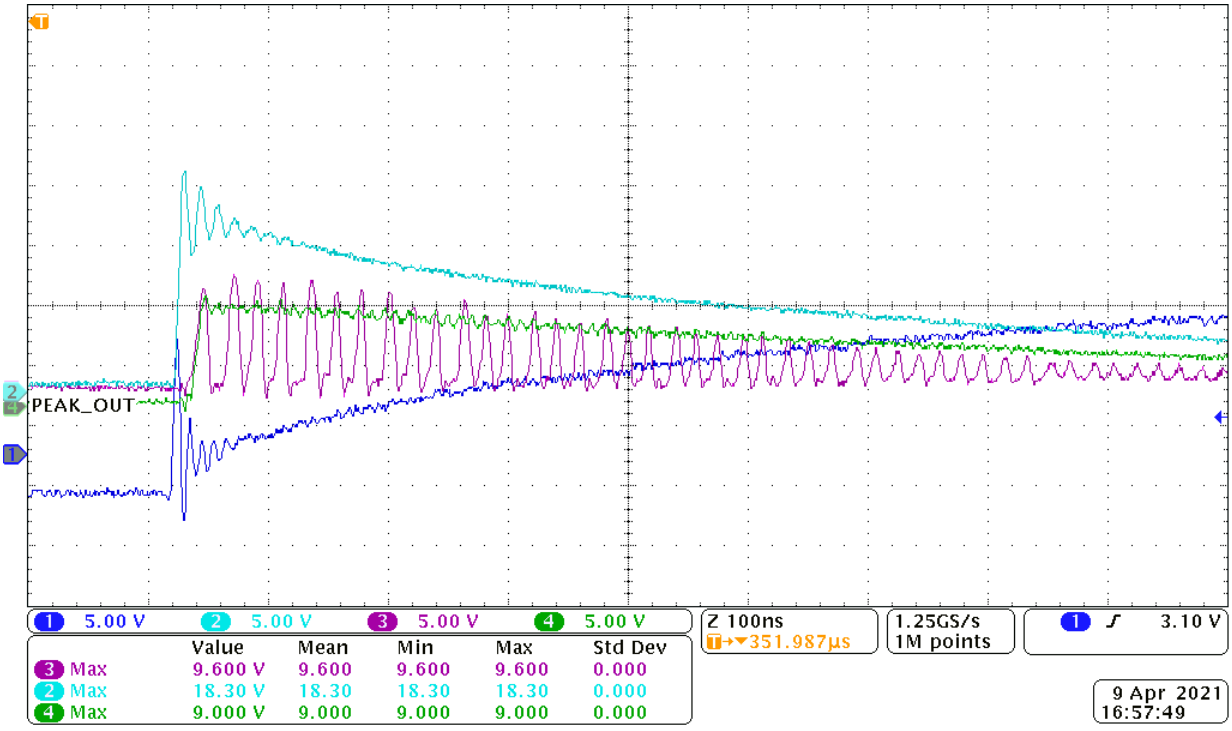

Figure 23: Initial Experiment 125˚C Results

4.3 Discussion of Performance

In the results presented in the previous section, the channel 3 signal should have followed the channel 2 signal almost perfectly, but instead introduced distortion and ringing that lasted way longer than the original voltage drop waveform. The second wave peak on the output of the differential OP amp was also higher than the initial peak, which did not follow the actual voltage drop on R_{gEXT} where every successive peak after the initial had a lower value. The results across temperature still followed the relationship established, however the ringing and distortion could not be overlooked. The problem was traced to the active components that were used to isolate the differential signal. The peak detection circuit (the capacitor, diode, and resistor used for holding the voltage peak) held the peak value of a sinusoid without distortion up to 25 MHz as can be seen in Figure 24. The y-axis is the voltage while the x-axis is time.

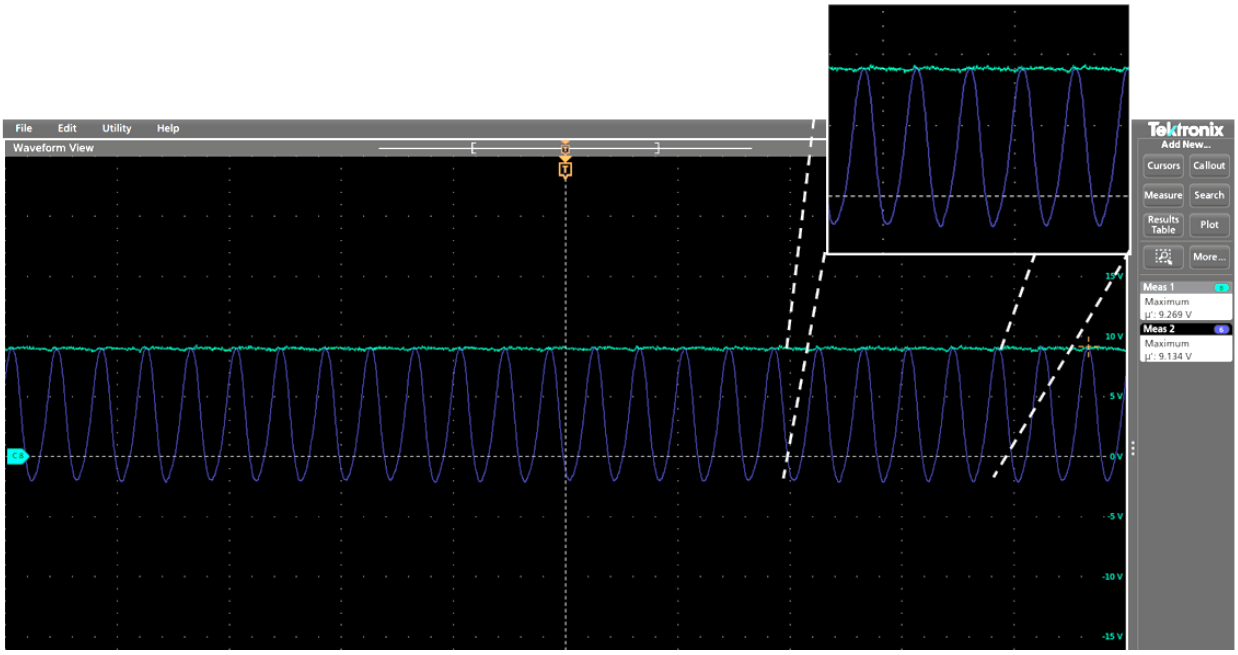

Figure 24: Peak Detection Circuit at 25MHz

This was proven by testing the PCB in separate sections. However, when the OP amp was used to isolate or pass the sinusoid, distortion and inaccurate peak measurements were

noticed as early as 3 MHz. The OP amps were rated to operate up to 400 MHz, but the OP amp could barely pass a 1 MHz sine signal without distorting some. Some of these distortions as seen went over the peak value of the sine wave being passed in.

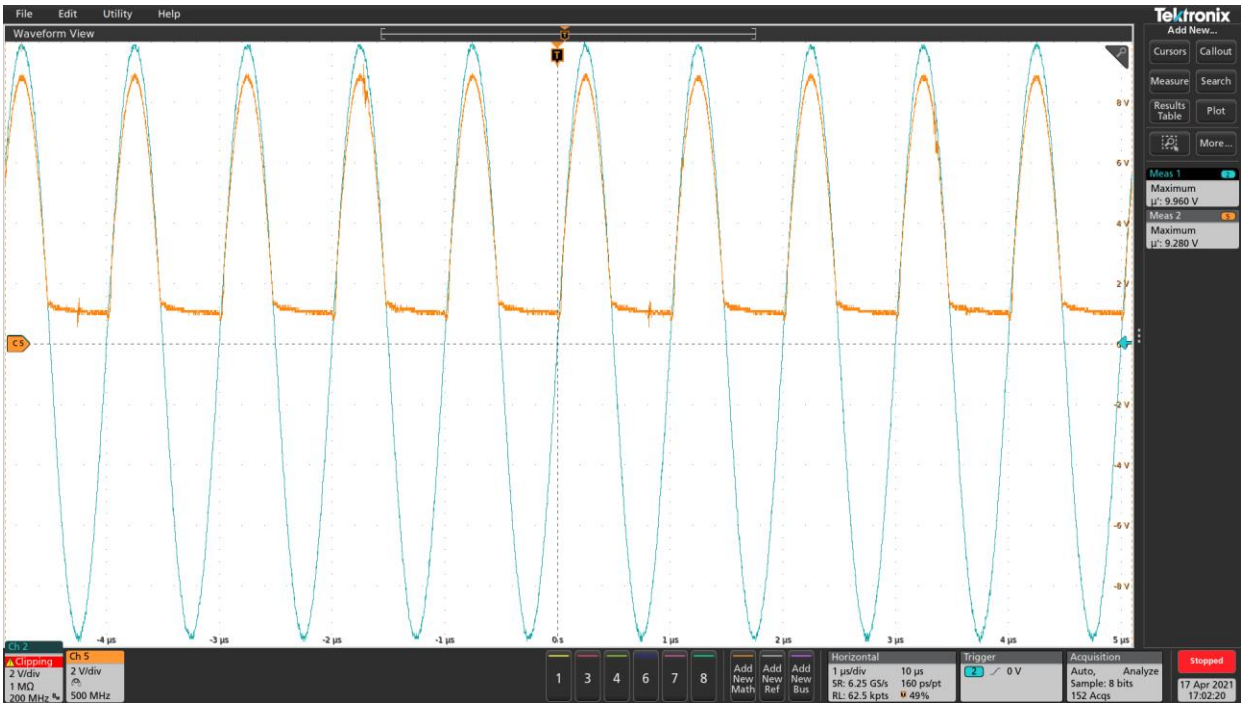

Figure 25: OP Amp Troubleshooting 1 MHz

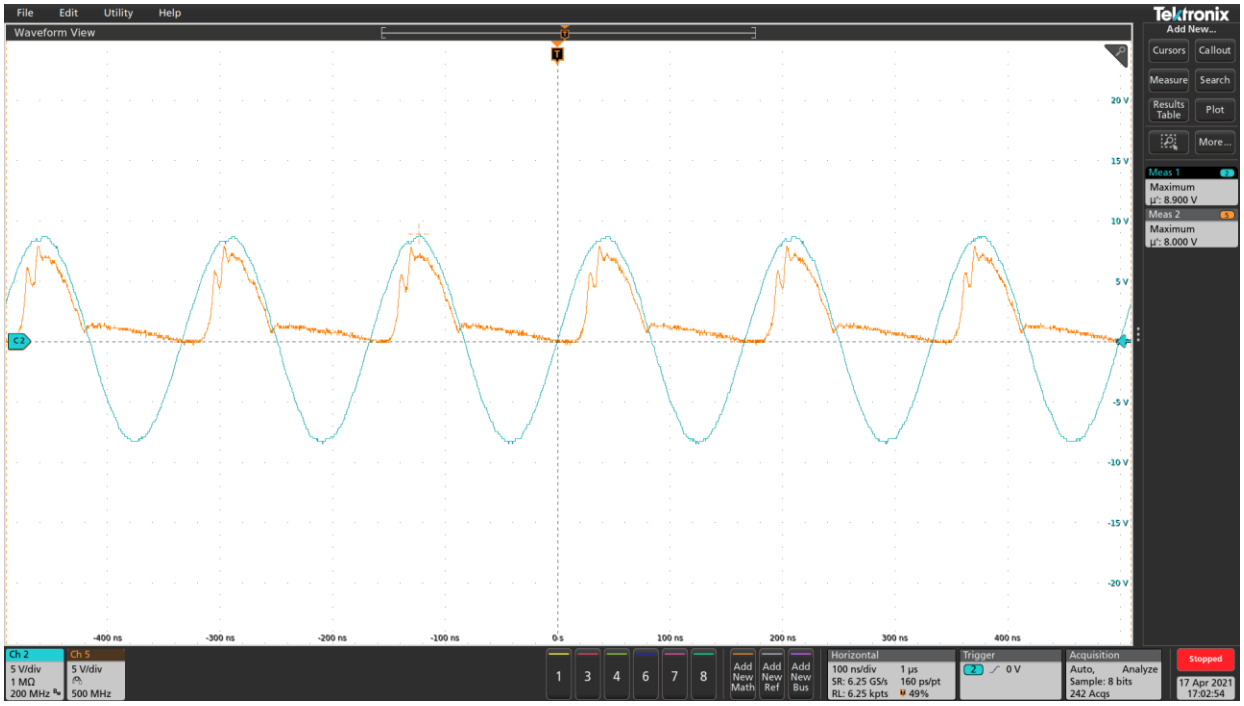

Figure 26: OP Amp Troubleshooting 6 MHz

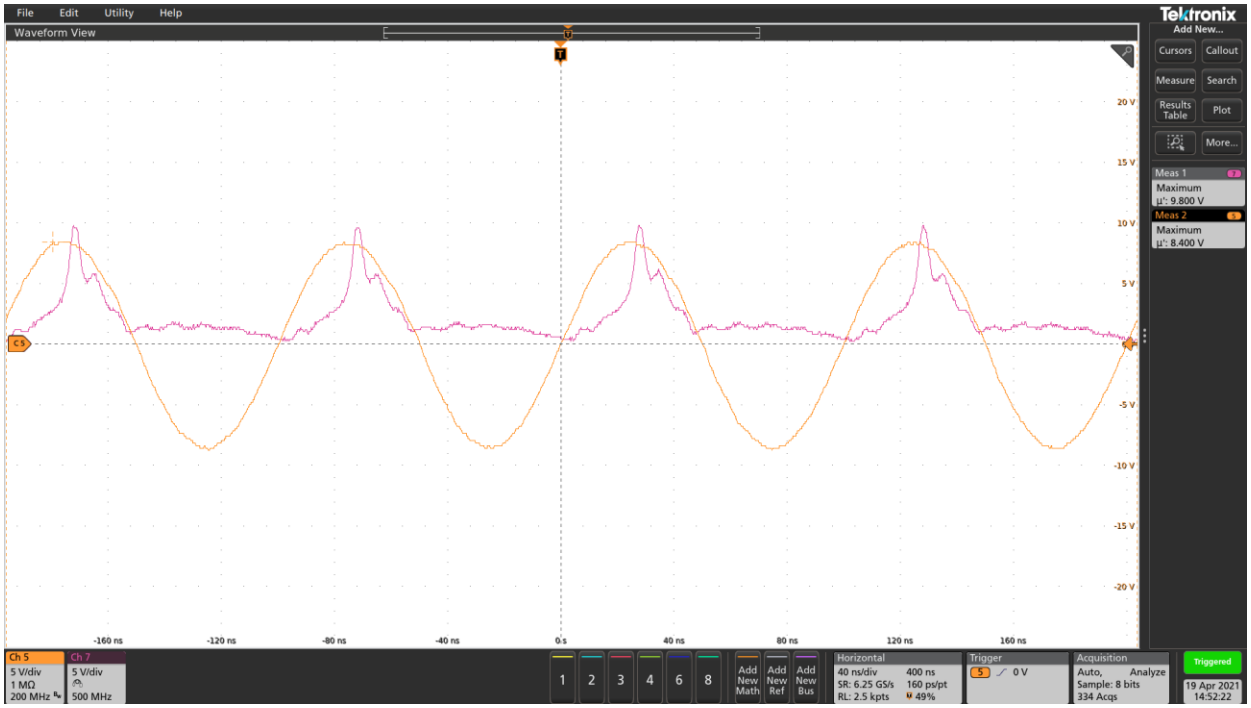

Figure 27: OP Amp Troubleshooting 10 MHz

Multiple approaches were attempted before moving away from the OP amp. Feedback resistors and capacitors were added to try and smooth the output and make it more stable, which

had limited success. This was tried because of a small note in the datasheet of the LT1818 OP amp that said, “In a unity gain configuration, LT1818 OP amp can drive a 20pF load and more with higher gain.” Another note also said, “When driving a larger capacitive load, a resistor of 10Ω to 50Ω must be connected between the output and the capacitive load to avoid ringing or oscillation [1].” The peak detector was changed slightly with a different capacitive load and an adjusted resistance for the RC time constant, but the diode also had a capacitance that put the circuit right at a 20pF capacitive load. These additions and changes to the circuit extended the range of the frequency bandwidth by 1 or 2 MHz before distortion happened, but it was still unable to pass a distortion free waveform at our estimated frequency of about 10 MHz. The peak value obtained from the distortion waveforms could not be trusted in determining the junction temperature. With proper biasing and calibration, OP amps could work, but that could take various extra components, way more time, and more than likely would be specialized based on frequency. With the inconsistency in what this circuit needs to measure, the active components seemed to cause more problems than solve, thus it was time to move away from this approach. A more general approach should be obtained in the pursuit of an accurate peak detection circuit that can operate at any range of frequency and with random sinusoidal signals.

4.4 References

[1] Analog Devices, “LT1818/LT1819: 400MHz, 2500V/us, 9mA Single/Dual Operational Amplifiers,” LT1818/LT1819 datasheet

CHAPTER 5

Redesign and Final Results of Prototype Testing

5.1 Redesign of Circuitry

As seen in the previous section, the active components of the PCB were causing distortions that could not be resolved without a complete redesign of the board. With that in mind, a new approach was considered that would eliminate the need of the active components but still measure the same TSEP talked about. The need for the OP amp to isolate that drop on the resistor was because the voltage drop was floating, both sides had an active voltage, and the difference was what was being measured previously. If a resistor could be inserted in the gate loop path with one of the terminals going to ground, then it would eliminate the need for an active component, like the differential OP amp to isolate that floating voltage. It could now be measured only by the passive components of the board, otherwise known as the peak detection circuit. The OP amp located after the peak detection circuit was also removed to eliminate any distortion and ringing the active components may have on the results. Since this OP amp was removed, the combination of the capacitance and resistance between the peak detection circuit and the low pass filter had to be carefully calculated to keep a suitable RC time constant along with a decent low pass filter that would help eliminate any extra noise created from the switching or extraneous events that could affect the results. A small sensing resistor was inserted in the gate loop at the kelvin source terminal of the power module. This formed the gate loop path with the internal and external gate resistors that cycled back over to the ground of the gate driver switching signal [1]. With the loop in place and the grounds connected, the peak detection circuit only had to be connected to the voltage side of the resistor. By controlling the Rsens resistance, as seen in Figure 28 below, the resolution of the TSEP can be controlled, and based on the

sensitivity of the passive voltage probes being used, general estimation of the junction temperature can be achieved.

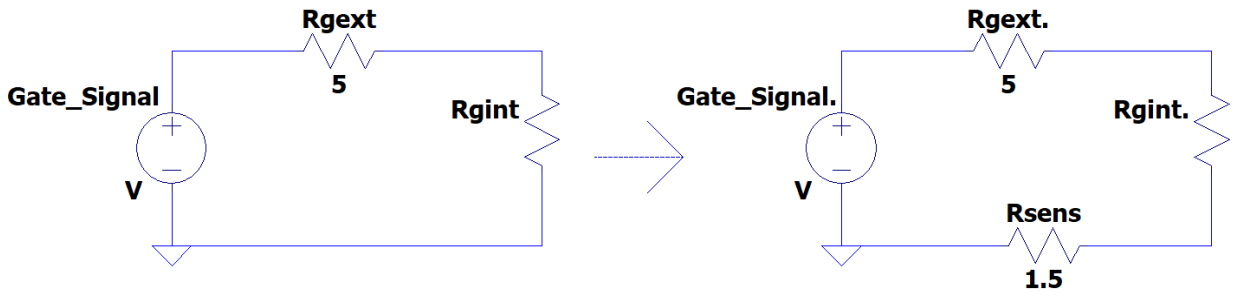

Figure 28: Modified Gate Loop Path [1]

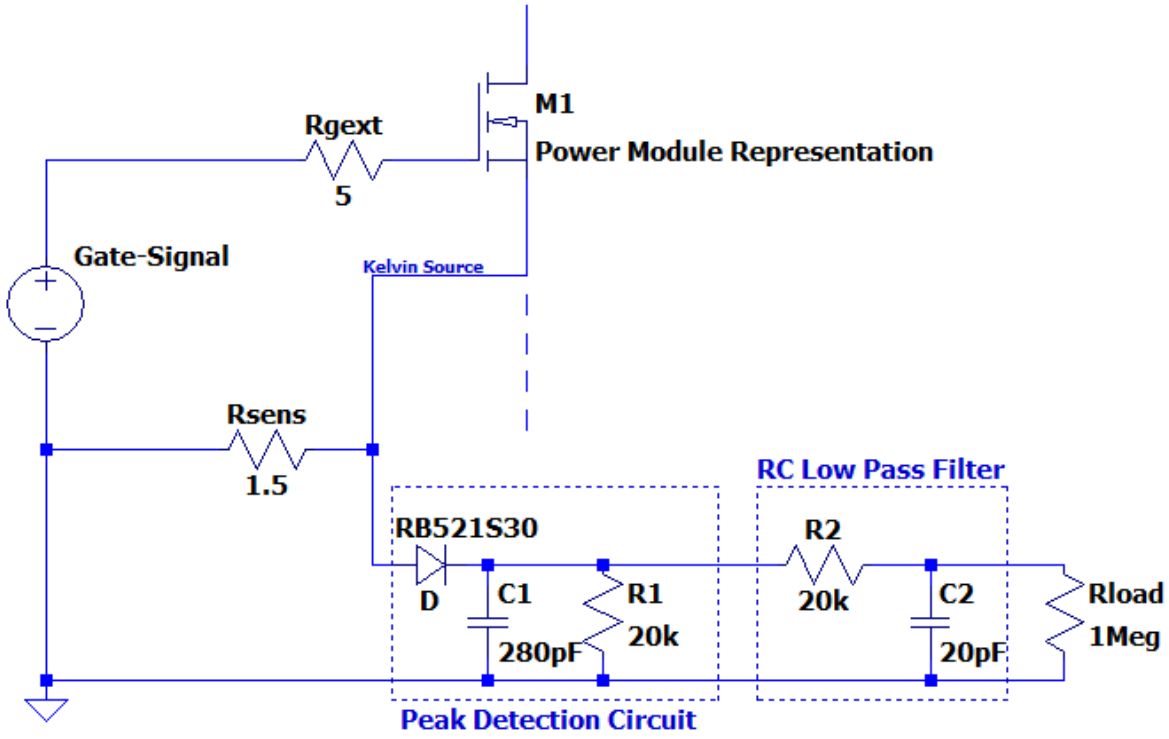

Figure 29: Final Circuitry for Gate Resistance TSEP

5.2 Test Setup

This test has a slight change from previous tests where all the same equipment is used, and the only difference is where the daughterboard is connected to. By adding the sensing

resistor directly in series at the gate loop in the connector pins, the daughterboard now connects via the two wires on either side of the sensing resistor, with one being the input to the peak detection portion of the circuit and the ground side of the sensing resistor being connected to ground of the board. The version 2 daughterboard was repurposed, and a wire was used to bypass where the differential OP amp pad was, and another wire was connected at the end of the low pass filter to be the wire the oscilloscope connected to for the peak voltage.

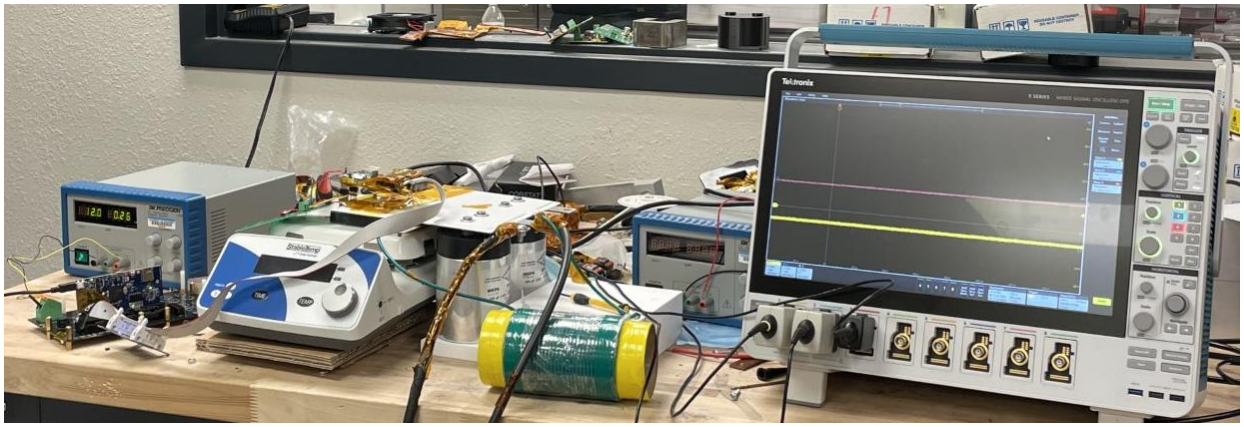

Figure 30: Final Test Setup

Figure 31: TSEP Board and Gate Driver Connection

5.3 Analysis of Final Results

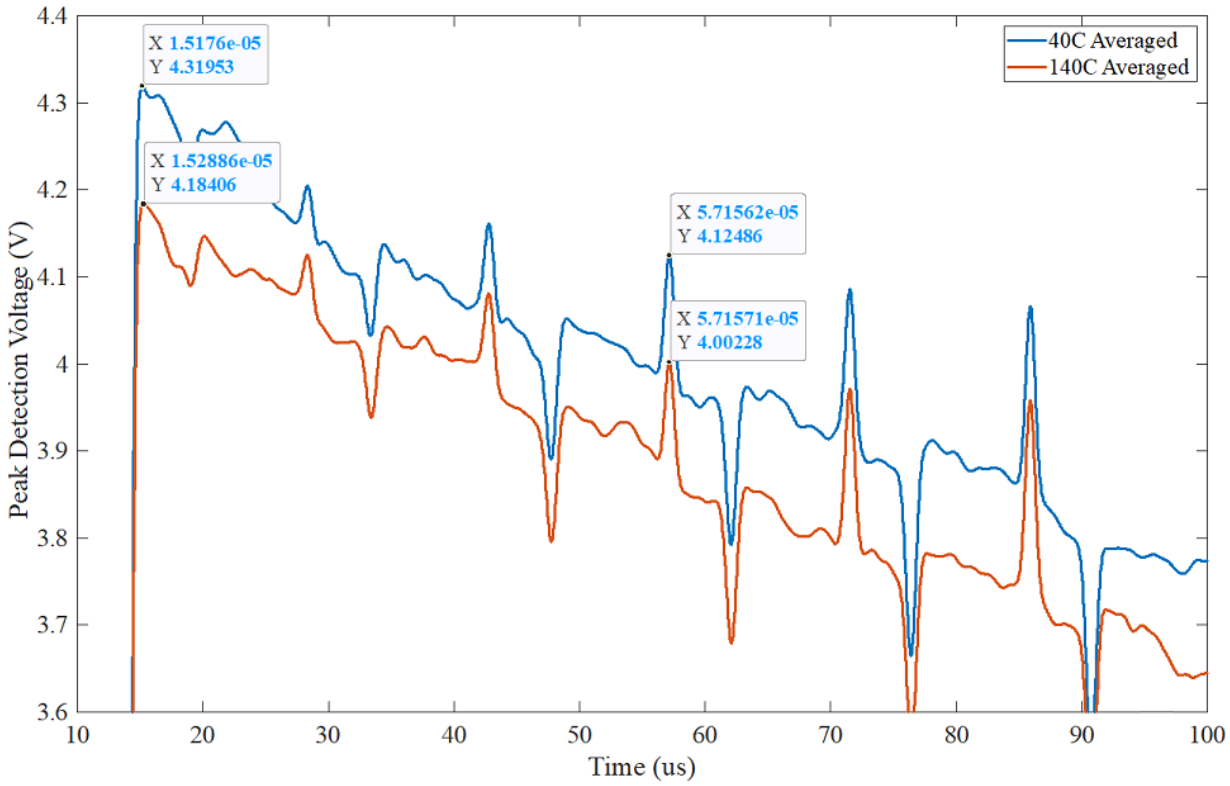

Figure 32: 40˚C vs 140˚C Peak Detection Average

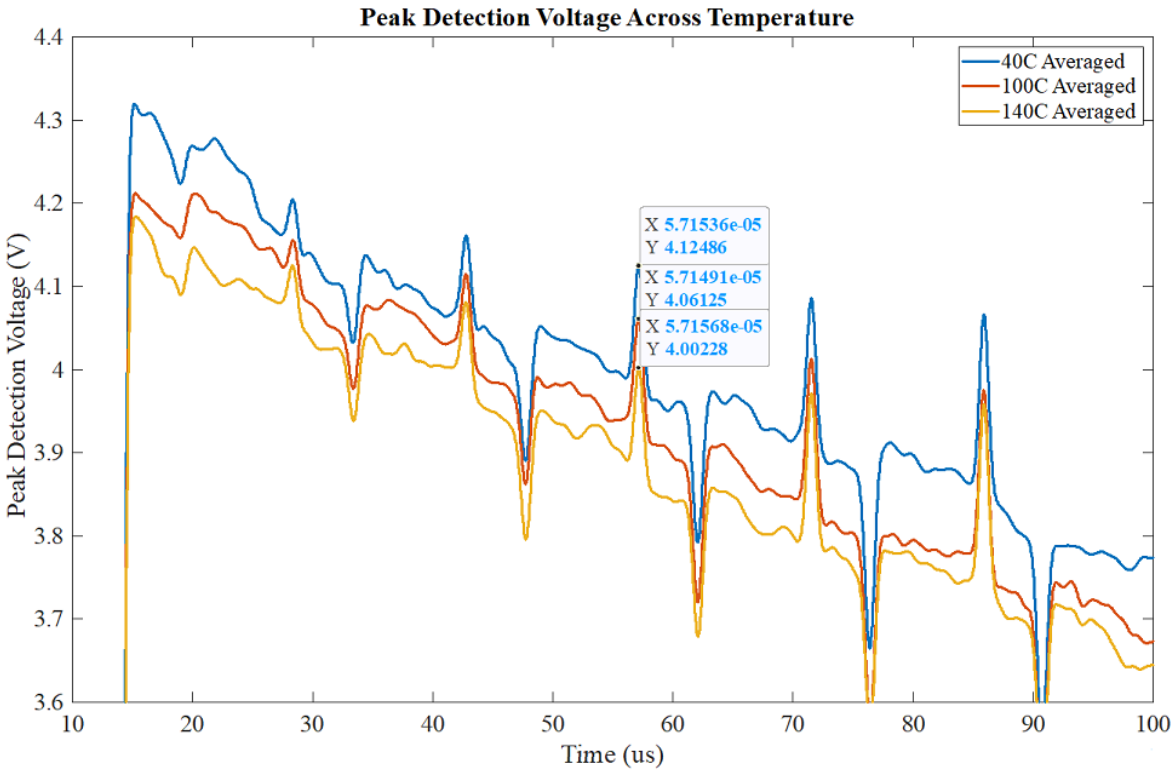

Figure 33: Peak Detection Average Voltage Across Temperature

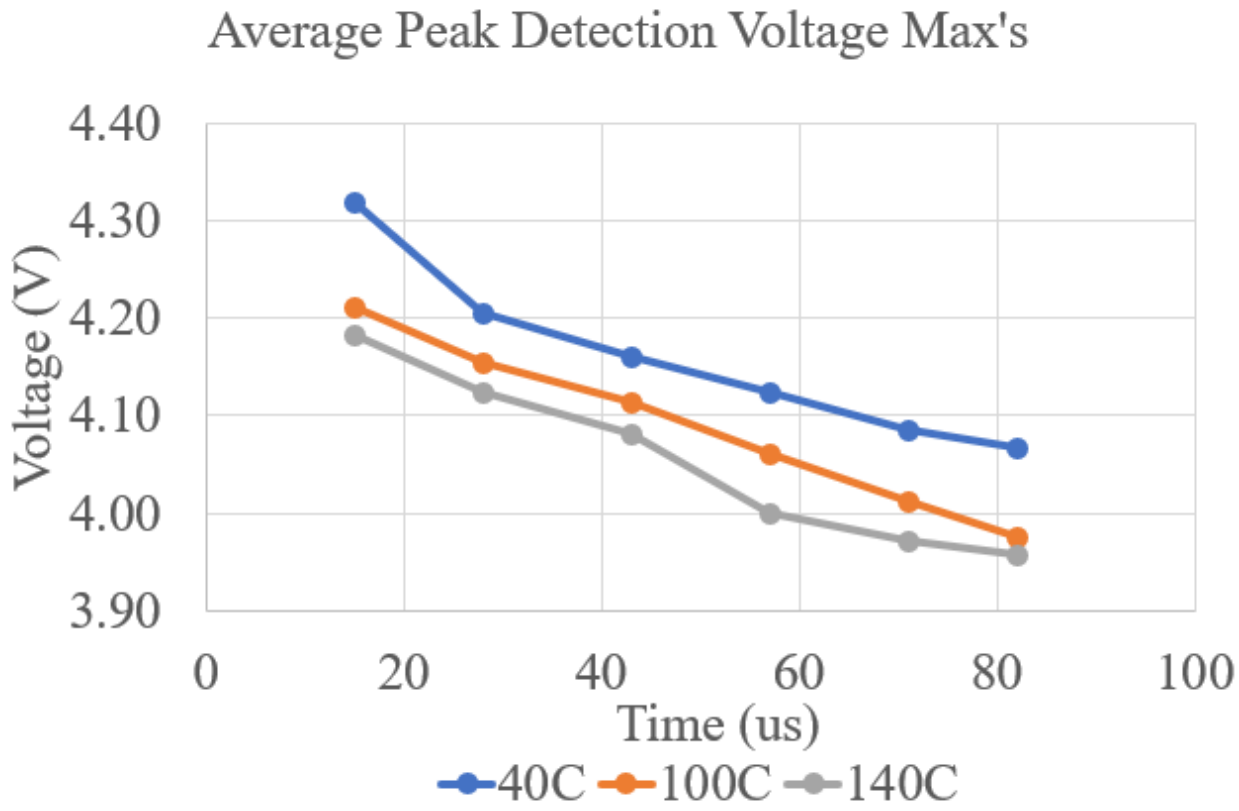

Figure 34: Average Peak Detection Voltage Max's Across Temperature

5.4 References

[1] R. Wang, J. Sabate, K. Mainali, T. Sadilek, P. Losee and Y. Singh, "SiC Device Junction Temperature Online Monitoring," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 387-392, doi: 10.1109/ECCE.2018.8558298.

CHAPTER 6

Conclusion and Future Work

6.1 Conclusion

Based on the graphs above in Chapter 5, Analysis of Final Results, a clear trend could be established from the results showing a higher voltage for lower temperatures. Keep in mind that the ideal equipment to be measuring these changes were not used but rather probes that are used for measuring high voltage. The passive probes were rated up to 300V whereas a passive probe for lower voltage would have been more suitable and accurate. The relative accuracy and trends established from these graphs could be much improved with the correct equipment, but even with the incorrect equipment, the results prove the concept is there to accurately measure the junction temperature of a SiC power module through use of the internal gate resistance as the TSEP. It was previously mentioned that typical sensitivity for internal gate resistance was 2-5 mV/ ˚C, however in this case that was not quite reached but rather a 1 mV/ ˚C was noticed [1]. This resolution can be altered and was a direct result of the 1.5 Ω resistance used for Rsens. If a higher value was chosen for this resistance value, then an improved resolution could have been obtained, but increased resistance in the gate path can also cause slower switching. A clear trend could still be established over large temperature swings with the wrong equipment. Other considerations can be taken from the results also such as improved shielding from the switching occurring in the module to help separate it from the peak output detector or tweaking the filter and peak detection circuit to hold the peak value longer and eliminate any extraneous signals. Other solutions that could improve the results would be adding a switch that could discharge the capacitance much faster between switching cycles. As the power module keeps switching, the switching speed is much faster than the time it takes for the capacitor to charge fully, thus the

spikes, along with some potential EMI, are seen on the graph. Even the spikes however show the temperature difference as they go up to their respective peaks before falling back down. Many of the extraneous signals were filtered out when a moving average was applied to the data to smooth out these results. When the peaks of the various spikes were plotted in Figure 34, the trend could easily be seen there as well. These spikes also got lower over time because as the module switches it still generates more heat that was added to their starting temperatures and that was tracked over the 1μs period for each temperature case. Overall, the results of the peak voltage drop on Rsens show a clear downward trend due to the junction temperature of the power module changing the internal gate resistance. This method provides an accurate estimation of T_J in real time which can be used to prevent the power module from failing due to a critical temperature.

6.2 Future Work

The purpose of the work explained in this paper is to eventually be incorporated directly onto a smart gate driver board for active monitoring. This concept is easily incorporated into the gate driver board with minimal components being added. A sensing resistor would be added into the gate loop path along with the peak detection circuit to monitor the sensing resistor. The low pass filter or voltage integrator could then be added afterwards. The peak voltage output would then be supplied to a microprocessor, which could perform any remaining post-processing functions, to actively monitor the peak voltage reported and shut the module down if approaching a critical temperature. This method is relatively simple to implement on the gate driver board and a microprocessor could easily perform the necessary post-processing functions to determine the junction temperature in real-time. This would also save money on countless external monitoring systems that might not be nearly as accurate at tracking T_J as this TSEP is.

This method is an accurate junction temperature measuring system with controlled resolution, based on the resistance value of the Rsens, and will be an excellent addition to the smart gate driver board.

6.3 References

[1] N. Baker, S. Munk-Nielsen, F. Iannuzzo and M. Liserre, "Online junction temperature measurement using peak gate current," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1270-1275, doi: 10.1109/APEC.2015.7104511.